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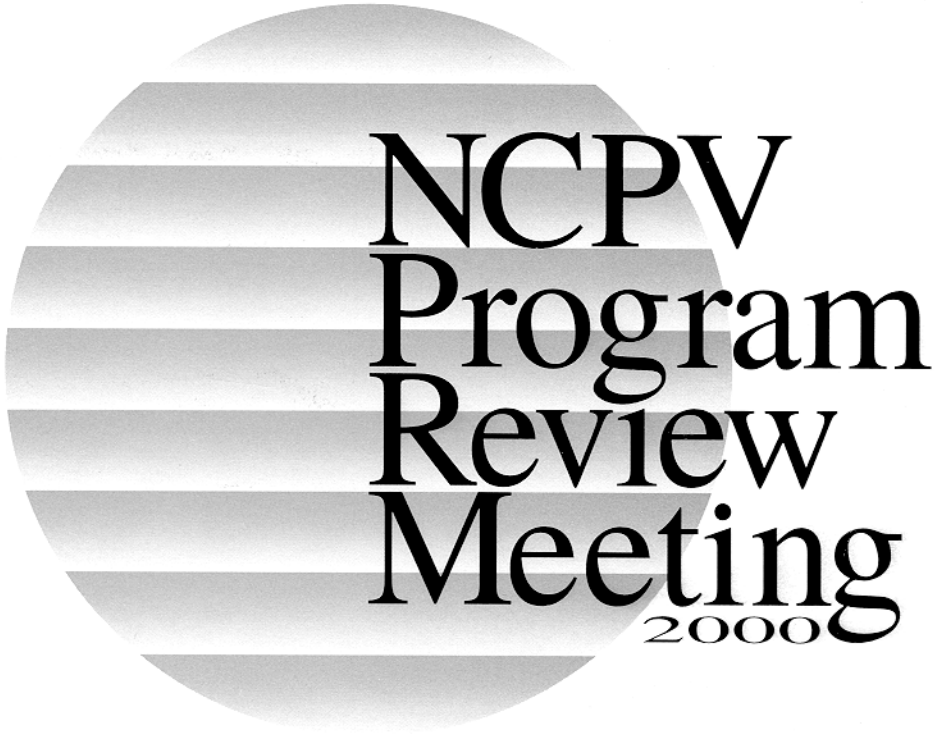

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Investigation of Deep Impurity Levels in CdTe/CdS Solar Cells

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ABSTRACT

We have studied deep impurity levels of CdTe/CdS solar cells by capacitance-voltage (C-V), deep-level transient spectroscopy (DLTS) and time-resolved photoluminescence (TRPL). CdTe/CdS devices were stressed under light soak of AM1.5 at 65°C for various lengths of time. C-V measurements indicate a high density of interface states. Using DLTS, a dominant electron (minority) and two hole (majority) trap levels were observed. These trap levels were labeled as E1 at Ec-0.28 to Ec-0.45 eV, H1 at Ev+0.35 eV, and H2 at Ev+0.45 eV. The H1 trap level is attributed to Cu substitutional defects. The E1 trap level is believed to be a deep donor. The calculated Shockley-Hall-Read (SHR) lifetime, using DLTS parameters, is about 0.85 ns, which is consistent with the lifetime values measured by TRPL. These results suggest that the E1 trap level is the lifetime-limiting defect.

Introduction

CdTe/CdS thin-film solar cells are one of the leading candidates for low-cost large-scale and terrestrial photovoltaic applications. The calculated maximum theoretical efficiency for single-crystal CdTe cells is close to 29% [1], but practically achieved results for polycrystalline CdTe/CdS heterojunction cells are around 16% [2]. Four problems appear to be dominant in polycrystalline CdTe/CdS thin-film solar cells: 1) recombination losses associated with the CdTe/CdS junction interface, 2) difficulty in doping the CdTe, 3) difficulty in obtaining low-resistance contacts to CdTe, and 4) degradation of the back contact [3].

Cu-doped ZnTe, HgTe, Cu_xTe and Au are currently being studied by various groups [4] as a back contact to CdTe thin-film solar cells in order to obtain low-resistance and a stable contact to the CdTe layer. Studies have shown [5] that Cu diffuses into the CdTe film during and subsequent to formation of the back contact. Uncontrollable Cu diffusion may severely reduce the stability of the devices and introduce deep-level impurities into the CdTe layer. In this paper, we study deep impurity levels of CdTe/CdS solar cells as a function of stress time. We discuss the origin of defects and their effect on the minority-carrier lifetime.

Experimental Procedure

The device structure of CdTe/CdS thin-film solar cells used in this study is described elsewhere [4]. A number of identical CdTe/CdS devices were prepared for stress testing. Devices were subjected to light soak under AM1.5 (1 Sun) at 65°C for various lengths of time.

The net carrier concentration (N_A-N_D) and the built in voltage (V_{bi}) of the devices were measured by using C-V measurements. C-V measurements were performed using an HP2474 multi-frequency LCR meter, at a frequency of 100 kHz on completed CdTe/CdS solar cells. The system used to measure the minority-carrier lifetime is described in reference [6]. DLTS is a powerful technique used to extract thermal properties of deep-level impurities such as the activation energy, capture cross section and the density of traps. Detailed information related to our DLTS system can be found in reference [7].

Experimental Results and Discussion

C-V measurements have revealed that the plot of (N_A-N_D) vs. applied bias (V) is not linear, indicating a nonuniform ionized impurity concentration with depth in the depletion layer. We have successfully fitted the data to two slopes, and the calculated doping densities are $8.2x10^{14}$ cm^{-3} at large reverse bias, which is associated with the bulk doping and $8.6x10^{13}$ cm^{-3} at forward bias that corresponds to the region near the CdTe/CdS interface. This reduction in net carrier concentration suggests a high density of surface or interface states due to compensation (deep donors) at the CdTe/ CdS junction.

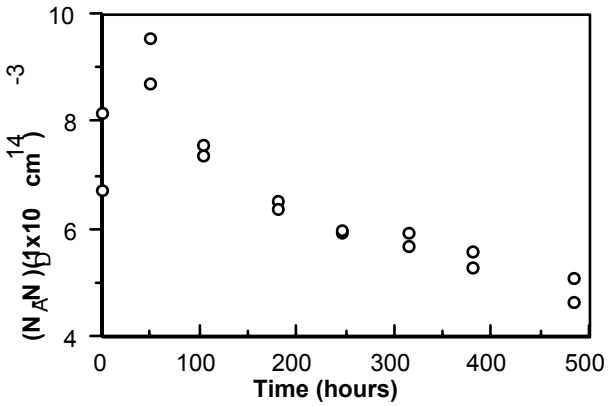

Figure 1 The net carrier concentration vs. stress time. The net carrier concentration was obtained from large reverse biases (from –2 V to –0.5 V).

We have monitored how the net carrier concentration was affected by stress time. Figure 1 shows that there is an improvement in carrier concentration upon the first 50 hours of stress which then decreases logarithmically. This

decrease in (N_A - N_D) is attributed to the presence of deep donors, which cause compensation that is likely to take place at longer stress times.

The DLTS data presented here were performed under identical bias conditions. Several trap levels were found in all samples in the temperature range of 80–300 K as shown in Figure 2. These trap levels are designated as E1, at E_C-0.28 eV to Ec-0.45 eV, H1 at E_V+0.34 eV, and H2 at E_V +0.45 eV. The trap concentrations of devices stressed about 500 hours are 1.5 x 10^{13}, 1.2 x 10^{13} and 8.5 x 10^{12} cm^{-3}, respectively.

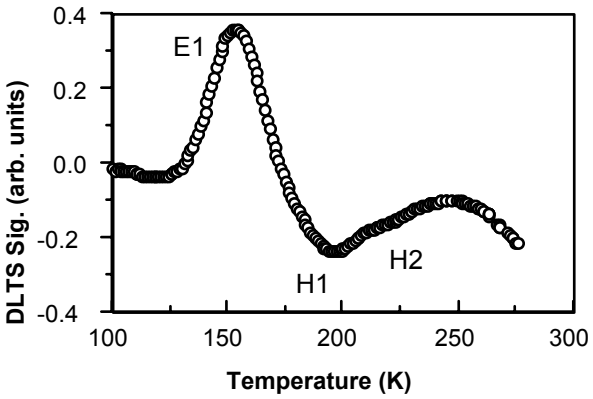

Figure 2 DLTS spectrum of an-as grown CdTe/CdS device.

Capture cross sections of E1 and H1 were not directly measurable with our system because, for the shortest reduced-bias pulse (≈1 μsec), all the levels were completely filled with the respective carriers. For this reason, the capture cross sections of the E1 and H1 trap levels were determined from the intercept of the Arrhenius plots. The values for devices stressed for 513 hours are $5x10^{-12}$ and $2x10^{-14}$ cm^2, respectively. The SHR lifetime of E1 trap level was calculated by using the appropriate values for thermal velocity, capture cross section, and trap concentration. The SHR lifetime is found to be about 0.85 ns for devices stressed for 513 hours, which is consistent with the lifetime values measured by TRPL as shown in figure 3. These results indicate that the E1 trap level is the lifetime limiting defect.

The H1 level observed here was previously reported to be associated with substitutional Cu impurities [5, 8]. Based on prior evidence [9–11] and the data presented here, we speculate that the E1 level is a deep donor due to the doubly ionized interstitial Cu (Cu_i^{++}) ions. C-V data suggests the presence of a high concentration of compensating donors that are responsible for compensation of net carrier concentration as shown in figure 1. We believe that the E1 level is responsible for the behavior of C-V data at low reverse biases, which corresponds to the interface.

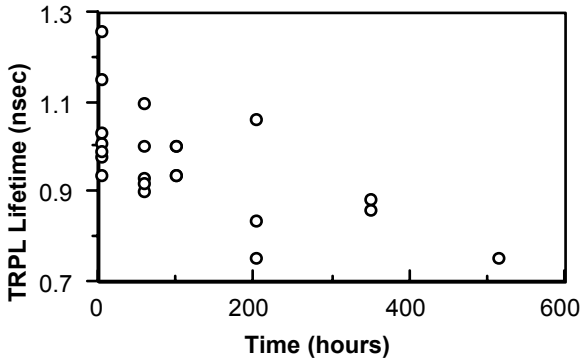

Figure 3 TRPL minority-carrier lifetime of several CdTe/CdS devices as a function of stress time.

In conclusion, the deep impurity levels and their effect on the minority-carrier lifetime in CdTe/CdS solar cells have been studied by C-V, DLTS, and TRPL. We have observed and identified a dominant electron trap, namely E1, that is an effective recombination center. The H1 level is attributed to the substitutional Cu impurities. The E1 level is likely to be a deep donor due to formation of Cu complexes near or at the interface and is the lifetime-limiting defect.

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