


# **PROGRAM AND PROCEEDINGS**



## **NCPV Program Review Meeting 2000**

**April 16–19, 2000**

**Adam's Mark Hotel**

**Denver, Colorado**



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# Effects of Surface Composition on CdTe/CdS Device Performance

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## ABSTRACT

The atomic composition of the back surface of the CdTe layer in a CdTe/CdS photovoltaic (PV) device has a significant influence on the quality of the electrical contact to this layer. This paper reports the results of a systematic study that correlates the composition of the back surface with pre-contact processing and device performance. We found that certain processing steps produce an oxide layer that degrades device performance by producing a metal-oxide-semiconductor (MOS) contact, rather than the intended metal-semiconductor, Schottky barrier contact. We also found that the as-deposited CdTe film is cadmium-rich for several hundred angstroms at the back surface. This n-type layer can impede current flow for majority holes, degrading device performance.

## 1. Introduction

An important issue in commercialization of CdTe-based thin-film solar cells is developing a method for making a stable, low-resistance back contact. Because no metal has a work function larger than the work function of p-type CdTe, a fundamental problem exists in forming low-resistance contacts. The standard method of producing low-resistance tunneling contacts by high doping of the surface is difficult because of the complexities in doping CdTe to high hole-densities.

There are various fabrication methods that produce high-efficiency polycrystalline CdTe/CdS PV cells. An essential step in all of these methods is exposure to CdCl<sub>2</sub> in conjunction with annealing. Most methods utilize either a solution-CdCl<sub>2</sub> (SCC) treatment, or a vapor-CdCl<sub>2</sub> (VCC) treatment. These treatments are followed by various types of surface-cleaning processes prior to back-contact application.

The National Renewable Energy Laboratory (NREL) CdTe device team has used both SCC and VCC treatments. In this study we have used X-ray photoelectron spectroscopy (XPS) to determine the atomic composition of the back surface at each step in the processing sequence for both SCC and VCC treatments. Devices have been fabricated from the films at each step of the processing in order to correlate back-contact performance with surface composition.

## 2. Sample Preparation

The polycrystalline CdTe/CdS thin films used in this study were deposited using close-spaced sublimation (CSS) at NREL. Samples used for surface characterization and

device fabrication consisted of multi-layer CdTe/CdS/SnO<sub>2</sub>/7059-glass structures typical of NREL CdTe/CdS devices[1].

We have studied two distinct processing “streams”. The first one is the SCC treatment. First, the sample is placed in a boiling CdCl<sub>2</sub>-methanol solution for 15-20 minutes. The sample is then annealed in air at 400°C for 30 minutes. Following the annealing step, the samples are etched in a 350:4:140 mixture of HNO<sub>3</sub>:H<sub>3</sub>PO<sub>4</sub>:H<sub>2</sub>O, (NP etch). The samples are rinsed in running deionized (DI) water to halt the etch process. Following the rinse, a mixture of Cu-doped HgTe in Electrodag 114 is applied, and the sample is annealed in air for 30 minutes at 260°C. Finally, silver paint is applied, and the device is annealed at 100°C in air.

In the VCC treatment, the samples are exposed to CdCl<sub>2</sub> vapor at 400°C in a modified CSS chamber in the laboratory ambient atmosphere. After this step, the samples are rinsed in flowing DI water, then etched in NP etch and rinsed again. The remainder of the contact application procedure is the same as above. NREL researchers regularly achieve devices with efficiencies of over 13% using either the SCC or the VCC treatments.

In addition to the standard conditions described above, we have also investigated the effects of annealing under vacuum, and of a weak nitric-acid solution. The vacuum annealing was performed at 10<sup>-3</sup> torr and 400°C for 10 minutes. The nitric acid etch consisted of 3 ml of 15.9 M nitric acid in 100ml of H<sub>2</sub>O. Etch time was 60 seconds, followed by a DI rinse to halt the etching process.

## 3. Results

XPS sputter depth profiles were used to characterize the atomic composition of the near-surface region for each sample. The sputter rate was calibrated at 17 Å per minute. XPS data were collected with a sputtering interval of 20 seconds, which is equivalent to removal of 5.7 Å, or approximately two monolayers of material between XPS surveys. The atomic composition was profiled within 10 minutes sputter time (170 Å) of the surface. The atomic percentages of the elements tellurium, cadmium, oxygen, chlorine, sulfur, and carbon were measured. No other elements were present at levels detectable by XPS.

The atomic percent (at%) of oxygen in the surface region is strongly correlated with device performance. The oxygen depth profile is approximately linear, and is parameterized in Table 1 below. Much more detailed results are available in an upcoming publication[2].

Sample Processing	at% oxygen at surface	at% oxygen at 10 min., or depth at% < XPS limit
as deposited	20	3 min
SCC only	15	2 min
SCC/anneal	50	25
SCC/anneal/DI	49	20
SCC/anneal/vac. anneal	45	20
SCC/anneal/DI/HNO <sub>3</sub>	10	0.5 min
SCC/anneal/DI/NPetch	6	6
VCC only	10	2
VCC/vacuum anneal	9	5
VCC/DI	30	5@4min 5@10min
VCC/DI/HNO <sub>3</sub>	8	0.3 min
VCC/DI/NP etch	6	6

Table 1. Atomic percent oxygen at the surface, and the sputter time the oxygen at% goes below the XPS limit (<0.1%), or the at% after 10 minutes of sputtering.

We have also found that all of the samples, except the NP-etched samples, are cadmium rich in the near surface region. This has important implications for contact formation, as it is known that cadmium interstitials and tellurium vacancies both form shallow donors which could make the near-surface region n-type. Such an n-type region would impede the flow of majority-carrier holes through the metallic contact at the back surface, producing a relatively high-resistance back contact and limiting the efficiency of the solar cell.

#### 4. Device Characterization

To correlate the back-surface composition with the quality of the back contact, we have fabricated devices from samples at each step of the processing. Considerable care has been taken to ensure that all of the devices are identical except for their back-surface processing. The primary measure of the quality of the back contact is the contact resistance,  $R_c$ . It is not practical to directly measure  $R_c$  in these devices; however, it is possible to determine the total series resistance of the device,  $R_s$ , using the following method. In forward bias, near  $V_{OC}$ , the series resistance,  $R_s$  can be expressed as the sum of the back-contact resistance plus the lumped resistance of the rest of the device,  $R_o$ :

$$R_s = R_o + R_c \quad (1)$$

Because the devices in this study are essentially identical except for their back-surface treatments, we propose that changes in  $R_s$  are primarily due to changes in  $R_c$ .

Series resistance can be calculated from the J-V curve using an analytical technique established by Sites for the J-V analysis of polycrystalline solar cells[3]. Using the standard photodiode equation and assuming high shunt resistance (which is the case for the devices in this study), one can derive an equation of the form:

$$\left(\frac{dV}{dJ}\right) = R_s + \frac{AkT}{q} (J + J_{sc})^{-1} \quad (2)$$

In the dark, the inverse current term reduces to  $J^{-1}$ . The series resistance is determined by taking the intercept of  $(dV/dJ)$  vs.  $J^{-1}$ . We have used this formalism to calculate values of  $R_s$  for each of the devices studied.

The efficiency and  $R_s$  values for the devices in this study are presented in Table 3. The values of  $R_s$  presented in the table are calculated from the dark J-V curves measured at 25° C.

Sample Processing	$R_s$ ( $\Omega$ -cm <sup>2</sup> )	efficiency(%)
as deposited	5.0	8.7
SCC only	NA	NA
SCC/anneal	8.3	12.05
SCC/anneal/DI	8.6	12.35
SCC/anneal/ vac. anneal	4.7	11.9
SCC/anneal/DI/HNO <sub>3</sub>	3.1	12.85
SCC/anneal/DI/NP etch	1.5	13.05
VCC only	2.3	13.1
VCC/vac. anneal	2.5	13.1
VCC/DI	4.5	12.25
VCC/DI/HNO <sub>3</sub>	2.3	12.5
VCC/DI/NP etch	1.9	13.3

Table 2. Device  $R_s$  and efficiency for each processing condition. No device was fabricated for the SCC-only.

The relationship between  $R_s$  and oxygen at% is clearly illustrated in Figure 1. The line in the figure is a linear fit to the data points. It is clear that  $R_s$ , and hence  $R_c$ , are approximately linear functions of the oxygen content at the surface of the CdTe-absorber layer. This is consistent with formation of an MOS back contact for the devices with significant amounts of oxygen, and a metal-semiconductor Schottky barrier contact for those devices with very little oxygen.

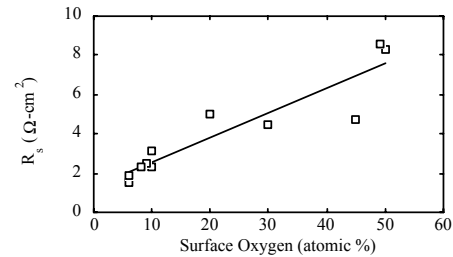


Figure 1. Dependence of  $R_s$  on oxygen atomic percent.

#### Acknowledgements

We wish to thank Yoxa Mahathongdy for assistance with vapor CdCl<sub>2</sub> treatments and device fabrication, and Rosine Ribelin for chemical bath deposition of the CdS layers. This work was supported by the US Department of Energy under Contract No. DE-AC36-99GO10337.

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