

II. CIRCUIT DESCRIPTIONS

The gate drive simplified schematic diagram is shown in figure 1. The design uses a commercially built Intelligent IGBT Gate Driver from Concept Technology Ltd. model IGD-515 [4]. It is compact and provides all basic functions of a standard gate driver. A single 15V source produces bipolar $\pm 15V$ gate trigger at $\pm 15A$ rated peak current. The collector-emitter de-saturation voltage of 15V or less is compared with a fixed reference voltage to activate the over-current protection that reduces the gate trigger pulse width. The gate drive power requirement is not a concern since the modulator only operates at a maximum rate of 120 PPS. Additional circuitries are necessary to boost up the gate voltage at turn-on, to clamp the remaining voltage level for over-current protection, to limit the collector-emitter voltage at turn-off, and to dynamically control the initial peak current during short circuits.

An extra 200V source provides the DC link voltage interlock, which prevents high voltages from being applied if there is a short in the core driver circuit. It also supplies power for the turn-on boosting circuit and for raising the de-saturation voltage detection level up to 150V. Figure 2 shows the resulting gate drive voltage and current waveforms.

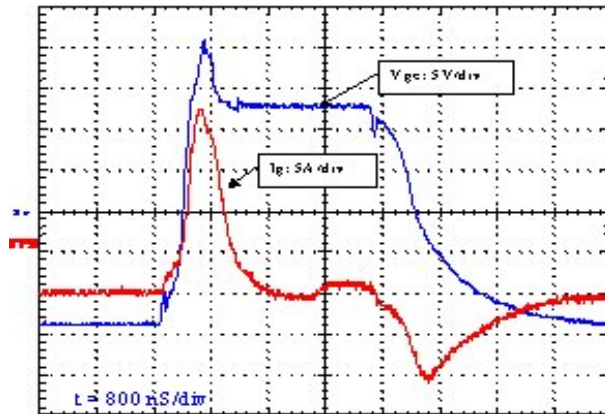


Fig. 2: Gate-emitter voltage and current.

A. Turn-on boosting.

While the FZ800R33KF2 can turn-off very fast, less than 200nS, its turn-on time is much slower. Therefore, a gate boosting circuit is needed to maximize the IGBT switching speed at turn-on. The booster delivers 22A into the gate with a peak voltage of 20V.

As the gate current begins to rise, voltages develop across the 0.5 Ω resistor R4 and trigger the SCR Q1. The capacitor C2, which was pre-charged at 60V by the resistor R1 and the zener diode D5, transfers its energy to the gate through the inductor L1, the common-mode choke T1, and the saturable transformer T2 after a short time delay for the T2 to saturate. The gate voltage rise time as measured is about 150nS. The fall time is slower due to lower gate voltages.

B. Clamping.

After an initial turned-on at full voltages, the remaining gate voltage level is clamped down to less than 15V for the IGBT over-current protection. The gate voltage triggers the SCR Q2 after a time delay that sets by the resistor R6 and the capacitor C3. The transzorb D6 then determines the final voltage. The selected 12V transzorb results in a clamped collector current of about 2200A. Negative gate transient voltages are limited by the 15V bi-directional transzorb D7.

The D3 consists of six transzorbs, rated at 400V each, connected in series. It serves two purposes. In the forward-bias direction, it is a high voltage blocking diode for the collector-emitter de-saturation voltage sensing. In the reverse-bias direction, it provides the over-voltage protection at turn-off during fault conditions. As the peak collector-emitter voltage, V_{CE} , exceeds D3 rating plus 220V of the bi-directional transzorb D4, the current flows to the gate and turns the IGBT back on, thus limits the V_{CE} level. Since the transzorbs have limited dissipation power, they are not intended for repetitive clamping. Power clamping was provided by the snubber capacitor and the fast recovery diode placed in the core driver circuit.

C. De-saturation detection level.

Detection of the de-saturation voltage to shut down the gate pulse for short-circuit protection is commonly used in most driver modules. It works well for long pulse applications where the IGBT is fully on and the collector-emitter saturation voltage, $V_{CE(SAT)}$, is less than the typical 15V supply source. However, with 3 μ S pulse durations and 3000A in the normal operation, the $V_{CE(SAT)}$ is still about 50V. For the protection to work, the detection voltage level must be raised above that voltage. It is done by the use of the 200V source and resistors R2, R3 and R5 to attenuate the measured $V_{CE(SAT)}$ down by a factor of 10 before processing. The buffer U1 provides the impedance isolation between the divider and the driver module resistances. The capacitor C1 along with the driver-integrated resistance sets the detection response time.

D. Short circuit protection.

Besides clamping the gate voltage to control the over-current, additional steps are also taken to limit the initial rising peak current in short-circuit conditions. An emitter-feedback scheme, which based on the voltage developed by di/dt between the control-emitter and the power-emitter terminals, is realized by the use of the saturable transformer T2 placed in the gate current path. As the gate voltage and the peak current rise during a short circuit, the rising di/dt generates a proportional voltage, which coupled through the gate in a reverse direction by the T2, immediately pulls the gate voltage down and stops the rising current. After the clamped gate voltage regains control of the IGBT, the de-saturation detection then kicks in and shuts down the gate pulse with high turn-off

impedances. Figure 3 shows the effectiveness of this short-circuit protection method.

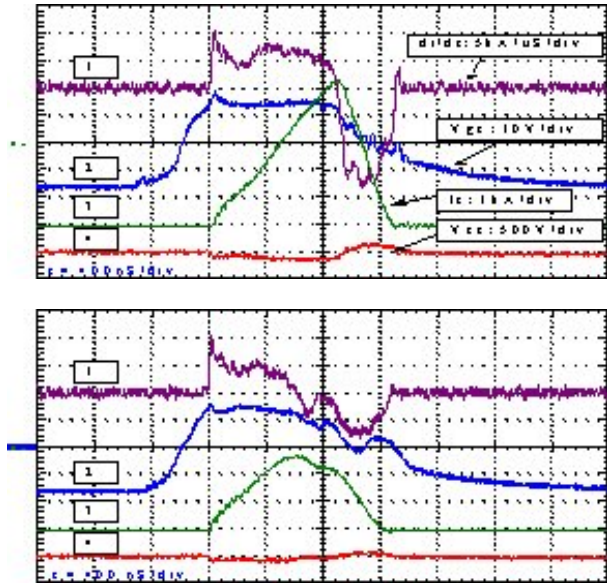


Fig. 3: Upper traces without emitter-feedback protection. Lower traces with the protection. Without protection, the peak current continues to rise as the V_{CE} increases. In the latter case, the current is already reaching its peak and is limiting by the clamped gate voltage.

During the time the initial peak current is falling, high di/dt generate hundreds of volts across the two-emitter terminals. This induced voltage, which coupled with stray capacitances in the driver module, causes the gate-emitter circuit to oscillate at extremely high frequencies that ultimately burns off the gate. The common-mode choke T1 is therefore added to further isolate the IGBT gate-emitter structure from the external driving circuitry.

The T1 consists of a single-turn flexible stripline for minimum inductances and seven magnetic cores. The T2 also has one turn and two cores. The core is Ceramic Magnetic CMD-5005 measured 3/8" O.D. x 3/16" I.D. x 3/16" L.

III. TEST RESULTS

The actual Metglas core driver PC board, with the exception of the current transformer CT and the resistive load, as shown in figure 4, is used to test the new gate driver.

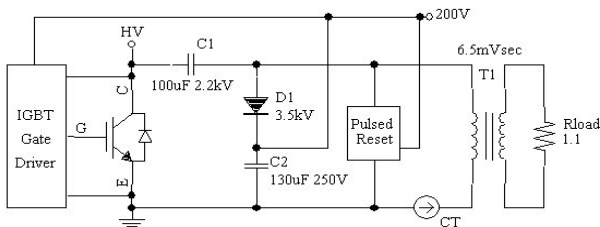


Fig. 4: Metglas core driver circuit.

As the IGBT is turned-on, the storage capacitor C1 transfers its energy to the load through the transformer T1. Fast diode D1 and the pre-charge snubber capacitor C2 catch the reflected energy generated by the T1 stray inductances and capacitances. They also clamp the V_{CE} during normal and fault conditions. A pulse current of 120A resets the core. Load resistances of 1.1 Ω and 0.7 Ω are used for pulse currents of 2000A and 3000A respectively. The waveforms in figure 5 show the tested IGBT at 2600V and 2000A with di/dt of 12000A/ μ S.

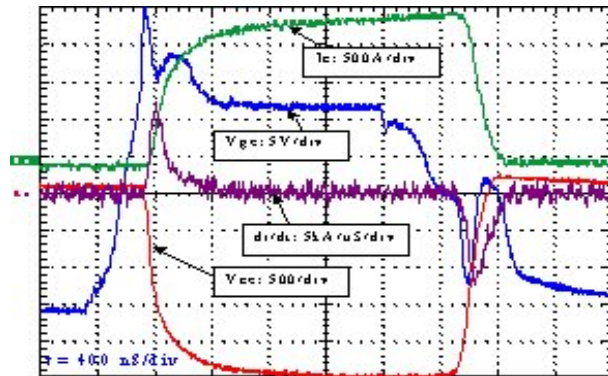


Fig. 5: FZ800R33KF2 in normal operation.

Two modes of short-circuit tests are performed. The hard short defined as the short circuit occurs when the IGBT is in the active region. A power shunt with a resistance of 0.0024 Ω , for current monitoring purposes, replaces the T1 for this test. A DC link voltage of 2200V is then applied before the IGBT switches on. The short-circuit waveforms are shown in figure 6.

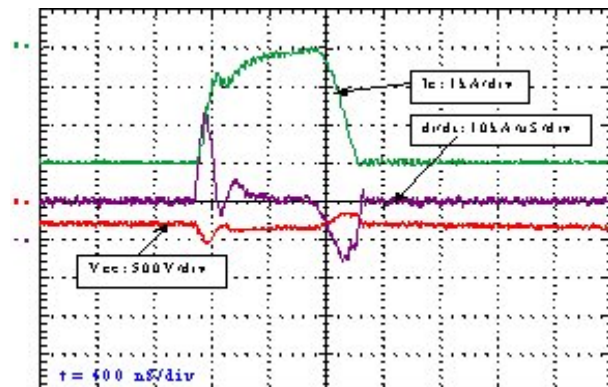


Fig. 6: FZ800R33KF2 hard-short test at 2200V.

A second mode of short circuit, the soft short, is when the IGBT is already turned-on and in the saturation region before the short circuit occurs. While the V_{CE} returns to the active region, high dv/dt that feedback through the gate-collector capacitance, which is also largest during this time, charge the gate-emitter capacitance. Stray inductances in the clamping circuit let the clamped gate voltage to rise resulting in even higher peak currents. Most of the tested IGBTs failed in this type of short-

circuit condition. To simulate this test, the core-reset pulse is removed. It allows the core to saturate into a short. Figure 7 shows the resulting waveforms.

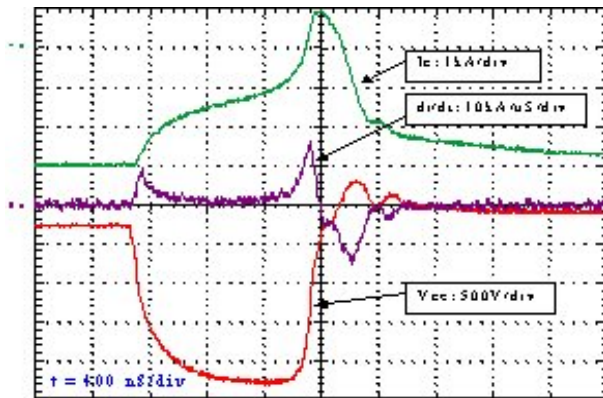


Fig. 7: FZ800R33KF2 soft-short test at 2200V.

Even though the FZ800R33KF2 can drive 3000A with higher gate voltages, it cannot be safely protected during soft-short conditions. New engineering samples with improved internal structure from another Eupec IGBT model FZ600R65KF1 are, however, tested successfully at full load 3000A with 15V gate voltage and reliably short circuit protected at 3000V. Figure 8 and 9 show the full load and short circuit waveforms of the new device.

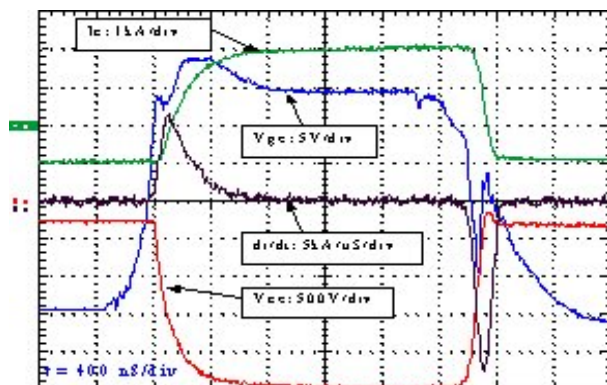


Fig. 8: FZ600R65KF1 in normal operation at 3000A.

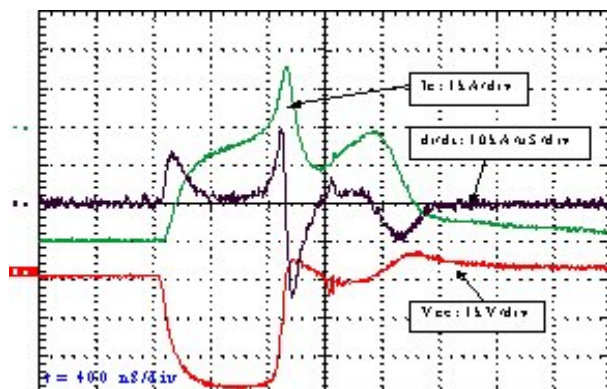


Fig. 9: FZ600R65KF1 soft-short test at 3000V.

Photographs of the gate driver board are shown in figure 10.

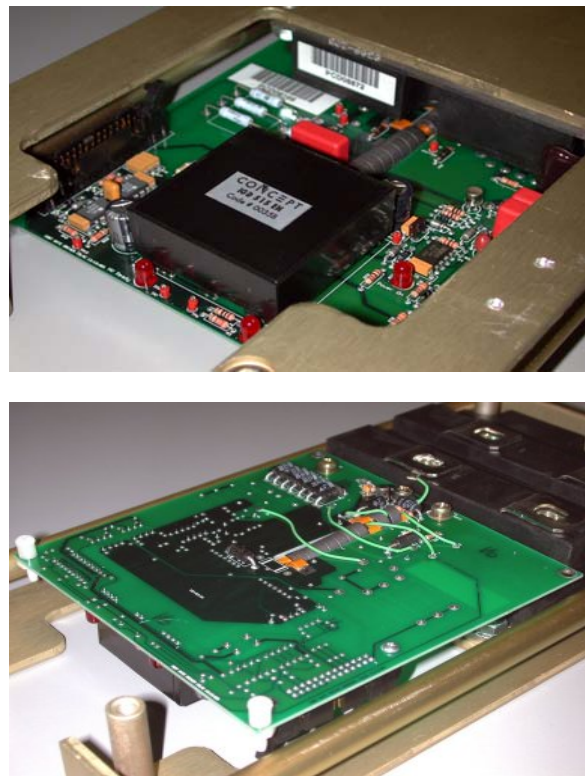


Fig. 10: Gate driver board mounted on IGBT module and the heat sink.

IV. CONCLUSIONS

An IGBT gate drive for the SLAC Induction Modulator has been developed and currently installed in two prototypes, the NLC Klystron Modulator and the 5045 Klystron Modulator [5]. While pushing the current generation of high power IGBT modules into new applications that require high currents, high di/dt and short pulse durations, a new type of IGBT failures has been discovered and new gate drive techniques have been devised to control and protect them.

V. REFERENCES

- [1] R. L. Cassel *et al.*, "A Solid State Induction Modulator for SLAC NLC", Proc. of the 1999 IEEE Particle Accelerator Conf., New York, pp. 1494 – 1496.
- [2] R. L. Cassel and M. N. Nguyen, "A New Type Short Circuit Failures of High Power IGBTs", these proceedings.
- [3] Eupec Electronic Data Book, Eupec Inc., Lebanon, NY.
- [4] Intelligent Power Electronics, CT - Concept Technology, Ltd.
- [5] J. E. deLamare *et al.*, "A Solid State Modulator for Driving SLAC 5045 Klystrons", these proceedings.