

MONOLITHIC ACTIVE PIXEL MATRIX WITH
BINARY COUNTERS IN AN SOI PROCESS*

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Monolithic Active Pixel Matrix with Binary Counters in an SOI Process

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Abstract:

The design of a prototype monolithic active pixel matrix, designed in a $0.15\ \mu\text{m}$ CMOS SOI process, is presented. The process allowed connection between the electronics and the silicon volume under the layer of buried oxide (BOX). The small size vias traversing through the BOX and implantation of small p-type islands in the n-type bulk result in a monolithic imager. During the acquisition time, all pixels register individual radiation events incrementing the counters. The counting rate is up to 1 MHz per pixel. The contents of counters are shifted out during the readout phase. The designed prototype is an array of 64×64 pixels and the pixel size is $26 \times 26\ \mu\text{m}^2$.

Introduction:

The best detector performances in imaging are achieved by providing an electric field in a depleted volume of a semiconductor detector and processing of information in each pixel. Processing functions require complementary transistors and sufficient space, not compromised with charge collecting elements, in each pixel. High resistivity (HR) substrate allows the depletion depths required for good detection efficiency, typically at a bias equal to a few tens of Volts. Unfortunately, HR substrates are not compatible with standard CMOS circuitry. Hence, both elements, i.e. detector wafers and readout chips are typically optimized and processed separately and connection is finally made using bump-bonding or similar process [e.g. 1]. The bump-bonding is expensive and troublesome. Silicon-on-insulator (SOI) process with a detector-grade silicon substrate allows fabrication of a monolithic imager fulfilling the requirements for optimisation of the detector and the processing electronics. The idea of using a thick silicon substrate as a detector volume and processing information in the electronics seated atop of it in an SOI process dates to early 90s [2]. These first attempts were not successful due to still not matured technology and cross-talks. The idea of a monolithic SOI detector was seized on later, resulting in fabrication of testable structures [3]. However, yield was rather poor, and due to the $3\ \mu\text{m}$ technology, the pixel sizes were big with little integrated functionality.

Technology:

The current design is done in the $0.15\ \mu\text{m}$ CMOS fully depleted SOI process by OKI, Japan [4]. The original CMOS process has been modified to include etching of vertical vias, smaller than $1\ \mu\text{m}$ in diameter, in a $200\ \text{nm}$ BOX. The resistivity of the silicon substrate is roughly $1\ \text{k}\Omega\text{cm}$. The vias are openings in BOX during source/drain implantation steps of the formation of MOS transistors, letting implants reaching the bulk [5]. Islands of p^+ or n^+ type are thus obtained avoiding additional

implantation or annealing. The general concept of an SOI monolithic active pixel sensor (MAPS) on a HR silicon substrate is shown in Fig.1. The rectifying junctions are on the BOX side and reverse voltage is applied using a bottom Al plate and/or n^+ contacts on the top side.

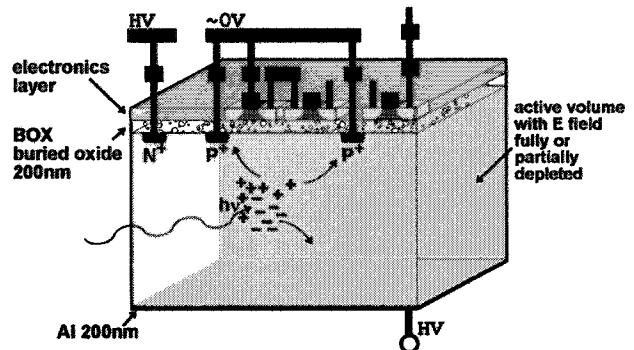


Fig. 1: Concept of a SOI monolithic active pixel sensor on a detector-grade high-resistivity silicon substrate.

A portion of the applied reverse bias is gradually distributed between the p^+ regions in the n-type bulk. This lateral gradient of potential in the surface zone leads to undesired shifts of the threshold voltage of transistors as the bulk may be seen as a back gate electrode. Respecting proper distances between diode implants and using as low as possible voltages for the reverse bias are required to minimize effects on transistors. It is worth noticing that voltage as low as $10\ \text{V}$ is sufficient to deplete about $50\ \mu\text{m}$ of n-type $1\ \text{k}\Omega\text{cm}$ silicon. Remarkably, detector of this thickness is adequate for applications in high energy physics, electron microscopy and imaging of soft X-rays. The separation of $13\ \mu\text{m}$ between diodes was chosen for the current design. The cross-section of the wafer part showing one pixel, peripheral circuitry and bias rings is shown in Fig. 2. The critical dimensions are shown in Fig. 2. The matrix of pixels extends to the right side. The thickness of the detector, delivered from the foundry, is $350\ \mu\text{m}$.

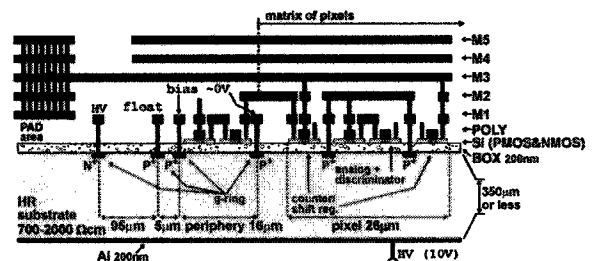


Fig. 2: Cross-section of the wafer part showing one pixel, peripheral circuitry and bias rings designed in the OKI $0.15\ \mu\text{m}$ SOI process.

Pixel Design:

Counting on a single event basis was chosen for the pixel operation, leading to a virtually noiseless image creation. The p-on-n type of the detector implies collection of holes. The pixel circuitry consists of a charge integrating preamplifier with a pole-zero cancellation block, an active continuous time CR-RC² shaping filter, a single threshold discriminator with positive feedback and a 12 bit, binary, ripple counter. A simplified schematic diagram of the pixel circuitry is shown in Fig. 3. The total continuous bias current of the processing chain is below 1 μ A per pixel. The design makes use of three types of transistors available in the process, i.e. high V_{th} , low V_{th} and depletion transistors. The depletion NMOS transistors were used for floating capacitors in the design. The size of the pixel is $26 \times 26 \mu\text{m}^2$ and it contains 280 transistors.

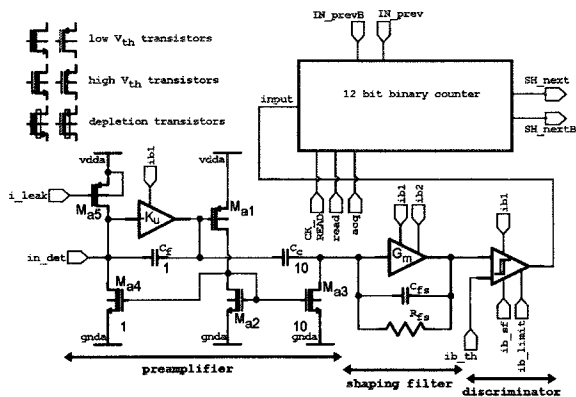


Fig. 3: Simplified schematic diagram of the pixel.

A basic, 12-bit, ripple counter architecture was used in the pixel. This crude counter configuration was chosen rather than the most area efficient pseudorandom counter [6] in order to be able to read directly pixel counts without decoding. The ripple counter was considered easier for handling and debugging during tests. A single bit cell of the counter is a static differential flip-flop built with only 12 transistors. Each cell is equipped with switches, to allow changing the configuration of individual counters in each pixel into a shift register for readout. Pixels are daisy chained and the readout is done with the external clock (CK_READ). During shifting out the contents of counters new initial values, typically all 0s, are shifted in to the matrix. A block diagram of the in-pixel counter configurable to a shift register and a block diagram of the single bit cell are shown in Fig. 4 and Fig. 5, respectively.

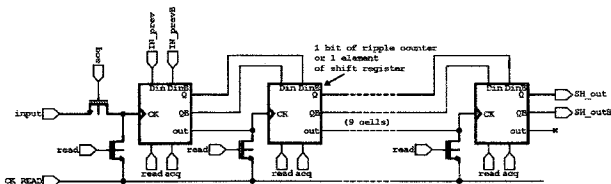


Fig. 4: Schematic diagram of the counter reconfigurable to the shift register.

A differential structure was chosen for the flip-flop in order to limit net cross-talk to the depleted volume underneath the BOX. The schematic diagram of the master/slave flip-flop is shown in Fig. 6. The use of only NMOS transistors as switches required a lowered power supply of 0.7 V for the counter, while the configuration selection is done with signals swinging from 0 to 1 V. All transistors in the counter are designed without connection to the bulk as it is allowed in an SOI process to save area.

The cascade of the preamplifier and the shaping filter provides an equivalent CR-RC² filtering with the peaking time equal to about 150 ns. The gain is nonlinear and the amplitude of time response saturates for input charge packets above $4 \times 10^3 h^+$.

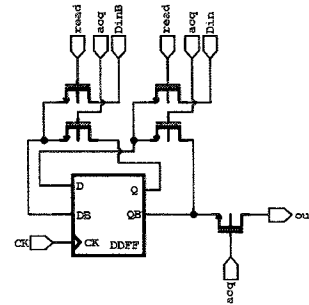


Fig. 5: Schematic diagram of the single bit cell of the counter.

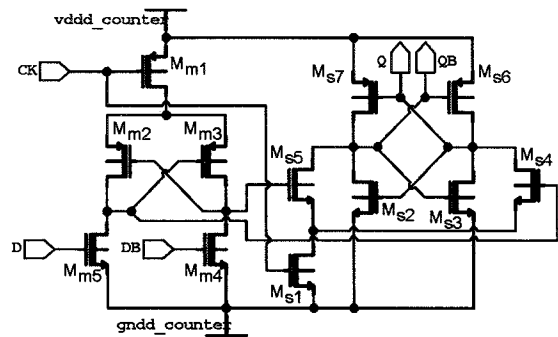


Fig. 6: Schematic diagram of the differential flip/flop used in the design of the counter.

The gain is about $300 \mu\text{V}/h^+$ for signals in the order of $0.5 \times 10^3 h^+$, then it decreases to $200 \mu\text{V}/h^+$ and $175 \mu\text{V}/h^+$ for signals equal to $1.0 \times 10^3 h^+$ and $2.0 \times 10^3 h^+$, respectively. The simulated response of the analog chain for different input charge packets is shown in Fig. 7. The return to the baseline is always within 1 μ s. Some undershoot is observed for higher signals due to the deviation of the transfer function from the ideal form.

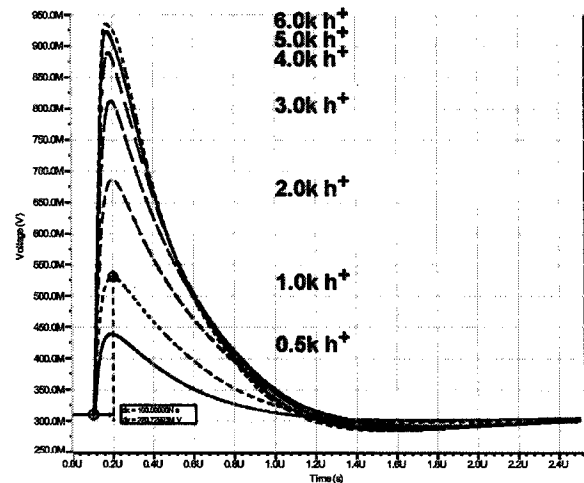


Fig. 7: Simulated response of the shaping filter.

The preamplifier is based on a simply common source inverting stage with a NMOS input transistor biased at a small current of 250 nA. The 5 fF feedback capacitor is used for charge integration. The coupling to the shaping amplifier is provided with a capacitor, whose value is scaled 10 times with respect to the integration capacitance

for gain. The preamplifier features a non-linear pole-zero cancellation circuit. The size of the input device is small, still fulfilling noise matching conditions, since the detector capacitance was estimated in the range of 10 to 20 fF. The leakage current of the detector that may be in the order of 100 fA is absorbed by the preamplifier. The pole-zero cancellation circuitry is self-adapting to the leakage current even above the expected levels [7]. The schematic diagram of the preamplifier is shown in Fig. 8. The preamplifier provides one pole in the transfer function, from the equivalent input capacitance, the feedback capacitance, MC_f , the transconductance of the input device, Ma_8 , and the load capacitance, Ma_6 . Large input charge packets may knock the amplifier out of normal operation for a long time compared to the shaping time. The role of the diode transistor, Ma_9 , is to decrease risk of saturation of the preamplifier.

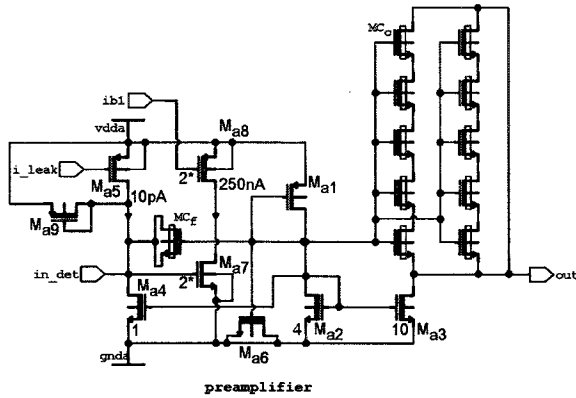


Fig. 8: Schematic diagram of the preamplifier.

The shaping filter is shown in Fig. 9. It uses the transconductance of a common source inverting stage with the NMOS transistor, Ms_1 , the feedback capacitor MC_{fs} and the high value feedback resistor MR_{fs} . The input transistor is biased at 125 nA. The required resistance of several tens of $M\Omega$ s is obtained by biasing the transistor MR_{fs} at constant channel current, equal to 5 nA, and using its channel conductance as a resistance. The gate-source voltage of the transistor, MR_{fs} , is forced constant using a low pass filter realized with transistors MC_s and Ms_6 .

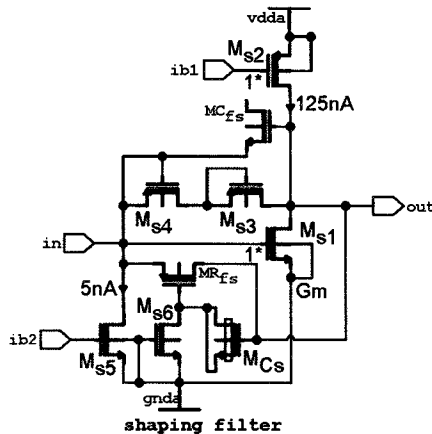


Fig. 9: Schematic diagram of the shaping filter.

Each transistor occupies its own island in a SOI process. This fact allows operation of a transistor without the body effect and is used in the design of the feedback resistance in the shaping filter. The gain limitation, described beforehand, is obtained with two diode-connected transistors Ms_3 and Ms_4 . Their action is to decrease the

equivalent feedback resistance for higher signal amplitudes. They turn on for output signals swinging approximately two threshold voltages above the baseline level. The simulated input referred noise of the analog chain is about $50 e^-$. This value includes only thermal noise, since the model parameters for $1/f$ noise were not available during the design.

The core of the comparator, shown in Fig. 10, is a differential pair with outputs feeding a cross-coupled active load for adding positive feedback. This simple architecture provides a fast comparison result with some hysteresis for noise immunity. The dispersion of comparator offset voltages amidst the electronic noise is critical for a high purity discrimination of signals. The typical value reported in the literature [8] for a pixel design with a differential pair coupled comparator in a hybrid detector is $\sigma=90e^-$ referred to the amplifier input. The presented design features almost three times higher gain, thus the equivalent noise from the offset dispersion is expected to be accordingly reduced. Therefore, the current design uses only a global threshold for the comparator. Two source followers with matched layout, located at the input of the comparator, allow setting of the threshold voltage and provide individual baseline tracking for each pixel. The source follower with the transistor Md_1 is biased at low current. Its response is not linear for fast transient signals and it clips pulses from the shaping filter. The clipped signal is filtered with the low pass filter, built with transistors Md_5 and Md_7 , and is used as a reference for the comparator. The second source follower with the transistor Md_2 is biased at higher current. The difference between gate-to-source voltages of transistors Md_1 and Md_2 defines the threshold for the comparator.

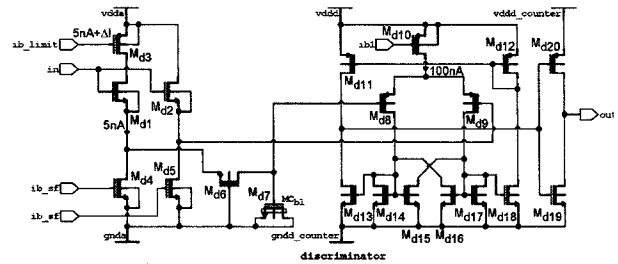


Fig. 10: Schematic diagram of the discriminator with individual for each pixel baseline tracking.

An example of the simulated discriminator response is shown in Fig. 11 for the input packet of $1.0 \times 10^3 h^-$ and the threshold current of 50 nA.

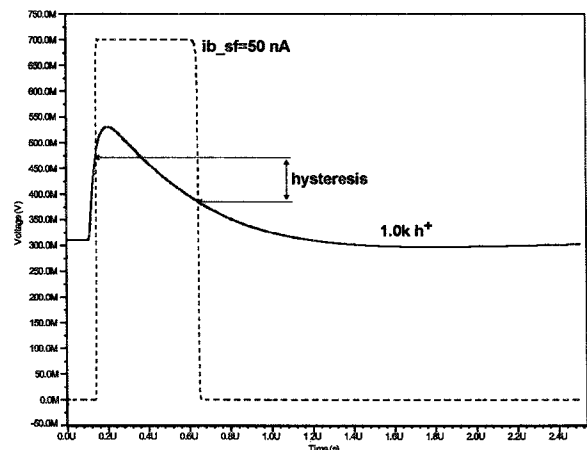


Fig. 11: Example of simulated response of the discriminator.

The analog part and the comparator operate from a single 1 V power supply. An inverter at the output of the comparator is used to adapt voltage levels for the counter. Critical transistors, like input devices of the preamplifier and the shaping filter or current sources were designed with bulk connections. The layout of the pixel is shown in Fig. 12. The central part of the pixel is occupied by the analog circuitry. There are four diodes with their anode terminals ganged and connected to the input of the preamplifier. The 12-bit counter occupies a ring around the analog part.

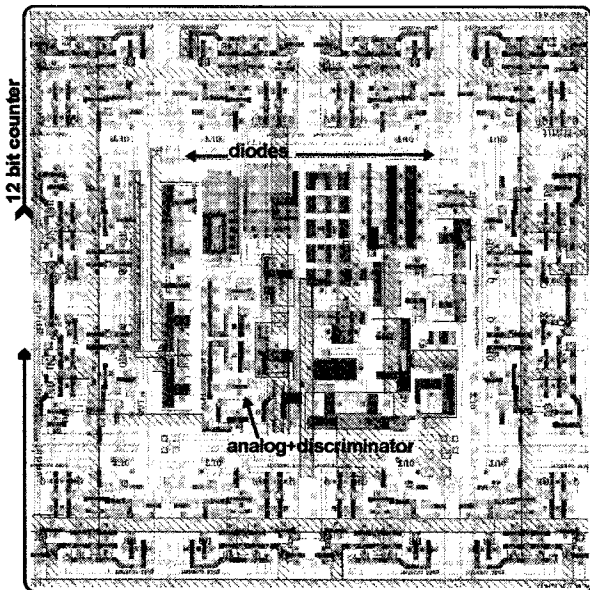


Fig. 12: Layout of the pixel.

Chip operation:

The data acquisition is done in two cycles, i.e. hit acquisition and readout. The selection of the cycle is done with external control signals. The readout of the chip is done through one differential output; the information has to be clocked through all pixels in the array. The maximum counting speed of the pixel counter is designed to be 1 MHz. The simulated response to the sequence of input pulses at 1 MHz rate is shown in Fig. 13. The first read cycle is used to reset the counter, and then the counter is counting comparator triggers in the hit acquisition phase. The second read cycle allows reading out the binary contents of the counter.

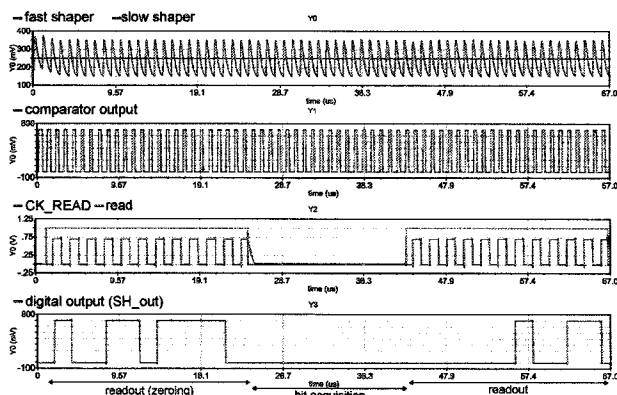


Fig. 13: Simulation of the shaping filter response, discriminator response, zeroing-counting-shifting out phases for the counter and the digital output of the pixel.

The tests of the 64×64 pixels chip are under

preparation. The tests set-up is designed to allow installation inside a vacuum chamber of a transmission electron microscope. The system, consisting of two small PC boards, includes generation of all current and voltage biases, including high voltage for the reverse bias of the detector. Data transfer is done to PC with the USB 2.0 interface.

Conclusions:

The prototype called MAMBO (Monolithic Active pixel Matrix with Binary counters) is aimed at, but not limited to, applications of scientific imaging for direct electron detection in electron microscopy, and soft X-ray imaging in synchrotron radiation or bio-medical experiments. It is one of the first imagers fabricated in an advanced SOI CMOS process modified to the detector needs. The next generation of the imager may include some changes in the concept of the pixel, like use of pseudorandom counters or improvements in the comparator threshold distribution network including a baseline restorer. The analog core of the current pixel design may be considered as a *prêt-à-porter* solution for the particle tracking application in high energy physics using the SOI detector option. However, before this happens, an important test for this new detector technology will be assessment of coupling between the electronics and the fully depleted detector layer. The digital activity on the top layer may lead to induction of charge packets to which analog circuitry may be sensitive. If this undesired coupling takes place, the modification, consisting for example in screening blanket implantation close to BOX, will have to be studied and the process accordingly modified.

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