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Abstract

For many thin-film applications substrate imperfections such as particles, pits, scratches, and general roughness, can nucleate film defects which can severely detract from the coating's performance. Previously we developed a coat-and-etch process, termed the ion beam thin film planarization process, to planarize substrate particles up to ~ 70 nm in diameter. The process relied on normal incidence etching; however, such a process induces defects nucleated by substrate pits to grow much larger. We have since developed a coat-and-etch process to planarize ~70 nm deep by 70 nm wide substrate pits; it relies on etching at an off-normal incidence angle, i.e., an angle of ~ 70^{o} from the substrate normal. However, a disadvantage of this pit smoothing process is that it induces defects nucleated by substrate paticles to grow larger. Combining elements from both

processes we have been able to develop a silicon-based, coat-and-etch process to successfully planarize ~70 nm substrate particles and pits *simultaneously* to at or below 1 nm in height; this value is important for applications such as extreme ultraviolet lithography (EUVL) masks. The coat-and-etch process has an added ability to significantly reduce high-spatial frequency roughness, rendering a nearly perfect substrate surface.

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I. Introduction

For a number of thin-film applications substrate imperfections such as particles, pits, scratches, and general roughness, can nucleate film defects which can severely detract from the coating's performance. An example of a cutting-edge technology requiring nearly perfect substrate surfaces is Extreme Ultraviolet Lithography (EUVL) [1]. EUVL is the leading candidate technology to enable Moore's law[2] to continue beyond the 2009 timeframe[3]. Moore's law is very important for many areas of science and technology which depend on accessing more computational power at flat or lower costs. EUVL mask blanks are fabricated by depositing reflective Mo/Si multilayer thin films on glass substrates and these *reflective* mask blanks, which need to be defect-free, are a significant departure from conventional transmission masks[1,4]. Simulations indicate that substrate pits only several tens of nm in depth and width could perturb the reflective multilayer enough to print as critical defects in extreme ultraviolet lithography tools[5]. Because a single mask would be used to produce many microprocessor chips, even a few mask defects could decrease the yield significantly and have an enormous economic impact, potentially jeopardizng the viability of EUVL. Consequently, it is very important to develop methods to minimize the effect of small substrate pits and scratches on the reflective multilayer film, particularly since no repair technique has even been envisioned for pit-induced coating defects.

One promising approach to eliminating such defects is to develop a thin-film process that sufficiently planarizes the substrate asperities to render them harmless. We have previously shown that by integrating the film deposition process and the direct etching of the film/substrate at normal incidence, the growth of multilayer defects

nucleated by *particles* can be significantly suppressed[6-9]. This is likely due in part to the strong dependence of the etch rate on the local angle of incidence; the etch rate has a peak around an angle of 45 - 50 degrees from the normal as shown in Figure 1. Consequently when etching a defect nucleated by a particle, the sides of the defect etch faster than the top. Figure 2a shows schematically how the defect profile could evolve. The enhanced etching at the sides can cause the profile to narrow until the sides meet and the defect essentially collapses.

Unfortunately, this process is not very effective for the planarization of concave substrate defects such as pits and scratches. The problem is illustrated in Figure 2b. In this case, the enhanced etch rate at the sides of the pit or scratch causes the profile to broaden, which essentially increases the size of the defect. We have observed experimentally that our process, which effectively planarizes particle defects, does not work well on pit defects, as shown in Figure 3. The coating defect nucleated by the pit gets much wider, making it much more difficult to planarize. A technique is therefore needed for planarization of substrate pits and scratches in addition to particles. If one can develop a thin-film-based technique to remove substrate pits and particles *simultaneously*, as well as surface roughness, it will also have applicability in areas in addition to that of EUVL masks, since nearly-perfect substrate surfaces are desirable for a number of applications, such as reflective optics which are being increasingly used for applications such as short-wavelength telescopes. Such a technique to render nearly perfect substrate surfaces has been developed and is described and demonstrated in this paper.

II. Procedure and Process Improvement

a) Fabricating substrates with programmed defects

In order to investigate the smoothing of pits we first needed to produce pits with the proper depths and widths. Since we have a significant amount of experience[9] smoothing ~70 nm particles we chose ~70 nm deep pits to begin our investigation. We also aimed for an aspect ratio of ~1 (i.e., ~ 70 nm wide pits) although we have less accuracy and control of the exact width than we do over the depth. The pit defects were synthesized by electron beam lithography on Si substrates using a process described in detail elsewhere[10]. A spin-on-glass resist (HSQ) process was employed and the pits were formed in a highly robust silicon oxide. For this study we also utilized lithographically-patterned particles with the proper heights and widths. The separate particle and pit defect substrates consisted of defects having the same depth but a variety of widths. Prior to planarization these programmed substrate defects were characterized on a Digital Instruments Atomic Force Microscope (AFM). We targeted a depth/height value of ~ 70 nm and came close to this according to the AFM measurements; the mean depth of the pits was ~ 68 nm and the mean height of the particles was ~ 71 nm. To simplify the discussion we will be focusing on substrate defects with an aspect ratio of 1 and will be referring to substrate defects ~70 nm deep or high by ~ 70 nm wide as “70 nm pits” or “70 nm particles”. While the pit defects are new, the particle-like substrate defects are very similar to those used and described previously[9]. The surface roughness of the samples with the pit substrate defects was ~ 0.7 nm rms, which is rougher than the < 0.2 nm rms generally obtained for the particle defect samples. Since the work that is

described in this paper the roughness of the pit substrate defect samples has been reduced further [10] by using a different process.

b.) Improving the Ion beam Thin Film Planarization Process.

As described previously[7,9], the ion beam thin film planarization process uses a *multilayer*-based coat-and-etch process shown schematically in Figure 3. Alternating layers of molybdenum (Mo) and silicon (Si) layers are deposited each several nm thick. For the Si layers, ~1-2 nm more Si is deposited and then etched away. This process was successfully used to smooth particles up to ~80 nm in diameter; however, this process was limited for pit smoothing, as shown in Figure 3. One possibility to enhance the performance of the smoothing process was to deposit much more Si and etch it away, but there are disadvantages with this approach. The pitfalls include argon incorporation, larger errors in the multilayer period, potential interface roughening, and a longer process time. The first three are issues only if the Mo/Si is to be used as the reflective layer for EUV lithography applications. An alternative approach is to eliminate the Mo layers altogether and use a *Si-only* ion beam thin film planarization process to smooth surface defects prior to the deposition of a reflective Mo/Si multilayer film. This frees one to develop and apply a more potent smoothing process since most (or all) of the Si can be etched away. A potential negative consequence of this approach is the potentially higher stress of the Si versus Mo/Si[11]; however, the fact that one could conceivable leave a smaller amount of residual film at the end of the process mitigates the effect of the higher

Si stress. All of results described in this paper derive from this improved version of the ion beam thin film planarization process.

Unless noted otherwise, approximately 8.7 nm of Si was deposited and different amounts were etched, as will be described when the results are presented and discussed. The deposition flux was directed at approximately normal incidence for all runs; the etch angle was varied, as will be described when the results are presented and discussed.

The primary ion source beam energy was 600 eV; these are the ions used to generate the deposition flux from the target. The energy of the secondary ion source, used for etching of the Si in the smoothing process was 250 eV. Argon was used as the source gas for both ion sources. A schematic diagram of the deposition system is shown elsewhere[7,9].

c) Characterization of substrate defects after planarization

After the application of the Si coat-and-etch process the samples were measured again with AFM to characterize the depth (for pits) and height (for particles) and width of the defects at the film surface. The values were determined by averaging over a number of defects, and the quoted error is the standard deviation of the values. Specifics about process parameters for particular coating runs, when and where appropriate, are listed throughout the tables and text.

Cross-sectional transmission electron microscopy (XTEM) samples were made by locating and sectioning the area of interest with a FEI 835 dual beam focused ion beam tool and then imaging the section in a JEOL 2010 TEM. Fiducial marks are located with the SEM and a thin, electron-transparent slice is milled out of the sample at the position

of the defect. A sacrificial layer of platinum is deposited on the sample surface before milling in order to prevent staining of the sample by the gallium ion beam. A final cleaning takes place using a low voltage ion beam to remove any material that may have re-deposited during sectioning. The section is placed on a copper grid and imaged in the TEM at a voltage of 200 kV.

III. Results and Discussion

A.) Planarization of pits

We discovered that the key element in a process to successfully smooth pit defects was to conduct the etching at angles well away from normal incidence The initial layer was deposited with an etch angle of ~ 70° and ~ 7.6 nm of the Si was removed for each coat-and-etch cycle; this process was repeated for 25 cycles. Characterization of the pits showed that the pits had been smoothed below the detectability threshold, which is estimated to be ~1 nm due primarily to the roughness of the surface; this process, not including mechanical motion, took ~ 82 minutes. The roughness after this process step was 0.88 nm rms, from the original ~0.68 nm rms. Thus unlike normal incidence etching[7,9,12], more oblique etch angles tended to increase the surface roughness (at least for the off-normal angles that we sampled). This is not a significant issue since to reduce the surface roughness we can apply a Si-only coat and etch process with a normal incidence etch angle. This was performed followed by the deposition of a standard Mo/Si multilayer with a bilayer period thickness of 6.9 nm; the roughness was reduced to 0.29 nm after these process steps were applied. The EUV reflectivity of the coating was measured; the peak reflectivity of 65.3% that was obtained is only slightly lower than the

peak reflectivity of 67.6% obtained from a sample produced in the same deposition run on a smooth Si substrate.

The key planarization mechanism in this process is expected to be shadowing, as illustrated in Figure 5. Due to shadowing, the etch rate at the bottom of the pit or scratch is essentially zero. The large difference between the etch rates at the surface of the film and the bottom of the defect causes the depth of the defect to rapidly decrease. Another potentially important contributor to the filling of the pits and the planarization process is redeposition of the etched material within the pit. The planarization model[8], which relies on surface relaxation and the dependence of the etch rate as a function of angle (Figure 1), has done a good job of describing particle planarization, but did not perform well when first applied to the planarization of pit defects. Incorporating the effects of shadowing and redeposition into the model produced simulations which were in good agreement with experimental results for pit smoothing at a 250 eV etch. These calculations and results may be discussed in more detail in a future publication.

B.) Planarization of Pits: Comparison of processes which etch during deposition versus after deposition.

The ion beam thin film planarization process[9 7] uses a sequential coat-and-etch process as described in section II. One wonders if similar planarization performance could be obtained by etching *during* deposition, as opposed to etching inbetween deposition steps. We performed a side-by-side comparison to evaluate this. Due to the inherent etch and deposition rates it was not possible to etch 7.6/8.7, or 87% of the silicon as was done in section IIA. We instead etched ~5.5 nm of the ~9 nm thick layers of

silicon and repeated this for 16 cycles. This yielded an equivalent amount of deposition and etching to a sample that was etched during deposition. We did not do 25 cycles as in section IIA since a side-by-side comparison might be problematic if both processes completely removed the pits; with a reasonable amount of the defect left unplanarized one could more effectively gauge any differences in the planarization performance of the two processes.

The mean depth and full-width-at-half-maximum (FWHM) of the ~ 70 nm substrate pits after planarization with the process that etches during deposition was -13 nm and 41 nm respectively. This is a little lower but reasonably close to the mean depth and FWHM values of -11 nm and 35 nm obtained for the ~70 nm substrate pits after planarization with the standard coat-and-etch process. The surface roughness of 0.47 nm rms for the etch-during-deposition process was a little higher than the roughness of 0.36 nm rms from the coat-and-etch process. Overall the results suggest that the planarization of substrate pits and the resulting surface roughness is slightly better with the coat-and-etch process. One item to note is that the coat-and-etch process will also take a little more time than the etch-during-deposition process.

C.) Planarization of Pits/Scratches and Particles *Simultaneously*

A key component of the pit planarization technique described above is to use an incidence etch angle that is significantly off-normal (e.g., about 70 degrees from normal). While excellent pit/scratch planarization occurred under these conditions, there were two drawbacks. The first, which is by far the most important drawback, is that substrate particles

are not planarized since they actually nucleate larger defects under these conditions. The second drawback is that the roughness of the surface was increased, requiring an additional step designed to reduce the high-spatial frequency roughness, as discussed above. An improved process which enables pits and particles to be smoothed simultaneously and which results in a low surface roughness is described below.

A key component of the improved process was the fact that the *design of the first process step should emphasize pit planarization without causing the substrate particle induced defects to get too large*. This entails using an etch angle closer to normal incidence that the 69 degree values used previously. Modeling suggested that a 45 degree etch angle could be a good compromise between pit smoothing and particle enlargement, since the widths of the defects nucleated by particles generally increase with increasing etch angle. A secondary consideration was that the roughness, particularly the mid-spatial frequency roughness, increased for etch angles > 45 degrees. For the first step of this new process, about 7.4 nm of the 8.7 nm of Si deposited per cycle was etched away. This sequence was repeated 15 times.

The second and subsequent planarization process steps were designed to emphasize particle planarization but to also have a beneficial effect on pit and scratch planarization. For this an etch angle of 0 degrees was used (normal incidence). For most of these process steps about 7.4 nm of the 8.7 nm of Si deposited per cycle was etched away; however, for a small fraction of the cycles, about 1.2 nm more was etched away than was deposited per cycle, i.e., 9.9 nm, which was found to enhance the planarization. To do this for more than several cycles can results in turning the particle into a significant crater in the

substrate, which can be undesirable. Table 1 lists all of the process steps that were used in the demonstration.

The particle and pit samples used in the Table 1 process sequence had a standard Mo/Si reflective multilayer film deposited on them. Figure 6a shows a cross-sectional AFM scan of the planarized pit defect along with the profile of the pit before planarization. Figure 6b is a close-up of the smoothed pit; the pit shape is difficult to see due to the higher surface roughness of the pit samples prior to planarization (as discussed in section IA). Figure 7a shows a cross-sectional AFM scan of the planarized particle defect along with the profile of the particle before planarization. Figure 7b is a close-up of the smoothed particle. Smoothing the particles (or pits) to ~ 1 nm or lower is important since this is where the defects begin to be noncritcal[5,13].

Cross-sectional transmission electron microscopy was performed on the samples and the images are shown in Figure 8 and 9 below for smoothed lines and trenches respectively. These images, coupled with the AFM profiles shown in Figure 6 and 7, convincingly demonstrate the effectiveness of the planarization process. It should be noted that the process time (not including mechanical motion) for the Table 1 process is ~ 7.5 hours. For EUVL mask blank fabrication it is important that this time be reduced; this work is underway and will be reported in a future publication. Also for EUVL mask applications it is important that the planarization process not add significant numbers of particles[14] and future work is planned in this area on an ultraclean deposition tool located at another institution[15].

D.) Planarizing Substrate Roughness

The reflectivity of EUV multilayer films is highly dependent on the high spatial frequency roughness of the underlying substrate.[16] For an EUVL lithography tool the throughput (i.e., how many wafers containing integrated circuits a tool can process per hour) is very dependent on the reflectivity of the reflective optics and mask in the tool (although the optics have more importance since they represent several reflections versus one for the lone mask). One can planarize roughness by etching the Si layers in a Mo/Si multilayer film or by etching the Si layers in a pure Si planarization layer and then deposit the (unetched) Mo/Si multilayer on top of the planarization layer. One disadvantage of the former process is that with heavy etching one can entrap a significant amount of inert gas (such as Ar) into the film from the ion source, and this will reduce the EUV reflectivity of the multilayer film. One may also increase the roughness of the Mo-Si interfaces with heavy etching as well as increase thickness errors, increasing wavelength errors in the reflected EUV light . By employing the present technique, one can coat and etch (and etch significantly) to planarize substrates with large roughness values and the multilayer needs to only be deposited after this process is completed, so there is no resulting damage to the multilayer.

As a demonstration this new process has been used to smooth a substrate having an initial roughness of 0.75 nm rms to a roughness of 0.20 nm rms. This process makes such a substrate smooth enough to use it for reflective optics in an EUVL stepper without the need for super-polish. Figure 10 shows the surface of the substrate before and after applying the present coat-and-etch planarization process. Figure 11 shows the power spectral density before (black) and after planarization (red, dashed). The measured EUV reflectivity after a standard Mo/Si multilayer film was deposited on the planarized substrate

was 65.5%; to the best of our knowledge this is a record EUV reflectivity for deposition on such a rough (0.75 nm rms) substrate.

IV. Conclusions

Our previous coat-and-etch process which successfully planarized ~70 nm substrate particle defects[9]and relies on normal incidence etching induces substrate pit defects to grow larger. We have developed a process to planarize ~70 nm substrate pits; it relies of utilizing etching at an off-normal angle. It also requires only silicon be used, i.e., not Mo/Si as was previously employed[6,7,9]. A disadvantage of this pit smoothing process is that it induces defects nucleated by substrate particles to grow larger. Combining some of the elements from both processes we have been able to successfully planarize ~70 nm substrate particles and pits *simultaneously* to at or below 1 nm in height, a value important for applications such as extreme ultraviolet lithography masks. The silicon-based coat-and-etch process has an added ability to significantly reduce high-spatial frequency roughness, generating a nearly perfect substrate surface.

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Tables

Table 1. The process sequence for planarizing ~70 nm substrate pits and particles simultaneously. In each cycle ~ 8.7 nm of Si was deposited before being etched by the amount denoted in the Table.

Sample #	# of cycles	Amount of Si etched per cycle (nm)	Pit depth (nm)	Pit FWHM (nm)	Particle depth (nm)	Particle FWHM (nm)	Etch angle (deg)
V1799	15	7.4	- 12.1	51.1	62.8	151.7	45
V1800	20	7.2	- 2.1	155.3	5.86	193.4	0
V1801	5	9.9	- <1	-	-	-	0
V1808	40	7.4	- 0.3	-	1.39	376.3	0
V1816	60	7.2	-0.3	“	1.03	387.2	0

Figure captions

Figure 1. The Si etch rate, normalized to the normal-incidence etch rate (0^o), as a function of incident angle for argon ions with an average energy of 250 eV.

Figure 2. Illustration of the progressive effect of normal incidence etching on a film defect nucleated by (a) a particle and (b) a pit.

Figures 3. Cross-sectional surface profile as measured by AFM for a ~70 nm deep by ~70 nm wide pit (far left), the pit after deposition of a standard Mo/Si coating (~350 nm thick) and after application of our planarization process which successfully smoothed ~ 80 nm diameter particles to less than 1 nm in height[9].

Figure 4. Illustration of the silicon coat-and-etch process used to planarize the substrate surface.

Figure 5. Illustration of how off-normal incidence etching can planarize substrate pits.

Figure 6. Cross-sectional surface profile as measured by AFM for (a) a ~70 nm deep by ~70 nm wide pit before and after application of the planarization process and (b) close-up of the smoothed pit. This pit was smoothed in the same experimental run as the particle shown in Figure 7.

Figure 7. Cross-sectional surface profile as measured by AFM for (a) a ~70 nm deep by ~70 nm wide particle before and after application of the planarization process and (b) close-up of the smoothed particle.

Figure 8. Cross-sectional TEM image of a substrate trench which was successfully planarized with the silicon coat-and-etch process described in Table 1 and then overcoated with a

reflective Mo/Si multilayer film. This planarization was accomplished in the same experimental runs as the substrate line shown in Figure 7.

Figure 9. Cross-sectional TEM image of a substrate line which was successfully planarized with the silicon coat-and-etch process described in Table 1 and then overcoated with a reflective Mo/Si multilayer film. This planarization was accomplished in the same experimental runs as the substrate trench shown in Figure 6.

Figure 10. Surface topography, as measured by AFM, for zerodur substrates before and after planarization.

Figure 11. Power spectral density curves, extracted from AFM measurements, for a zerodur substrate before and after planarization. The integrated roughness of 0.75 nm rms was reduced to 0.20 nm rms.

Figures

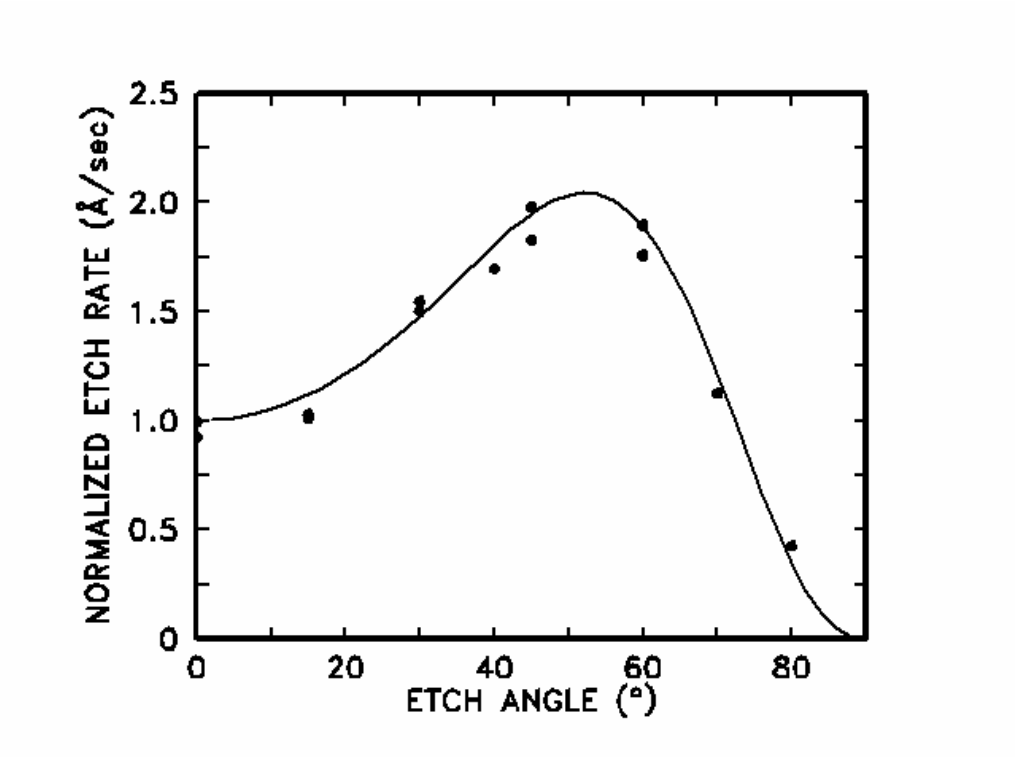


Figure 1

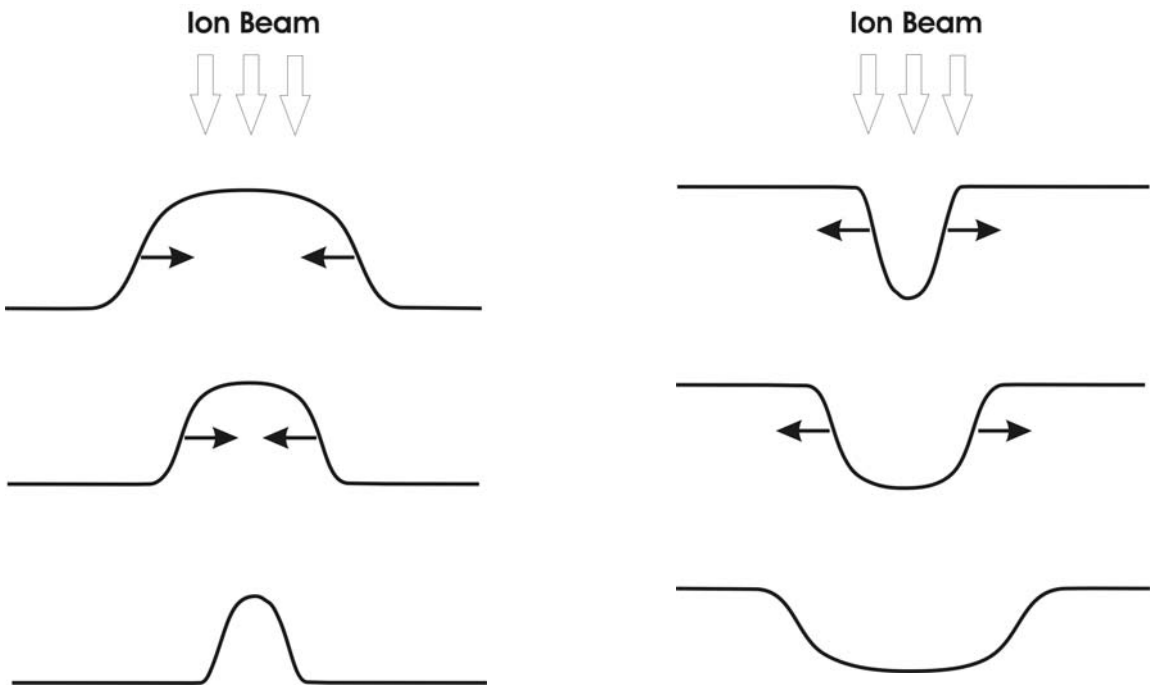


Figure 2

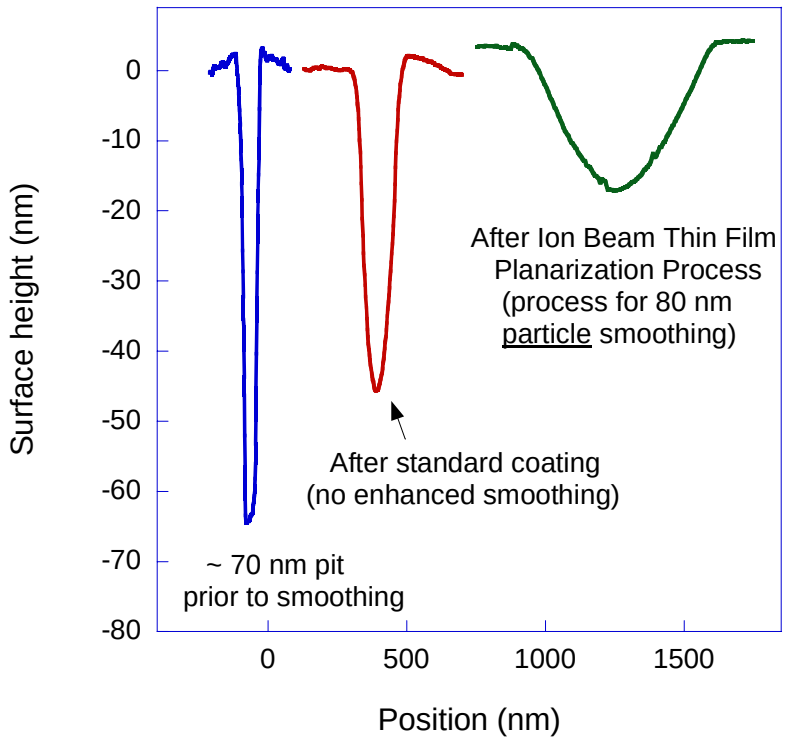

Surface height (nm)
0
-10
-20
-30
-40
-50
-60
-70
-80
0
500
1000
1500
Position (nm)
After Ion Beam Thin Film
Planarization Process
(process for 80 nm
particle smoothing)
After standard coating
(no enhanced smoothing)
~ 70 nm pit
prior to smoothing

Figure 3

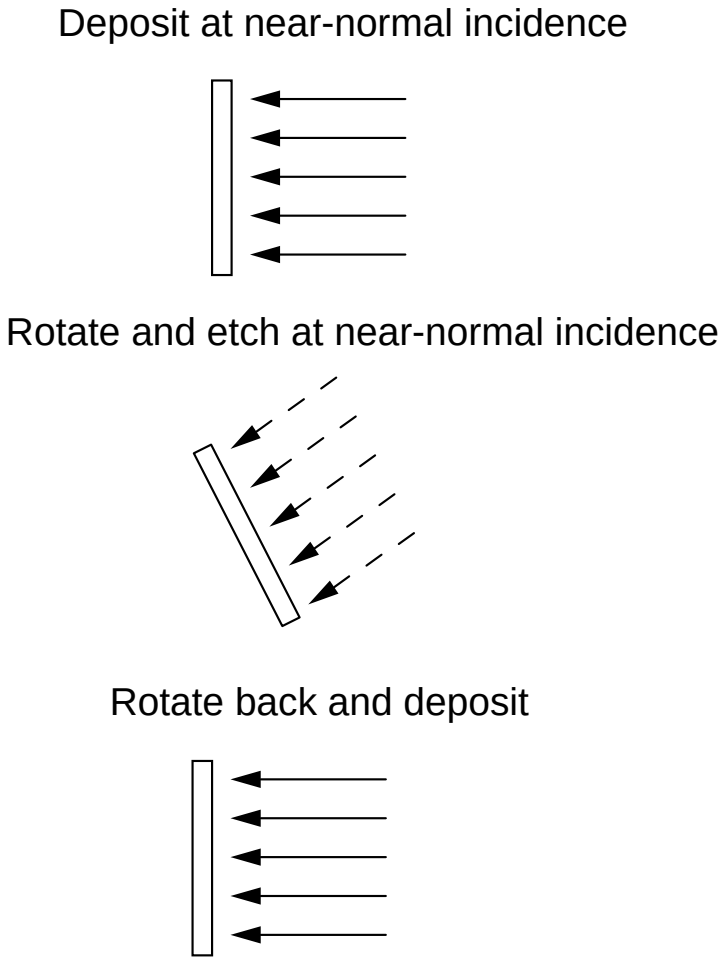

Deposit at near-normal incidence
Rotate and etch at near-normal incidence
Rotate back and deposit

Figure 4.

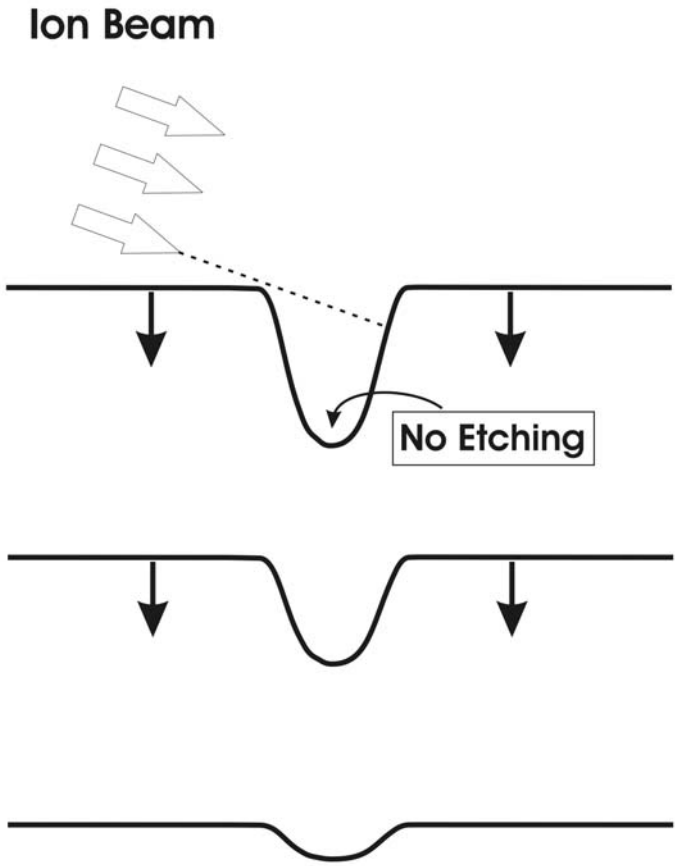
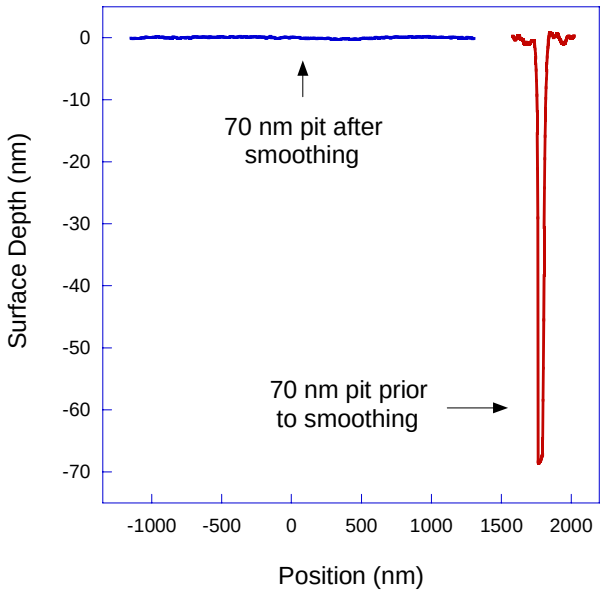
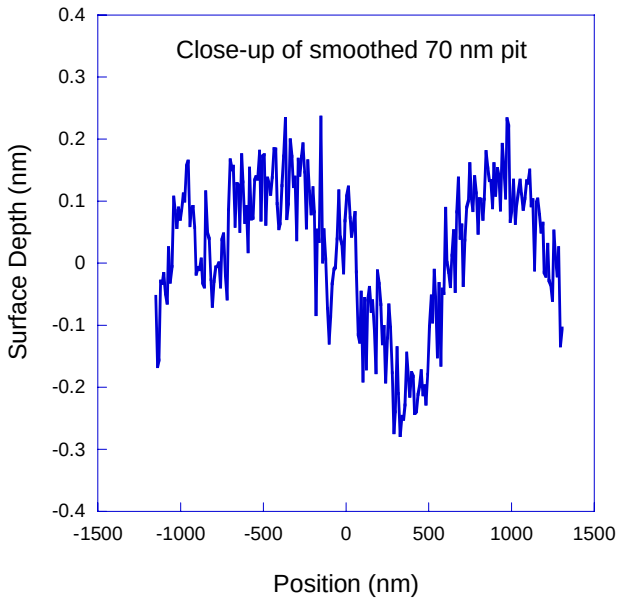


Figure 5

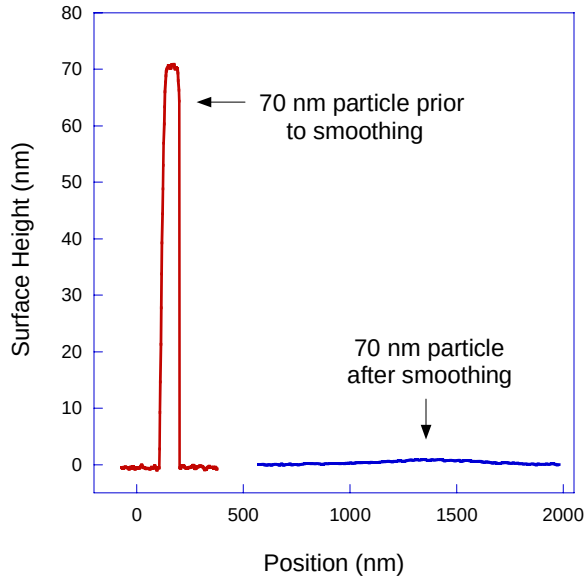

0
-10
-20
-30
-40
-50
-60
-70
Surface Depth (nm)
70 nm pit after
smoothing
70 nm pit prior
to smoothing
-1000
-500
0
500
1000
1500
2000
Position (nm)

(a)

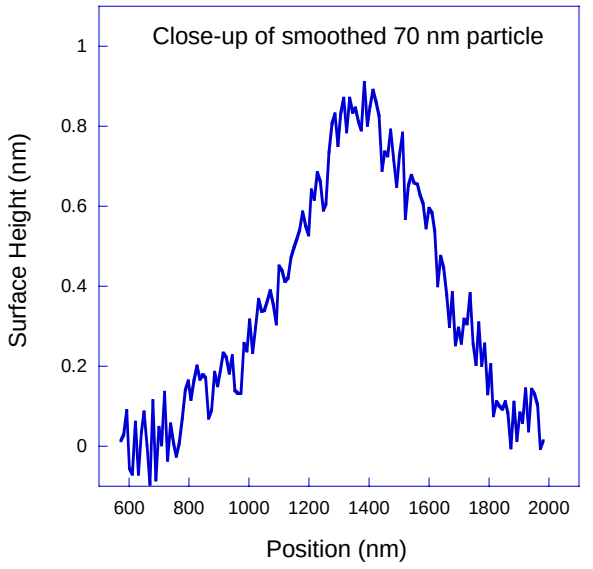

Close-up of smoothed 70 nm pit
0.4
0.3
0.2
0.1
0
-0.1
-0.2
-0.3
-0.4
Surface Depth (nm)
-1500
-1000
-500
0
500
1000
1500
Position (nm)

(b)

Figure 6


80
70
60
50
40
30
20
10
0
Surface Height (nm)
70 nm particle prior
to smoothing
70 nm particle
after smoothing
0
500
1000
1500
2000
Position (nm)

(a)


Close-up of smoothed 70 nm particle
1
0.8
0.6
0.4
0.2
0
Surface Height (nm)
600
800
1000
1200
1400
1600
1800
2000
Position (nm)

(b)

Figure 7

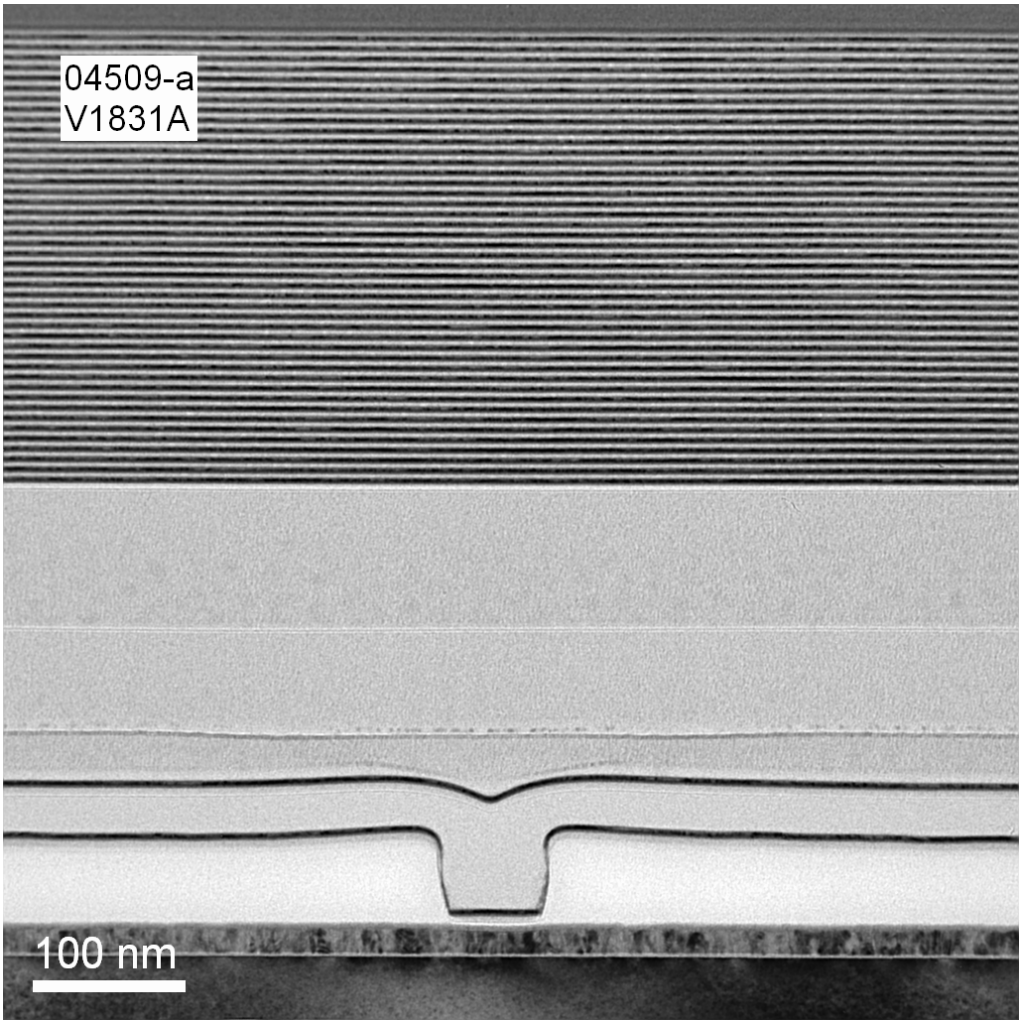


Figure 8

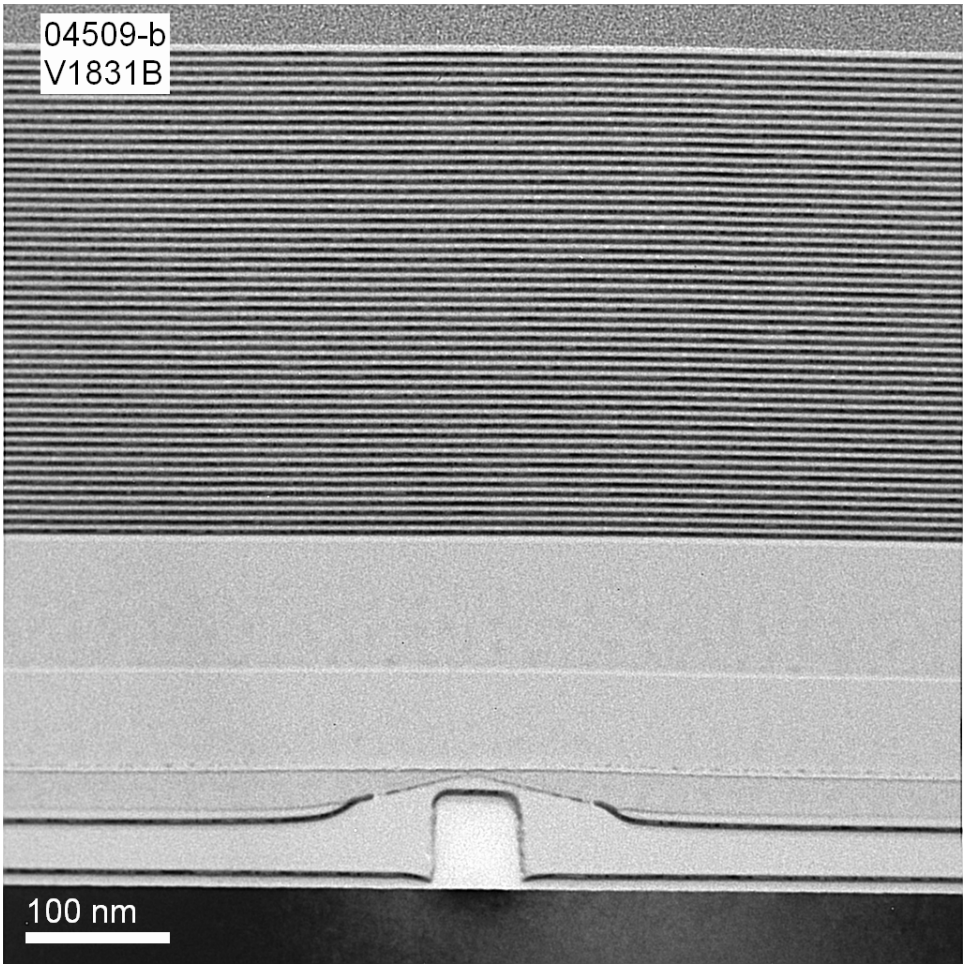


Figure 9

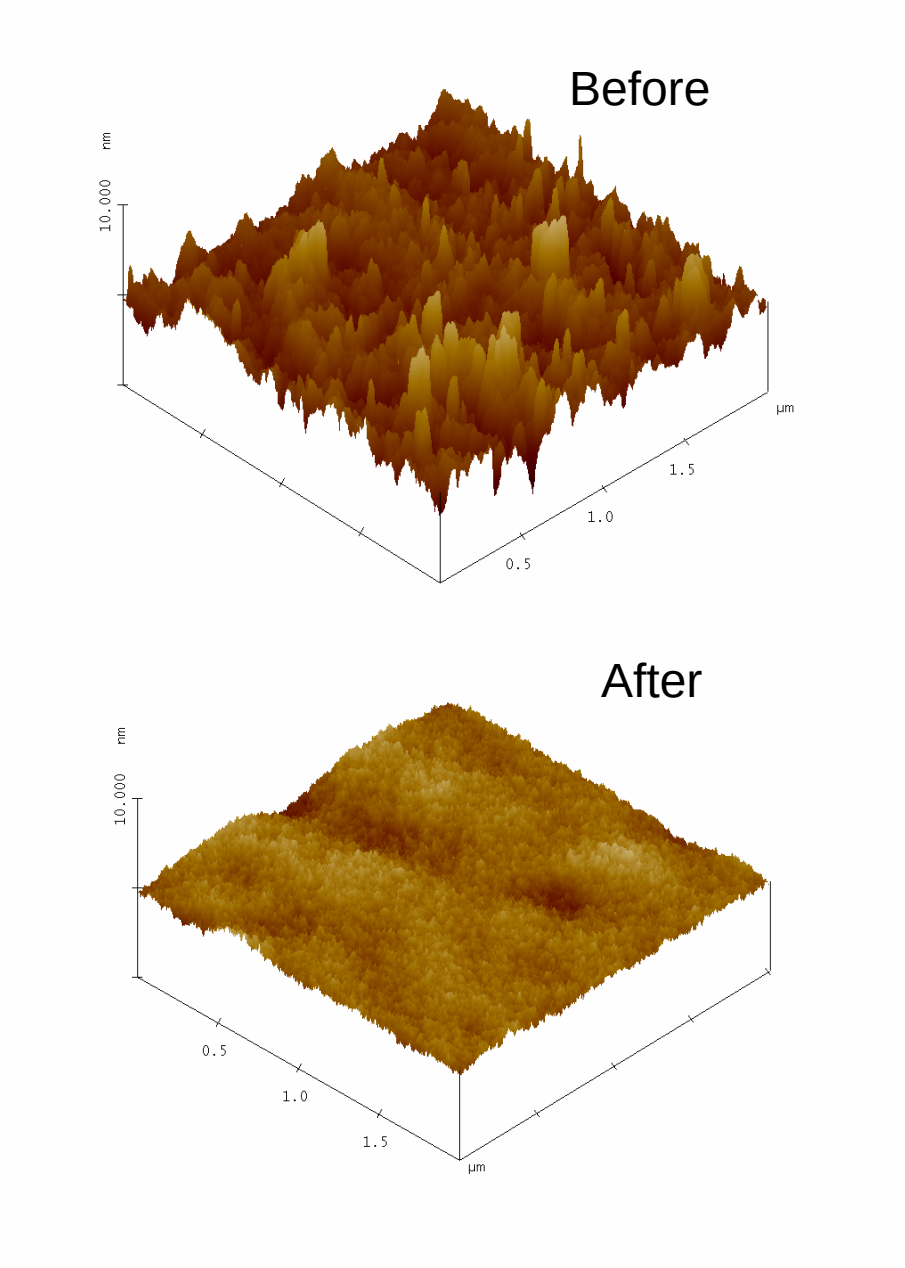


Figure 10

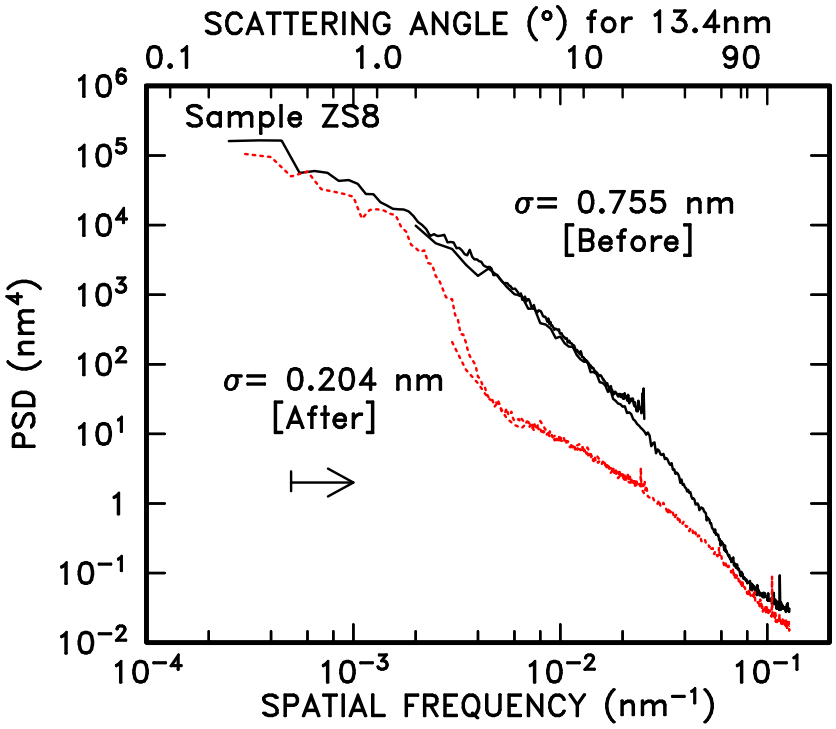

SCATTERING ANGLE (°) for 13.4nm
0.1
1.0
10
90
Sample ZS8
σ= 0.755 nm
[Before]
σ= 0.204 nm
[After]
PSD (nm⁴)
SPATIAL FREQUENCY (nm⁻¹)

Figure 11