SANDIA REPORT
SAND2006-6940
Unlimited Release
Printed November 2006

Electroforming of Bi(1-x)Sb(x) Nanowires for High-Efficiency Micro-Thermoelectric Cooling Devices on a Chip

Final LDRD Report

Michael P. Siegal, Donald L. Overmyer, William G. Yelton, and Edmund B. Webb III

Prepared by
Sandia National Laboratories
Albuquerque, New Mexico 87185 and Livermore, California 94550

Sandia is a multiprogram laboratory operated by Sandia Corporation,
a Lockheed Martin Company, for the United States Department of Energy's
National Nuclear Security Administration under Contract DE-AC04-94AL85000.

Issued by Sandia National Laboratories, operated for the United States Department of Energy by Sandia Corporation.

Available to DOE and DOE contractors from
U.S. Department of Energy
Office of Scientific and Technical Information
P.O. Box 62
Oak Ridge, TN 37831

Telephone: (865) 576-8401
Facsimile: (865) 576-5728
E-Mail: reports@adonis.osti.gov
Online ordering: http://www.osti.gov/bridge

Available to the public from
U.S. Department of Commerce
National Technical Information Service
5285 Port Royal Rd.
Springfield, VA 22161

Telephone: (800) 553-6847
Facsimile: (703) 605-6900
E-Mail: orders@ntis.fedworld.gov
Online order: http://www.ntis.gov/help/ordermethods.asp?loc=7-4-0#online

SAND2006-6940
Unlimited Release
Printed November 2006

Electroforming of $Bi_{1-x}Sb_x$ Nanowires for High-Efficiency Micro-Thermoelectric Cooling Devices on a Chip

Michael P. Siegal and Donald L. Overmyer
Advanced Materials Sciences Department

William G. Yelton
Photonic Microsystems Technologies Department

Edmund B. Webb III
Computational Materials Sciences and Engineering Department

Sandia National Laboratories
P.O. Box 5800
Albuquerque, NM 87185-1421

ABSTRACT

Active cooling of electronic systems for space-based and terrestrial National Security missions has demanded use of Stirling, reverse-Brayton, closed Joule-Thompson, pulse tube and more elaborate refrigeration cycles. Such cryocoolers are large systems that are expensive, demand large powers, often contain moving parts and are difficult to integrate with electronic systems. On-chip, solid-state, active cooling would greatly enhance the capabilities of future systems by reducing the size, cost and inefficiencies compared to existing solutions. We proposed to develop the technology for a thermoelectric cooler capable of reaching 77K by replacing bulk thermoelectric materials with arrays of $Bi_{1-x}Sb_x$ nanowires. Furthermore, the Sandia-developed technique we will use to produce the oriented nanowires occurs at room temperature and can be applied directly to a silicon substrate. Key obstacles include 1) optimizing the $Bi_{1-x}Sb_x$ alloy composition for thermoelectric properties; 2) increasing wire aspect ratios to 3000:1; and 3) increasing the array density to $\geq 10^9$wires/cm^2. The primary objective of this LDRD was to fabricate and test the thermoelectric properties of arrays of $Bi_{1-x}Sb_x$ nanowires. With this proof-of-concept data under our belts we are positioned to engage National Security systems customers to invest in the integration of on-chip thermoelectric coolers for future missions.

Acknowledgements

We thank Prof. Angie Stacy and her students, Jenny Keyani and Lynn Trahey, from the University of California – Berkeley for providing support growing BiSb nanowires and performing thermoelectric measurements. We thank Prof. Patrick Schelling from the University of Central Florida for assisting with the development of computational models. We also thank our students Benet Grill and Natalia Gurule who worked hard to develop electrochemical methods for both anodization and nanowire deposition. This work was supported entirely by Laboratory Directed Research and Development. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, or the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

Table of Contents

List of Figures

Electroforming of $Bi_{1-x}Sb_x$ Nanowires for High-Efficiency Micro-Thermoelectric Cooling Devices on a Chip

I. Introduction

In 1821, Seebeck discovered that dissimilar metals connected at two different locations (junctions) develop a micro-voltage if the two junctions are held at different temperatures. This is known as the "Seebeck effect" and is the basis of thermocouple thermometry.

In 1834, Peltier discovered the inverse of the Seebeck effect, known as the "Peltier effect." If a voltage is applied to a thermocouple, a temperature difference occurs between the junctions. This results in a small heat pump, or thermoelectric cooler (TEC).

Practical TECs use thermocouples in series to allow substantial heat transfer. Semiconductors like Bi, Sb, and Te are commonly used since they are poor thermal conductors. They are also heavily doped to improve their electrical conductivity. These combinations result in the highest possible thermoelectric figure of merit, ZT. Since peltier elements are active heat pumps, they can cool components below ambient temperature, which is not possible using conventional cooling or even heat pipes.

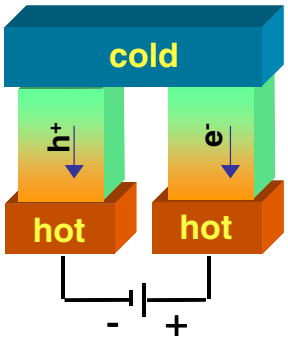


Fig. 1.1: Schematic of a typical thermoelectric cooler configuration

A diagram of a typical thermoelectric cooling system is shown in Figure 1.1. Our approach is to replace the bulk materials used for the *p*-type and *n*-type legs with oriented arrays of nanowires. To date, thermoelectric cooling has been limited to temperatures > ~ 130K due to limitations in the performance of the bulk thermoelectric materials, e.g. bismuth. The performance of thermoelectric systems is characterized by the dimensionless figure of merit, ZT:

$$ZT = \frac{S^2\sigma}{\kappa}T$$

where S is the Seebeck coefficient, σ is the electrical conductivity, κ is the thermal conductivity and T is the absolute temperature. ZT > 1 is typically required for efficient thermoelectric operation. It is somewhat counter-intuitive to require poor κ for a cooling device; however, the cooling mechanism is via electric charge transport. I.e. charge is pumped up-potential near the device to be cooled, removing heat, and then down-potential at the heat sink for removal. Low κ ensures that heat removed by charge does not return via the legs. The simultaneous need for good electrical conductivity and poor thermal conductivity is materials limiting. High thermoelectric power semiconductor alloys of Bi, Sb, and Te are used since they have poor thermal conductivity and can be doped to improve electrical conductivity.[Hicks and Dresselhaus, *Phys. Rev. B,* **47**, 16631 (1993).]

Theoretical studies of low dimensional systems (i.e. nanowires) have shown that ZT benefits from quantum effects related to carrier confinement (increased *S*) and from pronounced phonon scattering at the boundaries (decreased κ). Furthermore, it has been calculated that $Bi_{1-x}Sb_x$ nanowires can exhibit ZT ≥ 1.2 at 77 K due to 1) the large mass difference between Bi and Sb leading to increased phonon scattering hence decreased κ; 2) the coalescence of several valence sub-band edges to maximize the density of states at the Fermi energy resulting in an increase in *S* (O. Rabin, et al., Applied Physics Letters, **79**, 2001). This is shown in Figure 1.2. In this way, both the *p*-type and *n*-type legs can be fabricated from the same basic nanowires under different doping conditions. In order to replace the semiconductor legs of a standard thermoelectric device the nanowires need to be manufactured in high density (>10^{10}/cm^2 over ~ 0.2cm^2), oriented, high aspect ratio array (40 nm diameter by 100 mm length). Furthermore, the fabrication process needs to be compatible with on-chip processing.

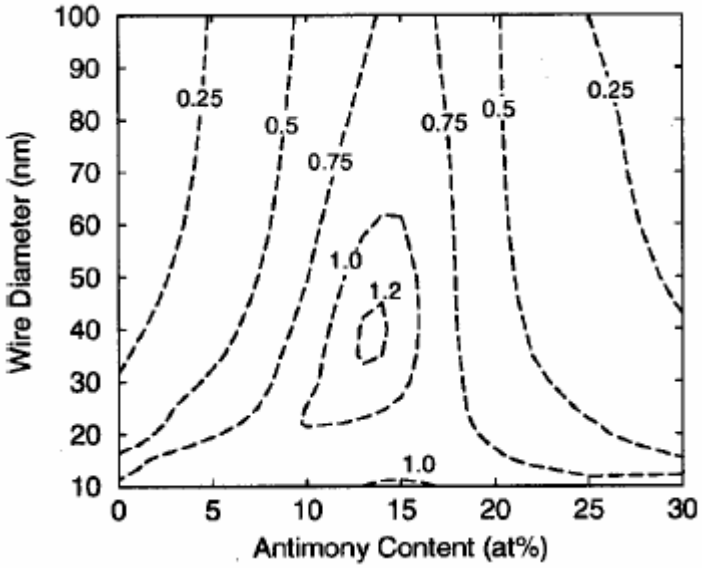


Fig. 1.2: Contour plot of ZT values for p-type $Bi_{1-x}Sb_x$ nanowires vs. wire diameter and Sb-content

Our approach was to develop anodized aluminum oxide (AAO) as a template for nanowire growth. The use of AAO templates is extremely advantageous from both a fabrication and cost standpoint. Anodization is a well-understood, inexpensive, and readily scaleable electrochemical process. Nanopore diameters generated in AAO can be controlled from 5 – 1000 nm, are quasi-hexagonal close-packed, and are separated by distances ~ the same as the pore diameters. Therefore, 200 nm diameter pores will yield a density > 10^9/cm^2. However, several technical issues prevent the widespread use of AAO templates for growing aligned nanowire arrays. First, high-purity Al foil or sheet is typically used. Substrates need to be ultrasmooth to be useful for electronic applications. Polishing Al to roughness < 200 nm is both difficult and time intensive and, hence, expensive. Second, such substrates are not integrated directly on-chip, which is preferred for optimal substrate cooling. Finally, while Al films can be deposited directly onto a substrate of choice, such as silicon, they exhibit roughness on the order of film thickness, with facets in many directions, and as such, are not reliable templates.

We used a nonaqueous solvent, not for solubility issues, but rather to minimize the chemical attack on the alumina templates during the long electroforming exposures. Typical aqueous solvents from any of the Bi or Sb salts can be either acidic or alkaline. Exposing the well-defined diameters of a controlled alumina template to either of these strong pH solvents will widen the pores, and lead to loss of $Bi_{1-x}Sb_x$ diameter control. To achieve the high ZT > 1.2 values, maintaining the template pore diameter is critical.

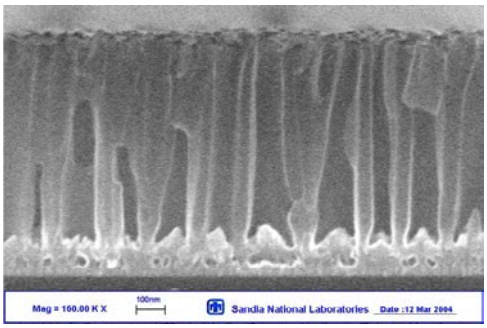


Fig. 1.3: Cross-section of an AAO template with 500-nm deep, 50-nm diameter pores from a Nd-doped Al film on Si(100).

We further developed a greatly improved AAO template process, investigated earlier at Sandia from an "Out-of-the-Box Science" LDRD, that uses Nd-doped Al films deposited onto a thin W adhesion layer that results in mirror-smooth films. Since all the deposition processes occur at room temperature, such films can be put onto any substrate. These films anodize similar to bulk Al. This new AAO process: 1) provides extremely uniform substrates to form the templates, and 2) makes the transition from bulk materials to on-chip $Bi_{1-x}Sb_x$ nanowire processing. By decreasing the AAO template pore diameter to 50 nm, shown in Figure 1.3, the array density approaches 10^{10} wires/cm^2. Furthermore, readily-achievable 20-nm pore diameters will provide array densities > 10^{11} wires/cm^2. Finally, a key component of this work is to attain AAO templates with ~ 100 μm deep nanopores. Typically, the deposition of such a thick metal film exceeds the critical thickness due to stress, resulting in spallation, or peeling of the film. However, we developed modified physical deposition processes that can minimize spallation.

We first planned to develop a uniform electroforming process using a rotating cylinder electrode (RCE) study to deposit the optimum $Bi_{1-x}Sb_x$ alloy into ≥ 200 nm diameter pores that are ~ 50 μm deep. Once this optimum composition process is established, we planned to continue decreasing the wire diameters to ≤ 40 nm using a modified pulse deposition regime to account for mass transport difficulties in the decreasing pore sizes of the template. Macro-uniformity problems will be overcome by using AAO templates from sputtered Nd-doped Al films for mirror-smooth surfaces, high uniformity and depth control, all demonstrated at Sandia, Figure 1.3. The continued use of bulk Al, by the rest of the scientific community, to form these templates results in severe uniformity difficulties. However, we observe greater uniformity of pore depth and diameter, with less surface variance, from our deposits---ideal for controlled growth of high-density arrays of nanowires. This inherent nature of the Nd-doped Al AAO template lends itself well for slow uniform growth of high-density nanowires longer than 100 μm deposited directly onto Si.

To minimize thermal transport properties, individual nanowires ideally extend away from the heat source with minimal contacts between neighboring wires. Contacts introduce boundaries into the system similar to grain boundaries and, since it is understood that internal surfaces interact with phonons, such boundaries could introduce a prominent scattering mechanism that significantly degrade thermoelectric properties. Given the very large aspect ratio desired for individual wires in the array, such contacts are likely unavoidable. To address this, we will use atomic-scale simulations to examine the impingement of phonon wave packets on relevant boundaries, elucidating the influence of the boundary on wave packet transmission. This will produce a quantitative relation between contact density and thermal transport degradation. From this information, we will establish a tolerance limit for contact density, below which thermal transport efficiency of the array will be maintained.

In the first year we provided proof-of-concept in AAO nanopores with depths ~ 1 μm, and determined via computation the necessity of developing a thin spacer to physically separate $Bi_{1-x}Sb_x$ nanowires. In year two, we scaled the electroforming process to ~ 70 μm deep high-density arrays formed from sputter deposited Nd-doped Al AAO templates and characterized the ZT of the resulting nanowire arrays.

II. Rotating Disk Electrode Study

Mass transport issues: Since nanowire diameters and lengths are controlled by the nanopore diameter and film thickness of the AAO templates, how do mass transport concerns affect the composition of Bi/Sb nanowires during high-aspect-ratio deposition as compared to similar operating parameters designed for films of the same target alloy composition on a flat surface? The reducing currents used to deposit material in the pores is a function of the driving potential, which is the product of three mass transport modes that act resistively to current flow: diffusion, convection, and ionic migration, each limiting the Nernst potentials needed to generate charge transfer. However, resistance to ionic migration is greatly reduced if the supporting electrolyte is highly conductive. Convective resistance is ruled out as a problem since agitation in pores < 200 μm is limited. This leaves diffusion-induced concentration gradients as the main mass transport issue.

Our original plan was to study alloy compositions and mass transport issues using a rotation cylinder electrode. The commercial system we looked into was too large, resulting in large hazard waste generation, so we turned to a simpler solution of using a rotating disk electrode (RDE) and a Hull cell to perform the same experiments. The voltammograms plotted in figure 1 are linear potential scans from -100 to -500 mV vs. Ag:AgCl [4 M KCl and AgCl] under electrochemical cell conditions reported in the CV experiments. The potential range represents the transition from non-faradic surface changing of the double layer (the upper right hand section of the scans), to faradic reduction of the active Bi/Sb species. Interestingly, very little improvement in total current is realized by decreasing Nernst diffusion layer thickness via increasing agitation (higher rpm's) at the RDE. At even higher rpm's (figure 2.2), further thinning the diffusion distance to the electrode surface, the only notable difference in the limiting current density is the change from a sharp transition curve for the double layer charging to activation controlled currents. At higher agitation rates (higher rpm's) the thickness of the highly-ordered electrical double layer in the interphase, the area above the working surface, is greatly disturbed.

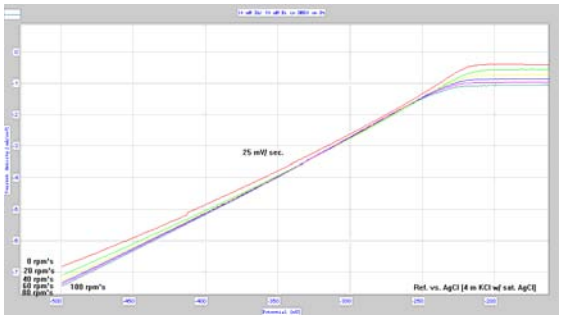


Fig. 2.1: Mass transport of Sb and Bi in DMSO at low convective agitation.

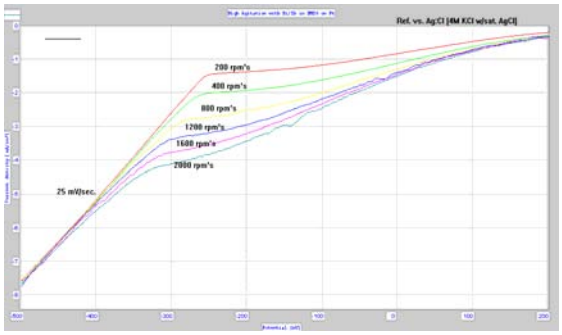


Fig. 2.2: High agitation of 30 mM Sb and 50 mM Bi in DMSO at room temperature on a Pt RDE.

What does this mean in terms of depositing nanowires at a given composition in pores? The overlapping voltammograms in figs. 2.1 and 2.2 show that the reduction of Bi/Sb, at depositing potentials is NOT a major issue concerning mass transport limitations. Maintaining the Bi/Sb composition ratio during deposition in nanopores will not be a problem. Rather, fig. 2.2 shows that the major current-limitations come from the rate of double-layer charging in the interphase. Beyond double-layer capacitance from the polarization of the surface, fig. 2.3 shows

that the active ions are kinetically limited by the applied potential, with Sb^{3+} ions reducing (CV scan in grey) at a more sluggish rate than Bi^{3+} ions (CV scan in red). When both Bi^{3+} and Sb^{3+} ions are reduced, Bi^{3+} ions dominate the kinetic reaction (CV scan in blue). In other words, as the potential increases more negative from thermodynamic equilibrium, or OCP (open circuit potential), the total cathodic current increases linearly for both Bi^{3+} and Sb^{3+} with Bi depositing at a greater ratio than Sb.

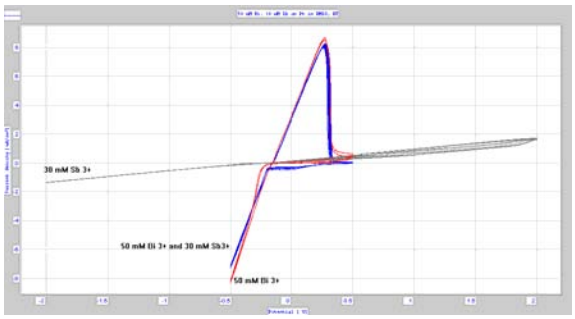


Fig. 2.3: Overlay of 3 independent cyclic voltammetries, with scan rate = 25 mV/sec. Potential vs. ref: Ag:AgCl [4 M KCL w/sat. AgCl]. Electroactive ions 30 mM Sb^{3+} and 50 mM Bi^{3+} in DMSO at room temp.

Hull cell results: Fig. 2.4 shows the results of depositing from a solution containing 30 mM of Sb and 50 mM of Bi in DMSO. With the potential fixed at -500 mV vs. Ag:AgCl for one hour, the total applied current across the cell was 23 mA. The Hull cell geometry positions the copper substrate 30° off parallel from the counter-electrode, forcing a spectrum of current densities. Since Bi is more electroactive than Sb, the deposited Bi composition ranged from 67 to 96 %. At lower current densities neither Bi nor Sb deposited. At each point marked on the panel are SEMs photographs of the surface morphology and corresponding Bi composition. The far left edge of the panel, the section closest to the counter electrode, yields the highest current densities, localized potentials, Bi composition, and the largest crystal grains with some greater than 5 μm.

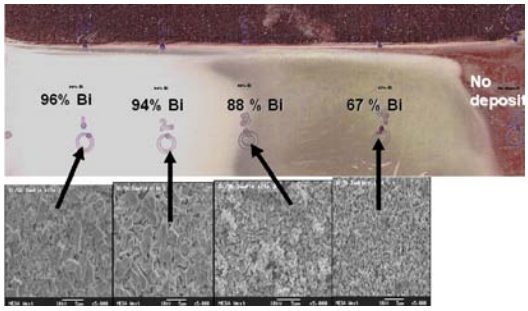


Fig. 2.4: Cu Hull cell panel showing a spectrum of current densities highest on the left and lowest on the right. The SEM images show the morphology of regions of particular Bi:Sb

These results show that a non-uniform field flux, which produces changes in the driving potential, controls both film composition and morphology. Since both Bi and Sb are highly dependent on the applied potential, the ionic solution composition controls the final composition. Taken together, the RDE and Hull cell results demonstrate that compositional uniformity in high-aspect ratio nanowires should not be a problem.

III. Anodizing Aluminum Oxide Films

This involves two main areas. First is the ability to fabricate templates with controlled nanopore sizes and densities over great lengths. Second is growing vertically-aligned BiSb nanowires in the templates. The effort to date focused on producing the necessary AAO nanopore templates. These form by depositing films onto Si substrates, the thickness of which determine the AAO nanopore depth. (Actually, we use Nd-doped Al since films deposit with less surface oxidation, resulting in mirror-like surfaces.) The AAO is formed electrochemically, followed by electrochemical nanowire deposition. The nanowire growth requires that the nanopore bottoms be electrically conductive. To accomplish this, we first deposit a stress-free 50 nm thick W film on the Si. W does not oxidize under the AAO formation conditions and adheres well to Si.

Ultimately, this project requires nanopore depths approaching 100 µm. Residual stress becomes a major issue. If the film stress gets too large, the films will delaminate, rendering the templates useless. We studied methods to reduce the film stress during deposition by controlling two parameters: Ar sputter pressure and RF sputter power. The higher the Ar pressure, the lower the kinetic energy of the depositing species, resulting in lower residual stress. However, the use of high sputter pressure also reduces deposition rates, which is relevant when the ultimate goal approaches 100 µm thick films. Fortunately, we found that the Nd-doping appears to assist with stress relaxation, and therefore were able to eliminate stress simply by controlling the RF sputtering power. Fig. 3.1 shows that at 107 watts, the residual stress of ~ 6 µm thick Nd-doped Al films on W-coated Si goes through a zero point as the stress goes from tensile to compressive. These films have negligible stress, remain highly mirror-like, and should not experience spallation at greater thicknesses.

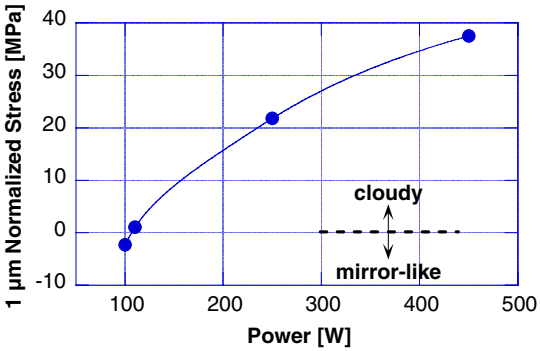


Fig. 3.1: Normalized stress vs. sputtering power for ~ 6 µm-thick Nd-doped Al films grown on stress-free 50 nm thick W-coated Si(100)

Using mirror-smooth Nd-doped Al films, we can fabricate controlled nanopore arrays with defined depths. These AAO nanopore arrays will be used as templates for aligned BiSb nanowire growth directly onto Si wafers where they are used. By controlling nanopore diameters and lengths via the anodization conditions and Nd-doped Al film thicknesses, we will create AAO templates with the appropriate pore size for a given BiSb nanowire diameter, providing the best possible thermoelectric cooling properties. Fig. 3.2 shows SEM images of AAO surfaces and cross-sections for templates with thicknesses of 0.2, 0.5 and 1.2 microns. These AAO templates have pore diameters of 50 nm, with an array density of 10^{10} nanopores/cm^2. These films were all anodized in phosphoric acid with a 60 V potential, and the images show that only the depth of the nanopores vary as a function of Al film thickness.

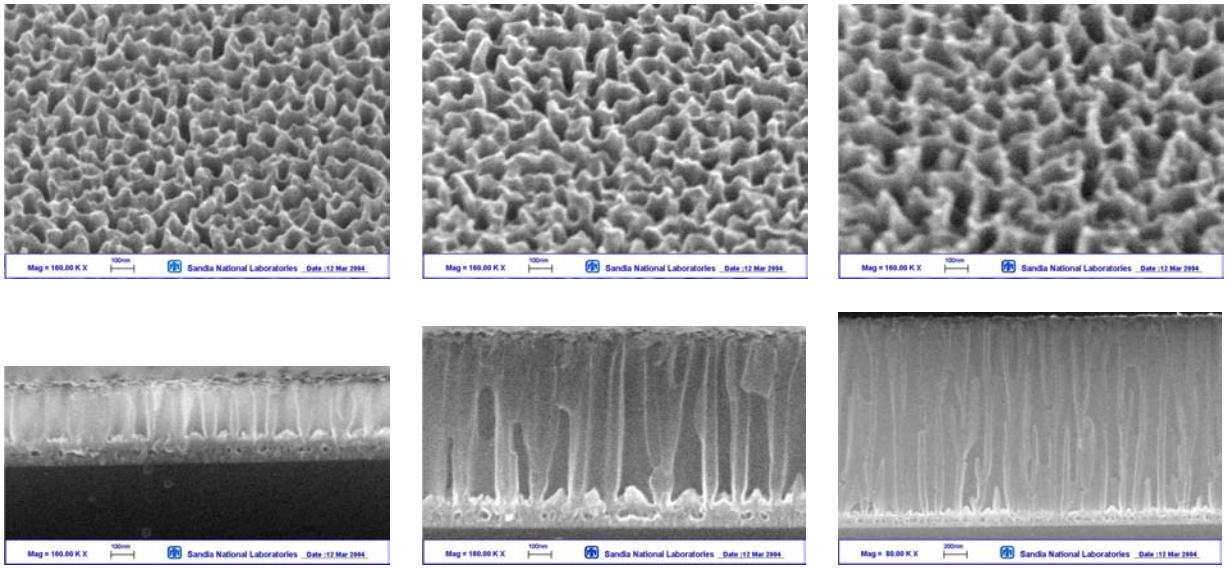


Fig. 3.2: AAO vs. Nd-doped Al film thicknesses of 0.2, 0.5, and 1.2 μm.

IV. Atomistic Modeling to Determine the Impact of Grain Boundaries

BiSb nanowires are polycrystalline with small grains (i.e. smaller than the phonon mean free path). This indicates that phonon scattering at grain boundaries (GBs) and free surface contacts may dominate mechanisms for heat flow resistance. We developed new tools necessary to model the influence of interfaces on phonon transport as a step towards predicting the thermal transport properties of synthesized nanowires. Via collaborative work with LDRD project 79773 (Atomic Scale Modeling of Phonon Mediated Thermal Transport in Microsystems), we developed the capability to model realistic GB structures in materials. Our fairly robust algorithm permits us to form boundaries of arbitrary twist with varying degree of disorder (indicative, for instance, of the rate at which the structure was grown, where a faster rate would result in a less-ordered boundary). In addition, the ability to model phonon wavepackets impinging upon boundaries has been developed along with analysis tools to extract relevant information (e.g. transmitted/reflected energy and frequency). Results from a trial simulation on an ideal interface agreed with those of the corresponding published result, validating our implementation. We completed a study of the effect on phonon transport of disorder in a GB structure for one value of twist angle and compared it to existing results on an ideal Si interface. We have established a collaboration with Prof. Patrick Schelling of the University of Central Florida, one of the originators of wave packet impingement simulations. This brought to our project the ability to model non-normal phonon incidence on GBs. Such simulations present unique challenges that our current method cannot address due to complexities. Prof. Schelling is actively pursuing this and will spend time at Sandia in the summer 2006 implementing the capability into our modeling suite. This is necessary to address the full phase space relevant to thermal transport in BiSb nanowires and other nanostructures.

Our computational approach was to build a vibrational spectrum from quasiharmonic approximations. A "phonon" is a Gaussian wavepacket with initial displacements determined from the dispersion relation, represented pictorially in figure 4.1. These wave-packets travel at group velocity $\mathbf{v_g}$ and have negligible decay in amplitude for small amplitudes.

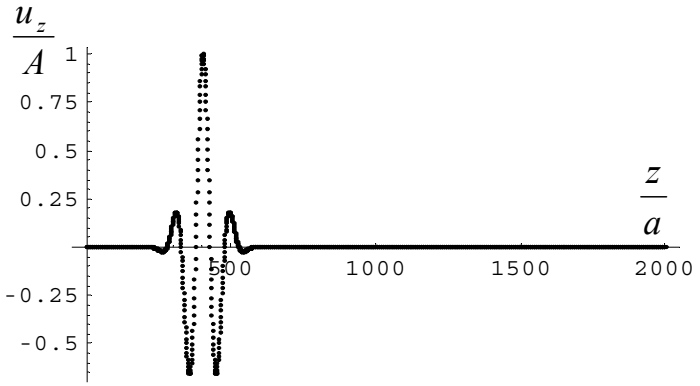


Fig. 4.1: Gaussian phonon wave.

The canonical molecular dynamics problem is heat conduction in a bicrystal. By inserting a grain boundary in a phonon pathway, such as our nanowires, the energy flow is disrupted and leads to a temperature discontinuity. This is shown in figure 4.2. To determine the full effect of such grain boundary, the transmission coefficient for each incident phonon with various wavevectors would need to be calculated. Such a problem is too time-consuming.

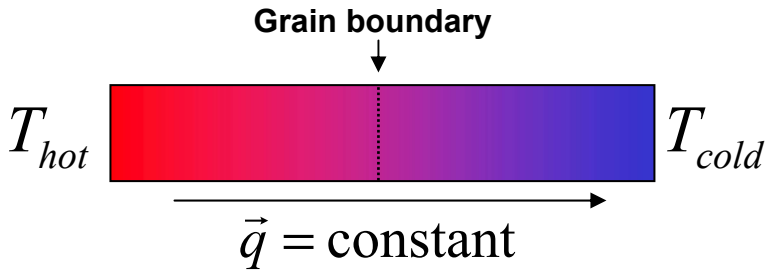


Figure 4.2: Cartoon of heat transport across a grain boundary.

Instead, we created Fourier codes to automate several computational features, shown in Fig. 4.3, including:

(1) initial grain boundary generation,
(2) displacement and velocity initial conditions for arbitrary combinations of wave-packets,
(3) normal-mode decomposition over time, and
(4) calculation of transmission and reflection coefficients of traveling phonons.

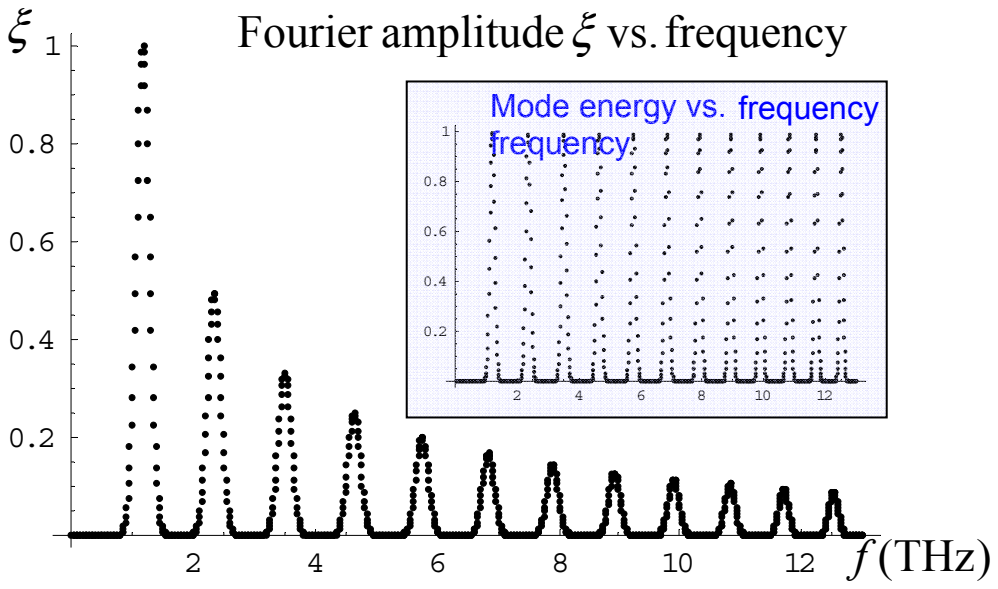


Figure 4.3: Sample Fourier generated wave packets.

This was applied to a phonon traveling across an ideal Si grain boundary, shown in fig. 4.4, where atoms are colored according to their potential energy; this shows the position of the phonon wave packet in the simulation as atoms in this vicinity have higher energy than the rest of the system. This formulation still needs to be applied to a realistic BiSb grain boundary.

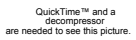


Figure 4.4: Phonon simulation across a Si grain boundary.

V. BiSb Nanowire Arrays and Thermoelectric Properties

Unfortunately, we experienced difficulties anodizing our Nd-doped Al films on Si that were greater than a few microns thick. This was due to the leakage of current through the substrate. To work around this problem, we tried to cover the Si backside and edges with various insulators, including both glues and bees wax. While these efforts worked to a certain degree, they made handling the samples for further measurements very difficult. We considered working on insulating glass substrates, but understood that this was an unrealistic substrate to study. I.e. the main focus needed to be on semiconducting substrates like Si or GaAs. We believe that if we used a double-side polished wafer with oxide grown at least on the backside, the results would be similar to working on standard bulk Al sheet. As such, our studies of BiSb nanowire growth, performed in collaboration with Prof. Stacy's group at the University of California – Berkeley, are hopefully representative of what is possible.

Great effort was made into developing the technology to backfill a completely anodized Al sheet with nanowires. Fig. 5.1 shows a typical commercially available AAO template used for these studies. This SEM image shows a nearly hexagonal array of nanopores with ~ 40 nm diameter nanopores. Cross-section images (not shown) find that these pore diameters are very homogenous through the entire thickness of the AAO sheet.

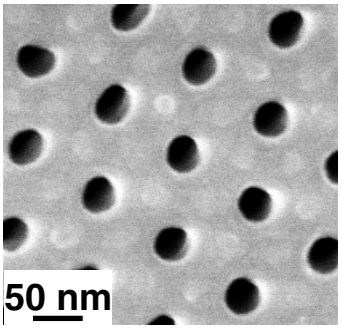
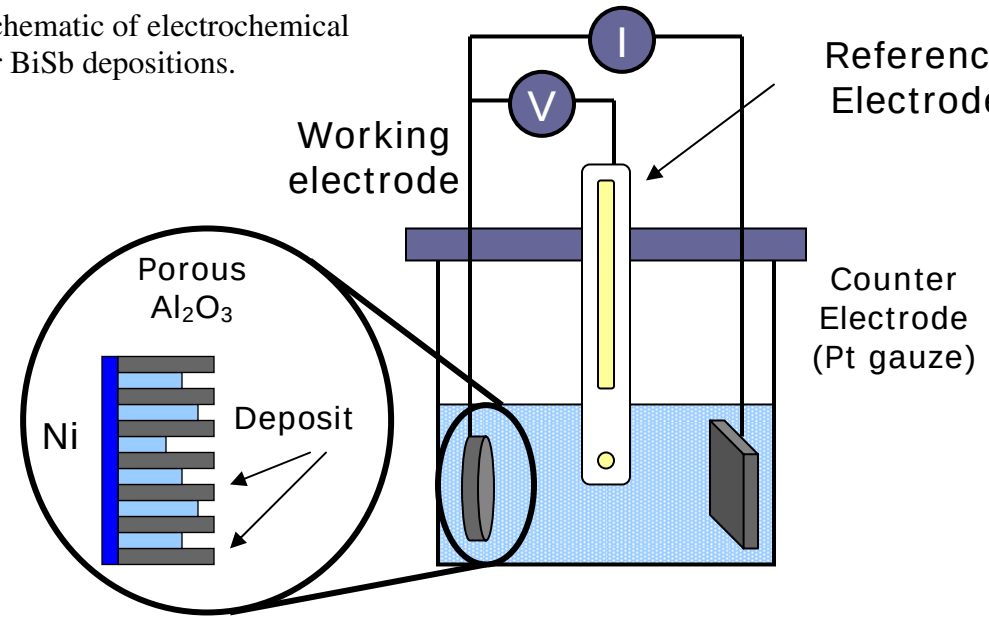


Fig. 5.1: SEM image of an AAO template surface with ~ 40 nm nanopores.

Fig. 5.2 shows a schematic of a standard electrochemical cell used to grow the BiSb nanowires into the AAO templates. First, a metal, in this case Ni, was deposited onto one side of the AAO to form a conducting surface to draw the ion charges into the nanopores for deposition. Of course, the backside of this Ni film was protected by an insulating coating so as not to draw charge away from the Ni surface exposed through the nanopores.

Fig. 5.2: Schematic of electrochemical cell used for BiSb depositions.



The solutes used were $Bi(NO_3)_3 \cdot 5H_2O$ and $SbCl_3$. The supporting electrolyte was tetra-n-butyl ammonium chloride, all dissolved into a solvent of dimethyl sulfoxide. The BiSb nanowires tend to be smooth, essentially filling > 90 % of the nanopores. It was found that electrodepositing at relatively slow rates (just over 1 μm/hour) leads to nanowires with very uniform lengths.

Fig. 5.3 shows an SEM image for BiSb nanowires grown in an AAO template that extend only ~ 40 μm long, however, note the relative uniformity of length in fig. 5.3(a). Fig. 5.3(b) is an image at higher magnification that shows the growth of the BiSb nanowires from the Ni metal surface. The apparent curvature is only due to the cleavage angle, instead note how uniform the diameters appear.

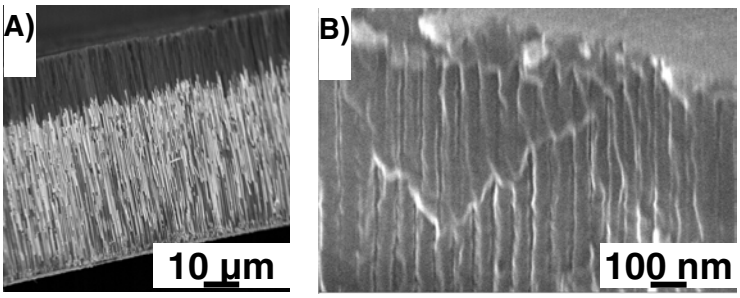


Fig. 5.3: SEM images showing BiSb nanowires in AAO templates.

However, for thermoelectric cooling to become reality, lengths must approach at least 100 μm. The longest successful BiSb nanowire deposition was into 70 μm deep AAO nanopores, however, the results were not homogeneous across the substrate, shown in fig. 5.4.

QuickTime™ and a
TIFF (LZW) decompressor
are needed to see this picture.

Fig. 5.4: SEM images showing BiSb nanowire growth in an AAO template. On the left, the image is taken from an edge of the AAO substrate, while the image on the right is from a region toward the center of the substrate.

The image on the left is taken from the edge of the AAO substrate where apparently greater ionic conduction occurs. The nanowires grown in the middle of the substrate only reached 50 µm in length, falling short of completely filling the nanopores. Clearly, more engineering design needs to occur to achieve greater uniformity of nanowire lengths across an entire substrate surface.

Nevertheless, an attempt was made to measure thermoelectric properties of the BiSb nanowires. In order to do this accurately, a full thermoelectric cooling device had to be fabricated. In order to complete the thermoelectric couple, a hybrid nanowire-bulk couple was assembled to measure the properties, as shown in fig. 5.5.

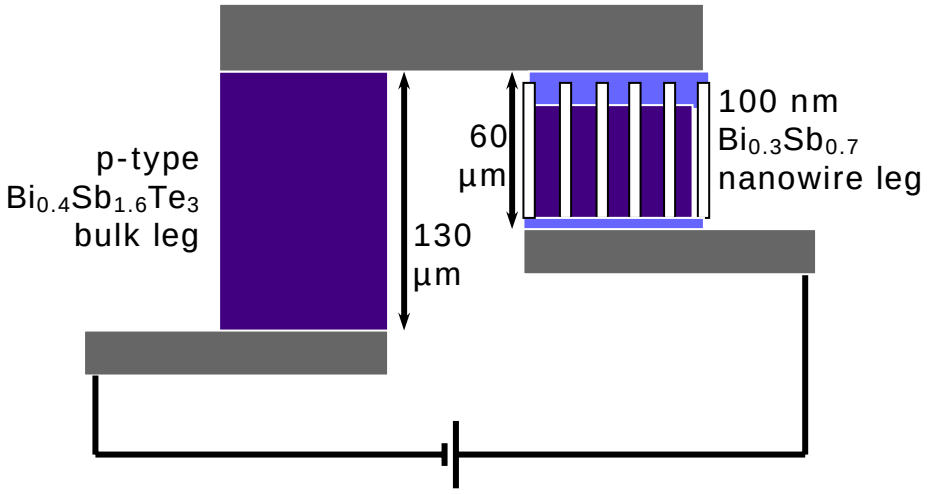


Fig. 5.5: Schematic of hybrid nanowire-bulk thermoelectric couple.

Other compromises were also made to make this first and only measurement somewhat easier. The nanowires grown were ~ 100 nm diameters, and unfortunately, the Sb composition was too rich. Nevertheless, ZT was measured ~ 0.12 and a temperature differential of $\Delta T \sim 7$ ˚C at room temperature. When compared to the computational result for nanowire diameter vs Sb-content, shown in fig. 1.2, this measured ZT is actually what would be predicted for a nanowire diameter and composition in the upper right hand corner of that plot. Finally, while typical thermoelectric cooling devices have a $\Delta T \sim 45$ ˚C, those measurements are performed at ~ 130 K with bulk legs of the correct compositions. Clearly, smaller nanowire diameters and compositional optimization will greatly increase the thermoelectric cooling efficiencies.

VI. Summary and Future Considerations

There is still much research to be done before thermoelectric nanowires can be used for cooling devices. Aside from further optimizing the properties of p-type BiSb nanowires, everything must be repeated for n-type BiTe nanowires.

We demonstrated high-density growth of > 70 μm long BiSb nanowires in conventional AAO templates. This work needs to be extended to our novel AAO template films that can be grown directly onto a device substrate surface to achieve better thermal contact for improved thermoelectric cooling.

In addition, the computational work can help identify better crystallographic orientations and grain boundaries to achieve the best electrical conductivity and the lowest thermal conductivity for thermoelectric optimization. While some degree of control over the nanowire crystallographic orientation is known, not shown in this report, due to the electrochemical deposition conditions, it is very likely that post-deposition annealing can improve the crystalline nature of individual grains and grain boundaries. However, consideration will also have to be given to the unwanted side-effect of creating residual stresses that could cause the nanowire/AAO array to spall from the substrate surface due to differences in thermal expansion coefficients.

Nanowire lengths determine the magnitude of the thermal gradient. The Sb-rich nanowire array described above for *ZT* measurement produced $\Delta T = 7$ K for only 50 μm long samples. This gradient should be greater using optimized nanowires by increasing *ZT* (x10 likely) and length (x2 possible), perhaps leading to $\Delta T \geq 100$ K. Since the concept is still new, such performance has never been measured.

The atomistic models were developed and demonstrated for phonon transport across ideal Si grain boundaries. However, classical potentials for BiSb and BiTe, the input for MD simulations, do not exist. Instead, potentials will need to be developed using a simplified approach focusing on capturing materials properties most relevant to thermal transport (atomic mass, bond strength, and phonon density-of-states). The prevailing thought in the literature is that this is sufficient to describe the influence of grain boundaries on phonon scattering. This computational work can greatly direct the experimental development of particular crystallographic orientations and grain boundaries in the nanowires. This is especially important given that the only real good way to measure thermoelectric properties is to build actual devices.

Thermoelectric cooling using nanowires remains an intriguing possibility. The work performed in this LDRD project made significant steps toward this development. No brick walls were encountered. Nevertheless, much work remains to be done, and unforeseen pitfalls may still exist.

VI. Publications, Presentations and Patent Disclosures

This section lists publications and presentations resulting from this project.

Publications

none

Presentations

none

Sandia Patent Disclosures

none

Distribution List

Copies	Mail Stop	Name	Org.
1	0123	LDRD Office, Donna Chavez	1011
3	1421	Michael P. Siegal	1126
1	1411	Ed Webb III	1814
1	1086	Bob Biefeld	1126
1	1411	Eliot Fang	1814
1	1425	Graham Yelton	1725
1	1082	Jim Hudgens	1725
2	0899	Technical Library	4536
2	9018	Central Technical Files	8944
1	0980	Steve Gentry	5703
1	0980	Toby Townsend	5703