Final Report

Compact Fluorescent Plug-In Ballast-in-a-Socket

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Executive Summary

The primary goal of this program was to develop a ballast system for plug-in CFLs (compact fluorescent lamps) that will directly replace standard metal shell, medium base incandescent lampholders (such as Levition # 6098) for use with portable lamp fixtures, such as floor, table and desk lamps. A secondary goal was to identify a plug-in CFL that is optimized for use with this ballast. This Plug-in CFL Ballast-in-a- Socket system will allow fixture manufacturers to easily manufacture CFL-based high-efficacy portable fixtures that provide residential and commercial consumers with attractive, cost-effective, and energy-efficient fixtures for use wherever portable incandescent fixtures are used today. The advantages of this proposed system over existing CFL solutions are that the fixtures can only be used with high-efficacy CFLs, and they will be more attractive and will have lower life-cycle costs than screw-in or adapter-based CFL retrofit solutions. These features should greatly increase the penetration of CFL's into the North American market.

Our work has shown that using integrated circuits it is quite feasible to produce a lamp-fixture ballast of a size comparable to the current Edison-screw 3-way incandescent fixtures. As for price points for BIAS-based fixtures, end-users polled by the Lighting Research Institute at RPI indicated that they would pay as much as an additional $10 for a lamp containing such a ballast.

The ballast has been optimized to run with a 26 W amalgam triple biax lamp in the base-down position, yet can accept non-amalgam versions of the lamp. With a few part alterations, the ballast can be produced to support 32 W lamps as well. The ballast uses GE's existing L-Comp[1] power topology in the circuit so that the integrated circuit design would be a design that could possibly be used by other CFL and EFL products with minor modifications. This gives added value by reducing cost and size of not only the BIAS, but also possibly other integral CFL and future dimmable integral and plug-in versions of the EFL products.

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Table of Acronyms and Abbreviations

A	Amperes
AC	Alternating Current
AM	Amplitude Modulation
ASIC	Application Specific Integrated Circuit
BIAS	Ballast-in-a-Socket
CCT	Correlated Color Temperature
CFL	Compact Fluourescent Lamp
CIE	Commission Internationale de l'Eclairage
CRI	Color Rendering Index
CTQ	"Critical To Quality" - i.e. a key criterion
DC	Direct Current
EMI	Electromagnetic Interference
FIT Rate	Failures per 10^9 hours
FM	Frequency Modulation
GE CR&D	General Electric Corporate Research & Development
GEL	General Electric Lighting
I	Symbol for current (amps)
I/O	Input/Output
IEEE	Institute of Electrical and Electronics Engineers
L	Symbol for inductance
LRC	Lighting Research Center
MOSPHET	Metal Oxide Semiconductor Field Effect Transistor
MTBF	Mean Time Between Failures
PM	Phase Modulation
RF	Radio Frequency
RPI	Rensselaer Polytechnic Institute
SPICE	A general-purpose circuit simulation program for nonlinear DC, nonlinear transient, and linear AC analyses. SPICE originates from the EECS Department of the University of California at Berkeley.
TBX	Triple Biax
TC	Thermocouple
THD	Total Harmonic Distortion
US DOE	United States Department of Energy
V	Volts
W	Watts

1 Program Goals and Benefits

The overall goal of this program has been to reduce energy consumption and concurrent pollution from fossil fuel power plants in the United States by increasing the use of compact fluorescent lamps (CFLs) in commercial applications (such as hotel rooms) as well as residential applications. Incandescent lamps, the most common type of lamp used in U.S. portable luminaire applications, are very inefficient light sources. They convert only about 3–5% of the electrical energy they use into visible light. CFLs are three to four times as efficient as incandescent lamps of equivalent light output and can be used in many sockets that are currently fitted with incandescent lamps. In spite of the opportunity to save substantial amounts of energy (and therefore to cut operating costs), CFLs have replaced only a small fraction of incandescent lamps in portable luminaire applications. Studies by the Department of Energy, the Electric Power Research Institute, and others have identified high initial cost as the major impediment to greater use of CFLs in commercial and residential applications. Additionally, with the commonly available integral CFL's, the chance for the user to revert to using incandescent lamps is quite high, especially if the user's first experience with CFLs is negative due to poor lamp quality or reliability.

To make CFL use more attractive in hotels and residential applications, the Ballast-in-a-Socket (BIAS) program has designed and prototyped a dedicated CFL ballast contained within a portable luminaire socket. By integrating the ballast into the luminaire, the user will not have to incur cost of the ballast each time the lamp burns out - making the replacement cost of the CFL lamps competitive with traditional incandescent lamp and overcoming one of the main impediments to greater market penetration. A dedicated fixture on the lamp means additionally that the user will be far less likely to revert to the use of incandescent lamps, as that would involve retrofitting the lamp or purchasing a new one.

2 Technical Approach

2.1 Lamp Choice

One of the obstacles to widespread penetration of a dedicated CFL lamp into commercial and residential spaces is the perception that CFL's give poor quality light. To determine what lamp would provide the optimal light for a BIAS lamp, the CR&D team examined the characteristics of two types of lamps at two common wattages.

2.1.1 Background

Amalgam and Non-Amalgam lamps were characterized to determine baseline lamp CTQs such as initial lumen output at start-up, time it took to reach 90% of full light output, color rendering index (CRI) over dimming range, correlated color temperature (CCT) over dimming range, and efficacy over dimming range. Three lamps of the 26W Triple Biax? (26W TBX), 28W 2-Dimensional (28W 2D), and 26W Double Biax? (26W DBX) were tested for initial specifications. The set-up used to take these measurements utilized a RF power amplifier to supply power to the wire lamps. This way the lamp characteristics could be tested independently of the different integral ballasts normally used to power them. The frequency was set at 40 kHz and remained constant over the dimming range. The power was decreased in 10% steps and data was recorded. Figure 2.1-1 gives a summary of the lamps tested and their lumen output and efficacy at full power. Three lamps of each lamp type were tested. Figure 2.1-1 represents data from one lamp of each type. The lumens and efficacy data was taken at full power. The 28W 2D and 26W DBX were non-amalgam lamps and the 26W TBX was an amalgam lamp.

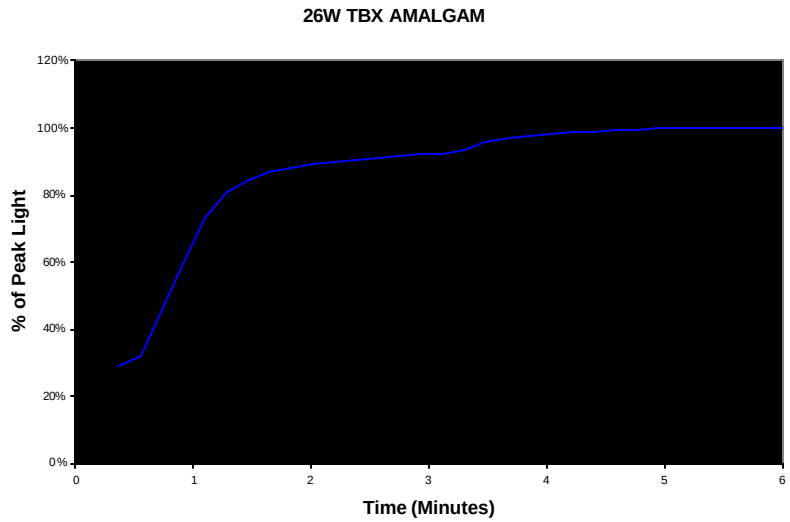
Lamp Type	Amalgam	Power	Lumens	Efficacy
26 Watt TBX	Yes	26	1800	69.2
28 Watt 2D	No	28	2050	73.2
26 Watt DBX	No	26	1710	65.8

Figure 2.1-1 Lamps tested with specifications

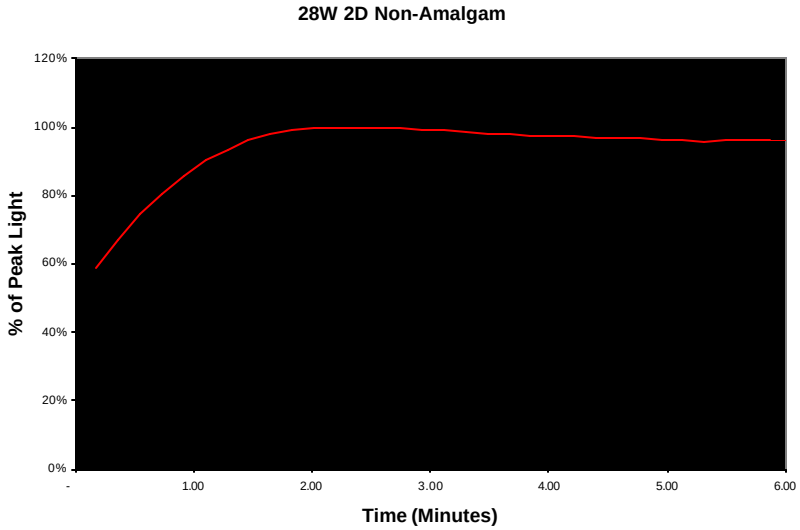
2.1.2 Lumen Output

A comparison of initial lumen output and start-up time for the 26W TBX and the 28W 2D are shown in Figure 2.1-2. As can be seen the time to reach 90% of total lumen output and the initial lumen output for the non-amalgam 28W 2D meet the specifications of the system CTQs (see Appendix A). The 26W TBX amalgam lamp not only took twice as long (120seconds) to reach 90% of total light output, but more

importantly, the initial lumen output was considerably lower (30% of total lumen output) than the 28W 2D non-amalgam. This was expected to be the case for the amalgam lamp vs. the non-amalgam lamp. Additional power at start-up will be required for the BIAS prototype if an amalgam lamp is utilized in the system to meet the CTQs of start-up time and initial lumen output. This will add complexity and cost to the circuit design, yet the amalgam lamp is currently more readily available off the shelf in the US and the shift in CCT is expected to be less drastic than for a non-amalgam lamp. Therefore, the use of an amalgam lamp used in the system is expected to negatively impact the CTQs on size and cost while positively impacting the CTQs on availability of bulb replacement and CCT.



(a)



(b)

Figure 2.1-2 A comparison of initial lumen output & start-up time for the 26W TBX amalgam lamp & the 28W 2D.

Figure 2.1-3 represents the lamp efficacy and lumen output data taken for the dimming characteristics for the 28W 2D lamp. The set-up utilized was only able to take data down to 30% of initial power before the lamp shut off. This was because the voltage required to keep the lamp lit at the lower dimmed levels was higher than what the RF amplifier could supply (when reducing power for dimming, current is reduced and the voltage which is needed by the lamp to remain lit increases). The change in efficacy and the linearity of the lumen vs. power reduction curve were considered acceptable over the entire dimming range.

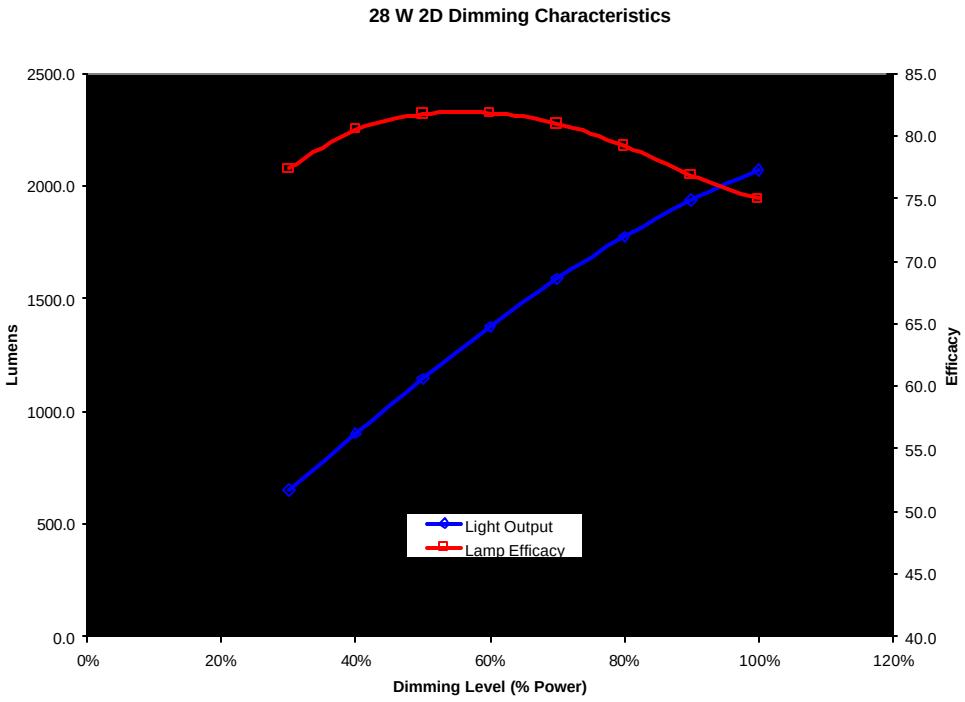
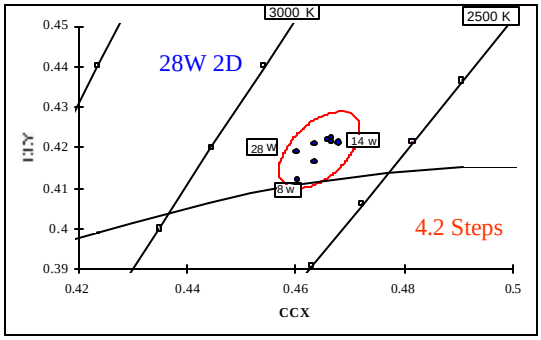


Figure 2.1-3 Light ouput and lamp efficacy as a function of percentage power reduction from total power.

2.1.3 Color Rendering Index & Color Temperature Measurements

Initial results of color rendering index (CRI) change during dimming determined that dimming would introduce a noticeable color change. The degree of color change was dependent on the lamp type used. Results are shown in Figure 2.1-4– Figure 2.1-6. A perceptible color change was defined as greater than two steps. Even though a color change will be noticeable, it was determined that the CRI shifted more towards the black body curve, which is more esthetically pleasing to the eye. Since the CRI shift was considered to be in the preferred direction, it was determined that one lamp would be sufficient for the dimming range from 1710 lumens to 342 lumens. This reduced the complexity required of the power

circuit topology and the ASIC design. The LRC's human factor study on the acceptance of the color change while dimming in mid March confirms that this color range is acceptable, though the LRC noted that most people preferred lamps with higher color temperatures (i.e. ~3500K) (see section 4, of this report - Market Analysis).

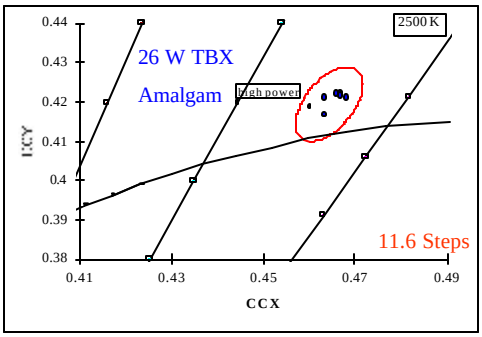


28 Watt 2D Non-Amalgam			
Power	**%**	**CCT**	**CRI**
28.02	100	2759	81.66
25.22	90	2726	82.78
22.42	80	2704	83.22
19.62	70	2693	83.72
16.83	60	2687	84.04
14.01	50	2668	83.34
11.19	40	2694	84.19
8.41	30	2704	84.03

Figure 2.1-4 Color change while dimming for the 28W 2D lamp.

The correlated color temperature (CCT) was used for sources that do not fall on the black body curve and was defined as the temperature of the black body radiator whose perceived color most closely resembles that of the source. According to the CIE (Commission Internationale de l'Eclairage) 29.2, there are three color appearance groups. For interior lighting, the CIE (CIE1986b) considers a correlated color temperature below 3300K to have a warm color appearance. Lamps with lower CCT appear to be on the warm side of white whereas lamps with higher CCT appear to be cooler. The desired CTQ parameter for CCT for the BIAS prototype is 2800K, which correlates to the color temperature of a soft white incandescent bulb. The acceptable CCT range for the BIAS prototype was defined to be 2800K +/- 200K. The CCT was determined to remain within the CTQ specifications for the BIAS prototype for two of the three lamps tested. The CCT variation over the entire dimming range was most significantly for the 26W DBX ranging from above 3000K to around 2600K. The 28W 2D held its color temperature to within 2700K +/-60K over the dimming range of 100% to 30% of the total lamp output power and the 28W TBX CCT ranged from 2947K at 100% power to 2624K at 40% power.

Color rendering capability is specified by the color rendering index (CRI). This is an important CTQ for both residential consumers and hospitality industry. This index is unity for a standard incandescent lamp corresponding to a point on the black body curve. The higher the CRI, the closer its color matches the color of a source at the same temperature on the black body curve. The CIE (CIE1986b) specifies a CRI of 80 or above to be used in homes. The CTQ range for the CRI for the BIAS prototype is required to be above 80.



26 Watt Triple Biax Amalgam			
Power	%	CCT	CRI
26.03	100	2947	77.69
23.41	90	2883	78.87
20.81	80	2798	80.2
18.22	70	2722	81.34
15.62	60	2670	82.29
13.03	50	2641	83.16
10.43	40	2624	83.25

Figure 2.1-5 Color change as a function of dimming for 26W Triple Biax? Lamp.

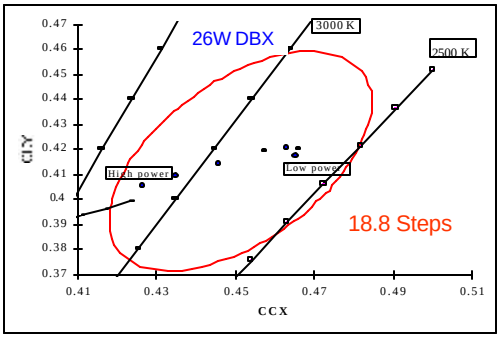


Figure 2.1-6 Color change as a function of dimming for the 26W Double Biax? Lamp.

2.1.4 Summary: Amalgam vs. Non-Amalgam Lamps

Figure 2.1-7 - Figure 2.1-10 illustrate the performance differences between the 26W and 32W Amalgam and non-Amalgam lamps. The non-Amalgam lamps provide more lumens at a given dimming level, and

show roughly the same color temperature distribution over the dimming range. In both kinds of lamps, however, the color temperature over the dimming range, while noticeable, is still considered acceptable.

Dimming	Vl (V)	Il (mA)	Pl (W)	Ic1 (mA)	Ic2 (mA)	Lumens	CCT (K)	CRI (RA)	%Full Lumens
100%	84.7	320	26.9	18.5	24.2	1677	2663	82.0	100.0
90%	89.4	274	24.2	46.2	47.2	1480	2618	82.8	88.3
80%	93.7	233	21.5	87.0	86.9	1329	2600	83.0	79.3
70%	97.3	198	18.8	126.0	118.9	1109	2577	83.5	66.2
60%	100.3	165	16.1	152.6	152.0	915	2571	83.7	54.5
50%	104.6	133	13.5	189.5	188.8	704	2557	83.9	42.0
40%	108.8	102	10.8	219.5	219.7	521	2548	84.1	31.1
30%	119.2	71	8.1	250.4	251.4	359	2550	84.1	21.4
20%	138.0	40	5.4	281.4	280.9	214	2577	83.7	12.8
10%									
5%									

Figure 2.1-7 26W Triple Biax® Amalgam Lamp Average. Data was taken in base down position.

Dimming	Vl (V)	Il (mA)	Pl (W)	Ic1 (mA)	Ic2 (mA)	Lumens	CCT (K)	CRI (RA)	%Full Lumens
100%	90.0	320	28.5	24.7	29.5	1934	2655	81.9	100.0
90%	95.5	271	25.6	49.8	49.1	1798	2630	82.3	93.0
80%	102.8	224	22.8	95.9	95.8	1628	2598	82.9	84.2
70%	109.9	184	19.9	137.0	136.8	1445	2582	83.3	74.7
60%	117.5	148	17.1	172.4	172.8	1240	2564	83.3	64.1
50%	125.2	116	14.2	203.2	204.0	1014	2556	83.6	52.4
40%	135.7	86	11.4	234.7	234.8	807	2553	83.8	41.8
30%	146.2	60	8.5	261.7	261.2	597	2556	83.8	30.9
20%	159.9	37	5.7	284.0	263.4	389	2567	83.7	20.2
10%	166.5	18	2.8	304.5	304.7	179	2583	83.7	9.3
5%	168.8	9	1.4	314.1	313.9	73	2582	83.7	3.8

Figure 2.1-8 26W Triple Biax® Non-Amalgam Lamp Average. Data was taken in base down position.

Dimming	Vl (V)	Il (mA)	Pl (W)	Ic1 (mA)	Ic2 (mA)	Lumens	CCT (K)	CRI (RA)	%Full Lumens
100%	99.1	320	31.30	20.5	27.3	2099	2724	81.5	100.0
90%	107.0	267	28.20	59.0	56.5	1840	2675	82.3	87.9
80%	112.4	227	25.03	95.1	95.7	1653	2651	82.8	79.1

Dimming	Vl (V)	Il (mA)	Pl (W)	Ic1 (mA)	Ic2 (mA)	Lumens	CCT (K)	CRI (RA)	%Full Lumens
70%	119.0	187	21.90	134.4	134.0	1442	2627	82.7	69.0
60%	126.0	152	18.77	169.1	167.9	1208	2618	83.3	57.9
50%	134.3	120	15.67	201.7	201.3	971	2606	83.5	46.6
40%	139.3	94	12.53	229.3	230.5	704	2593	83.7	33.9
30%	148.9	66	9.41	255.7	255.4	485	2600	83.7	23.5
20%	164.2	40	6.27	282.0	281.7	272	2617	83.4	13.2
10%	177.8	19	3.00	300.3	300.4	189	2613	83.3	9.8
5%									

Figure 2.1-9 32W Triple Biax® Amalgam Lamp Average. Data was taken in base down position.

Dimming	Vl (V)	Il (mA)	Pl (W)	Ic1 (mA)	Ic2 (mA)	Lumens	CCT (K)	CRI (RA)	%Full Lumens
100%	99.1	320	31.5	21.4	26.1	2182	2723	81.1	100.0
90%	106.2	269	28.3	50.9	50.9	2051	2677	81.7	94.0
80%	117.0	217	25.2	100.1	99.5	1879	2630	82.6	86.1
70%	127.6	175	22.0	145.5	145.6	1682	2604	82.9	77.2
60%	143.3	134	18.9	185.9	182.9	1440	2577	83.5	66.1
50%	155.9	103	15.7	219.9	219.2	1184	2568	83.6	54.4
40%	168.1	77	12.6	242.3	243.5	938	2562	83.7	43.2
30%	181.4	53	9.4	266.7	267.4	665	2566	83.8	30.6
20%	190.6	34	6.3	287.9	288.1	411	2569	83.8	19.0
10%	190.1	17	3.1	301.9	302.6	174	2576	83.9	8.3
5%	191.2	9	1.6	311.7	312.0	101	2559	83.7	5.0

Figure 2.1-10 32W Triple Biax® Non-Amalgam Lamp Average. Data was taken in base down position.

Startup time for the different lamps also affects their appropriateness for use in a BIAS fixture. The LRC study indicates that any noticeable startup time (i.e. > 20 seconds) was considered too long by the focus group participants. Figure 2.1-11 shows that with higher wattage, the Non-Amalgam lamps start much more quickly than the Amalgam, but that much of that effect is lost on the 26 W lamps - their startup curves are very similar.

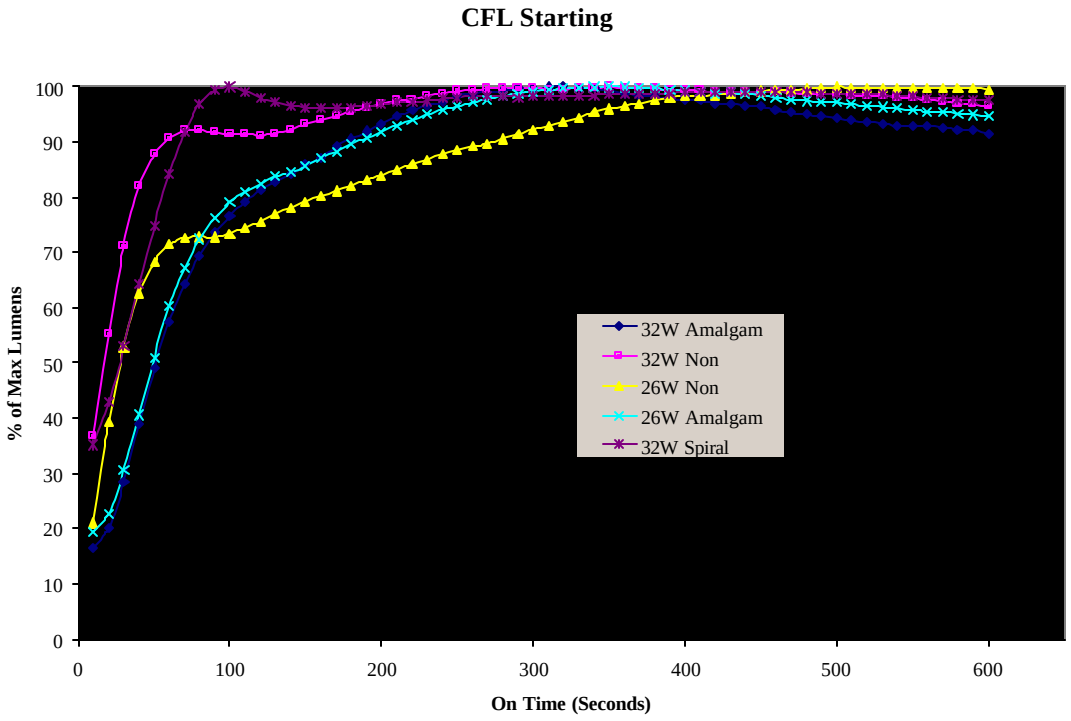


Figure 2.1-11 Amalgam vs. non-Amalgam lamp startup times

It was decided that the BIAS prototype should be able to accept two different plug-in lamps with minimal component changes, a 26W triple Biax® and a 32W triple Biax®, since the keying on both lamps is the same. It was also decided that the BIAS prototype would be optimized for the 26W amalgam triple biax lamp, yet would be able to accept the 32W plug-in lamps, as well as, non-amalgam versions of the each wattage. The amalgam was chosen since it is a readily available lamp to the US consumer, yet measurements were necessary on the amalgam vs. non-amalgam to determine the benefits to the final product if a non-amalgam lamp were made readily available.

2.2 Circuit Requirements

The ballast must meet several requirements to be useful in a typical US household or commercial environment as a replacement for standard incandescent lamps. The requirements listed below are necessary to develop the ballast.

2.2.1 Line Voltage

The ballast and lamp combination must operate with a line voltage of 120VAC (+10, -15%), at a frequency of 60Hz+/-1Hz. Nominal lumen output is to be achieved under nominal line conditions. The ballast must operate correctly over the specified range, albeit the lumen output may be reduced.

2.2.2 Lamp Starting

The ballast should be able to consistently start a good lamp. The lamp should be able to meet the specified number of starts.

2.2.2.1 Cathode Preheat

The ballast should preheat the lamp cathodes prior to lamp starting to reduce the starting damage as the lamp ignites.

2.2.2.2 Starting Voltage

The ballast should provide adequate voltage to start the lamp.

2.2.3 Dimmable Operation

The ballast is to have a user input, e.g. a knob that allows the user to dim the lamp to 20% of full lumen output. Operating in a dimmed condition must not significantly degrade the life of the lamp.

2.2.3.1 User Input

The user must be able to control the lamp power such that the lamp may be dimmed from 100% to 20% of rated lumen output. The dimming range should be continuous.

2.2.3.2 Power Control

The ballast must translate the user input into control of lamp power such that the range of rated lumen output is met.

2.2.3.3 Cathode Heating

The ballast must provide supplemental heating to the lamp cathodes as the lamp is dimmed, so that the lamp life is not degraded.

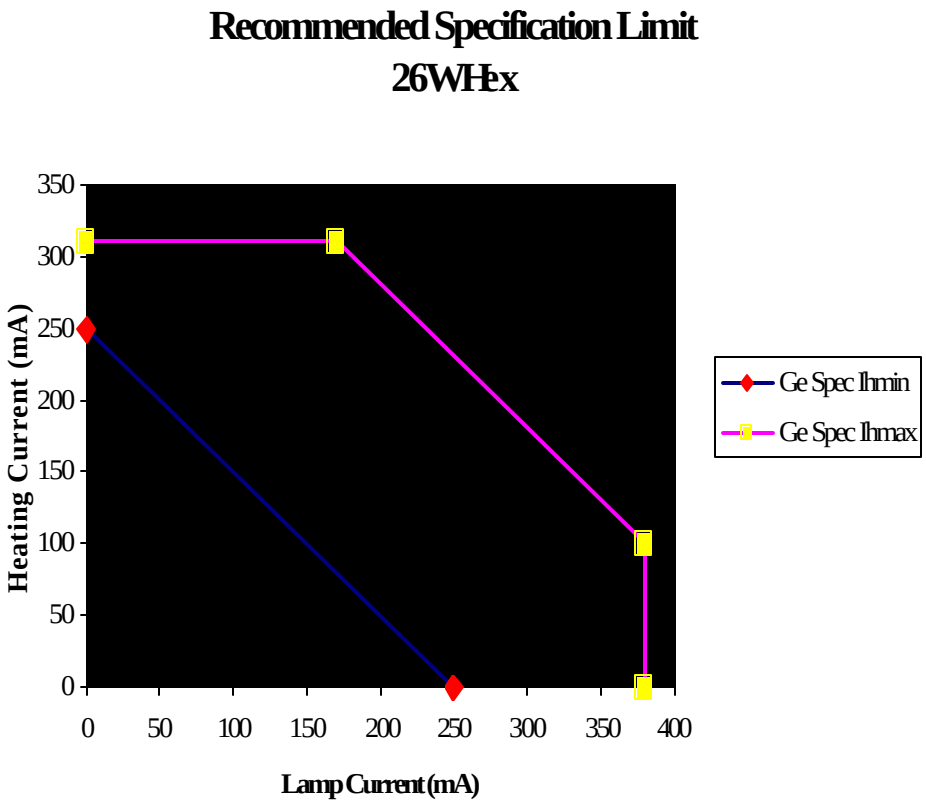


Figure 2.2-1 Specification Limits for 26W Hex CFL

2.2.4 Lamp Failure Protection

Since the ballast is intended to operate a removable, replaceable lamp, it must not fail under lamp failure conditions.

2.2.4.1 No-lamp startup

The ballast should sense the absence of a lamp upon power-up, and shut down the ballast if no lamp is present, without damage to the ballast.

2.2.4.2 Lamp start failure

If the lamp does not start, the ballast must detect this and shut itself down, without damage to the ballast.

2.2.4.3 Lamp Removal or Breakage

If the lamp is removed or broken while operating, the ballast must detect this and shut itself down, without damage to the ballast.

2.3 Low-Risk Path

2.3.1 Initial Tradeoffs

The development of the BIAS ballast had numerous possible approaches, ranging from low to high risk. Early in the program, several approaches were examined to determine the technique which best balanced pay-off and risk. The circuit can be split into two main parts: the ballast block and the inverter-control block. Tradeoffs were performed on each of these two blocks to decide on the main path.

2.3.1.1 Ballast topologies

The majority of modern ballast topologies consist of some sort of reactive network that connects a high-frequency AC voltage source and the lamp. The purpose of the network is to add enough impedance to the lamp's negative impedance so that the AC voltage source sees a positive impedance. This prevents the current from running away until one of the components is catastrophically destroyed. In principle, modern ballasts differ from older "magnetic" ballasts by the fact that the operating frequency is much higher than the line frequency.

At the beginning of the project, the team decided to look at alternative low-cost ballast topologies that minimized resonant component usage. It was found that the majority of these approaches had high associated risks, particularly in implementing the control required for dimmable operation and in potential generation of high levels of electromagnetic interference (EMI).

After many alternatives were considered, the final candidate emerged, based on the 29W 3-way CFL initially developed by GE Lighting. Although the lamp power was actually less than 24W, the lamp differed substantially from the target lamp in impedance, and had cathode resistances greater than twice those of the target lamp, it was felt that there was enough commonality to adapt the basic concept to the BIAS lamp.

The basic topology consists of a series-parallel LCC topology driven by a half-bridge MOSFET inverter (Figure 2.3-1). It differs from the more typical resonant tank ballast two ways. First, the series capacitor appears after the parallel capacitor. The benefit of this is that the lamp impedance is better matched to the

parallel resonant tank over a wider dimming range, which allows smaller circulating currents, lower losses, and smaller components. This placement precludes the practical use of shunt-cap control of cathode heating, so that the cathodes are heated when necessary by deriving an additional cathode current source from the resonant inductor. This results in a slightly more complex inductor, but provides a large dividend in the form of an additional degree of freedom for controlling the cathode current.

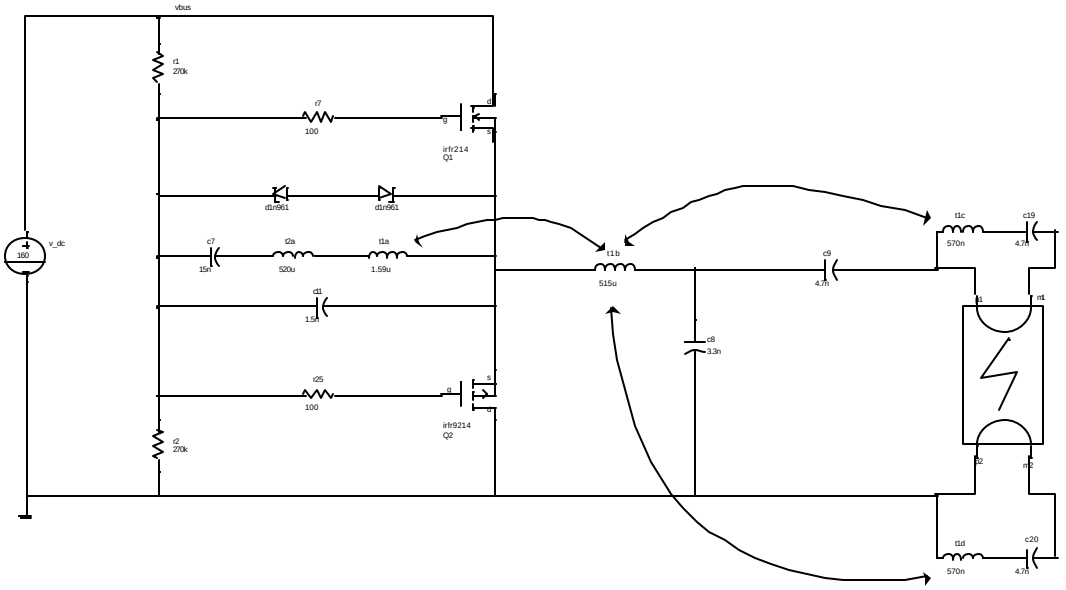


Figure 2.3-1 Basic ballast topology.

This approach had a number of benefits. First, GEL has substantial experience with this topology and the team at CR&D could benefit from their experience. Second, we could make use of custom-GEL parts that would otherwise be difficult for us to obtain. Third, the use of the common topology would make possible the development of a more general control IC that could be migrated into other product lines, vastly increasing commercialization potential and promising cost reduction as a result of higher component volumes. Fourth, the circuit has the potential to be very low cost.

2.3.1.2 Inverter

The ballast shown in Figure 2.3-1 must be driven by high-frequency voltage source. As the frequency of this source is varied, the reactive components of the ballast regulate the amount of energy into the lamp load. To minimize the size of the resonant components, the operating frequency must be kept relatively high. An upper limit on frequency is determined by considering EMI. If the maximum frequency is kept below 150kHz, the third harmonic will be below the 450kHz FCC limit and simplify the design. Thus,

the maximum frequency should be close to 150kHz. This requires MOSFETs as switches due to their high speed switching capability.

MOSFETs require a control signal to turn on and off, which is provided by a gate drive circuit. Several gate drive methods were examined, including transformer drives and commercial gate drive integrated circuits. After some consideration, GEL's proprietary L-comp gate drive was chosen.

The L-comp has the following key benefits: First, it has the potential for very low cost. Second, it is self-oscillating, and its oscillation is very robust and therefore resistant to disturbances. Third, it automatically maintains the frequency of oscillation above resonance, simplifying control. Fourth, it can automatically start and then run a lamp, without external control. Fifth, it can be designed to work under a large variety of conditions, from ultra-low-cost integrated CFLs to high-end electrodeless fluorescent lamps such as Genura.

The L-comp does have some drawbacks. First, its design can be quite complex due to interaction of components in a non-linear manner. Changes in one component can require changes in many others. Second, it requires the use of a P-channel power MOSFET. Versions of such parts suitable for fluorescent lamp ballasts are less common than their N-channel counterparts, and this limits the ballast to power levels under 50W unless complexity or cost is increased. Third, it requires a more complex magnetic component. While the more complex transformer is a slight drawback, it has the advantage of additional degrees of freedom in the design of the gate drive and the cathode heating control.

It was felt that the benefits of the L-comp outweighed the drawbacks; hence, it was used for the BIAS design.

2.3.1.3 Control

Several requirements of the BIAS ballast dictated that there be some means of controlling the ballast (Sections 2.2.2.1, 2.2.3.1, 2.2.3.2, 2.2.4.1, 2.2.4.2, and 2.2.4.3). Several approaches were considered:

- Discrete control
- Commercial ballast ICs
- GE-developed ASIC with conventional gate drive
- GE-developed ASIC for L-comp gate drive

Discrete control of the ballast was quickly ruled out based on simple considerations of cost and space. There was simply not enough room in the ballast envelope to fit all the required features at a reasonable

cost. While special manufacturing techniques (for example, flex-circuits and high-density interconnect) may have made it possible to implement the ballast, the cost would have been prohibitive.

A discrete version of the BIAS ballast was built in the first year, but no lamp protection was implemented in it. It was built primarily to test the ballast topology.

Several commercial ballast ICs were also investigated. These initially appeared quite attractive, but no single IC provided all the features necessary. Furthermore, many of the ICs with additional features were costly, some of them completely exceeding the budget for the entire ballast. The most promising of the commercial ICs was used in an early prototype, but the sensitivity of the circuit to component variations meant that expensive, tight-tolerance components would have to be used in the resonant tank. This would have raised the cost of the tank several fold, assuming that such parts could actually be obtained.

Dissatisfaction with commercial designs put us on the path of developing our own ASIC with all necessary features. We first considered a conventional gate drive type of control IC, whereby the IC would drive the MOSFET gates directly or through a transformer. However, once this path was investigated further, it was realized that this would require a great deal of silicon area as well as requiring older or non-standard proprietary IC processes. This approach would mean that the IC cost would be high, and that GE would be hostage to whatever supplier owned the process, i.e. GE could not shop around for the best price and quality.

After lengthy discussions with GE Lighting (GEL), it was decided to develop an IC that would be compatible with GEL's L-comp gate drive. It appeared possible to design such an IC, which would be compatible with standard IC processes, and which would have a very small silicon area. Furthermore, it was realized that the IC could be put in a very small, low-cost package. Finally, it was determined that the IC could also be made compatible with existing GE products, in particular, the GEL 3-way lamp. This last point was very important, since it maximized the chance that some of the work would be useful no matter the outcome of the program. Furthermore, the initial volumes of the 3-way lamp are high, and giving a cost-saving opportunity for the IC.

The details of the control IC are discussed in Section 2.3.2.5.

2.3.2 Ballast Design

The overall ballast was designed via a combination of simulation and experiment. Simulation tools are useful for trying out new ideas, or estimating variables that are impractical or impossible to measure.

However, simulations are only as good as the component models. Accurate models for all components are difficult to obtain, and often are too complex to simulate with usable speed. Experimental development is required in this case.

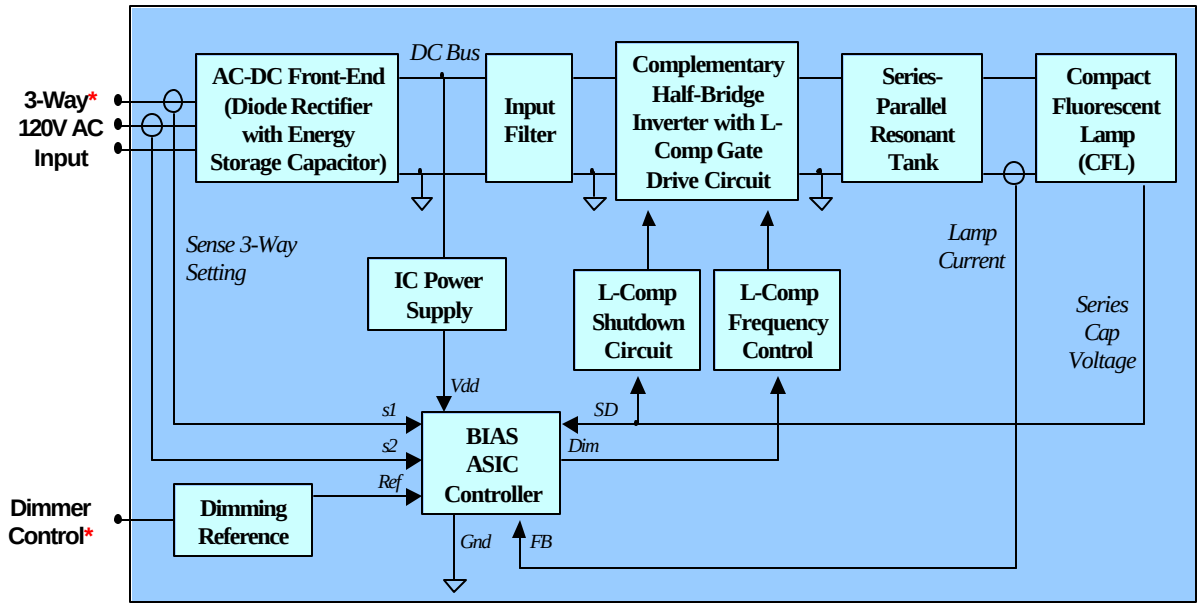


Figure 2.3-2 Block diagram of ballast.

We can begin the discussion at the power input. The AC line is connected to the AC-DC front end, which consists of a conventional full bridge rectifier with capacitive filter. The filter supplies the DC bus voltage, which has an average nominal value of about 155VDC. Three terminals are shown because the design is also compatible with the GEL 3-way. The BIAS only requires two of these.

The DC bus provides power to both the inverter and the IC. The inverter is supplied through the input filter, which prevents high-frequency energy from the inverter from getting to the AC line. This is necessary to meet EMI regulations. The IC power supply derives a low-voltage to supply the ballast controller ASIC.

The inverter with L-comp gate drive converts the DC bus voltage to a high-frequency square wave to the series-resonant parallel tank. The gate drive is controlled by the ASIC via a special frequency control circuit and a shutdown circuit, which work independently of each other.

The resonant tank filters the high-frequency square wave and provides a high-impedance source to drive the lamp, i.e. it provides the actual ballasting function. As the frequency of the inverter signal varies, so

does the impedance of the resonant tank circuit. This gives control over the lamp current and thus the lamp power.

The lamp current is sensed and fed back to the ASIC controller so that the lamp current may be regulated under closed-loop control. This provides more stable dimming, the ability to easily accommodate different lamps, and reduction of lamp crest factor, which is required for long life.

The series capacitor voltage is sensed to determine information about the lamp. In particular, it can be used to help sense the presence or absence of the lamp so that the controller can shut down the ballast when necessary.

The entire ballast is under the control of the BIAS ASIC controller. The ASIC is described in detail in Section 2.3.2.5, but the basic functions are described here. It provides a preheat-start for the lamp when the power is first applied. It then senses the user input either from a knob and potentiometer (in the case of BIAS) or the 3-way sense circuit (in the case of the 3-way CFL). The ASIC is designed so that it automatically senses which circuit it is in, so the same IC is compatible with either ballast at no additional cost or complexity. The user input is used to control the reference to the lamp current regulator, thus controlling the lamp lumen output via the L-comp frequency control. If no lamp is present on power-up, the ASIC senses this and does not attempt to start the lamp. If the lamp fails to start, or the lamp fails during operation, the ASIC senses this and shuts down the ballast before it overheats and fails

2.3.2.1 Lamp Modeling

In order to properly use simulation tools, it was necessary to develop a suitable model for lamp simulation. This model was based on the model of [3]; however, certain changes were necessary. In the original model, a quadratic curve fit was used to model the lamp I-V characteristic, but this was found to present problems at the extremes of practical operation. After much experimentation, an exponential curve fit was found to fit the data well and present benign behavior beyond the normal operating bounds of the ballast. This allowed reliable simulations to proceed.

The data used to fit the curve was based on 10 lamps. Each lamp I-V characteristic was measured, and the group of curves averaged. The average curve for the 26W lamp is shown in Figure 2.3-3. A general Saber model was developed that allows the input of the three curve-fitting parameters k0, k1, and k2, as well as a fourth parameter that models to first order the dynamic lamp behavior due to plasma recombination. This model is shown in Figure 2.3-4. The dashed blue line shows the curve derived from the average lamp data, and the red line shows the curve fit.

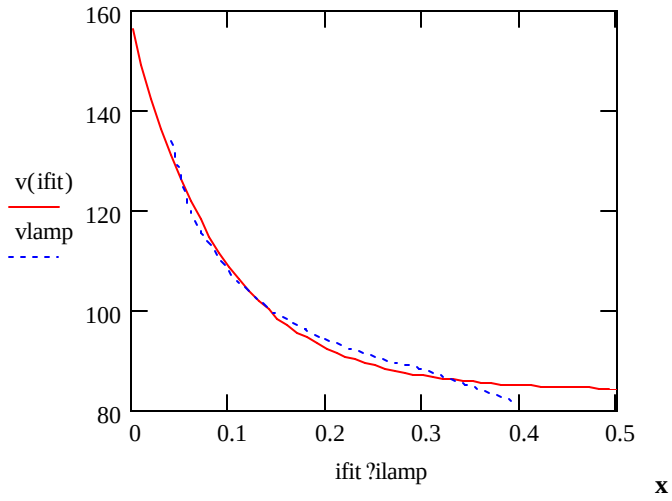


Figure 2.3-3 Three-parameter exponential curve fit for averaged 26W lamp data.

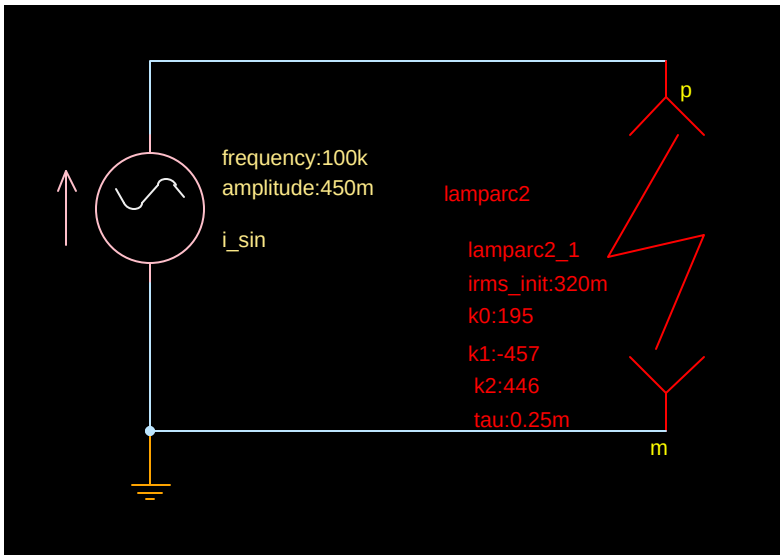


Figure 2.3-4 Saber model of lamp arc with test circuit.

2.3.2.2 L-Comp Ballast Operations

Basic operation of L-comp ballast with control

2.3.2.3 Ballast Design and Operation

The physical construction of the ballast is shown in Figure 2.3-5 , Figure 2.3-6, Figure 2.3-9, and Figure 2.3-10. Figure 2.3-5 shows the pieces of the BIAS ballast final prototype. Note that the circuit itself consists of two printed circuit boards, mounted back-to-back. The boards divide up the circuit into high-

frequency and low frequency sections. These will be discussed in more detail below. Figure 2.3-6 shows how the actual circuit board assembly fits into the ballast shell.

Figure 2.3-5 Main components of BIAS assembly.

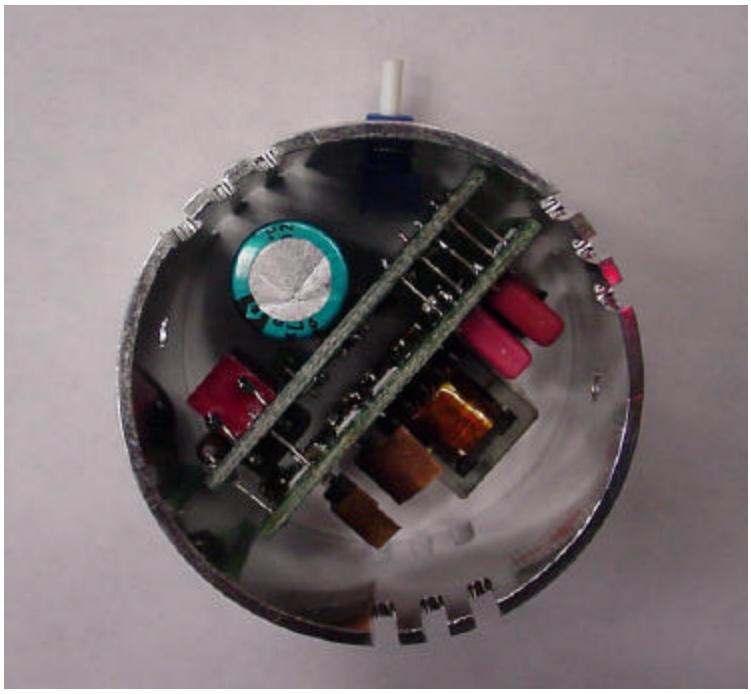


Figure 2.3-6 Photograph of BIAS assembly with lamp socket and bottom plate removed for clarity.

Figure 2.3-7 shows the final BIAS schematic. Figure 2.3-8 show a schematic with each of the blocks described in Section 2.3.2 delineated. The board in Figure 2.3-9 is the Inverter/Ballast board, which

contains the L-comp gate drive and inverter, the series-parallel resonant tank, and the L-comp shutdown circuit. The board in Figure 2.3-10 is the Input/Control board, which contains everything else.

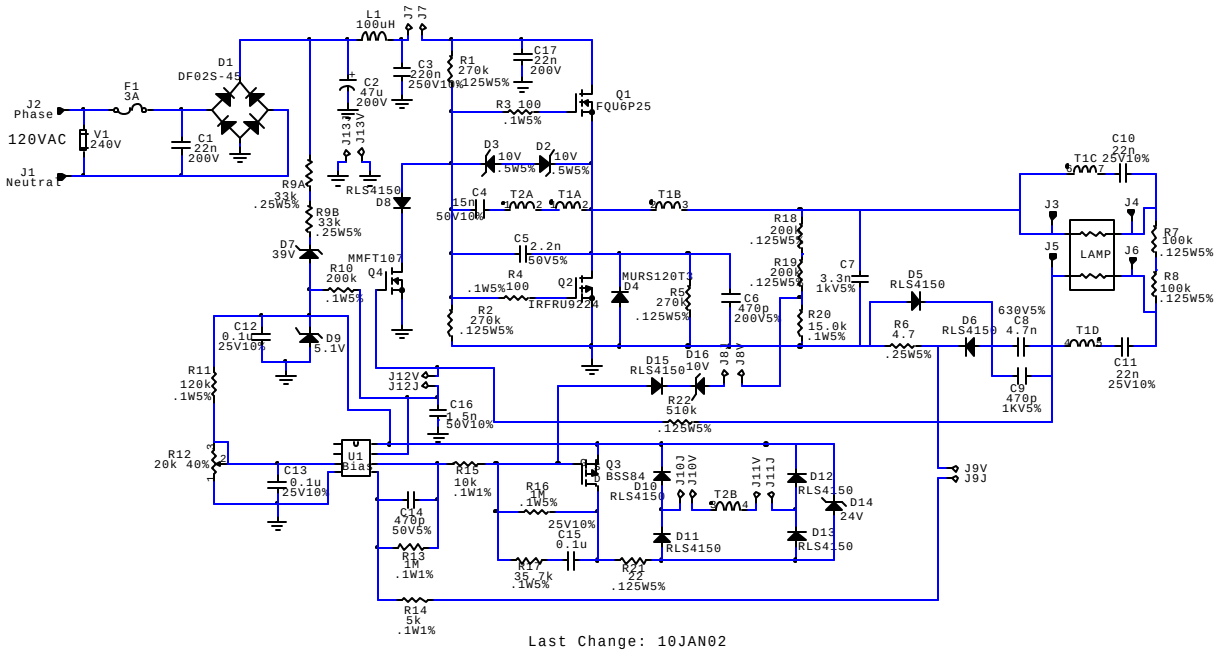


Figure 2.3-7 Final schematic of BIAS ballast

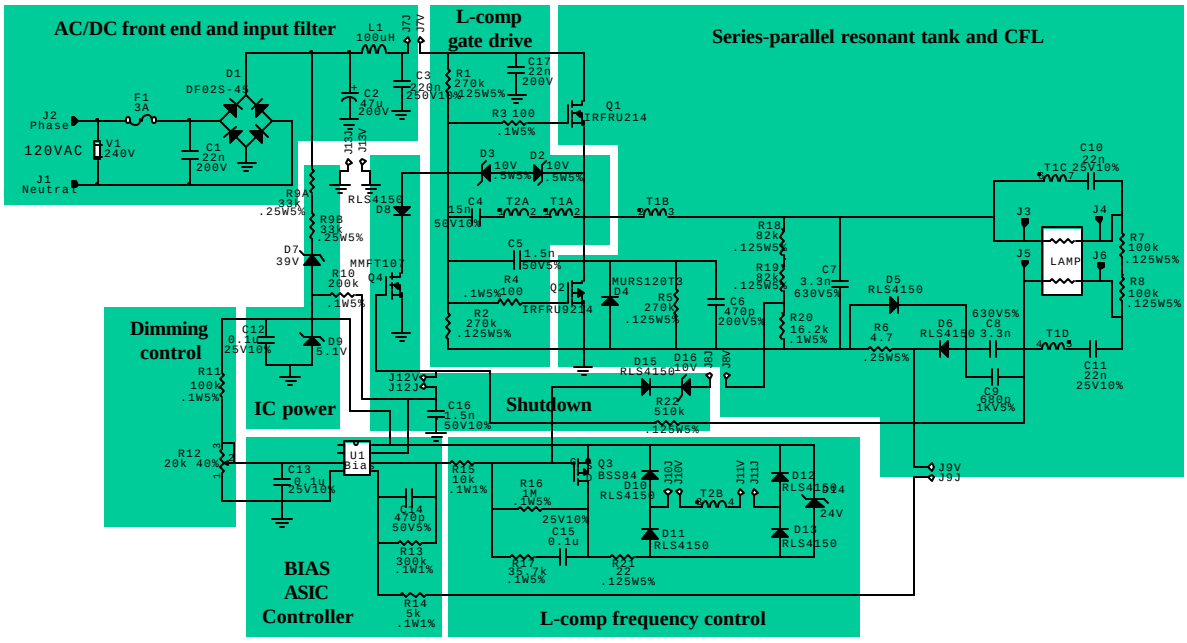


Figure 2.3-8 Ballast schematic with blocks corresponding to functionality.

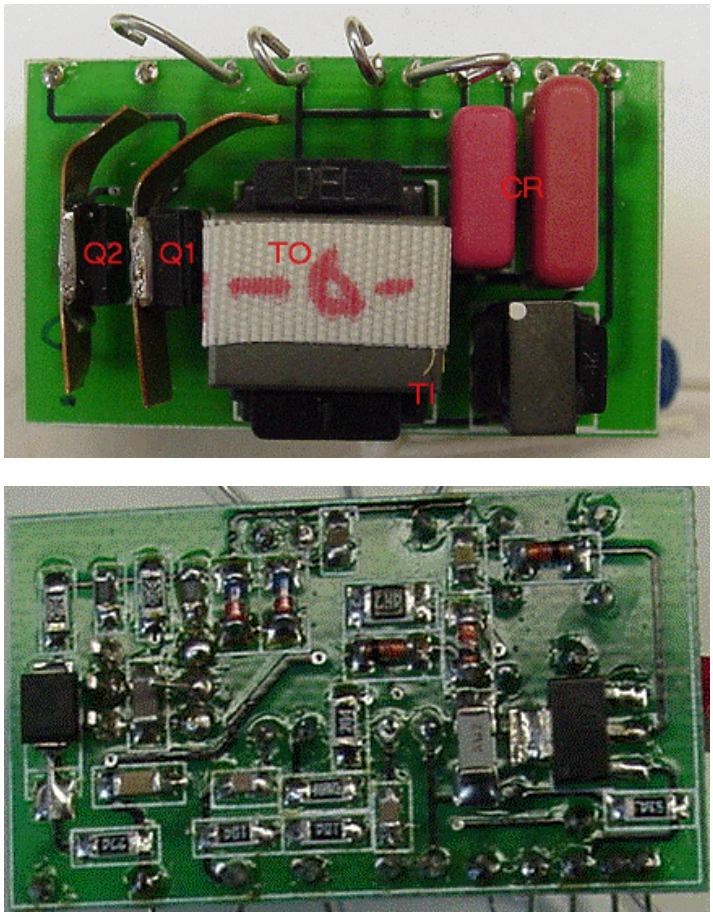


Figure 2.3-9 Inverter/Ballast printed circuit board.

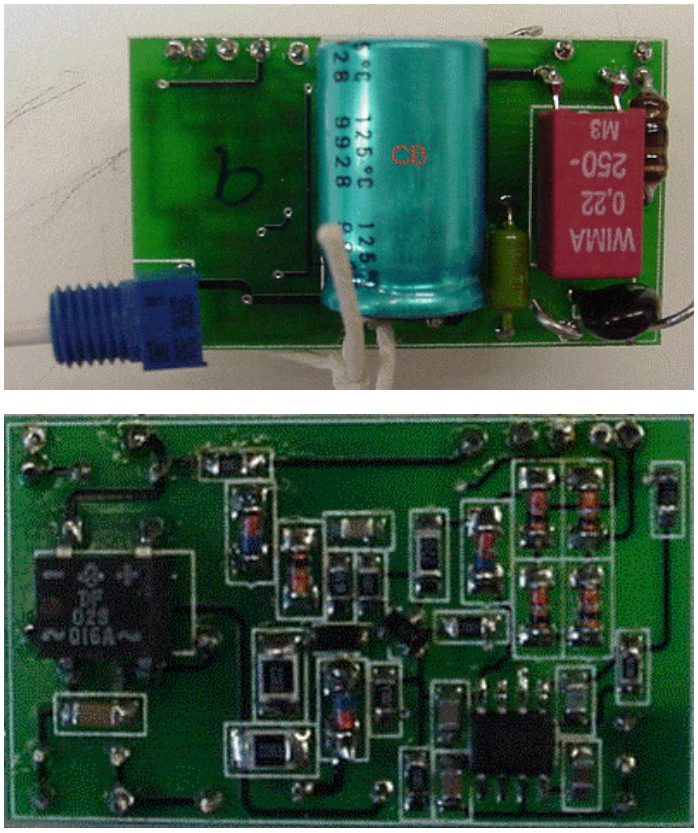


Figure 2.3-10 Input/Control printed circuit board.

2.3.2.4 Comments on BIAS design

The circuit basically performs as desired. There are a couple of key points to notes about the design to consider.

First, some functions were not integrated, namely the lamp removal protection and the lamp shutdown control. The lamp removal protection uses a discrete circuit with very fast response to bypass the current regulator loop. This is required in order to clamp the resonant tank voltage so that the ballast will not fail before the ASIC can shut it down. This approach results in lower ballast cost and size overall, since it allows the use of lower voltage components. It is likely that an improved implementation of the ASIC could integrate this function. The shutdown circuit is also unable to be integrated due to a high-voltage transistor required to force the gate drive off. This was an unexpected side-effect of the robustness of the L-comp self-oscillating behavior. There were alternate solutions, but these required additional windings, which did not fit on the desired magnetic core. Again, it may be possible to add this to the ASIC, but this

change will also require more extensive changes to the rest of the ballast, with currently unknown ramifications.

Second, the prototype circuit draws a small amount of power when connected to the AC line, although the ballast is off. The original discrete prototype used a control pot with an AC line switch, but this was developed for halogen lamps with large inrush currents. this meant that the switch itself was very large. The final version of the BIAS for the consumer market will need to have a new switch made to eliminate this loss. This was explored briefly with some switch and control manufacturers, who said that this was relatively simple, but would require tooling and NRE costs that were not in the development budget.

2.3.2.5 ASIC Controller

Overview:

The GEN-Ia IC is a low-voltage control IC developed for cost and component reduction in the integral 3-way and ballast-in-a-socket (BIAS) compact fluorescent lamps (CFLs) at GE-Lighting (GEL). The system diagram below overviews the application, where the 8-pin IC performs dimming control of a CFL lighting ballast, which consists of a rectifier, input filter, inverter (GEL proprietary L-Comp), and resonant tank.

This first iteration (Ia) is a test-chip that includes a fully functional core (as envisioned for the production part) along with additional circuitry and test points for design validation. It was packaged in both a 28-lead ceramic SOIC package for IC design validation and characterization and an 8-lead plastic SOIC package for pre-production system testing and demonstration. The test-chip was implemented in the AMI C5 0.5u double-poly, double-metal process, with dimensions of 1.7mm x 1.7mm. If the testing circuitry and pads were removed, the core along with the required eight I/O pads would have dimensions of 1.0mm x 0.5mm.

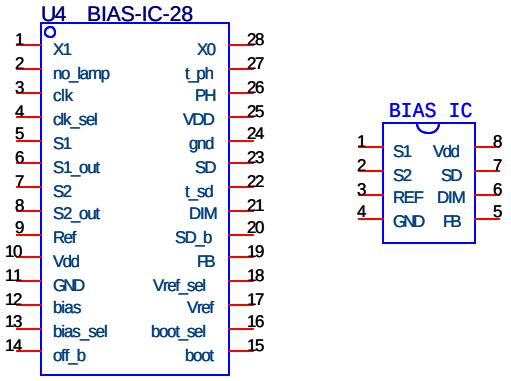


Figure 2.3-11 BIAS IC Pin Diagram

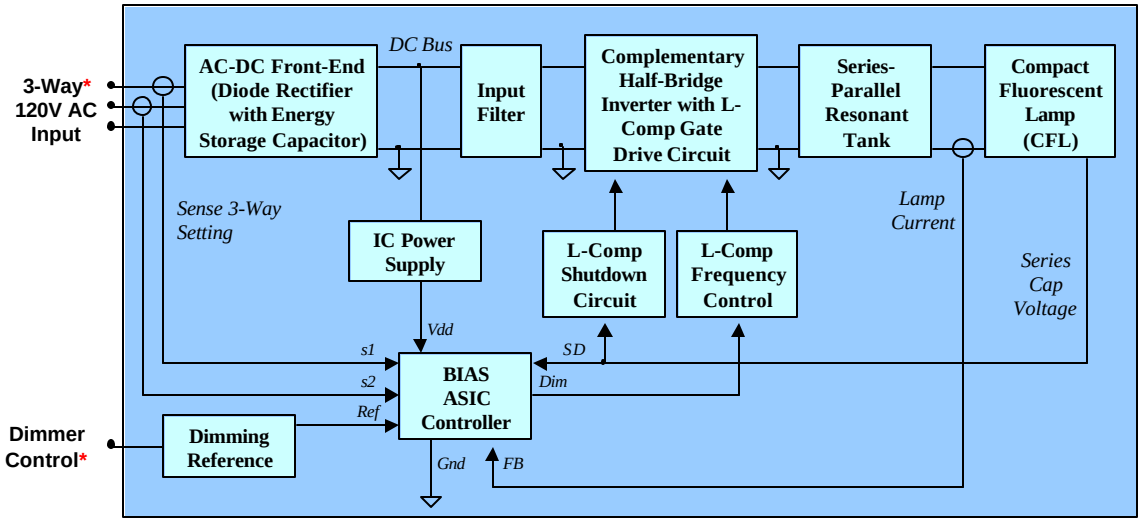
Features:

- ?? Closed-loop dimming control of GEL L-comp based CFL ballasts
- ?? On-chip 3-way sense circuitry for 3-way dimming -- significantly reduces components for integral 3-way product
- ?? Reference input for continuous (or multi-level) dimming and setting nominal lamp current level
- ?? Digital state-machine control for pre-heat and shutdown modes
- ?? Lamp failure (or no-lamp condition) protection via failure sensing and shutdown -- dual-purpose SD pin used for no-lamp/bad cathode detection and gate-drive shutdown (optional)
- ?? Compatible with standard 3-way socket, designed for low-high-med sequence to match current integral GEL 3-way product

Package Design:

Two package designs: (1) 8-LEAD SOIC, 0.150”, (2) 28-LEAD CSOP (for testing), as shown below.

System Functional Diagram:

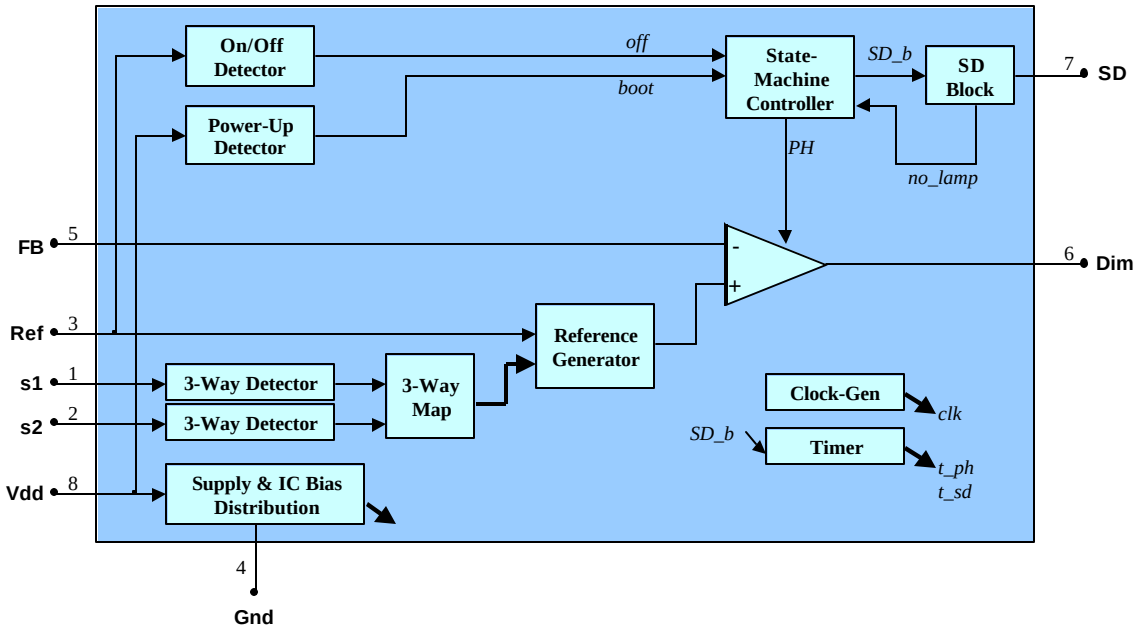


Pin Description:

28-Lead Pin #	8-Lead Pin #	Symbol	Description
5	1	S1	3-way input 1: To be tied directly to J1 (on 3-way schematic) via a large resistor (i.e. 1MOhm), must have a peak current between 10uA<Ipk<200uA
6		S1_OUT	Monitor 3-way detection of s1: HIGH=(Ipk>10uA), LOW=(Ipk<10uA); sampled via 500ms on-chip clock
7	2	S2	3-way input 2: To be tied directly to J3 (on 3-way schematic) via a large resistor (i.e. 1MOhm); must have a peak current between 10uA<Ipk<200uA
8		S2_OUT	Monitor 3-way detection of s2: HIGH=(Ipk>10uA), LOW=(Ipk<10uA); sampled via 500ms on-chip clock
9	3	REF	Voltage reference for feedback opamp: used for continuous dimming (BIAS) or nominal lamp current (3-way) reference input; 0.2V<Vref<3.5V; for Vref<0.2V IC enters OFF state
10		VDD	Secondary Vdd input for 28-lead package
11	4	GND	Primary ground pin
12		BIAS	Dual purpose test pin for on-chip current bias: SEL=HIGH ✍ p-channel current mirror input for setting IC bias current (Iin=4*Ibias); SEL=LOW ✍ p-channel current mirror output for sensing on-chip current bias (Iout=4*Ibias)
13		BIAS_SEL	Sets BIAS pin operation; on-chip pull-down sets SEL=LOW if no connection
14		OFF_B	Monitor output of Off Detector, active low; OFF_B=LOW for Vref<0.2V
15		BOOT	Input for forcing boot of state machine (enter INIT state)
16		BOOT_SEL	Enable for BOOT input; BOOT_SEL=HIGH ✍ off-chip boot control; on-chip pull-down default to LOW
17		VREF	Analog output for monitoring the reference input to the feedback op-amp
18		VREF_SEL	Enables sensing of VREF; on-chip pull-down default to LOW (disable)

28-Lead Pin #	8-Lead Pin #	Symbol	Description
19	5	FB	Feedback input: inverting input to feedback op-amp
20		SD_B	Monitor state-machine output for shutdown, active low
21	6	DIM	Feedback op-amp output to drive external control FET and compensation; shorted to Gnd during Pre-Heat state; performs dimming control in Normal Operation state
22		T_SD	Monitor nominal 500ms Shut-Down on-chip timer output
23	7	SD	Dual purpose pin: (1) during normal operation, shorts SD to < 1V (sinks up to +1mA, -500uA) while sensing current input to pin (for determining no-lamp or bad cathode condition), and (2) during shutdown, makes pin high-impedance to allow passive L-comp shutdown. For sensing no-lamp condition, pin is tied to positive series capacitor node via a (i.e. 500K Ohm).
24		GND	Secondary ground pin for 28-lead package
25	8	VDD	Primary VDD pin, 5V; estimate 3mW power consumption
26		PH	Monitor state-machine output for driving pre-heat
27		T_PH	Monitor nominal 1sec pre-heat timer output
28		X0	Monitor internal operating state
1		X1	Monitor internal operating state
2		NO_LAMP	Monitor SD Block output for no-lamp detection
3		CLK	Dual purpose: monitor/drive on-chip clock
4		CLK_SEL	Select CLK function: HIGH = drive IC clock; LOW = monitor / use on-chip clock; on-chip pull-down for default LOW

IC Functional Diagram:

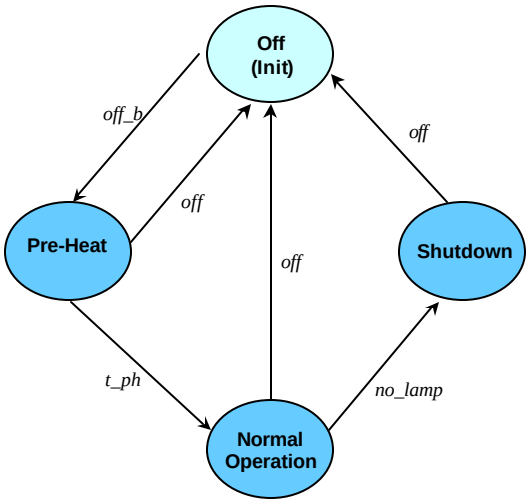


General Description:

The IC uses the same analog op-amp based compensation approach as the current 3-way integral product. The op-amp is integrated along with a state-machine controller and supporting detector circuitry to perform the functions of preheat, closed-loop dimming control, 3-way dimmer socket position sensing, and shutdown (for lamp failure or removal).

Functional Description:

State-Machine Diagram:



State-Machine Inputs:

Input	Description
t_ph	Output from pre-heat timer
no_lamp	output from SD block
off	output from on/off detector
boot	(not shown): asynchronous reset for SM to force OFF state on power-up

State-Machine Outputs:

Output	Description
PH	drive ballast into pre-heat mode by forcing “DIM” pin low
SD_b	control operating mode of SD pin – HIGH = short SD to ground and sense current, LOW = SD pin to high impedance

State Output Table (Moore Design):

State \ Output [X1 X0]	PH	SD_b
Pre-Heat [0 1]	1	1
Normal Op [1 0]	0	1
Shutdown [1 1]	1	0
Off (Init) [0 0]	1	0

State Description:

State	Description
Off (Init) State	At power-up or turn-off the IC enters the OFF state. While in the OFF state, PH is set high (setting DIM low and driving ballast into preheat), and SD_b is set low to allow the (optional) shutdown circuit to force the ballast to stop oscillating. The power-up condition is determined through a detection circuit that monitors the "VDD" input and outputs a "boot" command to the state-machine. The BOOT signal is tied to an asynchronous reset for the state-machine, forcing the OFF state. Turn on/off is used for the BIAS product to turn the CFL on and off through the dimming control in the socket. An on/off detector senses the analog REF input and outputs a high on OFF when the reference is below the minimum value (0.2V).
Pre-Heat State:	When in the OFF state and a low is detected on the OFF input, the IC enters the PRE-HEAT state. In this state, the pre-heat timer is enabled (through SD_b) and the PH output is used to force the op-amp DIM output low, driving the ballast to its maximum (or cathode pre-heat) frequency. The pre-heat timer is used to set the cathode heating time (nominal 1 sec.). For the Integral CFL product, the IC enters the OFF state at power-on, then immediately transitions into the PRE-HEAT state.
Normal Operation State:	When the pre-heat cycle is complete, the pre-heat timer output goes high, and the IC enters the NORMAL-OP state. The IC remains in this state until the SD block outputs a "no_lamp" condition, at which point the IC enters the SHUTDOWN state. The SD block functions as a lamp detector during normal operation by sensing the peak positive voltage on the series power stage capacitor (one node tied to ground, in series with the lamp). A large resistor (i.e. 500K) is connected between the cap and the SD pin. A resistor may also be placed in parallel with the lamp (such that current flowing through parallel resistor must flow through lamp cathodes) to prevent shutdown when lamp extinguishes prematurely and cathodes are still good. The SD block senses the current through the SD pin and outputs a high "no_lamp" condition if the current is ever continually below the reference (Iref=100uA) for the sample period (500ms). If the optional shutdown circuit is being used (BIAS product), then during normal operation both the SD self-biasing current and the capacitor voltage sensing current flow through the SD pin. The scaling of these currents should be selected to achieve the desired noise margin for shutdown detection. One possibility for the 32W/26W BIAS product is to use Isd_bias = 40uA (4MEG resistor from Vbus, 120Vac supply), Rcap_sense = 500K, resulting in total peak SD pin currents ranging from 650uA to 185uA over the worst case dimming range (300mArms to 25mArms). The additional margin allows normal operation under continuous low-line conditions (initial experimental results show ballast and lamp operating down to Vac=45Vrms, resulting in total peak SD current in above scenario of 122uA). The 500ms sampling window allows rejection of momentary extreme low-line conditions (exp. results show Vbus and lamp current decaying to zero in ~60ms, and IC supply decaying to 1.5V in 300-500ms). If the brown-out / black-out exceeds 500ms in duration, then the IC supply will drop and the power-up/boot circuit will reset the state-machine when the AC power is restored. In the event of a lamp failure or removal, the SD pin current will drop (to zero or Isd_bias, typically within 200-300ms) continually below the reference and the IC will enter the SHUTDOWN state. The ballast must be designed to operate continually open-circuit for up to one second (interval could be adjusted in next IC iteration or for production run).

State	Description
Shutdown State:	In the SHUTDOWN state, the PH output is high (forcing the ballast to the pre-heat frequency) and the SD_b output is low (allowing the optional shutdown circuit to stop L-comp gate-drive oscillations). The next state is always the OFF state, which can be entered by turning the BIAS control off (OFF=1) or by cycling the power (BOOT=1). The SD_b output is also used to reset the pre-heat/SD timer.
Off (Init) State:	The outputs are identical to the previous state. The purpose if this state is to allow direct on/off control of the BIAS product (through the min threshold on REF). To re-start the integral CFL product, the power must be cycled. In addition, for the BIAS product, if the lamp is removed and re-inserted, either the power or on/off switch must be cycled to re-start the lamp.

Circuit Description (Implementation)

The complete schematics of the prototype IC are attached to this datasheet, along with physical package descriptions from AMI. Each of the circuit schematic blocks is described briefly below:

Top Level:

The top-level schematic combines the functional blocks along with I/O pad drivers and testing circuitry for external monitoring and control. The MUX circuit (MUX1) near the Clock Gen block (upper-left) is used to select on or off chip clock and allow monitoring of the on-chip clock through the CLK and CLK_SEL pads. The circuitry surrounding the I-Bias block (lower-left) is used to control on or off chip current bias. P-channel device Mp7 is configured as a current-mirror input or output, with current scaled to 4*Ibias (Ibias=10uA, nominal). A resistor can be used from BIAS pin to ground for sensing or controlling on-chip current bias, according to setting of BIAS_SEL pin. Mp8 and Mn2 (lower-center) are used to allow sensing of on-chip voltage reference (output of Ref Gen, input to fb_opamp). Sensing can be turned on/off via VREF_SEL so loading and noise coupling of VREF pad can be removed. BOOT and BOOT_SEL pins, along with tri-state buffer ITD1 allow off-chip forced state-machine reset. All testing selection pads are default to LOW via on-chip resistors to allow open-circuit operation with only eight core pads in use.

State Machine:

The state machine was designed using the Moore approach, with the outputs determined by the current state alone. The state transition table is given shown below in Figure 2.3-12.

		Inputs			Outputs		
Current State	Current State	t_ph	no_lamp	off	PH	SD_b	Next-State
Off (Init):	0 0	x	x	1	1	0	0 0
		x	x	0			0 1
Pre-Heat:	0 1	0	x	0	1	1	0 1
		x	x	1			0 0
		1	x	0			1 0
Normal Op:	1 0	x	0	0	0	1	1 0
		x	x	1			0 0
		x	1	0			1 1
Shutdown:	1 1	x	x	0	1	0	1 1
		x	x	1			0 0
	X1 X0	I1	I2	I3	O1	O2	X1 X0

Figure 2.3-12 BIAS IC Prototype State Transition Table

Clock Generator:

The clock generator uses an on-chip oscillator (fosc = 131kHz) followed by 12 flip-flops to generate a 32Hz on-chip clock. This clock is used to drive the state machine and timer blocks. The oscillator is derived from a bi-directional current source that supplies +/- Ibias/5 = +/- 2uA to an integration capacitor, Cosc, followed by a schmitt trigger with 2V hysterisis.

Pre-Heat / SD Timer:

The oscillator frequency was selected so that the two timer outputs (t_ph=1sec, t_sd=0.5sec) would be powers of two from the clock to reduce components to simple flip-flops vs. full counters. Four flip-flops are used to generate t_sd, and three additional flip-flops are used to generate t_ph with proper timing. The state-machine output SD_b is used as a reset (reset during shutdown and off states), and the t_ph output is guaranteed to stay LOW after res_b goes HIGH for the pre-heat duration (vs. t_sd which ripples HIGH on first clock).

Feedback Op-Amp:

In the application, the feedback op-amp is used as a compensator for the lamp current feedback loop. In the current 3-way CFL product, the compensation is a low-pass-filter with low frequency gain Acl=30 and crossover frequency of fc=1.13kHz. The highest frequency with significant harmonic content is at the ballast operating frequency, ~100kHz. As a rule-of-thumb, the op-amp was designed to have an open-loop gain significantly greater than the closed-loop filter gain at the maximum frequency of interest, or

Aol(100kHz) > 50*Acl(100kHz) = 15 = 23dB, which requires GBW>1.5MHz. The resulting design has Ao = 60dB, GBW=3.4MHz, PH=55 degrees at unity feedback configuration. Additionally, the other specs were analyzed for the CFL application as summarized below:

Feedback Op-Amp Specs:

- (Vcm) range: 0V < Vcm < 3.5V
- (Vo) range: 1.5V < Vo < 5V (assuming external short to ground for preheat)
- GBW > 3MHz
- Ao > 60dB
- SR > 0.1 V/us
- (Io)max > 300uA
- Stability: PM>50 deg at unity-feedback configuration (also test at current 3-way configuration)
- (Voffset)max = 5mV

Reference Generator:

The feedback reference is generated using a unity-gain op-amp to buffer the voltage reference input (REF), followed by a resistive divider and analog MUX for controlling 3-way settings.

Vref Op-Amp:

The reference op-amp was designed for very large DC gain, very low offset voltage (likely much more so than necessary), and low bandwidth for stable operation and filtering of noise from reference input. A symmetrical OTA design was used with cascade current mirrors and common drain output. The predicted specs are given below:

Reference Op-Amp Specs:

- Ao = 77dB
- GBW = 250kHz
- Vcm range: 0V < Vcm < 3.8V
- (Io)max > 1mA (only require 35uA max, positive)
- Vo range: 0V < Vo < 3.8V
- PM ~ 90 deg at unity-feedback configuration
- Voffset < 1mV (but up to 25mV would be acceptable)

The reference op-amp area could be reduced in future iterations using a simpler voltage buffer with reduced requirements (current design is pad limited for area).

SD Block:

The shutdown block uses a current mirror to sense the current through the SD pin (while maintaining an input voltage below Vsd < 1V) and compare it to a current reference (Ibias=10uA, Mp1). The flip-flops (ff1, fff2) are used to sample the current comparison over the clk interval (clock tied to t_sd=500ms in top level). The sampling is such that the current through the shutdown pin must be below the reference (Isd < 10*Ibias=100uA) continually for an entire sample period (500ms) for the no_lamp signal to go HIGH. The SD_b input and devices Mn3 and Mn4 are used to determine whether the input is a current mirror (for pre-heat and normal op states) or a high impedance node (shutdown and off states).

Off Detector:

The Off Detector was designed to sense the REF input and output a low on Off_b (active low) when REF was below 0.25V. In addition, a 0.2V hysterisis was added for noise immunity and tolerance of the external potentiometer. The function of the Off Detector allows a single low-power potentiometer to be used for dimming and on/off control of the BIAS CFL product, where a detent near the setting that delivers 0.25V to the REF input could be added for tactile feedback to the user that the lamp is off. The circuit is designed around a differential pair input (0V to 3.5V Vcm) with 0.34V reference, a differential decision circuit for 0.2V hysterisis, and symmetrical OTA to drive the output.

3-Way Detect:

The 3-way detector compares the input current to a reference current (Ibias=10uA), and samples the output over a clock interval (t_sd=500ms). The sampling is such that the input current must be below the reference for the entire sampling interval for the output Sx_OUT to go LOW. This circuit allows a single resistor to be tied from the input Sx to a respective AC Phase input to the rectifier (follows positive AC sine wave for half-cycle, one diode drop below ground for half-cycle). Input device Mn1 was designed for Vsx = 2.5V at 200uA input; maximum expected input current is 170uA with 1MEG Ohm resistor tied between line and Sx.

Current Bias:

The current bias is a Vt reference bias with startup circuit. The bias resistor Rb=64K is implemented in a high-resistance poly layer (1000 Ohm/sq). This circuit could be changed for a smaller resistor if this layer were not available in another process.

Power-up (Boot):

The boot circuit is a fixed-current source based design, where a capacitance (via Mn3) is charged after Vdd exceeds the combined threshold of Mn1 and Mn2. The combination of fixed threshold and charge time guarantee that the boot signal will rise slow enough to provide the (active low) reset to the state-machine, assuring the INIT state on power-up. The circuit dissipates a quiescent current of ~ 5uA during normal operation. The reverse body diode of Mp2 dissipates the charge on Mn3 when Vdd decreases.

I/O Pad Cells – BID, IN, and OUT:

These bi-directional, input, and output digital cells were used to drive / buffer the IC pads. The pad cells used were standard ESD pads from AMI, and pads with built in digital I/O drivers were not available.

Packaging Diagrams and Information:

The bonding diagrams and package descriptions supplied by AMI are attached for the 8-lead and 28-lead packages.

2.3.3 Conclusions from Low-Risk Path

The design of the ballast was successfully completed. It employs a custom ASIC that works to control all low-cost, high-performance ballast. Section 3 covers performance tests in detail.

During the development of the ballast, several new ideas came to mind that have the potential to further improve ballast performance/cost ratio. Many of these ideas had substantial risk associated with them, but the potential benefits were great enough that some time was spent exploring them. These are discussed in Section 2.4

2.4 High-Risk, Very Low Cost Path

2.4.1 Overview

As discussed previously, several ideas with potential for much improved ballast performance and cost were briefly examined. While these ideas did not make it into this version of BIAS, they offer possible benefits not only to a commercial version of BIAS but other lighting products as well. In this section we will discuss some of the technologies which were discussed but not fully developed due to scope and time constraints.

2.4.2 PWM Method of Continuous Frequency Control for L-Comp

2.4.2.1 Background

Self-oscillating resonant inverters, such as commonly used in compact fluorescent electronic ballast, typically operate by deriving a transistor switching waveform from one or more windings that are magnetically coupled to a resonant inductor. When the need arises to control the converter output to the load, one method to accomplish this is discussed in U.S. Patent # 5,965,985 (Nerone)[1], whereby the effective reactance of a reactive element is controlled by a variable resistance that may be in series or parallel with said reactive element, as determined by the needs of the circuit. This variable resistance is commonly implemented with an active element such as a transistor, where the effective resistance across two terminals is a continuous function of the magnitude of the control signal. The applied control signal is also continuous, and has a maximum frequency component substantially lower than the switching frequency of the converter. This is shown in Figure 2.4-1.

Transistor Q forms the active element. The diode bridge network allows the typically unipolar Q to act as a bipolar resistive element. In this case, the reactive element to be controlled is an inductor L, which is implemented in this case as a coupled inductor. This implementation in not necessary in principle, but is beneficial in practice.

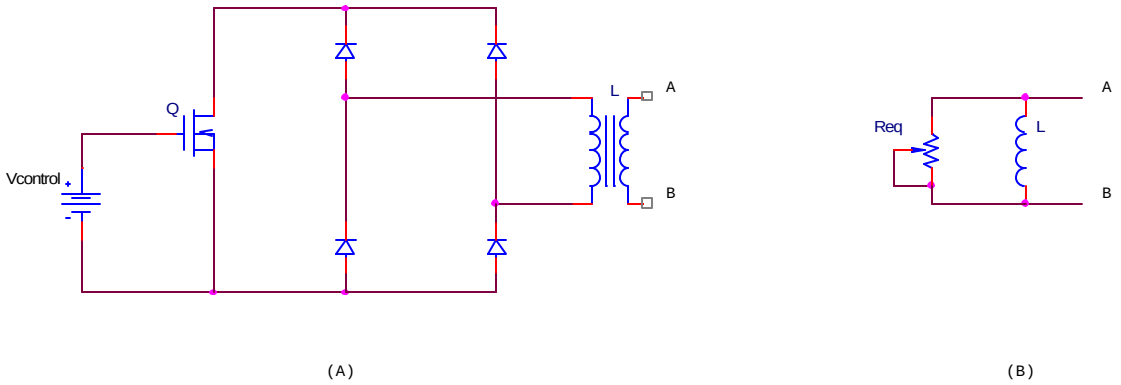


Figure 2.4-1 Current implementation of variable reactance control element for self-oscillating control. Actual circuit shown in (A), and equivalent circuit shown in (B).

Applications for the aforementioned converters, such as CFL ballasts, typically require small size and low cost. In order to achieve these goals, it is desirable to integrate as much of the electronics as possible onto a semiconductor integrated circuit (ASIC). Furthermore, digital electronics have the potential for lower cost and decreased sensitivity to parameter variations compared to analog electronics. It therefore is desirable to implement as much of the circuitry in digital form as possible. However, the aforementioned digital approach requires a D/A converter which adds substantially to the complexity of the system. Another difficulty in integrating the above approach is the fact that substantial power may be dissipated in the control element, which makes it more difficult to integrate on the chip.

A possible solution is to control the switch such that it turns on and off for part of each switching cycle. This approach, its many variations, and its properties are well described in the literature, but it has a serious drawback in that the switch control waveform must be synchronized to the power waveforms in the converter tank circuit. In the case of the self-oscillating converter, this requires even more complexity in the form of a frequency-tracking circuit such as a zero-crossing detector or phase-locked loop.

Another approach that does not require synchronization is described in a patent application by Louis R. Nerone of GE Lighting (GEL). In this invention, the switch is turned on and off at a rate much slower than the switching frequency. The ratio of time spent in each of the two states controls the average power to the load. However, this control method necessarily lowers the response speed, or control bandwidth, of the converter. Furthermore, this may present other difficulties for some applications of the switching converters.

The objective of this invention is to control a self-oscillating switching power converter by means of an active controlling device that is implemented by turning a switch either fully on or fully off in a manner

that does not require the control switch waveform to be synchronized with the converter switching frequency. This is to be accomplished without compromising the response speed of the converter. The basic implementation of the controllable reactance is shown in Figure 2.4-2 for controlling the effective reactance of an inductor. The diode network serves to make a bi-directional application practical with commonly used active devices, which are usually unidirectional. The switch Q1 is turned completely on and off at a frequency F_1 , which is substantially greater that the maximum frequency F imposed on the terminals A and B. In the simplest implementation, the switch is Q_1 which is controlled by a pulse-width modulated waveform with a duty cycle D, as shown in Figure 2.4-3. The effect of this waveform is to vary the average resistance seen in parallel with the inductance L between nodes A and B, where the average resistance is given by R_{eq}=R/D. This relies on the assumption that the value of R is substantially greater that the on-resistance of switch Q1. This in turn varies the effective inductance between A and B in a manner well known to those versed in the art.

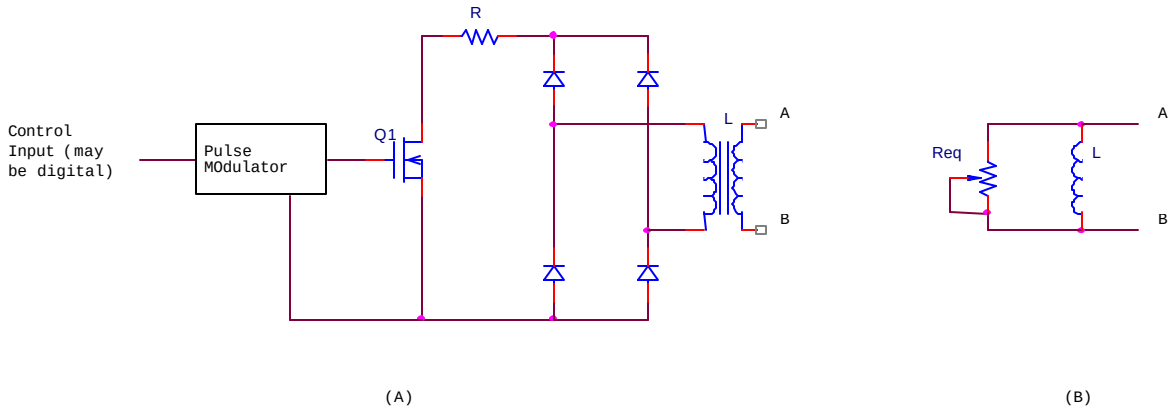


Figure 2.4-2 Switched resistor control (A) and equivalent circuit (B).

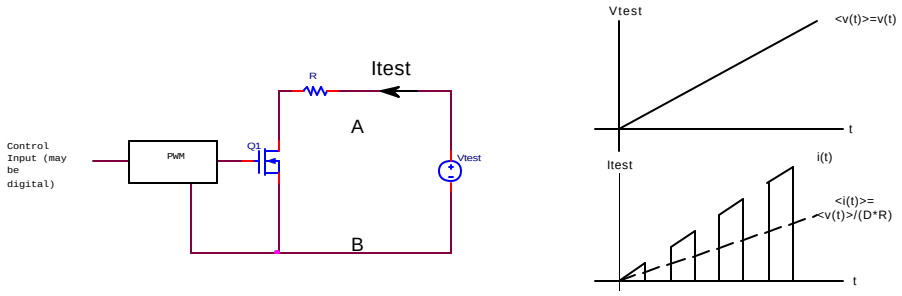


Figure 2.4-3 PWM control and effective resistance. Transistor Q1 is controlled via conventional pulse-width modulation.

This approach has several major advantages over other approaches. First, because the Q1 control frequency is substantially greater than the switching frequency, the intrinsic bandwidth of the switching

converter is not compromised. Second, because no synchronization is required, the complexity is reduced. Third, this approach increases the digital portion of the control ASIC and reduced the analog portion. This adds the benefits of increased robustness, lower cost, and reduced ASIC support components, the latter being difficult or expensive to implement on an IC.

Fourth, since R is substantially greater than the on-resistance of switch Q1, the majority of the power dissipation occurs in R. This component can be left off the ASIC, and the reduced dissipation in Q1 allows it to be integrated on the IC. Finally, the effective resistance generated by this method shows a very small dependence on the transistor parameters. Therefore the effect is more consistent and predictable even in the face of large transistor parameter variations.

Other modulation methods besides PWM are also possible. One such method would be to modulate the control signal with a band-limited pseudo-random binary stream. This would have the additional benefit of spreading the frequency spectrum of the switching converter and thereby reduce the effective electromagnetic interference generated by the circuit.

Saber simulations verify the validity of this concept, as applied to a compact fluorescent lamp electronic ballast, shown in Figure 2.4-4. The results of the simulations based on an electronic ballast are shown in Figure 2.4-5 and Figure 2.4-6. Figure 2.4-5 shows startup waveforms for a CFL ballast with where the aforementioned PWM control has been substituted for the analog control. After startup, it can be seen that the lamp current and power are regulated quite well. Figure 2.4-6 is from the same simulation data set, but a small section of time. The output of the PWM is shown in this figure, and its variation is apparent as the control loop starts to regulate the lamp current. In addition, Figure 2.4-6 shows the waveforms on the control inductor T1. The pulsed current in T1 occurs when the switch Q1 is on. While the peak current is high, the average current is such that the equivalent average resistance is the same as the resistance produced by the original circuit of Figure 2.4-1. The change in duty-cycle as the control loop brings the lamp current into regulation is readily apparent.

The invention has not been reduced to practice.

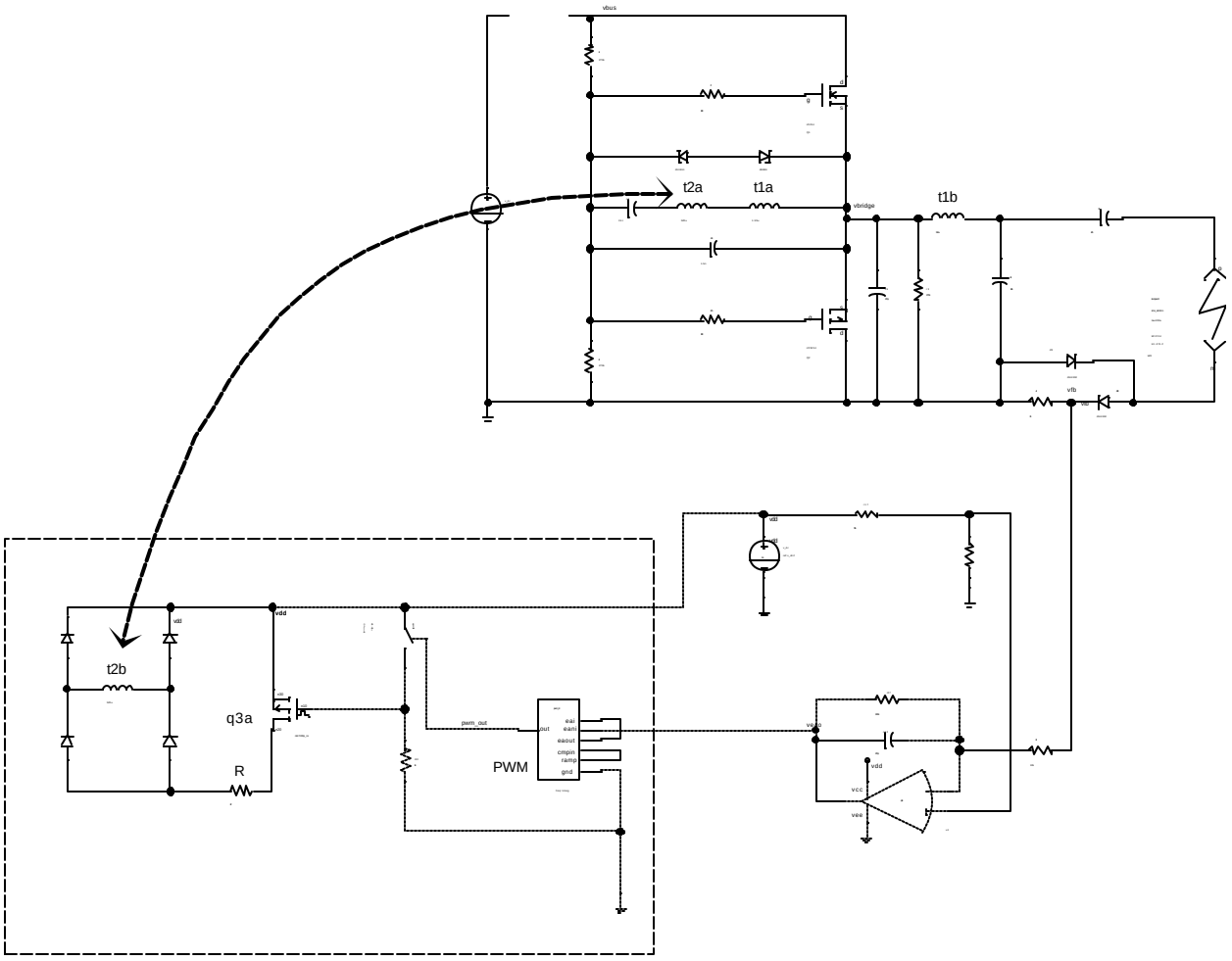


Figure 2.4-4 Schematic for simulation of CFL ballast application of invention. The area within the dashed line includes the pulse-width modulator, switch Q3a (same as Q1 in Fig. 2), coupled inductor T2 (same as L in Fig. 2), and resistor R. The curved line linking T2A and T2B explicitly shows the coupling.

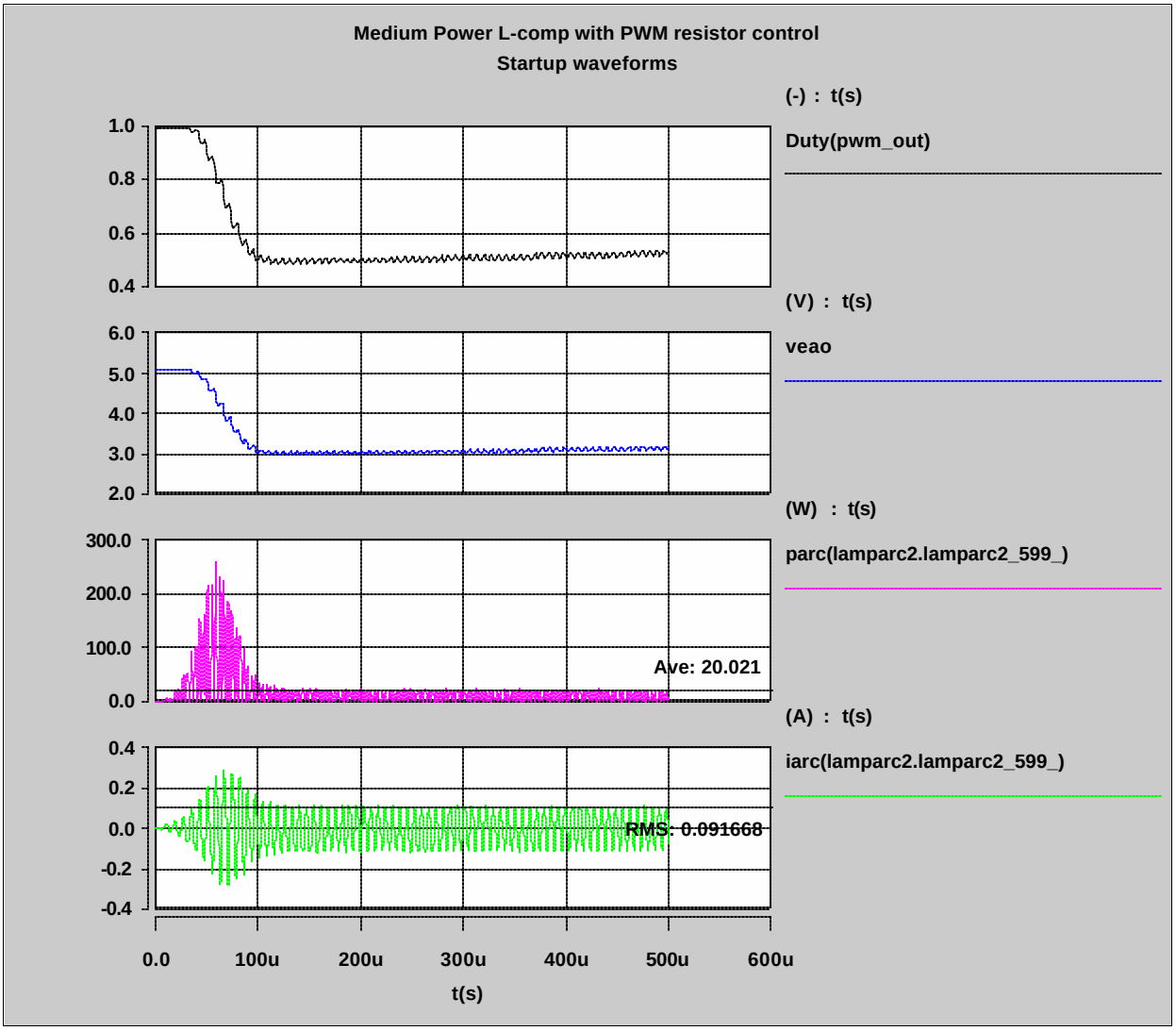


Figure 2.4-5 Startup waveforms of CFL ballast circuit of Figure 2.4-4. After an initial transient, the control loop is regulating the lamp current as shown, indicating the proper operation of the control loop and the PWM controller. Without an control loop, this ballast is unstable and the lamp extinguishes (lamp current goes to zero).

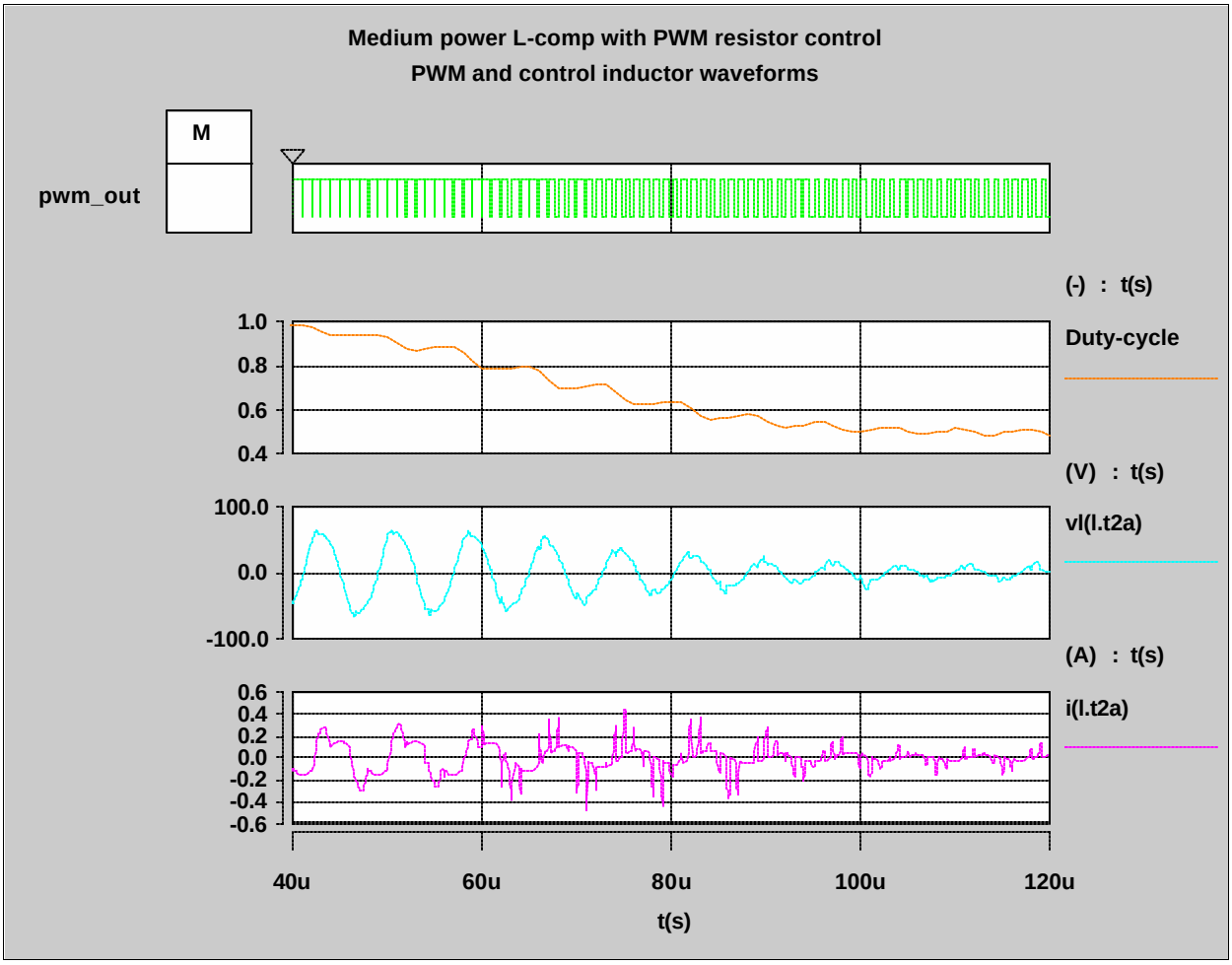


Figure 2.4-6 Detailed view of same ballast showing operation when control loop begins to regulate the current. The top waveform shows the PWM signal to the switch, and the 2nd from the top shows the value of the corresponding duty cycle. The lower two waveforms show the voltage and current of the control inductor T2. The spikes in the current waveform occur when Q3A is turned on.

2.4.3 Dynamic Analysis of Frequency-Controlled Electronic Ballast

2.4.3.1 Introduction

With the growing demand for more intelligent and universal lighting products, there exists a significant need for improved design-oriented tools for the development of lighting electronic ballasts. This report presents design tools for analyzing the dynamic behavior of dimming fluorescent ballasts, which aid the design of feedback controllers and give an intuitive understanding of the effects of component and load changes on the loop stability.

Generally, dimming ballast designs rely on the stable open-loop "current-source" characteristics of the resonant tank to assure stability over the complete dimming range when a simple low-frequency feedback loop is added for dimming control. However, in practice, oscillations can result at low power levels due to the high Q of the resonant circuit and negative incremental resistance of the fluorescent lamp. In order to predict and compensate for these phenomena, dynamic analysis of the control to output transfer function is needed. As shown in Figure 2.4-7, the control input can be bus voltage variations (amplitude modulation, AM) or frequency control (frequency modulation, FM), and the desired output is the resulting envelope variations in the lamp current. These issues were investigated and modeled using a time-varying phasor transformation in [5] for the special case of operation at resonance with AM In [3], [4] a SPICE model was developed using the phasor transform to enable envelope transient simulation of AM and phase modulation (PM). Additionally, AC analysis was performed through repeated transient simulations while adjusting the modulation frequency.

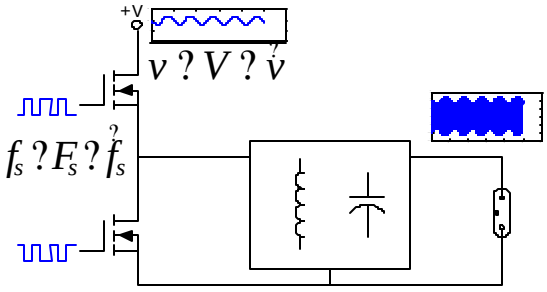


Figure 2.4-7 The high-frequency ballast driven by AM/FM input

In this report we present a complete large and small-signal model of the frequency controlled (FM) dimming ballast through a modification of the phasor transform used in [3] [4][5]. A SPICE-compatible model is then described for direct AC analysis of the ballast system. Finally, a closed-form solution of the frequency-to-output transfer function of the ballast is given, along with key observations that facilitate simple and intuitive solution of the transfer function low-frequency gain and system poles, which can be used for development of the feedback network.

2.4.3.2 Modified phasor transformation and its application to the ballast

The object in performing the phasor transformation is to remove the switching frequency components of the waveforms and analyze the dynamics of the signal envelopes. The transformation approach was first proposed in [1], where any sinusoidal signal can be represented by a complex phasor:

$$x(t) \approx \mathrm{Re}[\underline{\tilde{X}}(t)e^{j\omega_s t}],$$

Equation 2.4-1

and $\underline{\tilde{X}}(t)$ is the time-varying phasor corresponding to $x(t)$. The transform was intended for systems operating with constant frequency ω_s, but a very significant case for dimming ballasts is variable frequency control. In order to accommodate FM, we propose a modified phasor transformation:

$$x(t) \approx \mathrm{Re}[\underline{\tilde{X}}(t)e^{j\int_0^t \omega_s(t)dt}],$$

Equation 2.4-2

which removes the FM component from the phasor $\underline{\tilde{X}}(t)$. By applying Equation 2.4-2 to the basic circuit elements, we can get the phasor models for the basic circuit elements as shown in Figure 2.4-8. These models are similar to those in [1], except that here the imaginary resistors can be time varying. Perturbing and linearizing the elements yields the small-signal phasor models, which are also shown in Figure 2.4-8.

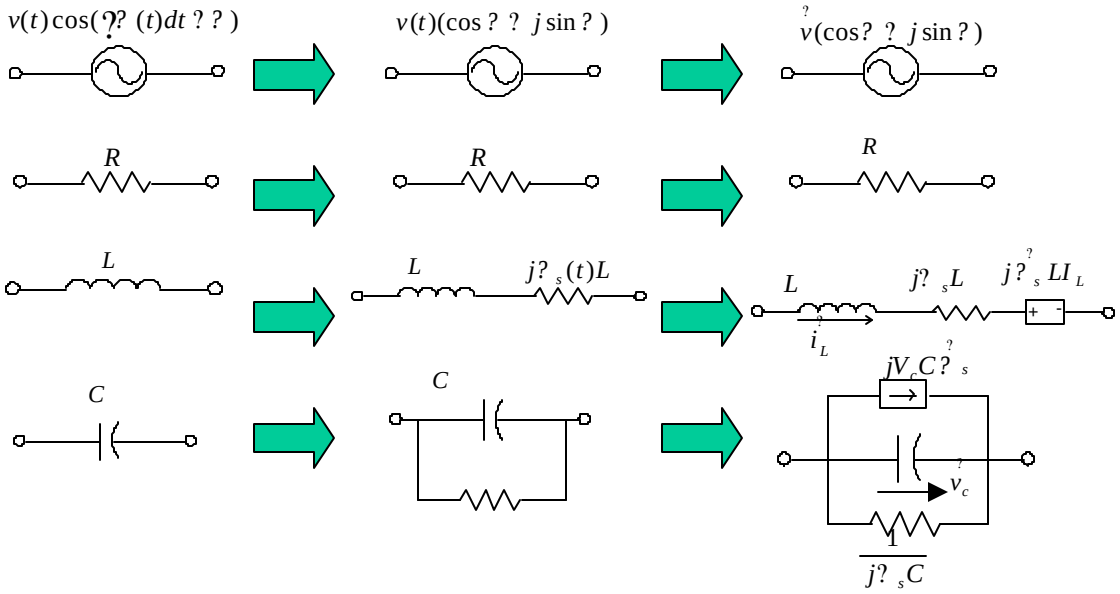


Figure 2.4-8 Large signal and small signal phasor models for basic circuit elements

The transformation of any resonant topology can then be found by simply replacing the basic elements according to Figure 2.4-8, as shown in Figure 2.4-9 for typical LCC resonant ballast. Once the phasor of any signal is obtained by solving the phasor model, the original signal envelope can be recovered by finding the magnitude of the phasor as [3] [4]

$$|x(t)| = \sqrt{x_1^2 + x_2^2}$$

Equation 2.4-3

Its small-signal relationship is:

$$|\hat{x}(t)| = \frac{1}{X}(X_1 \hat{x}_1 + X_2 \hat{x}_2)$$

Equation 2.4-4

where X, X_1 and X_2 represent the steady-state values of $x(t)$ and its real s and imaginary parts.

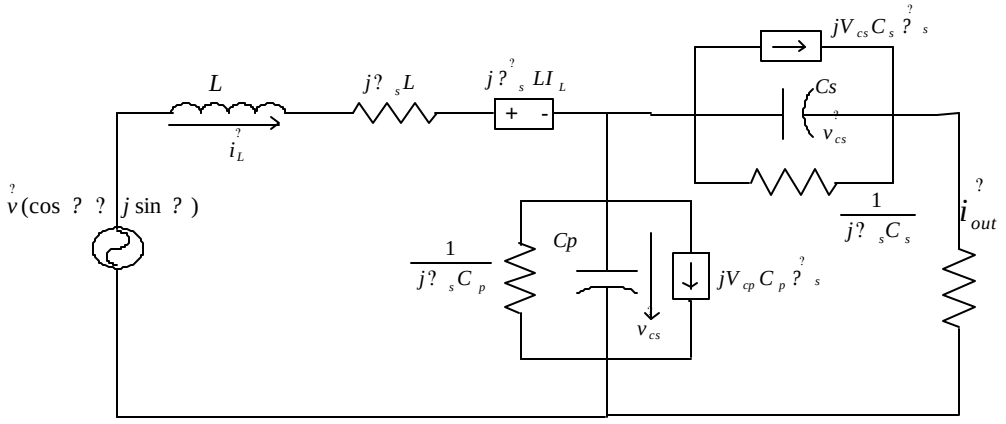


Figure 2.4-9 Small-signal phasor model for LCC ballast

2.4.3.3 SPICE-Compatible Model and Experimental Verification

Due to the existence of imaginary resistors, the model in Figure 2.4-9 cannot be directly realized in a SPICE-compatible simulator. However, using the same approach presented in [3], this complex circuit can be split into real and imaginary parts, as shown in Figure 2.4-10, then implemented in a SPICE simulator for transient and AC analysis. Figure 2.4-11 compares PSpice simulation and experimental results of the transfer function from frequency control to output current. After the gains of the V/F converter (which is used to generate the switching frequency modulation) and the current sensors are taken into account, the actual measured low-frequency gain is –97db, which is in good agreement with the simulation results. The large-signal transient analysis has also been conducted, which is shown in Figure 2.4-12 . It can be seen that the model accurately predicts the envelope of the original AM signal.

In the discussion above, the simulation and experimental results are found using a resistive load. For more accurate results, the lamp model can be incorporated into the ballast model, as shown in Figure

2.4-13 [4]. The simulation and experimental results are compared in Figure 2.4-14, where a 26W compact fluorescent lamp (CFL) was used as the load.

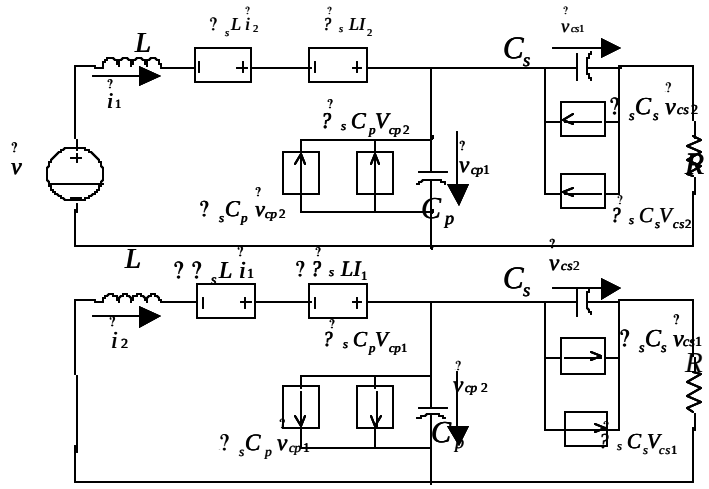


Figure 2.4-10 Spice-compatible small-signal phasor model for LLC ballast

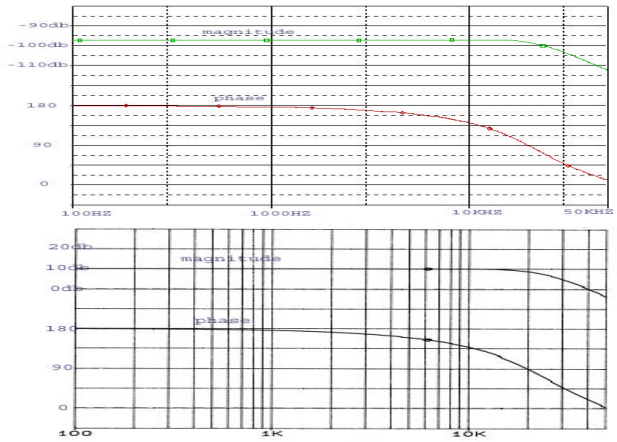


Figure 2.4-11 Simulation (top) and measurement (bottom) results of frequency-to-output current transfer function

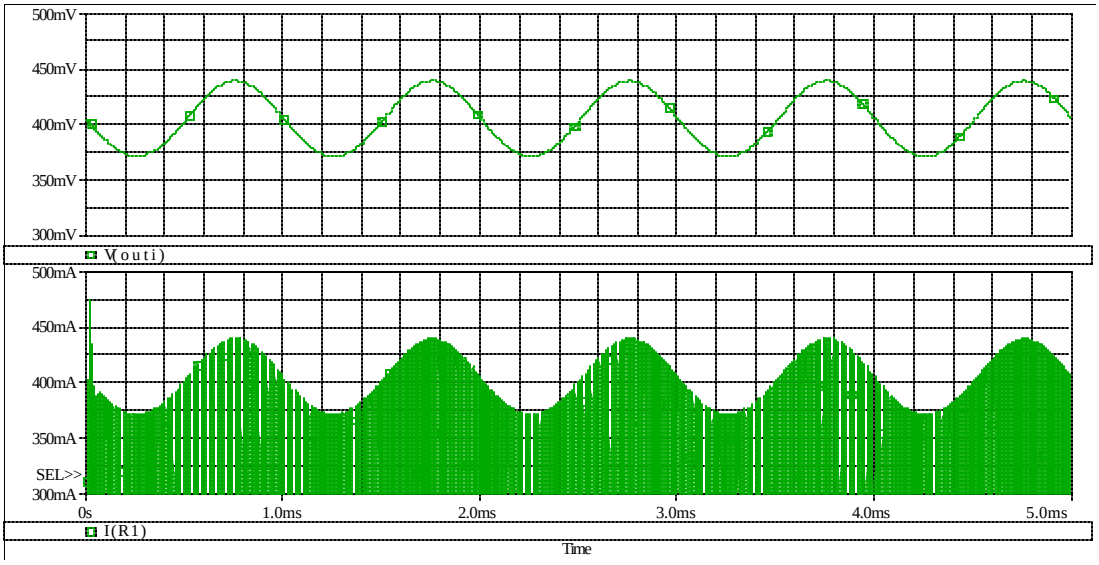


Figure 2.4-12 Transient analysis given by the model (top) and the original LCC ballast (bottom)

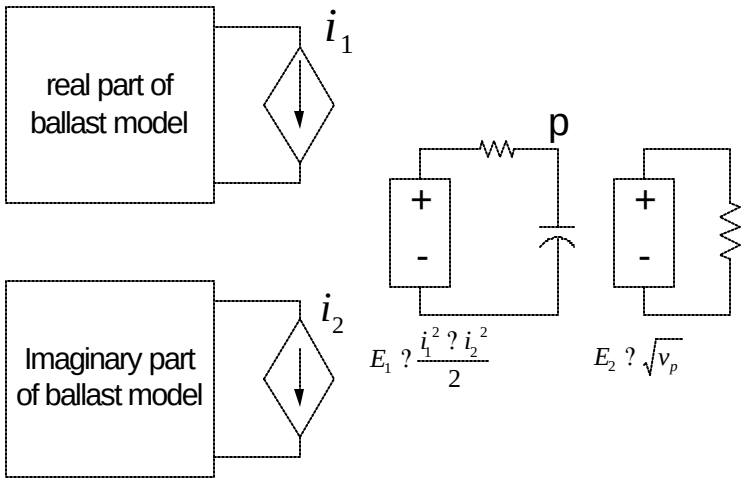


Figure 2.4-13 Spice model for fluorescent lamp frequency-to-output transfer function using a 26W CFL load

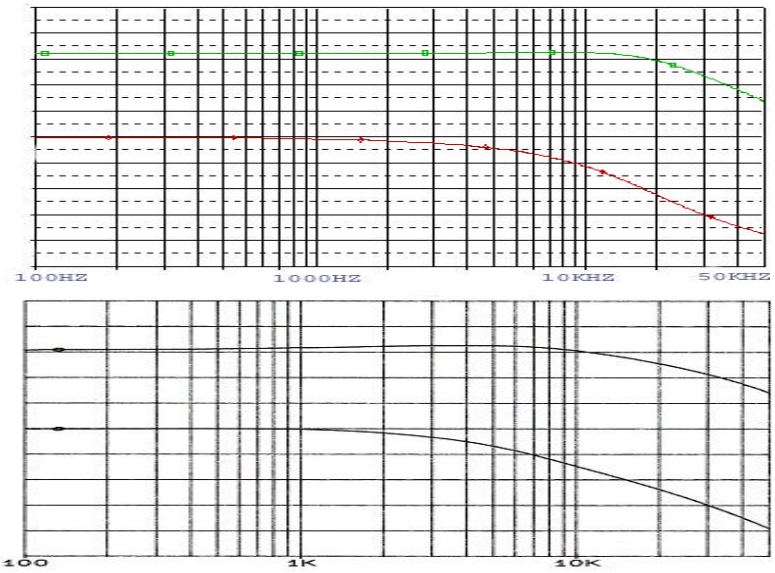


Figure 2.4-14 Simulation (top) and measurement (bottom) results for frequency-to-output transfer function using a 26W CFL load

2.4.3.4 Design-Oriented Analysis

The SPICE models of Section 2.4.3.3 facilitate dynamic analysis of dimming ballasts, but still lack intuitive design-oriented aids useful for the development of ballast systems. In this section, we highlight a few key observations from the theoretical analysis that give a more intuitive feel for the system operation. By solving the model in Figure 2.4-9, the phasor transfer function from frequency to output current can be manipulated into the following closed form:

$$G_{f\,?\,ph}(s)\,?\,\frac{\overset{?}{i}_{out}}{\overset{?}{f}}\,?\,\frac{N(s\,?\,j?_s)}{D(s\,?\,j?_s)}\,?\,\frac{N(s\,?\,j?_s)D(s\,?\,j?_s)}{D(s\,?\,j?_s)D(s\,?\,j?_s)}\,?\,G_{f\,?\,ph\_re}(s)\,?\,jG_{f\,?\,ph\_im}(s),$$

Equation 2.4-5

where D(s) represents the characteristic equation of the original LCC tank, and N(s) is a second order polynomial. Then, the transfer function from frequency to output current envelope of the original circuit can be expressed as:

$$G_f(s)\,?\,\frac{|\overset{?}{i}_{out}|}{\overset{?}{f}}\,?\,\frac{1}{\sqrt{I_{out1}^2\,?\,I_{out2}^2}}(I_{out1}G_{f\,?\,ph\_re}(s)\,?\,I_{out2}G_{f\,?\,ph\_im}(s))$$

Equation 2.4-6

Although the resulting closed-form solution is an intimidating sixth-order transfer function, when put in the form of Equation 2.4-5 and Equation 2.4-6, it can be seen that the poles of the system are simply the poles of the original LCC tank D(s) shifted up and down by $j?_s$. This is a nice intuitive result, as it agrees with a classical communications style approach to the problem, which would see the input as a frequency modulated carrier that is passed through the LCC tank. As the ballast is generally operated near and above the resonant frequency, this creates complex pair of poles at low frequencies, which dominate the open-loop response over the bandwidth of a typical feedback controller. The pole diagram for a typical ballast is shown in Figure 2.4-15, where "*" represents the poles of the ballast, and "?" represents the poles of the small-signal model. The low-frequency gain of the transfer function can also be determined from the closed-form solution, although it may be even simpler to determine the DC gain directly from the steady-state solution of the ballast, as the slope of the output current-to-frequency curve, as shown in Figure 2.4-14.

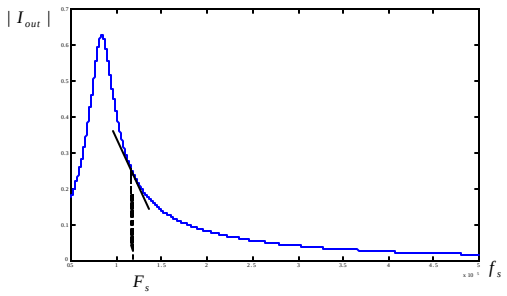


Figure 2.4-15 Low-frequency gain of the model

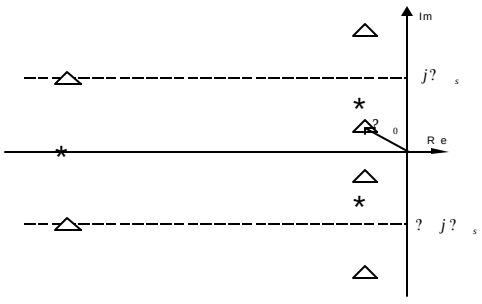


Figure 2.4-16 Poles of the ballast and the small-signal model

2.4.3.5 Conclusions

In this report, we have presented tools useful for dynamic analysis of dimming electronic ballasts and development of feedback compensation networks. A SPICE-compatible model was presented for direct AC analysis of the effects of frequency control on the lamp current envelope. This model has also been used for envelope transient simulations, resulting in significantly reduced simulation times. To aid development, key observations were presented that give intuitive analytical results on the low-frequency gain and pole locations of the control-to-output transfer function.

3 Ballast Performance

3.1 Electronics Performance

Figure 3.1-1 shows the final BIAS prototype operating with a standard 26W plug-in CFL. The overall ballast performance has been verified by independent testing at the LRC (Section 3.4). This section shows waveforms that verify the main performance of the ballast.

Figure 3.1-1 Final version of BIAS with 26W lamp operating at full power.

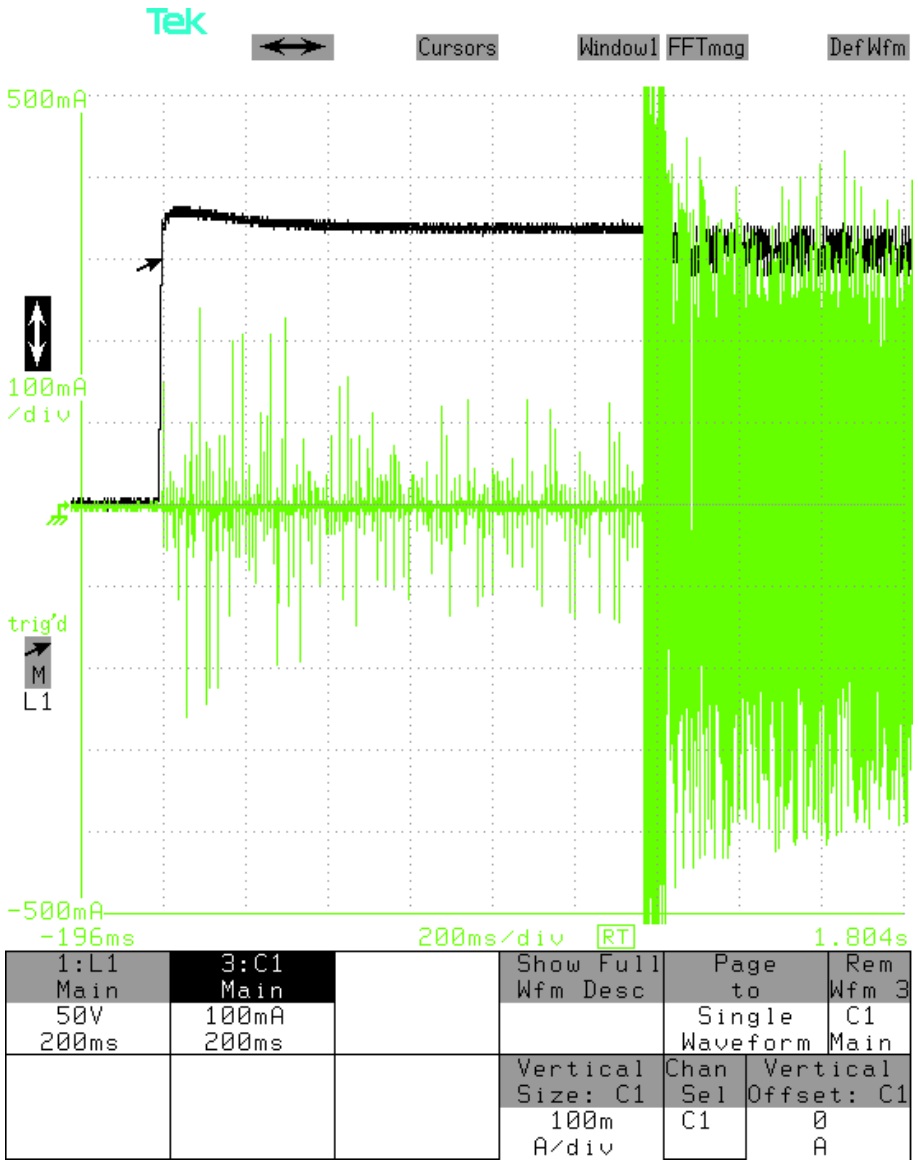


Figure 3.1-2 Cathode preheat waveforms.

Figure 3.1-2 shows the preheat interval. The black trace is the DC bus voltage, and the green trace is the lamp current. As can be seen, the lamp starts about 1.1 seconds after the bus voltage comes up, very close to the nominal preheat interval of 1 second. The preheat current is somewhat lower than optimum, but adequate for reliable lamp starting. The preheat current had been optimized, but changes to the ballast design required to reduce temperatures resulted in a lower preheat current. This is a simple adjustment due to the degree of freedom provided by using heater current derived from resonant inductor windings.

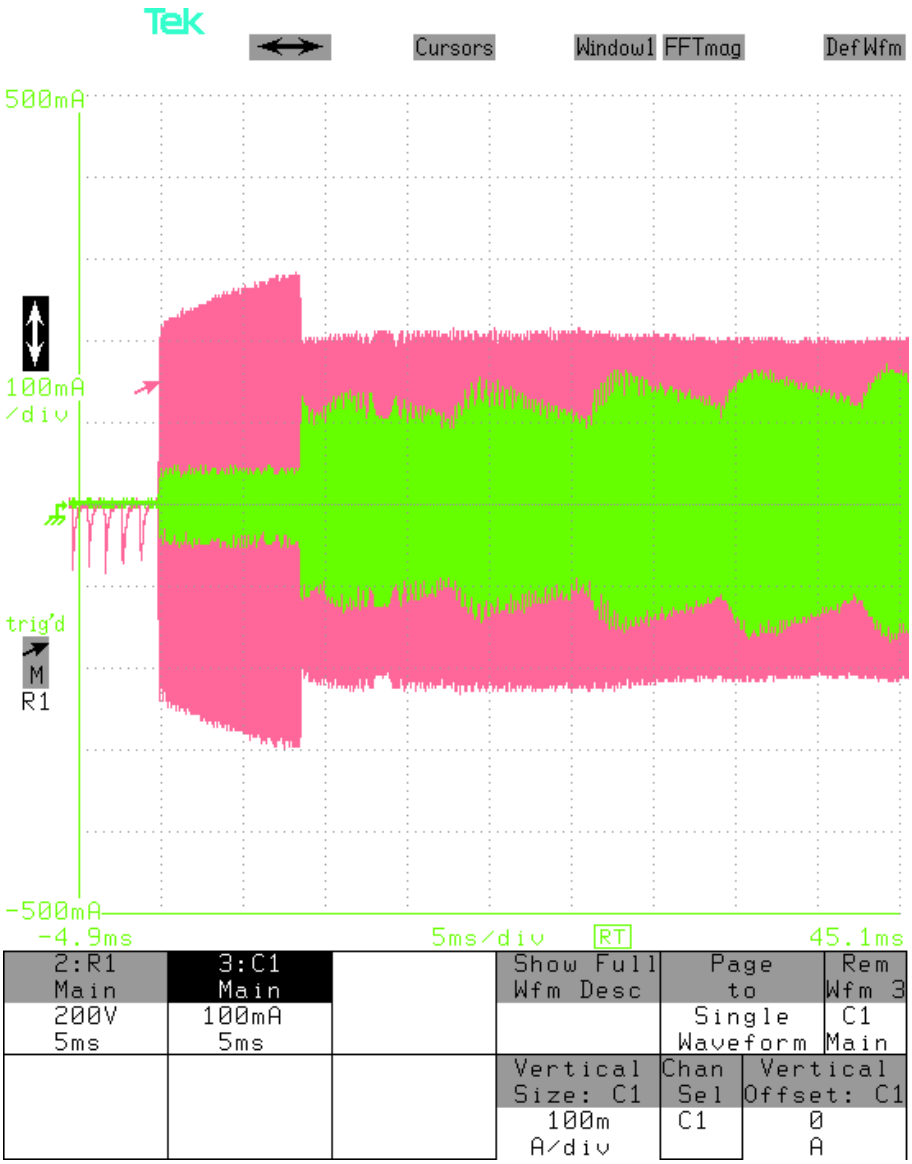


Figure 3.1-3 Lamp starting waveforms.

Figure 3.1-3 shows the lamp current (green) and voltage (pink) at lamp startup. These are very clean startup waveforms. The initial small current occurs while the lamp glows, transitioning to a clean start as time progresses.

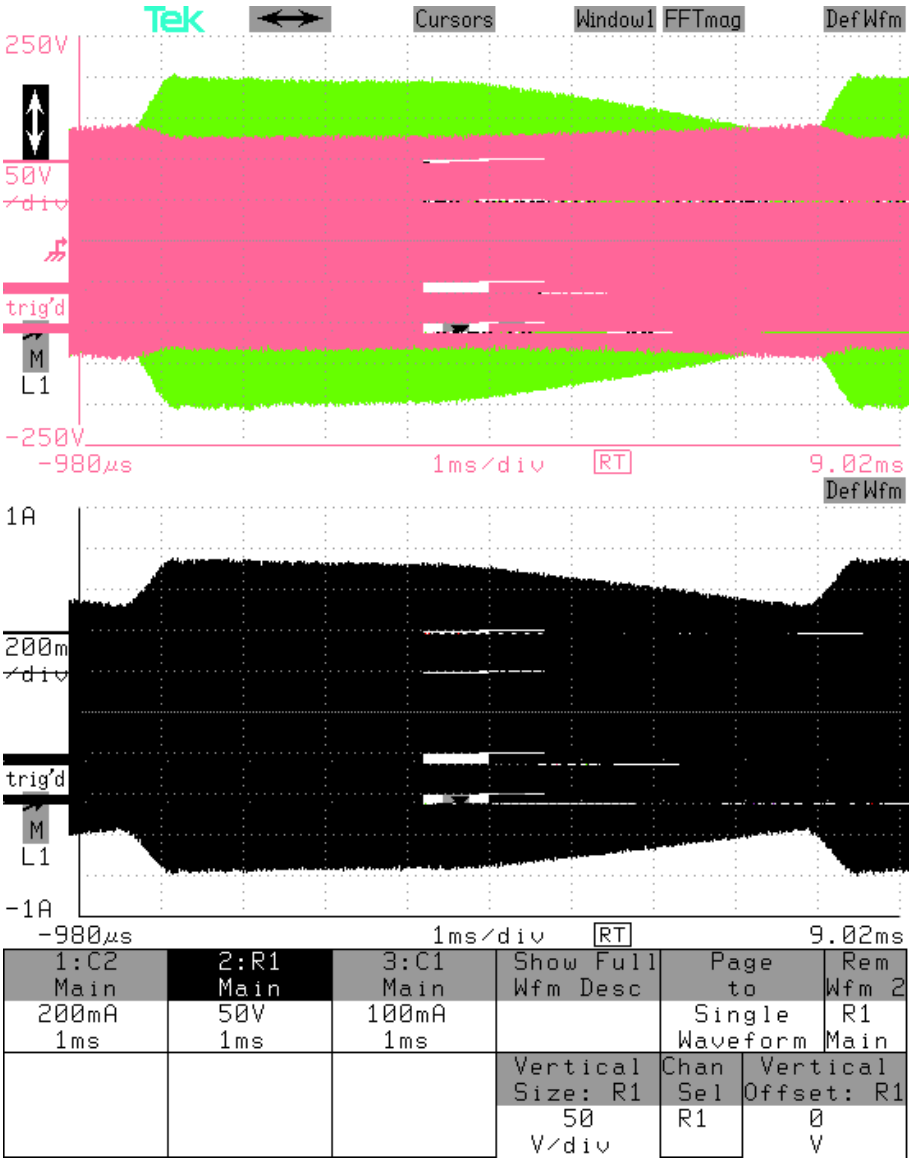


Figure 3.1-4 Full power waveforms.

Figure 3.1-4 shows the lamp current (green) and voltage (pink) with the lamp running at full power. Some 120Hz ripple is evident in the waveforms. This could be eliminated by increasing the rectifier filter capacitor, but the main effect would merely be prettier waveforms. The slight improvement in crest factor would have negligible impact on lamp life.

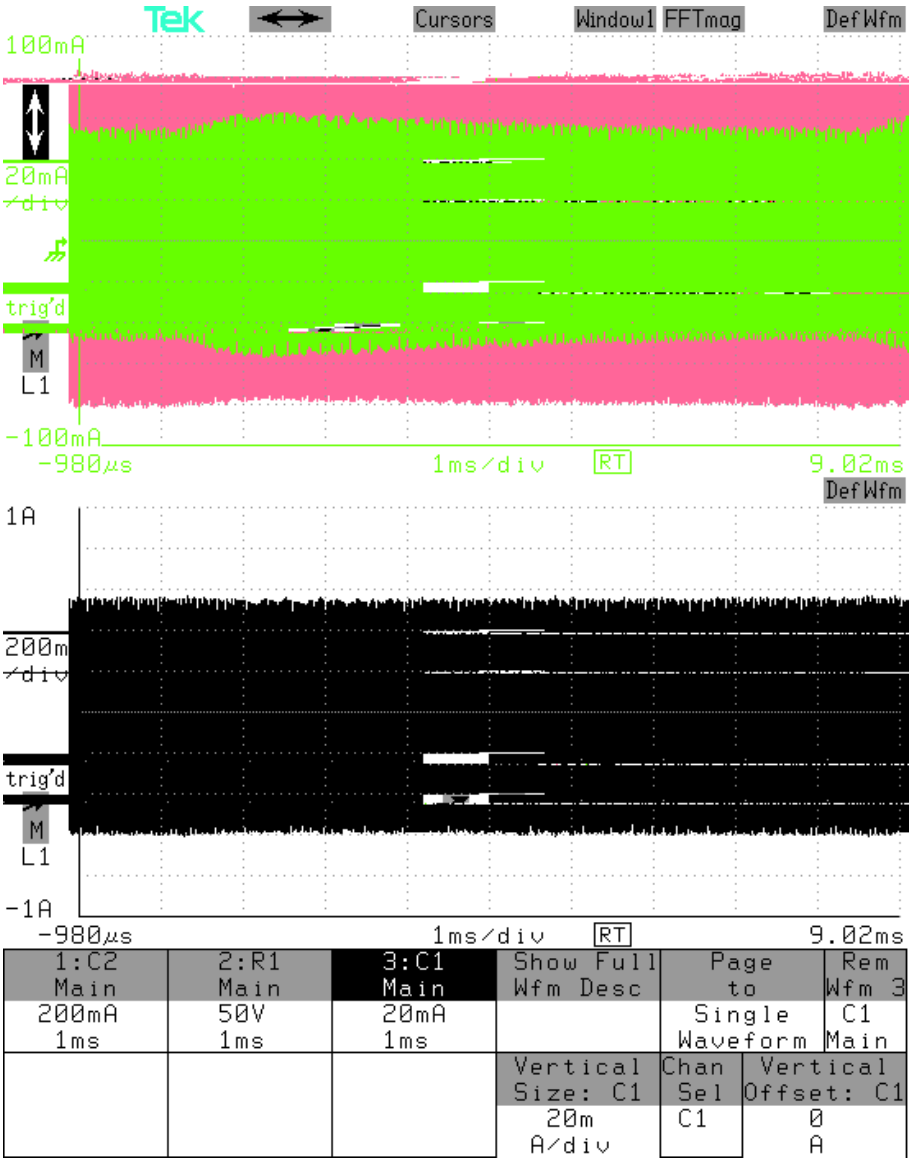


Figure 3.1-5 Medium power waveforms.

Figure 3.1-5 shows the lamp current (green) and voltage (pink) at medium power (50%). Note the reduced ripple due to the lower line current draw.

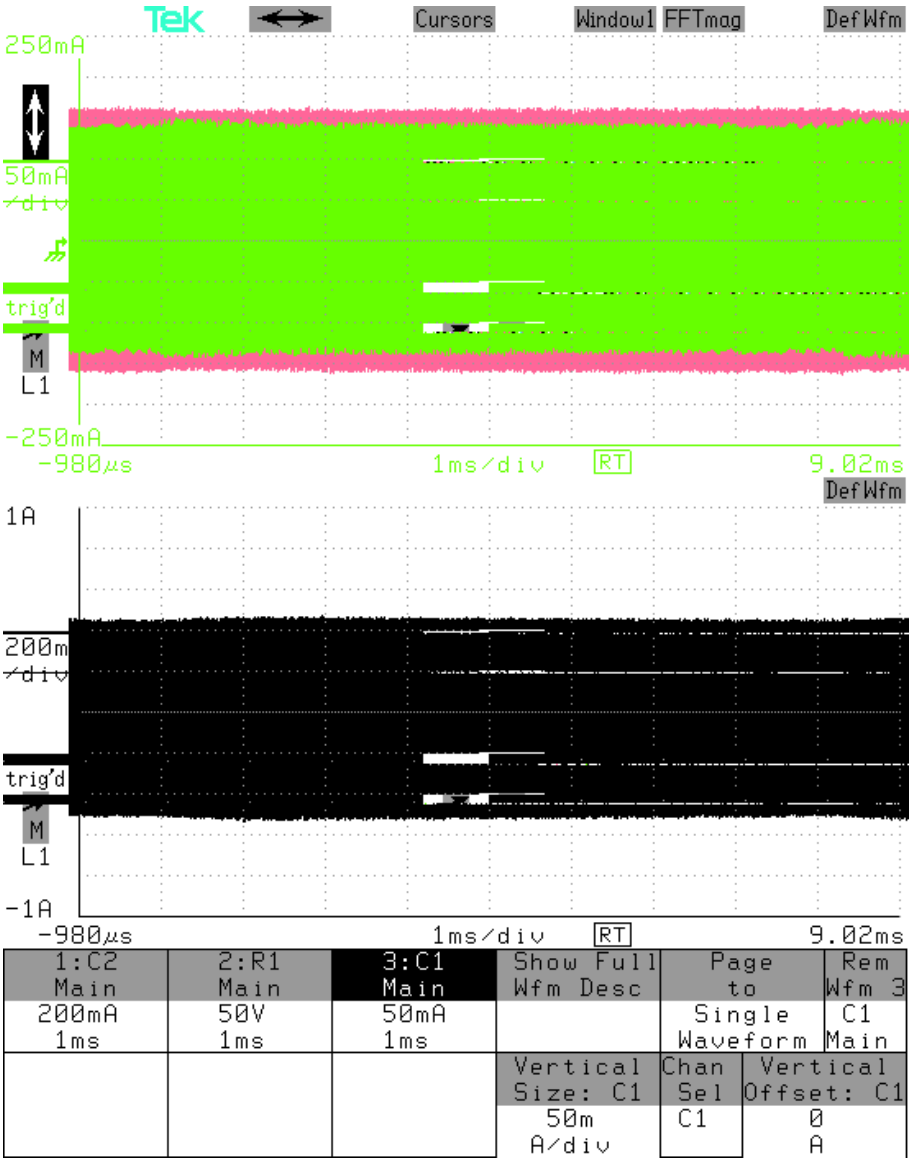


Figure 3.1-6 Low power waveforms.

Figure 3.1-6 shows the lamp current (green) and voltage (pink) at medium power (20%).

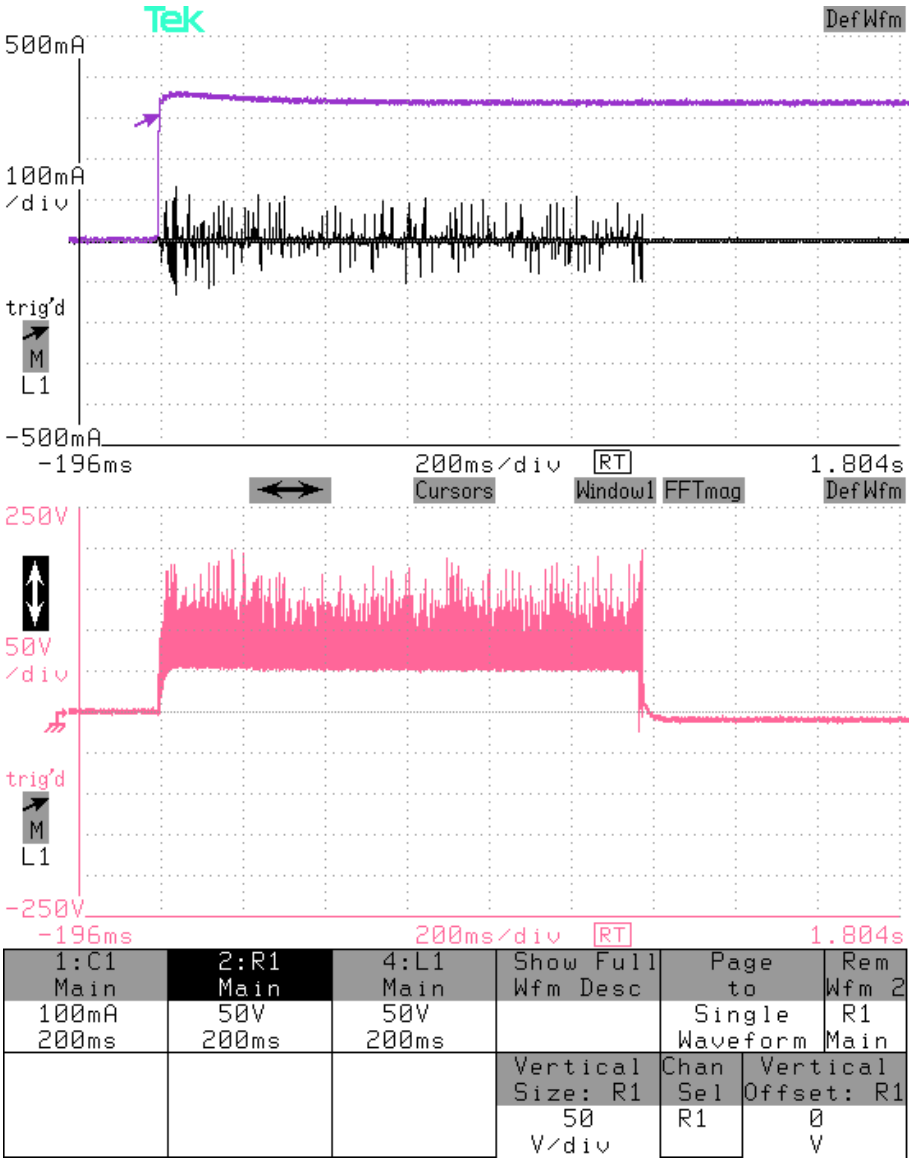


Figure 3.1-7 BIAS power on with no lamp in socket.

Figure 3.1-7 shows ballast startup with no lamp in the socket. The DC bus (purple trace) comes up, and the ballast attempts to preheat the lamp (black trace). After the preheat interval, the ballast shuts down. The pink trace shows the parallel capacitor voltage. This component is the one most prone to failure when the lamp is out of the circuit. It is well within ratings, and never sees starting voltage in this case.

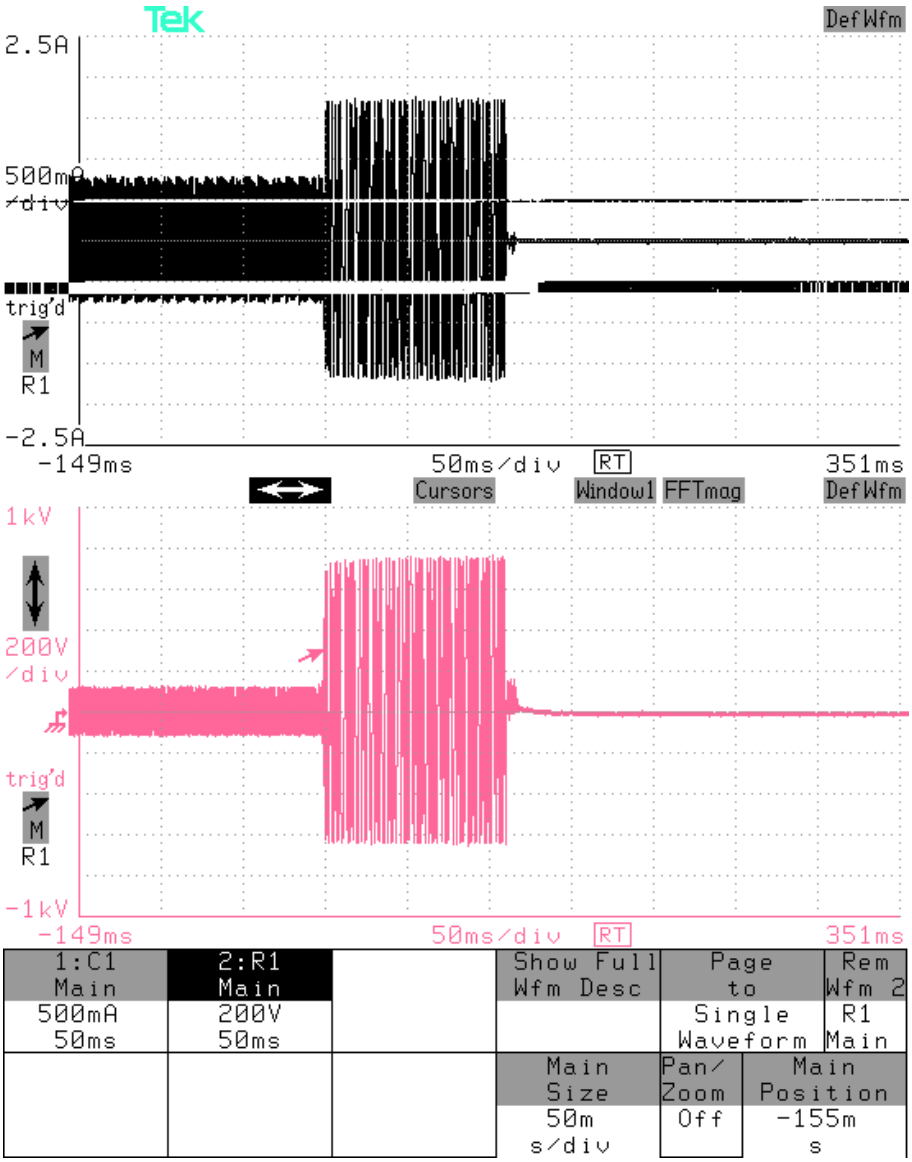


Figure 3.1-8 BIAS with lamp removed from circuit under full power.

Figure 3.1-8 shows lamp removal while the ballast is operating at full power. This is the most stressful condition for the ballast. The black trace shows the resonant inductor current and the pink trace shows the parallel capacitor voltage. The latter is the one most prone to failure when the lamp is out of the circuit. It is well within its DC rating (1kV, and operates at its AC rating for a brief interval before the ballast shuts down. Without the protection circuit, failure was seen every time as the capacitor voltage exceeded 900VAC, and the part failed before the ASIC could shut down the circuit. The protection circuit has been tested numerous times without ballast failure.

3.2 Thermal Performance

Dr. Erwin Liang and Leon LaGalles completed an evaluation of the thermal performance of the prototype ballasts in late October 2001. Their preliminary results below indicate the need for further investigation, as several of the component temperatures are approaching the point at which reliability would be compromised.

3.2.1 Thermal Measurement Setup

Infrared imaging and thermocouple (TC) are the two most common methods for investigating temperatures of electronics. Infrared measurements are not only accurate but also the fastest available and offer the least disturbance to the point being measured. They provide the entire picture of how the heat is distributed over the part and how it is changing in real time. However, most electronics are enclosed by metal or plastic shells, which prevents infrared camera from making thermal imaging with no viewing window. The component temperatures without the housings will be very different from those with. Therefore, thermocouple became the method of choice for measuring the temperatures of major ballast components.

When a TC is attached to a surface, heat flows from the measured components into the TC, and the heat flow depresses the local temperature. The time dependent depression is influenced by the pertinent parameters including: thermal conductivity of the surface and the thermocouple, orientation of the thermocouple relative to the surface, air flow velocity, thermocouple diameter and junction thickness, and any material used to reduce the thermal contact resistance between the thermocouple and the surface. Consequently, the measured temperature always appears lower than the "true" temperature. To minimize this installation error, J-type thermocouples of small diameter (~ 0.25 mm OD including sheath) were used and an epoxy of high thermal conductivity (1.4 W/m-K) was applied to mount thermocouples onto the component surfaces and as parallel to the surfaces as possible.

All the thermocouples from the electronic components were connected to A/D boards and then to a computer on which LABTECH data acquisition software was running in 0.1 Hz to convert voltages to digital temperature data and then record them as shown in Figure 3.2-1. The power to the light bulb was supplied and regulated by a 120VAC, 60Hz, AC power source (Pacific Smart Source). Three power levels: 100%, 50%, 25% corresponding to ballast input powers of 29.4W, 15.5W, and 10.5W, were selected to test the thermal performance. Power level was monitored by a wide band spectral power analyzer (Valhalla Scientific) and was digitally recorded in the data acquisition system. Light bulbs were

given at least an hour of initial warm-up before tests commenced. Measurements always started at full power, then shifted to the lower powers. There were at least 15 minutes for the bulb to reach its new equilibrium when changing power levels. Steady-state temperature at each specified power was obtained by averaging the temperatures over a period of 1 hour or more. Temperature variation over the same period was also computed for references. For the purpose of repeatability and reproducibility, two lamps were tested and each lamp had multiple runs.

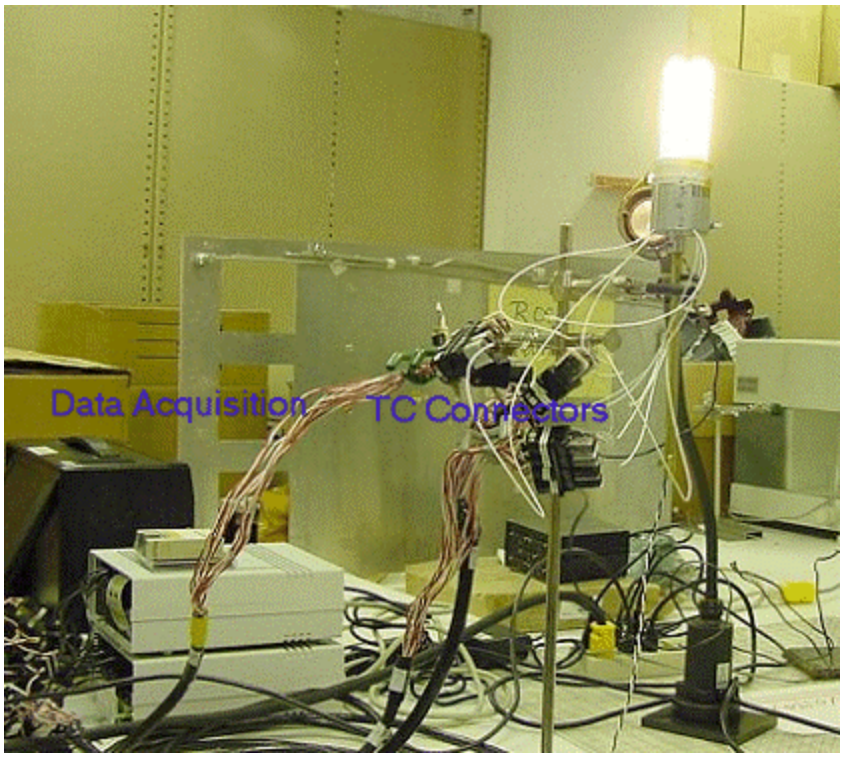


Figure 3.2-1 Thermal measurement setup.

3.2.2 Component Temperature Profiles

Thermal ratings of electronic components are critical to the CTQ parameters of lifetime and reliability of the product, and thus the system performance. Temperatures of 13 components in the prototype ballast including FET, diode, capacitor and transformer were examined in addition to the Aluminum housing and ambient temperature monitoring. For the purpose of identification, the locations where the thermocouples attached are illustrated in Figure 3.2-2 and Figure 3.2-3 with labels.

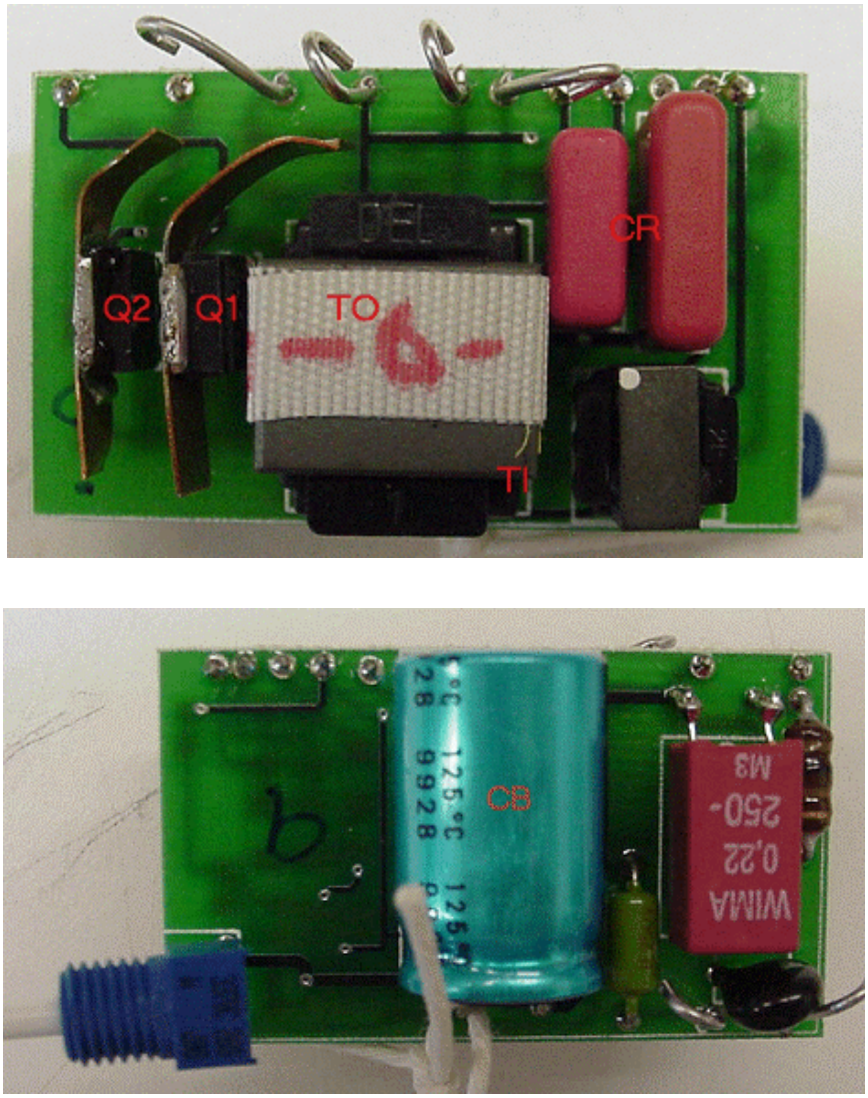


Figure 3.2-2 Components on the topside of the board.

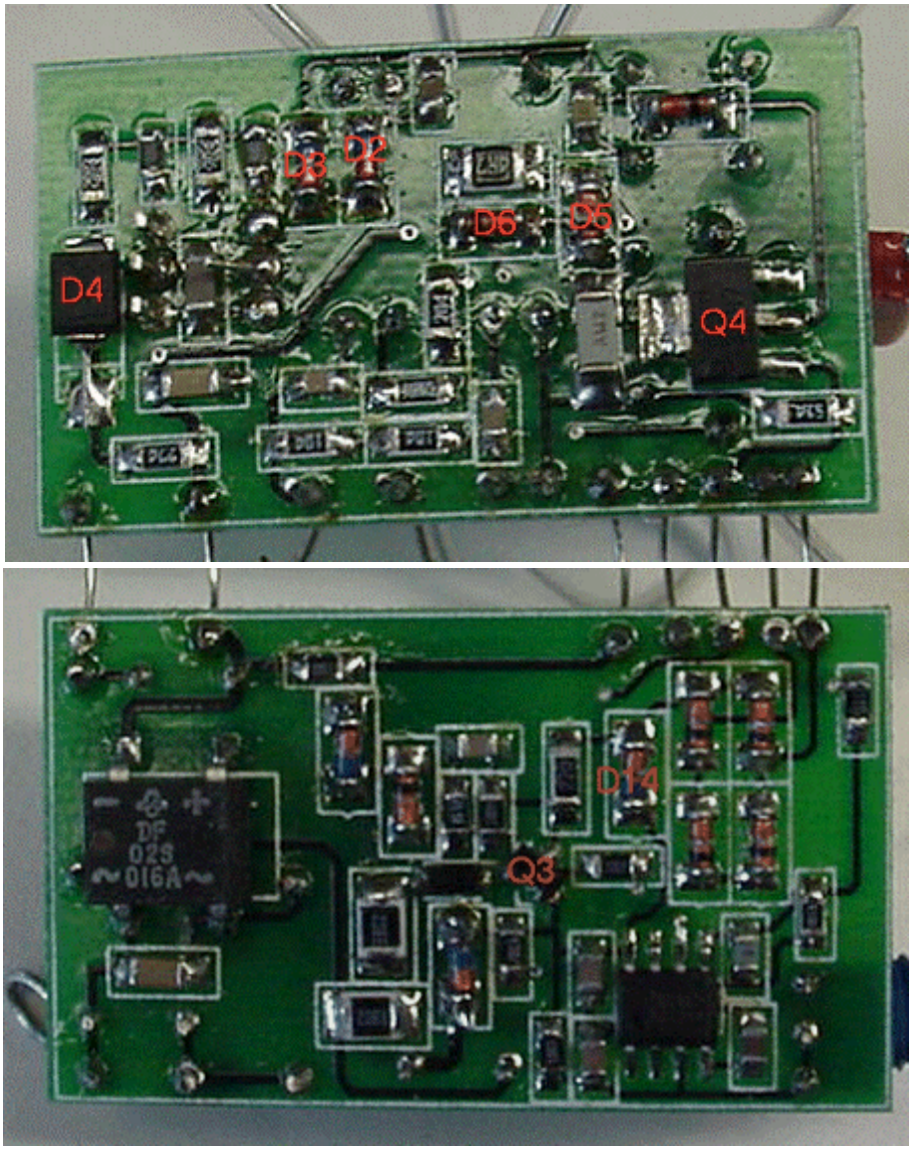


Figure 3.2-3 Components on the bottom side of the board.

The typical temperature traces of FET Q1, capacitor CB, diode D3, and transformer TI in one of the many thermal tests conducted are shown in Figure 3.2-4. Apparently, it took at least an hour for all the components to reach steady states at 100% power and the subsequent two steady-state temperatures were obtained at 50% and 25% power levels for long enough periods for averaging. It appeared that the fluctuation of signals taken by the data acquisition system increased with decreased power and it was the worst at 25% power level. The variations from the average could be as high as 20% of the average value at this low power level. These variations were contributed to the electrical noise resulting from the electromagnetic interference (EMI) of the components with the sensor circuits. Among the component

monitored, transformers had the worst noise level. To reduce this kind of noise, the TC wires have to be kept inside a metal shield that is grounded at one point only.

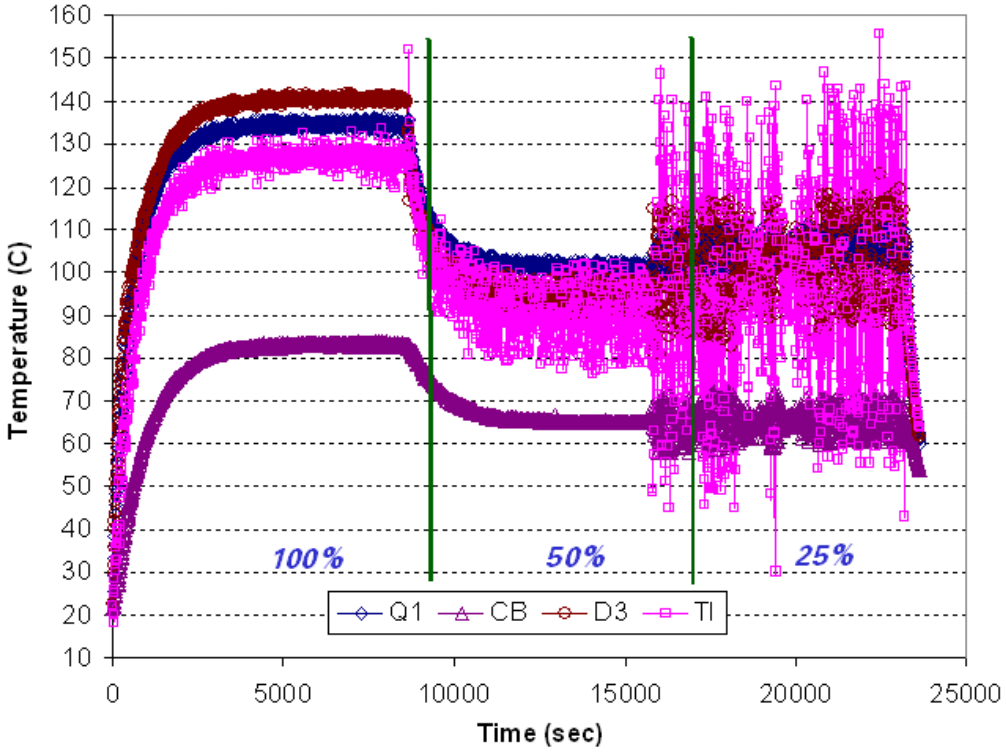


Figure 3.2-4 Typical temperature traces in a thermal test.

The averaged steady-state temperature of each component as a function of averaged ballast input power is plotted in Figure 3.2-5. Among all the components and power levels, the maximum temperatures occurred at diodes D2, D3, and D6 at full power and were about 140 °C. For most the components the average temperatures at 50% and 25% power levels were fairly close to each other and they were substantially lower than the temperature at full power. For some components, the averaged temperatures were actually higher at 25% power level than at 50%. Some of the components such as FETs tend to have higher thermal dissipation at the lower power level since the phase of the inductor current is larger at the low dimming point. Aluminum housing temperature is about 21 °C above the ambient temperature at lower powers and reaches 48 °C (or 29 °C above the ambient temperature) at full power.

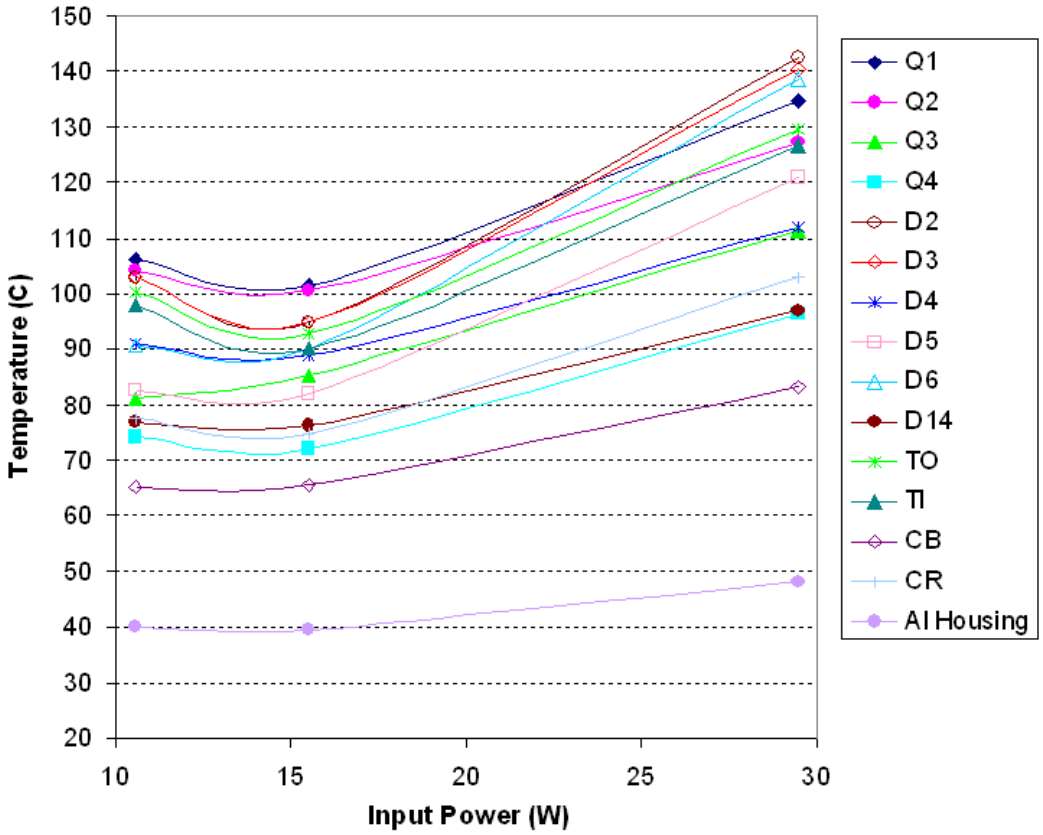


Figure 3.2-5 Averaged component temperatures in terms of ballast input power.

Figure 3.2-6 lists the average and standard deviation for the steady-state temperatures of each component at each power level obtained from a particular test on one of the two lamps. The ambient temperature was the temperature measured from a TC in the air less than 1" from the aluminum housing. The far-field room temperature was 18.6 °C on the average. The ballast input power was clearly under very tight control. The standard deviations of the transformer temperatures (TO and TI) were the largest among all at 25% power level, but these are much more electrical than thermal. Thermal measurement variations were at realistic levels for all the other components. Diode D3 appeared to have exceptionally higher thermal variation than other diodes (D2, D4, D5 and D6).

The average and standard deviation of the steady-state temperatures for every component at each power level acquired from four tests (two lamps and two runs for each lamp) are summarized in . The differences between the corresponding results in Figure 3.2-6 and mainly resulted from part to part variation, different numbers of thermocouple, and ambient temperature variation, but they were within 5%. The consistent thermal results indicate that the measurements were very repeatable between lamps and from run to run.

POWER [W]	Q1	Q2	CB	CR	TO	TI	Al Housing	Ambient
29.46	134.63	127.35	83.22	102.91	129.69	126.76	48.02	19.24
0.01	0.53	0.26	0.18	0.48	1.65	1.68	0.25	0.56
15.50	101.56	100.64	65.52	74.78	92.89	90.02	39.37	18.72
0.05	0.83	0.48	0.44	2.00	5.93	5.83	0.28	0.32
10.55	106.33	104.24	65.14	77.63	100.22	97.95	39.99	18.59
0.01	2.15	0.54	2.89	5.52	21.61	21.08	0.21	0.27

(a)

POWER [W]	Q3	Q4	D2	D3	D4	D5	D6	D14
29.46	111.43	96.31	142.62	140.42	111.86	120.99	138.51	96.94
0.01	0.20	0.28	0.12	0.47	0.20	0.18	0.21	0.25
15.50	85.19	72.12	94.80	94.75	88.88	81.90	90.17	76.27
0.05	0.86	0.59	0.55	2.02	1.08	0.81	0.60	1.26
10.55	81.06	74.07	102.84	102.92	90.84	82.67	90.82	76.90
0.01	2.59	1.64	0.57	7.17	1.98	0.63	0.96	1.96

(b)

Figure 3.2-6 Averages and standard deviations of the steady-state temperatures at three ballast input powers for the components at the (a) topside and (b) bottom side of the boards obtained from one test.

POWER [W]	Q1	Q2	CB	CR	TO	TI	D2	D4	D6	Al Housing	Ambient
29.55	139.09	127.52	79.85	100.21	131.85	131.23	138.37	113.11	136.57	47.05	19.99
0.02	0.89	0.49	0.22	0.58	2.26	2.33	0.31	0.23	0.36	0.77	0.71
15.43	102.56	99.70	62.27	72.42	92.60	92.43	91.25	87.94	87.55	38.62	19.83
0.10	0.44	0.29	0.50	1.48	4.24	4.88	0.36	0.69	0.39	0.56	0.53
10.54	108.80	104.15	62.43	75.44	103.51	103.04	98.79	90.44	88.81	39.57	20.08
0.02	4.12	1.42	3.22	4.56	17.87	18.51	2.10	1.46	2.41	3.09	0.56

Figure 3.2-7 Averages and standard deviations of the steady-state component temperatures at 3 input powers measured from four tests.

It is clear from the thermal testing that miniaturization to meet size requirements has forced temperatures of several key components to reach the point at which product reliability/life would be compromised. Preliminary testing of an optimized ballast indicates that temperatures of several key components can be reduced by as much as 10-15 degC with simply the substitution of new values. Reliability estimates reflect these measurements.

3.3 Reliability Predictions

This section of the report was prepared by Dr. Ljubisa Stevanovic. Reliability is the probability that an item will perform its intended function without failure for a specified period of time and under stated

conditions. In other words, reliability is "meeting customer performance expectations over time in real world conditions". It is a prime measure of quality - as viewed by the customer.

3.3.1 Causes of Electronic System Failures

Failures can generally be divided between intrinsic and extrinsic. Intrinsic failures are inherent to the components. Examples of intrinsic failures are:

- Electro-migration of electrical connections on a circuit board, or on a semiconductor chip,
- Contact wear in electrical relays
- Contamination effects, such as: corrosion, deposition of contaminants (e.g., oil, salt, dust,...)
- Solder joint fatigue

Extrinsic failures occur due to external factors, such as:

- Electrostatic discharge
- Electrical overstress (voltage, current, power, …)
- Mechanical shock and vibration
- Humidity or condensable water
- Mishandling

Wear out failures are typically caused by intrinsic failures, while most "random" failures of components are typically caused by extrinsic factors.

The failure rate over time in most systems, including electronic ballast, tends to follow a so-called bathtub curve. The failure rate is typically higher at the beginning and the end of the product life, as shown in Figure 3.3-1.

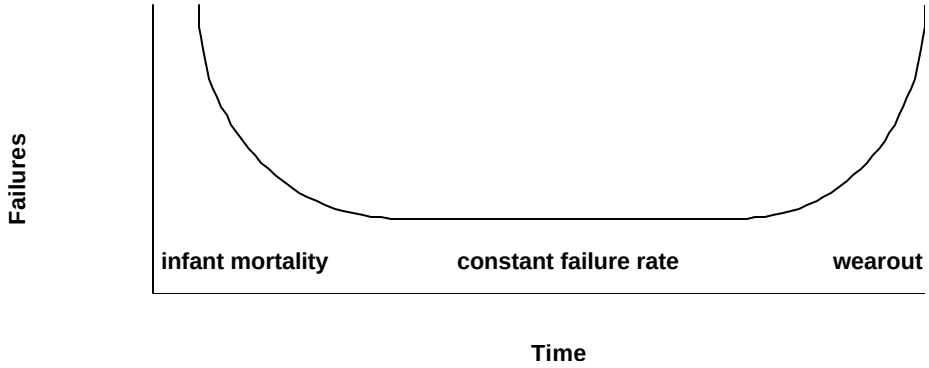


Figure 3.3-1 Reliability Bathtub Curve Infant mortality is typically caused by manufacturing defects and can be reduced by application of quality processes in manufacturing, supplier screening and component qualification. After the infant mortality period, the failure rate becomes lower and relatively constant. During the constant failure rate period, failures tend to be extrinsic and can be reduced by understanding external factors and by addressing them in the design phase. Wear out failures are typically intrinsic and can be predicted through accelerated testing and Weibull analysis. Electrical devices susceptible to wear out are: relays, electrolytic capacitors, fans, connectors, solder joints. Semiconductor devices are less susceptible to wear out.

3.3.2 Reliability Modeling

There are two widely used standard models for predicting failures under constant failure rate conditions:

- Bellcore TR-332, Issue 5, Dec '95, Method I(parts count), Case 3 (general case): *Reliability Prediction Procedure for Electronic Equipment*
- MIL-HDBK-217F, Notice 2: *Reliability Prediction of Electronic Equipment*

A comparison of the Bellcore and the MIL-HDBK-217F models follows:

- Both use generic failure rates, corrected for temperature, stress and environment
- MIL-HDBK-217F has additional corrections (learning factors, package style)
- Different failure rates for non hermetic parts (no penalty vs. ~10X multiplier)
- Different methods for handling temperature (ambient vs. junction)
- Only MIL-HDBK-217F includes solder joint fatigue
- Only Bellcore has first year multiplier for infant mortality (depends on burn-in)
- Only Bellcore includes systematic way to include vendor data

Models are useful for estimating the Mean Time Between Failures (MTBF), or the reliability as a function of time, if no test data are available. The accuracy of either model is typically within a factor of 2 to 3. Occasionally, the accuracy can be off by as much as factor of 10 if defective parts, bad manufacturing processes, or poor workmanship are present.

While test data is better than a predictive analysis, reliability modeling can help identify reliability issues during design phase and prior to testing

3.3.2.1 Bellcore Reliability Model

Bellcore reliability model is based on an assumption that failure rate of an assembly can be calculated by adding component failure rates. If $?i$ represents the failure rate of a part i, then the failure rate of an assembly is sum of failure rates of all parts multiplied by a scaling factor that accounts for application environment:

$$? = environment\ factor * ? ??i$$

Reliability of each component is affected by following factors: temperature, electrical stress, quality and extrinsic factors. Failure rate for a component is calculated as follows:

$?i = ?gi * ?Qi * ?Si * ?Ti$ (failure rate for a component), where:

- $?gi$ represents generic failure rate (for integrated circuits it scales by transistor/gate count)
- $?Si$ is electrical stress factor
- $?Ti$ is temperature factor (for ambient temperature at 1/2" above the component)
- $?Qi$ is quality factor
- Single environment factor $?E$ applied at assembly level

$? = ?E ? ?i$ (failure rate for an assembly)

Acceleration Factors: Electrical Stress

Higher stresses lead to higher failure rates. This correlation is governed by the following equation:

$?S = e^{m*\{p1-p0\}}$ (Stress acceleration factor), where:

- m represents fitting parameter
- $p0$ is reference stress = 50%
- $p1$ is applied stress.

Figure 3.3-2 shows examples of failure acceleration due to electrical stress for several electronic component types.

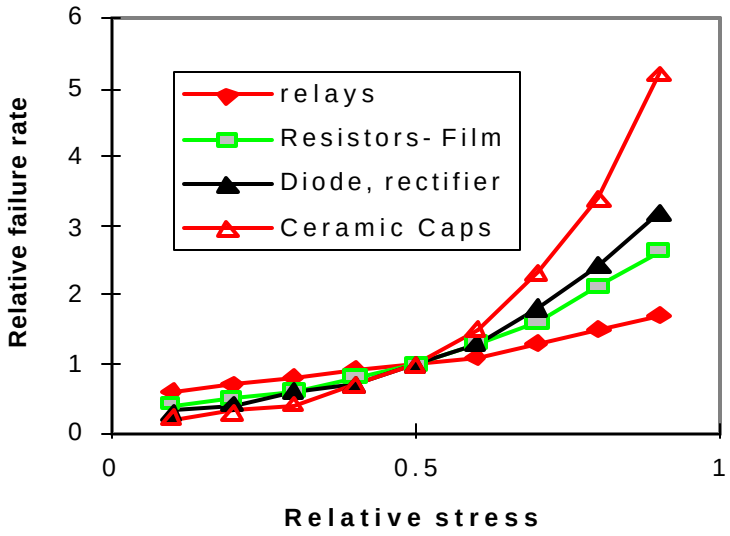


Figure 3.3-2 Example of Electrical Stress Acceleration

Depending on the component type, electrical stress factors for components are calculated as follows:

- Capacitors: Sum of applied dc voltage and ac peak voltage / rated voltage
- Diode, rectifier: Average forward current / rated forward current
- Diode, zener: Actual zener current or power / rated zener current or power
- Relays: Contact current / rated current
- Resistors: Applied power / rated power
- Transistors: Dissipated power / rated power

In all cases, lower stress (de-ratings) will enhance component life. Therefore, the application of stress de-ratings may be the single best way to ensure a long-lived design.

Acceleration Factors: Temperature

Higher temperatures lead to higher failure rates. This is governed by Arrhenius equation:

$$?T = e^{Ea/k * \{1/To - 1/T1\}}$$ (Temperature acceleration factor), where:

- *Ea* is activation energy
- *To* is reference temperature = *40 +273 = 313 degK*
- *T1* is ambient temperature, in degrees *K*, 1/2" above the component.

Figure 3.3-3 shows examples of failure acceleration due to elevated temperature for several electronic component types.

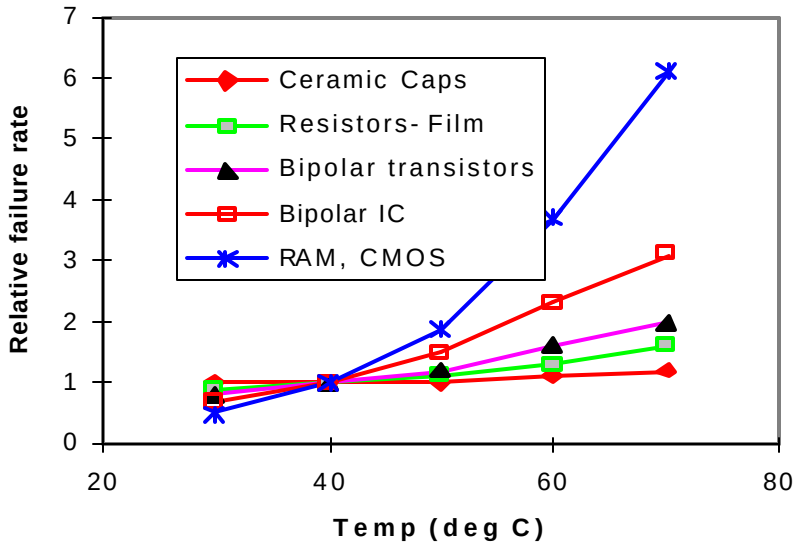


Figure 3.3-3 Examples of Temperature Acceleration

3.3.3 Reliability Modeling of BIAS Ballast

Reliability modeling of BIAS ballast was performed based on the Bellcore model. Electrical stresses of all components were calculated over the range of nominal input voltage and output power conditions. Highest stress values were used for reliability calculation. Component temperatures were based on thermal measurements at three lamp power settings. Again, the highest temperature value was used for calculations. Ambient air temperature inside the ballast housing was estimated at 55 degC based on housing temperature. This temperature was used as a baseline for all components that have negligible power dissipation and that are not in close proximity to the power components that are hot. Figure 3.3-4 is the Bellcore spreadsheet for the ballast circuit, showing electrical stresses and temperatures for all components. Total ballast FIT rate is calculated by adding FIT's of all components and the MTBF is calculated assuming controlled (residential) environment.

Notation:

FIT Rate = Failures per 10^9 hours

MTBF = $1x10^9$ / (FIT) , units are hours

Part #	Description	Manuf Part #	Qty	Electrical Stress # 1 (% rated)	Electrical Stress # 2 (% rated)	Temp (deg C)	FIT
U1	BIAS 8 pin IC	Custom ASIC	1	NA	NA	55	118.8
Q1	250V Power N-FET	FQU6P25	1	3	NA	139	137.1
Q2	-250V Power P-FET	IRFU9214	1	2	NA	128	114.6
Q3	-50V Dimm P-FET	BSS84	1	50	NA	111	541.9
Q4	Shutdown FET	MMFT107T1	1	0	NA	55	26.2
D1	200V, 1A Bridge Rectif	General Semi. DF02S	4	46	92	86	120.0
D2,3	10V, 0.5W Gate Zeners	ZMM5240B	2	20	NA	138	33.0
D4	1A, 200V Ultrafast P-FET diode	MURS120T3	1	50	86	113	52.2
D5	50V, 0.2A ilamp sense	RLS4150TE-11	1	75	50	121	87.7
D6	50V, 0.2A ilamp sense	RLS4150TE-11	1	75	50	137	112.9
D7	39V, 0.5W IC Supply Zener	MMSZ5259BT1	1	16	NA	82	7.6
D8	50V, 0.2A shutdown ckt	RLS4150TE-11	1	0	0	55	2.9
D9	5.1V, 0.5W Vdd Zener	ZMM5231B	1	1	NA	55	3.6
D10-13	50V, 0.2A dimm bridge	RLS4150TE-11	4	50	50	55	52.3
D14	24V, 0.5W Zener	ZMM5252B	1	50	NA	55	11.6
D15	50V, 0.2A OVSD diode	RLS4150TE-11	1	0	90	55	5.0
D16	10V, 0.5W Zener	ZMM5240B	1	0	NA	55	3.5
V1	Varistor	Panasonic - ECG ERZ-V05D242	1	0	NA	55	9.1
R1-R22	SMD film resistors	SM/R/****	22	10	NA	55	25.3
R12	20k Pot	Bourns3370	1	0	NA	55	50.5
C1,17	22nF, 200V X7R	1206SMD	2	86	NA	55	28.6
C2	47uF, 200V E'lytic	Rubycon RX-20	1	86	NA	80	1565.8
C3	.22uF, 250V Polyester	WIMA MKT	1	86	NA	55	32.4
C4	15nF, 50V X7R	Kemet, 0805SMD	1	10	NA	55	0.6
C5	1.5nF, 100V NPO	Mallory C1206SMD	1	11	NA	55	0.7
C6	.47nF, 200V NPO	Panasonic 1206SMD	1	86	NA	55	14.3
C7	3.3nF, 630V, 5% Polypropylene	WIMA MKP-10	1	79	NA	65	25.6
C8	3.3nF, 630V, 5% Polypropylene	WIMA MKP-10	1	48	NA	65	3.9
C9	0.68nF, 1kV NPO SMD	AVX1808AA681JAINA	1	30	NA	55	1.4
C10-16	X7R	0805SMD	7	20	NA	55	6.7
T1	Resonant T	4 windings: T1A,B,C,D	1	NA	NA	132	201.5
T2	Gate dimming	2 windings: T2A,B	1	NA	NA	55	15.5
L1	Input Inductor	Siemens B78108-S1104-J	1	NA	NA	55	27.1
						Base FIT Rate	3439.8
	Tballast ambient@p100%=	55			MTBF in Residential Environment:		290714.7

Figure 3.3-4 Ballast reliability results The ballast FIT rate is 3440 and the MTBF is approximately 290 thousand hours. Ballast reliability can now be calculated using following equation:

$$R = e^{-?t}$$

?? where $?=1/MTBF$, with units hr^{-1},

?? and t represents number of hours of operation.

Figure 3.3-5 shows predicted probability that the ballast will not fail during a certain number of run-time hours. According to Figure 3.3-5, probability that the ballast will last 30,000 hours is 90%, while the probability that it will last 50,000 hours is 84%.

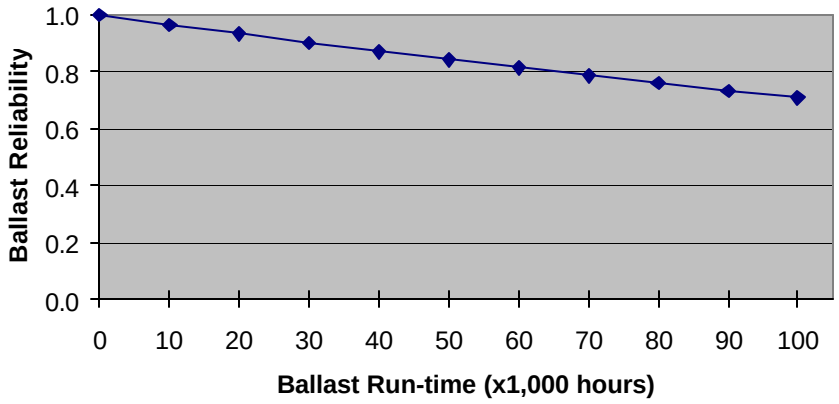


Figure 3.3-5 Predicted Ballast Reliability

Calculated ballast reliability represents initial estimate and it would have to be validated and refined through reliability testing, such as: high temperature life test, thermal cycling, power cycling, electrical tests at extreme temperatures, etc. Ballast reliability can be improved by additional circuit optimization and better thermal management.

3.4 System Performance

The Lighting Research Center (LRC) was subcontracted by GE to independently evaluate of the performance of their ballast developed, against the target specification developed at the beginning of the BIAS project. The LRC measured the electrical characteristics, light output, dimming range, color, effect of voltage fluctuations, and warm-up time for the two BIAS lamps provided by GE. In all cases, the LRC followed the testing protocol recommended by the *IESNA Approved Method for the Electrical and Photometric Measurements of Single Ended Compact Fluorescent Lamps* (LM-66-00). The results show that the lamps generally conformed to the desired specification for all parameters with the exception of warm-up time. This discrepancy can be attributed to the lamps rather than the ballasts.

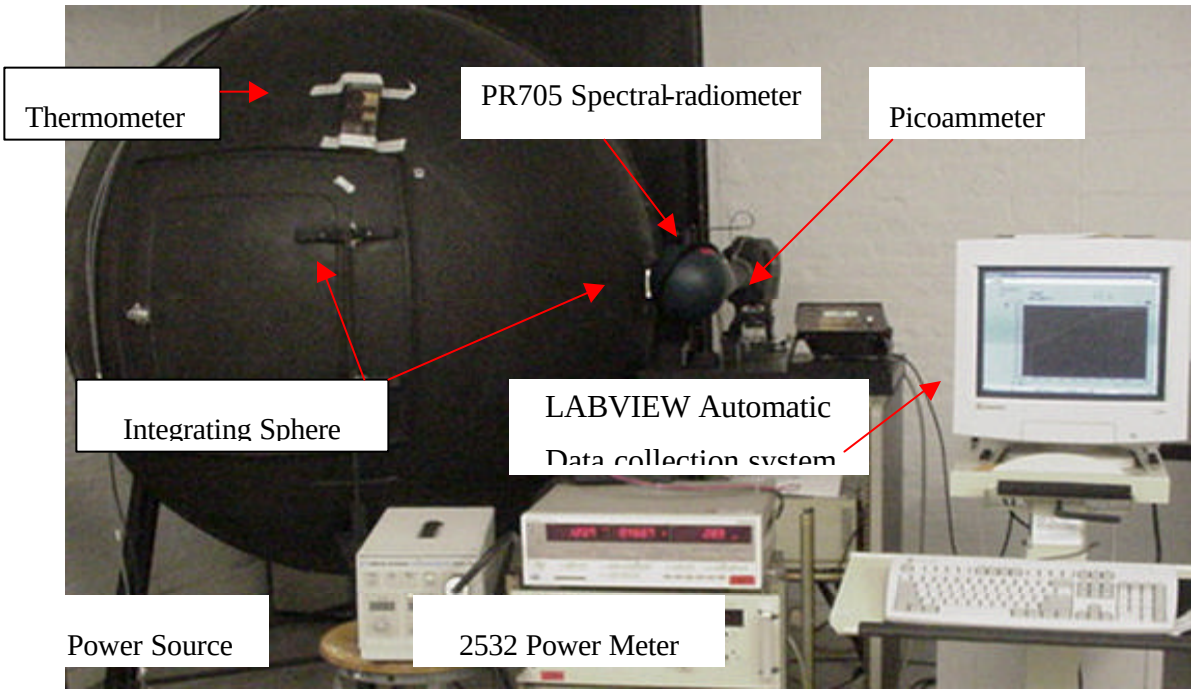
3.4.1 Background

General Electric Corporate Research and Development (GE CR&D) is developing a miniature ballast for plug-in CFLs that can be mounted in a package that is approximately the same size as the standard metal

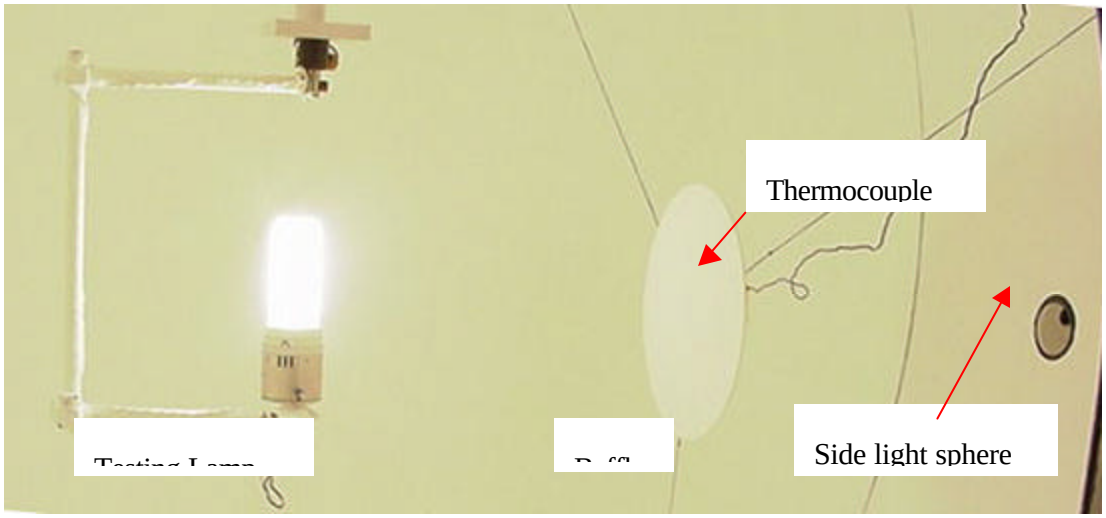
shell lamp holder currently used in portable fixtures designed for incandescent lamps. This project is funded by the United States Department of Energy (US DOE) and GE. The Lighting Research Center (LRC) was subcontracted by GE to support their ballast development program. One of the final tasks of this project is an independent evaluation of the ballast performance by LRC, against the target specification developed at the beginning of the project. This section documents the test procedure used for evaluating the two prototype ballasts supplied by GE and the results.

3.4.2 Test Procedure

The target specification for the system is shown in Appendix A. The LRC tested two systems, lamp and ballast, supplied by GE for electrical and light output characteristics. These include light output, dimming range, color, effect of voltage fluctuations, and warm-up time. GE supplied the two lamp systems after burning them for 100 hours. The two samples, labeled system A and system B, were tested using the experimental setup shown in Figure 3.4-1.



(exterior of sphere)



(interior of sphere)

Figure 3.4-1 Experimental Setup

The entire measurement system was carefully calibrated before measurement. For all the testing, the *IESNA Approved Method for the Electrical and Photometric Measurements of Single Ended Compact Fluorescent Lamps* (LM-66-00) was consulted for the measurement protocol. Lamp light output stabilization status was monitored by the LABVIEW? automatic data collection system through the Keithley 485 Autoranging Picoammeter. The ambient temperature was monitored, but it was not controlled. Ambient temperature ranged from 22 °C to 27 °C. Three measurements were made for each lamp over an eight-day period. Figure 3.4-8 summarizes the results for system A. Figure 3.4-9 summarizes the results for system B.

3.4.3 Test Results

3.4.3.1 Electrical Characteristics

Figure 3.4-8 and Figure 3.4-9 in Section 3.4.4 show that both systems' electrical characteristics meet the GE-CRD-provided system specification (Appendix A): 120V input volts, input current of 0.485A, input wattage of 30 +/-2W, and power factor of 0.5. Testing of the systems' electrical characteristics followed standard IESNA protocols.

3.4.3.2 Light Output

As Figure 3.4-8 in Section 3.4.4 shows, at 120V input volts lamp A has a light output of 1701 lumens. As Figure 3.4-9 shows, lamp B has a light output of 1690 lumens for the same input voltage. The measurement uncertainty of the lumen output measurement system used at the LRC laboratory is

estimated at 5%. Therefore, both lamps meet the light output specification requirement of 1710 lumens. Testing of the lamps' light output followed standard IESNA protocols.

3.4.3.3 Dimming Range

As Figure 3.4-8 in Section 3.4.4 shows, lamp A can be dimmed to 22.2% of full lumen output. Lamp B, as described in Figure 3.4-9, can be dimmed to 19.7% of full lumen output. Beyond this dimming range, the lamps will extinguish or flicker. Testing of the lamps' dimming ranges followed standard IESNA protocols.

Figure 3.4-2 indicates that dimming within certain ranges may actually increase the lamp's efficacy. For example, at 80% of full lumen output, the lamp's luminous efficacy is 2.2% higher than it is at full light output. Dimming more than 50% dramatically decreases lamp efficacy, however.

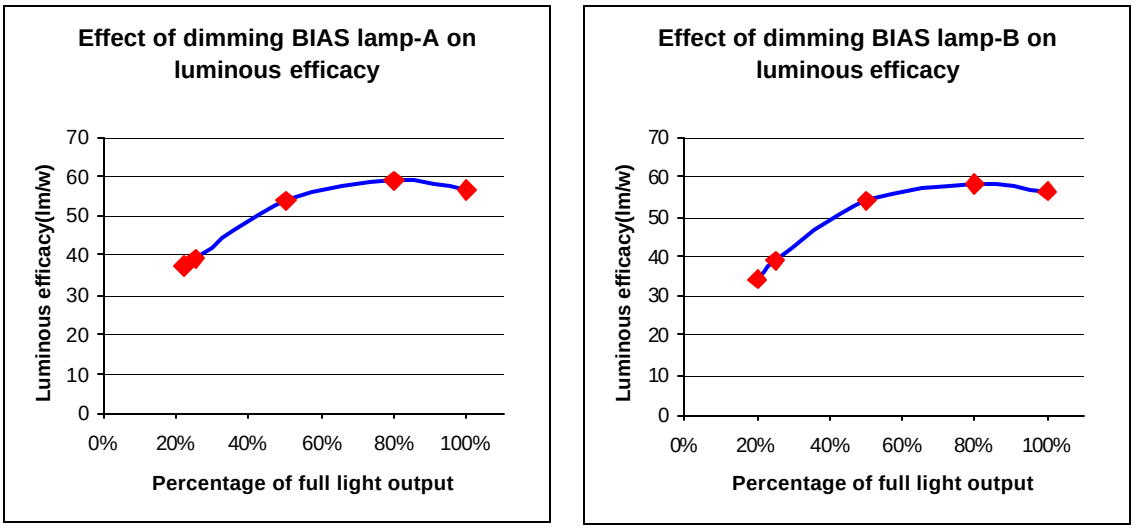


Figure 3.4-2 Effect of Dimming on BIAS Lamp Luminous Efficacy

Dimming to below 25% of full light output will cause visible lamp flicker. Figure 3.4-3 shows the lumens stabilization curve of lamp B when dimmed to 18% of full light output.

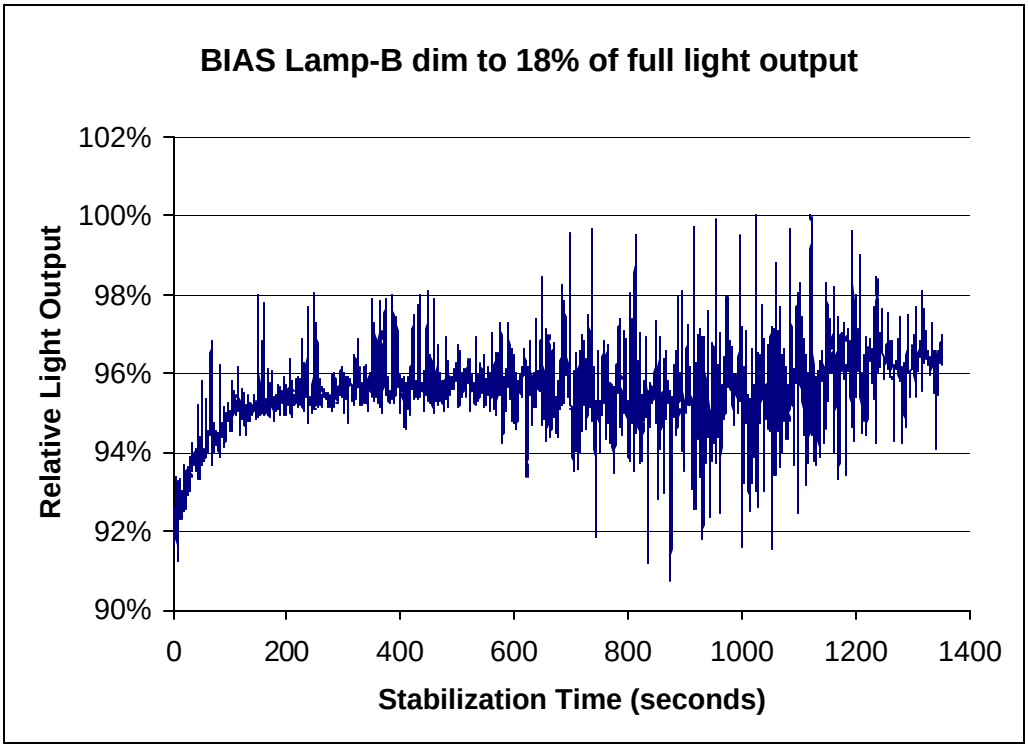
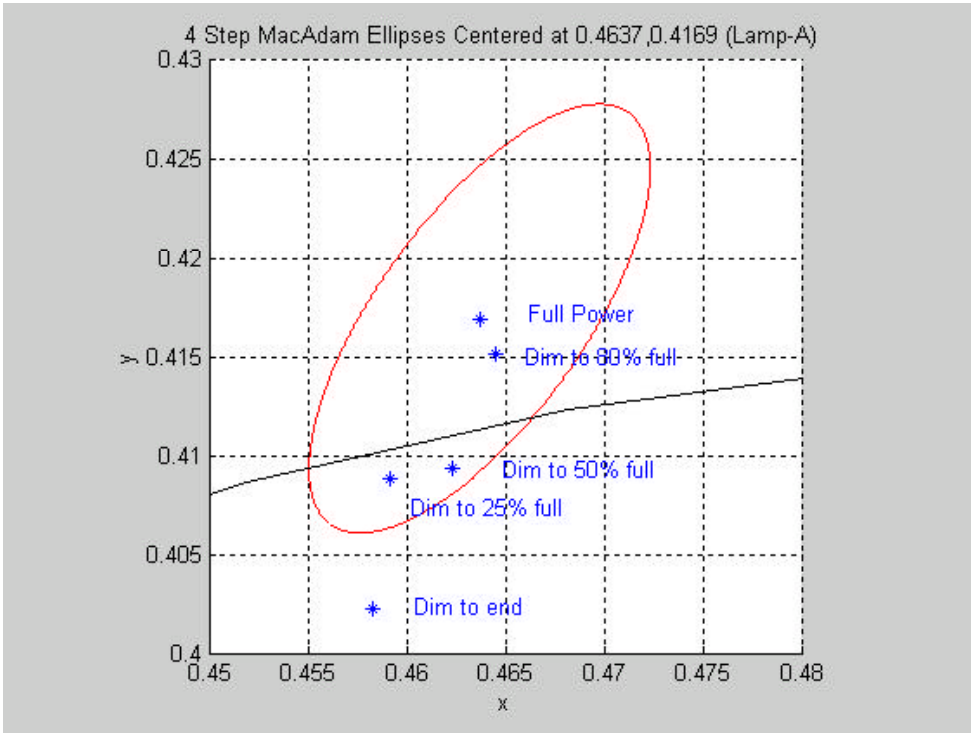


Figure 3.4-3 Dimming to End Causes Visible Flicker

3.4.3.4 Color

As can be seen in Figure 3.4-8 and Figure 3.4-9 in Section 3.4.4, at 120V input volts lamp A has a CRI of 82.8 and a CCT of 2705K while lamp B has a CRI of 82.1 and a CCT of 2758K. The specification requires a CRI of 82 and CCT of 2800K at full power, so both lamps meet the CRI specification. Although both lamp systems did not meet the CCT specifications exactly at 2800K, they are within 100K of the target value, which is acceptable. Dimming lowers CCT and raises CRI, but even with these effects, the lamps are still within the specification. Dimming from full power to the minimum dim level reduces the CCT by only 40K and increases the CRI by only one.

Figure 3.4-4 shows the effect of dimming on lamp chromaticity coordinates. Lamp chromaticity coordinates are well within the 4-step MacAdam Ellipse when dimming from full power to 25% light output. Testing of the lamps' color characteristics followed standard IESNA protocols.



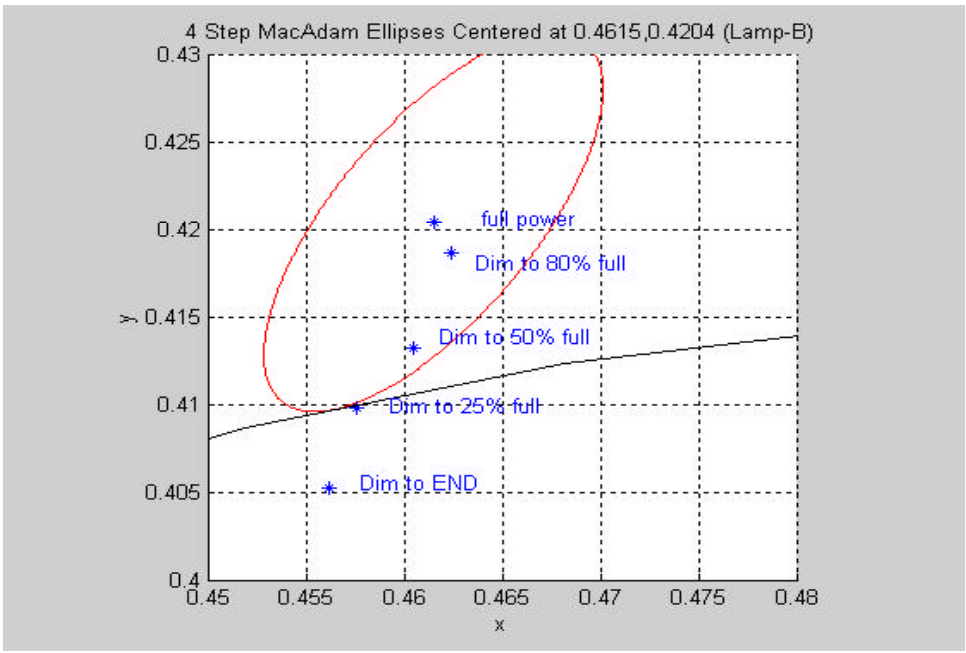
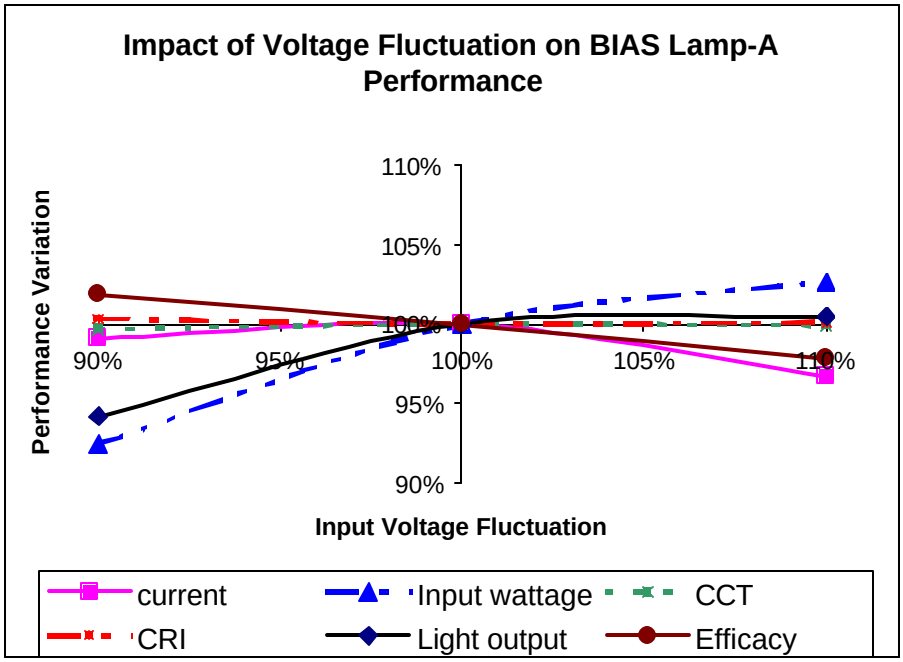


Figure 3.4-4 Effect of Dimming on Lamp Chromaticity Coordinates

3.4.3.5 Effect of Voltage Fluctuation on BIAS Lamp Performance

Figure 3.4-5 shows that BIAS lamp system performance in terms of color, light output, and electrical characteristics is quite stable within a 10% voltage range. The effects of voltage fluctuation are also

documented in Figure 3.4-8 and Figure 3.4-9 in Section 3.4.4. Testing of the effect of voltage fluctuation on lamp performance followed standard IESNA protocols.



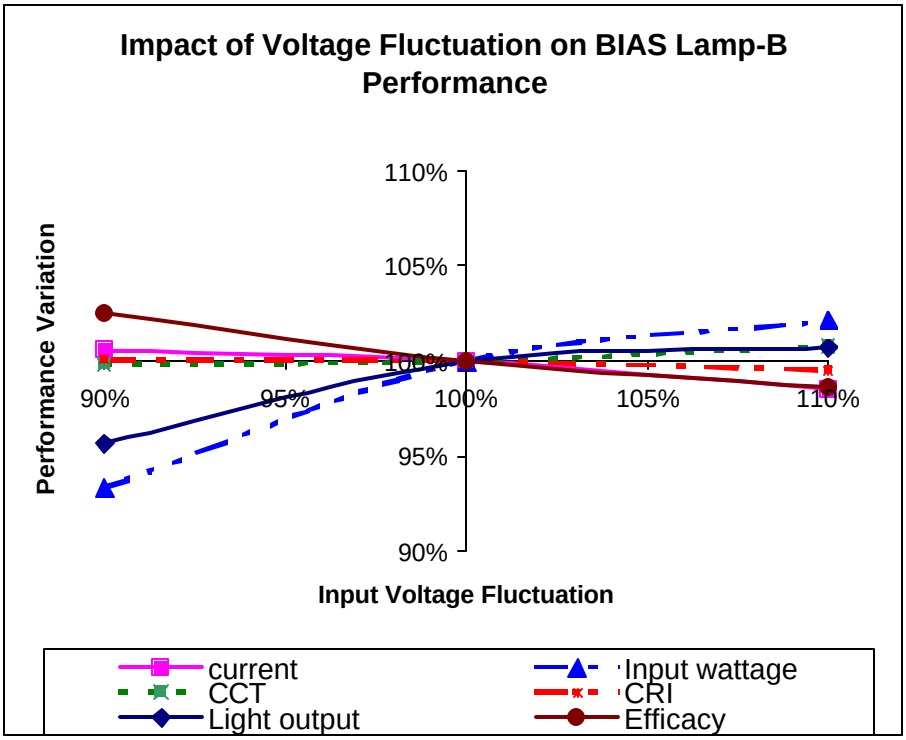
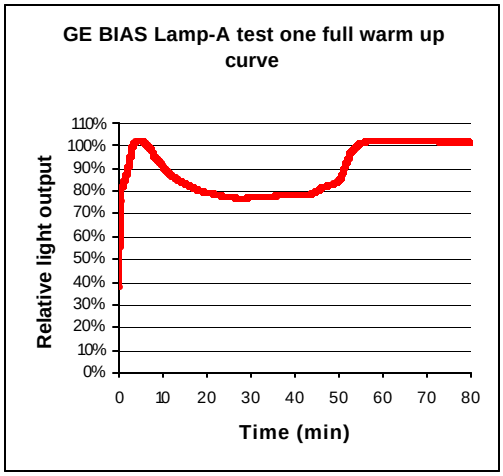
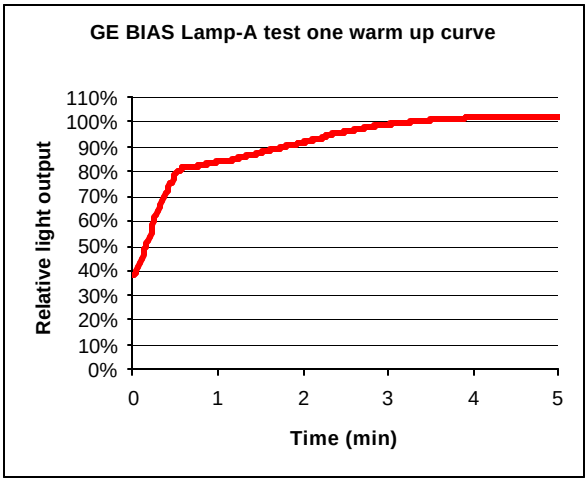


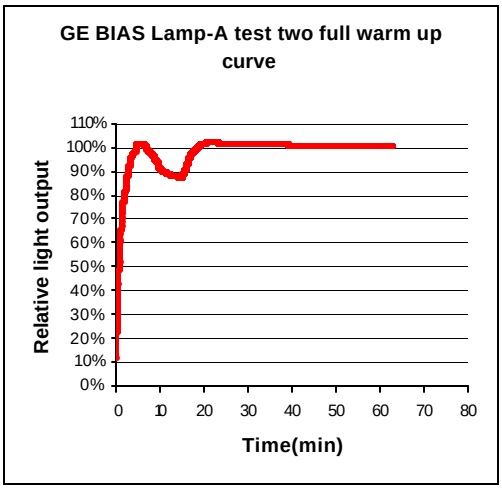
Figure 3.4-5 Impact of Voltage Fluctuation on BIAS Lamp Performance

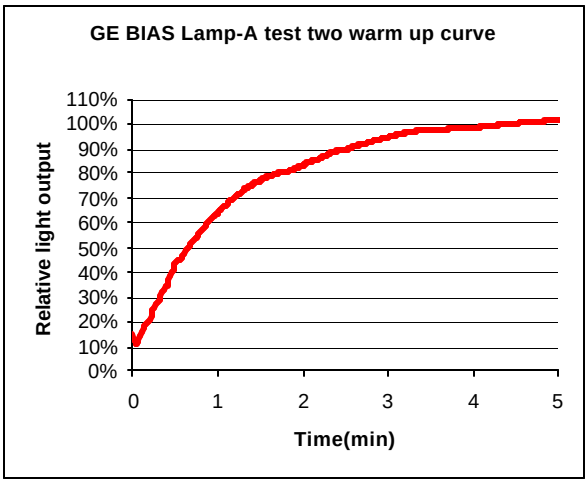
3.4.3.6 Warm-Up Time

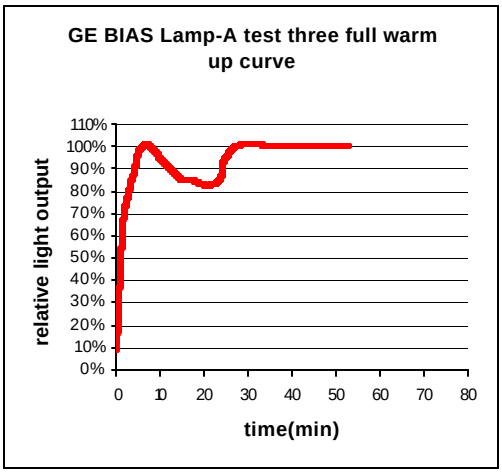
It takes 163 seconds for lamp A and 198 seconds for Lamp B to reach their 90% light output levels. These figures are given in Figure 3.4-8 and Figure 3.4-9 in Section 3.4.4. These warm-up times are higher than the system specification of 100 seconds, so the lamps do not meet the specification in this area. and show the three measurements of warm-up curves for lamp A and lamp B, respectively. The warm-up curve in test one was performed without any additional lamp burn-in. The other two tests were conducted after 8 hours of additional burn-in time. IESNA protocols were followed in the testing of the lamps' warm-up times.











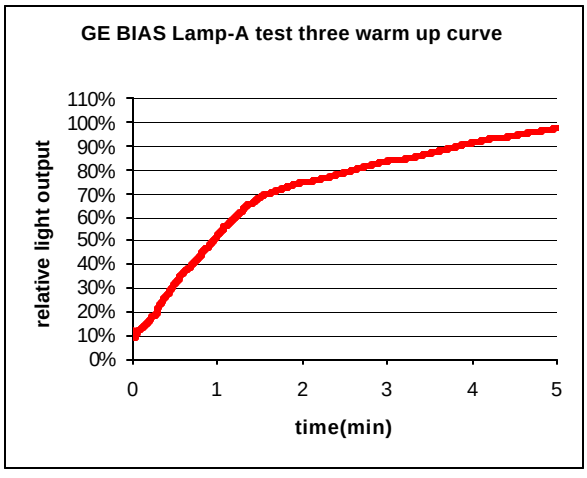


Figure 3.4-6 Lamp A Warm-Up Curve

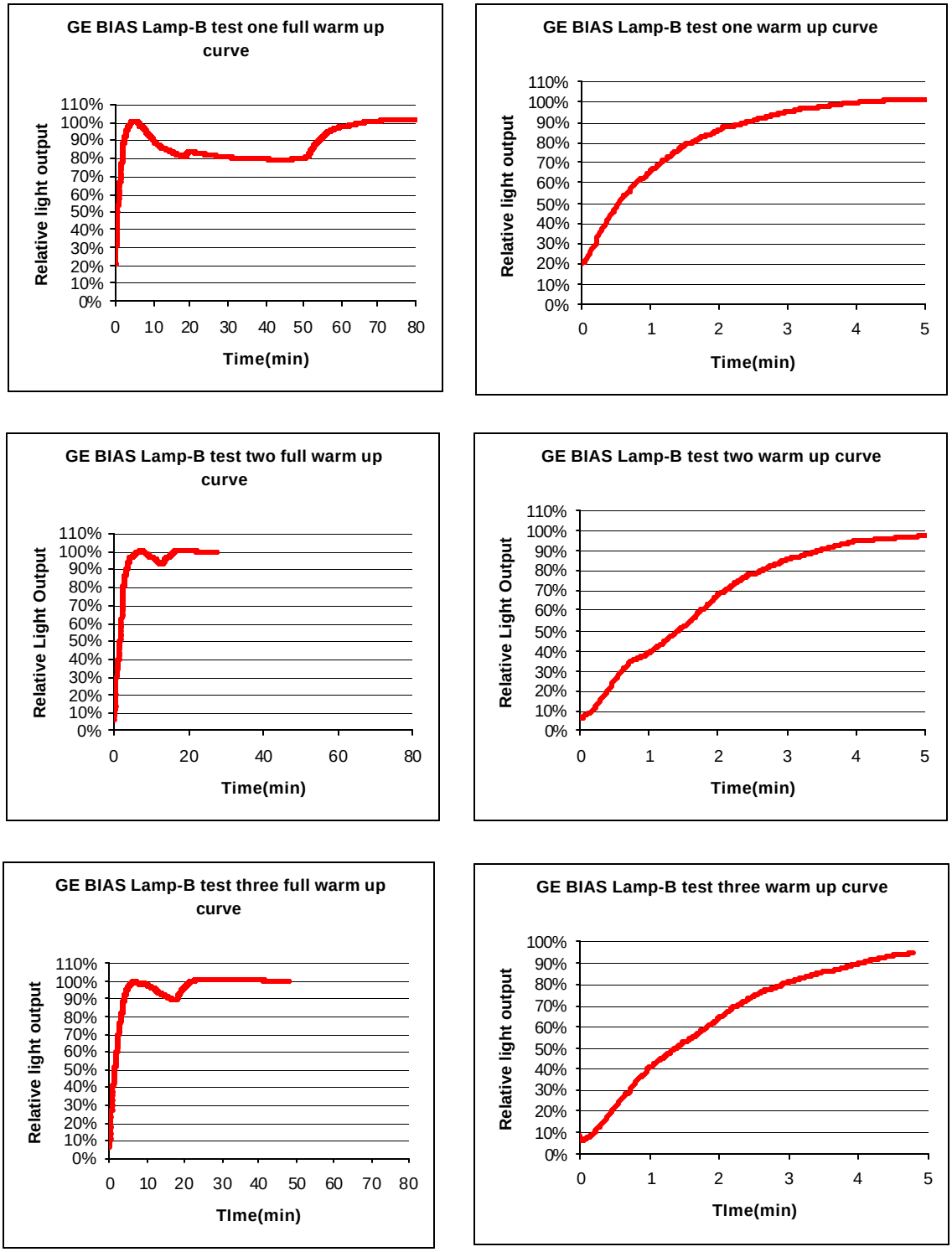


Figure 3.4-7 Lamp B Warm-Up Curve

3.4.4 Data Tables

Lamp-A: Mean and Standard Deviation from three measurements

Test condition	Ambient temperature (°C)	Input volts (v)	Current (A)	Input wattage (W)	Power factor	CCT	CRI	x	y	Light output (lm)	Efficacy
Voltage fluctuation	26.0 (+1.2)	108.1	0.491(+0.011)	28.0 (+0.3)	0.53 (+0.02)	2700(+30)	82.8(+0.5)	0.4639	0.4167	1627 (+16)	58.2 (+0.3)
	25.8 (+1.5)	120.0	0.489 (+0.019)	30.0 (+0.1)	0.51 (+0.02)	2705(+32)	82.8(+0.5)	0.4637	0.4169	1701 (+6)	56.8 (+0.1)
	25.2 (+2.2)	132.1	0.481(+0.001)	30.6 (0)	0.48 (0)	2726(+34)	82.4(+0.6)	0.4637	0.4199	1713 (+9)	56.0 (+0.3)
Dimming effect	26.2 (+1.2)	100%	0.487(+0.019)	29.9 (+0.2)	0.51 (+0.02)	2705(+31)	82.8(+0.5)	0.4637	0.4169	1695 (+8)	56.8 (+0.1)
	25.7 (+0.9)	80%	0.391(+0.017)	22.7 (+0.1)	0.48 (+0.02)	2679(+34)	83.3(+0.5)	0.4645	0.4151	1345 (+6)	59.2 (+0.2)
	25.6 (+0.9)	50%	0.291(+0.017)	15.6 (+0.2)	0.45 (+0.02)	2665(+33)	83.7(+0.3)	0.4623	0.4093	836 (+11)	53.8 (+0.1)
	22.9 (±1.3)	25%*	0.219(±0.001)	10.6 (±0.1)	0.40 (0)	2704 (±1)	83.4(±0.1)	0.4592	0.4088	415 (±9)	39.3 (±0.7)
	25.3 (±1.0)	End	0.204(±0.008)	10.0 (±0.1)	0.41 (±0.02)	2665(±33)	83.7(±0.2)	0.4583	0.4022	376 (±8)	37.5 (±0.6)
Dimming range	22.2%		Warm-up time (seconds)		163	** Numbers in the parenthesis are standard deviations.					

Lamp A: First Measurement

Test condition	Ambient temperature (°C)	Input volts (v)	current (A)	Input wattage (W)	Power factor	CCT	CRI	x	y	Light output (lm)	Efficacy
Voltage fluctuation	25.7	107.9	0.479	28.3	0.55	2681	83.1	0.4639	0.4140	1643	58.1
	25.6	120.0	0.467	30.0	0.54	2686	83.0	0.4637	0.4142	1706	56.9
	23.0	132.1*	0.481	30.6	0.48	2748	82.0	0.4636	0.4228	1723	56.3
Dimming effect	26.0	100%	0.465	30.0	0.54	2686	83.0	0.4637	0.4142	1704	56.8
	25.7	80%	0.372	22.6	0.51	2657	83.6	0.4646	0.4124	1339	59.3
	25.6	50%	0.271	15.4	0.47	2645	83.8	0.4623	0.4068	828	53.9
	22.0	25%*	0.218	10.5	0.40	2704	83.4	0.4590	0.4083	406	38.5
	25.3	End	0.195	10.1	0.43	2646	83.8	0.4579	0.3990	382	37.7
Dimming range	22.4%		Warm-up time (seconds)		108.0						

Lamp A: Second Measurement

Test condition	Ambient temperature (°C)	Input volts (v)	Current (A)	Input wattage (W)	Power factor	CCT	CRI	x	y	Light output (lm)	Efficacy
Voltage fluctuation	27.3	107.9	0.498	27.8	0.52	2684	83.1	0.4633	0.4133	1626	58.5
	27.4	120.0	0.499	29.9	0.50	2687	83.1	0.4632	0.4137	1694	56.7
	27.4	132.1	0.482	30.6	0.48	2686	83.0	0.4634	0.4138	1709	55.9
Dimming effect	27.4	100%	0.499	29.9	0.50	2687	83.1	0.4632	0.4137	1694	56.7
	26.6	80%	0.401	22.8	0.47	2661	83.6	0.4642	0.4120	1350	59.2
	26.5	50%	0.298	15.5	0.43	2648	83.9	0.4615	0.4058	831	53.7
	22.2	25%*	0.218	10.5	0.40	2703	83.5	0.4592	0.4088	417	39.7
	26.3	End	0.209	10.0	0.40	2646	83.9	0.4579	0.3993	380	38.0
Dimming range	22.5%		Warm-up time (seconds)		150						

Lamp A: Third Measurement

Test condition	Ambient temperature (°C)	Input volts (v)	current (A)	Input wattage (W)	Power factor	CCT	CRI	x	y	Light output (lm)	Efficacy
Voltage fluctuation	25.0	107.9	0.497	27.8	0.52	2734	82.3	0.4646	0.4227	1612	58.0
	24.5	120.1	0.500	30.0	0.50	2741	82.2	0.4641	0.4229	1702	56.7
	25.1	132.0	0.481	30.6	0.48	2743	82.1	0.4640	0.4230	1706	55.8
Dimming effect	25.1	100%	0.497	29.7	0.50	2741	82.2	0.4641	0.4229	1688	56.8
	24.9	80%	0.402	22.8	0.47	2718	82.8	0.4648	0.4209	1345	59.0
	24.7	50%	0.302	15.8	0.44	2703	83.3	0.4631	0.4154	849	53.7
	24.4	25%	0.220	10.6	0.40	2705	83.4	0.4594	0.4092	422	39.7
	24.4	END	0.208	10.0	0.40	2703	83.5	0.4590	0.4082	367	36.8
Dimming range	21.7%		Warm-up time (seconds)		232						

Figure 3.4-8 Lamp A Measurement Results

Lamp-B: Mean and Standard Deviation from three measurements

Test condition	Ambient temperature (°C)	Input volts (v)	Current (A)	Input wattage (W)	Power factor	CCT	CRI	x	y	Light output (lm)	Efficacy
Voltage fluctuation	25.0 (+1.7)	108.1	0.494 (+0.001)	27.8 (+0.1)	0.52 (0)	2749(+23)	82.3(+0.5)	0.4621	0.4200	1592 (+12)	57.3 (+0.3)
	24.8 (+1.5)	120.0	0.499 (0)	30.0 (+0.1)	0.50 (0)	2758(+26)	82.1(+0.6)	0.4615	0.4205	1690 (+6)	56.3 (+0.2)
	25.0 (+1.6)	132.1	0.483 (0)	30.8 (+0.1)	0.48 (0)	2755(+23)	82.2(+0.5)	0.4617	0.4204	1697 (+4)	55.1 (+0.2)
Dimming effect	24.8 (±1.7)	100%	0.498 (±0.001)	29.9 (±0.1)	0.50 (0)	2757(±25)	82.1(±0.5)	0.4615	0.4204	1684 (±13)	56.2 (±0.5)
	24.8 (±2.0)	80%	0.403 (±0.002)	23.0 (±0.2)	0.48 (0)	2733(±21)	82.8(±0.4)	0.4624	0.4186	1343 (±4)	58.4 (±0.7)
	24.5 (±2.1)	50%	0.299 (±0.002)	15.6 (±0.2)	0.44 (0)	2720(±22)	83.2(±0.4)	0.4605	0.4132	842 (±10)	53.8 (±0.9)
	22.8 (±1.0)	25%*	0.220 (±0.002)	10.7 (±0.1)	0.40(0)	2732(±1)	83.2(±0.1)	0.4576	0.4098	415 (±14)	38.9 (±1.4)
	24.1 (±2.0)	End	0.202 (±0.002)	9.7 (±0.1)	0.40 (0)	2717(±23)	83.4(±0.3)	0.4562	0.4052	332 (±29)	34.4 (±2.7)
Dimming range	19.7%		Warm-up time (seconds)		198	** Numbers in the parenthesis are standard deviations.					

Lamp B: First Measurement

Test condition	Ambient temperature (°C)	Input volts (v)	Current (A)	Input wattage (W)	Power factor	CCT	CRI	x	y	Light output (lm)	Efficacy
Voltage fluctuation	26.5	108.1	0.495	27.8	0.52	2723	82.9	0.4607	0.4137	1602	57.6
	26.1	120.0	0.499	30.0	0.50	2728	82.7	0.4602	0.414	1685	56.2
	26.4	132.1	0.482	30.8	0.48	2729	82.7	0.4603	0.4141	1701	55.2
Dimming effect	26.7	100%	0.497	29.8	0.50	2728	82.7	0.4602	0.4140	1684	56.5
	26.9	80%	0.401	22.8	0.47	2709	83.2	0.4608	0.4123	1348	59.1
	26.8	50%	0.296	15.4	0.43	2694	83.6	0.4588	0.4067	844	54.7
	22.0	25%*	0.221	10.7	0.40	2732	83.2	0.4575	0.4095	399	37.4
	26.2	End	0.205	9.8	0.40	2691	83.8	0.4549	0.3994	363	37.2
Dimming range	21.6%		Warm-up time (seconds)		144						

Lamp B: Second Measurement

Test condition	Ambient temperature (°C)	Input volts (v)	Current (A)	Input wattage (W)	Power factor	CCT	CRI	x	y	Light output (lm)	Efficacy
Voltage fluctuation	25.2	107.9	0.496	27.8	0.52	2763	82.1	0.4627	0.4233	1594	57.3
	25.2	120.0	0.499	30.0	0.50	2774	81.7	0.4622	0.4240	1696	56.5
	25.3	132.0	0.483	30.8	0.48	2769	81.9	0.4622	0.4233	1697	55.1
Dimming effect	24.3	100%	0.499	30.0	0.50	2774	81.7	0.4622	0.4240	1696	56.5
	24.4	80%	0.403	23.0	0.48	2745	82.5	0.4632	0.4218	1342	58.3
	24.2	50%	0.301	15.8	0.44	2733	82.9	0.4613	0.4165	851	53.9
	23.9	25%	0.219	10.6	0.40	2731	83.3	0.4576	0.4098	424	40.2
	23.8	END	0.201	9.6	0.40	2731	83.2	0.4568	0.4082	306	31.9
Dimming range	18.0%		Warm-up time (seconds)		207						

Lamp B: Third Measurement

Test condition	Ambient temperature (°C)	Input volts (v)	Current (A)	Input wattage (W)	Power factor	CCT	CRI	x	y	Light output (lm)	Efficacy
Voltage fluctuation	23.2	107.9	0.493	27.7	0.52	2761	82.0	0.4629	0.4231	1579	57.0
	23.2	120.0	0.499	30.1	0.50	2771	81.8	0.4622	0.4236	1688	56.1
	23.3	132.1	0.482	30.9	0.48	2767	81.9	0.4626	0.4237	1694	54.8
Dimming effect	23.3	100%	0.498	30.0	0.50	2769	81.9	0.4622	0.4232	1671	55.7
	23.0	80%	0.405	23.2	0.48	2744	82.6	0.4633	0.4216	1340	57.8
	22.6	50%	0.300	15.7	0.44	2732	83.0	0.4613	0.4164	831	52.9
	22.4	25%	0.222	10.7	0.40	2732	83.2	0.4577	0.4100	421	39.3
	22.3	END	0.202	9.6	0.40	2730	83.2	0.4570	0.4081	328	34.1
Dimming range	19.6%		Warm-up time (seconds)		243						

Figure 3.4-9 Lamp B Measurement Results

3.4.5 Summary

The LRC measured the electrical characteristics, light output, dimming range, color, effect of voltage fluctuations, and warm-up time for the two BIAS lamps provided by GE. In all cases, the LRC followed the testing protocol recommended by the *IESNA Approved Method for the Electrical and Photometric Measurements of Single Ended Compact Fluorescent Lamps* (LM-66-00). The results show that the lamps generally conformed to the desired specification for all parameters with the exception of warm-up time. This discrepancy can be attributed to the lamps rather than the ballasts.

4 Market Analysis

4.1 Executive Summary

The market research study conducted by the Lighting Research Center (LRC) shows that a representative sample of Unites States (U.S.) households has quite favorable feelings about compact fluorescent lamps (CFLs) in general and the prospect of incorporating CFL technology into dedicated table or floor lamps in particular.

The LRC study found that:

- Based on tests with four common types of CFLs, shape of the lamp does not affect the amount of light on the work surface.
- Table lamps generally require CFLs with approximately 1800 lumens.
- Consumers very much liked having the choice of lamp illumination colors (different correlated color temperatures [CCTs]).
- Consumers were concerned about the high cost for CFLs relative to incandescent lamps.
- Consumers wanted fast warm-up time.
- Long lamp life was not a major motivator for many consumers. Some who favored long lamp life wanted some sort of guarantee.
- A majority of the consumers preferred dimming in their portable fixtures, and they are willing to pay approximately $5.00 more for this feature, within a wide range of typical luminaire costs.
- A majority of the consumers used table and floor lamps in their bedrooms, family rooms and dens, but a significant portion of them did not use CFLs in these fixtures. These facts point to an opportunity to market both CFLs and dedicated CFL table or floor lamps for these living areas.
- A consumer education campaign, and reduced disparity between price and perceived value will increase the use of CFLs in residential applications.

4.2 Background

General Electric Corporate Research and Development (GE CR&D) is developing a miniature ballast for plug-in CFLs that can be mounted in a package that is approximately the same size as the standard metal shell lamp holder currently used in portable fixtures designed for incandescent lamps. Use of this Ballast-

in-a-Socket will allow fixture manufactures to very easily manufacture a wide range of portable fixtures that use only energy-efficient compact fluorescent lamps. This project has been funded by the United States Department of Energy (US DOE) and GE. The Lighting Research Center (LRC) was subcontracted by GE to support their ballast development program. Transforming portable lighting fixtures, such as table and floor lamps, to use CFLs instead of the conventional incandescent or halogen-incandescent lamps could result in significant energy savings for consumers and the country.

Although CFLs consume less energy and have longer operating life than conventional incandescent or halogen-incandescent light sources, their acceptance in residential applications, especially in the United States, has been low. One of the barriers for widespread acceptance has been the lack of properly designed luminaires for CFLs. Portable lighting fixtures such as table and floor lamps are ideal for accommodating CFLs since they do not have the ventilation problem experienced by enclosed luminaires. Here again, most portable luminaires presently have screw-base sockets. Consumers who have attempted to use screw-base CFLs in these fixtures have often found that many screw-base CFLs are too long to fit into the harps that hold the shades on existing fixtures. Those that do fit raise the center point of the source relative to the shade, which changes the optics of the fixture. A second key factor is that screw-base CFLs are rather expensive compared to the incandescent lamps they are designed to replace, while a third factor is that some consumers object to disposing of the complete lamp and ballast system when only the lamp has burned out. In addition, some consumers have complained about the reduced light levels on the work surface near the table lamp where they frequently performed tasks such as reading and writing. One of the main reasons for reduced light levels is that, unlike incandescent lamps, the base of screw-base CFLs is wider than the light-producing portion, therefore occluding a significant portion of the downward directed light.

The Ballast-in-a-Socket is designed to resolve these and other issues associated with the use of CFLs in portable fixtures. GE CR&D, in cooperation with GE Lighting, is developing miniature ballast for plug-in CFLs that will fit within a shell that is about the same size as the incandescent lamp socket used with table or floor lamps. Manufacturers of table and floor lamps can install the Ballast-in-a-Socket in place of the standard Metal Shell Edison Socket on virtually any portable fixture they now manufacture. This will convert these luminaires into dedicated CFL luminaires. It is hoped that many luminaire manufactures would adopt this ballast to create dedicated plug-in CFL luminaires, reducing energy costs for consumers and the country while not decreasing the choice of table and floor lamps for end users.

4.3 LRC Project Goals

The LRC's role in this project is to identify consumers' preferences with regards to features and their willingness to buy dedicated CFL luminaires and replacement CFLs. The original prototype was developed by CRD in parallel with the work being conducted at the LRC. We expect that as this prototype evolves into a product, the design will be guided by the work conducted at the LRC. The US DOE will also use this consumer preference information to help plan future R&D programs. As part of this program, GE CR&D will retrofit one or two table lamps with this new ballast and provide them to the LRC a few months before the conclusion of this program so the LRC can evaluate their technical performance and verify them against the performance targets established by GE.

There are four parts to the LRC's study: a lighting industry manufacturer/specifier survey, a laboratory evaluation of table lamp light distribution, a focus group study, and a direct-mail consumer survey.

1. Lighting Industry Survey: The goal of the survey was to contact various groups in the lighting industry who had information about or influenced the use of CFLs. These groups were contacted in order to understand the state of the art of table lamps and the reasons for low penetration of CFLs in residential applications.
2. Light Distribution Study: The goal of the laboratory study was to determine how the lamp, fixture, and shade design impacted light distribution on the work surface from a table lamp.
3. Focus Group Study: The goal of the focus group study was to explore consumer opinions of CFLs and dedicated CFL luminaries and develop an understanding of the key issues that should be measured in the direct-mail survey.
4. Direct-Mail Survey: The goal of the direct-mail survey was to understand and measure consumers' preferences for features of a dedicated CFL luminaire and their willingness to buy a dedicated luminaire and replacement CFLs.

The intent of this summary chapter is to synthesize the information gathered in each of the four individual studies and to provide GE CR&D with specific information about dedicated CFL luminaires and recommendations for specific design features to be included into the new dedicated CFL luminaire.

4.4 Results and Recommendations

4.4.1 Table Lamp Features and Specifications

4.4.1.1 Dimming Control

During the lighting industry survey, one of the leading portable luminaire manufacturers commented that dimming is not necessarily a required feature, since most customers put regular lamps into fixtures that come with 3-way sockets. In addition, they did not think there was substantial preference between 3-way and continuous dimming. However, the LRC found that a majority of the consumers preferred dimming, with either 3- way or continuous, compared to single-way switches (see Figure 4.4-1 below). This requirement became evident during the focus group study and in the direct-mail survey. It was evident from the direct-mail survey that a slight majority preferred continuous dimming to 3-way dimming. However, during the focus group study, a majority of the participants preferred continuous dimming, especially after they had a chance to experience different dimming features (see Figure 4.4-4). The direct-mail survey indicates that consumer are willing to pay around $5.00 more for the dimming feature regardless of the cost of the luminaire. In addition, focus group participants indirectly emphasized the need for dimming by mentioning the requirement for different light levels to perform different tasks.

Response	*Percentage*
3-way dimming	26.7%
Continuous dimming	37.4
No dimming	18.2
Not Sure	1.4
No Answer	16.2

Figure 4.4-1 Percentage who prefer dimming type (results from direct-mail survey)

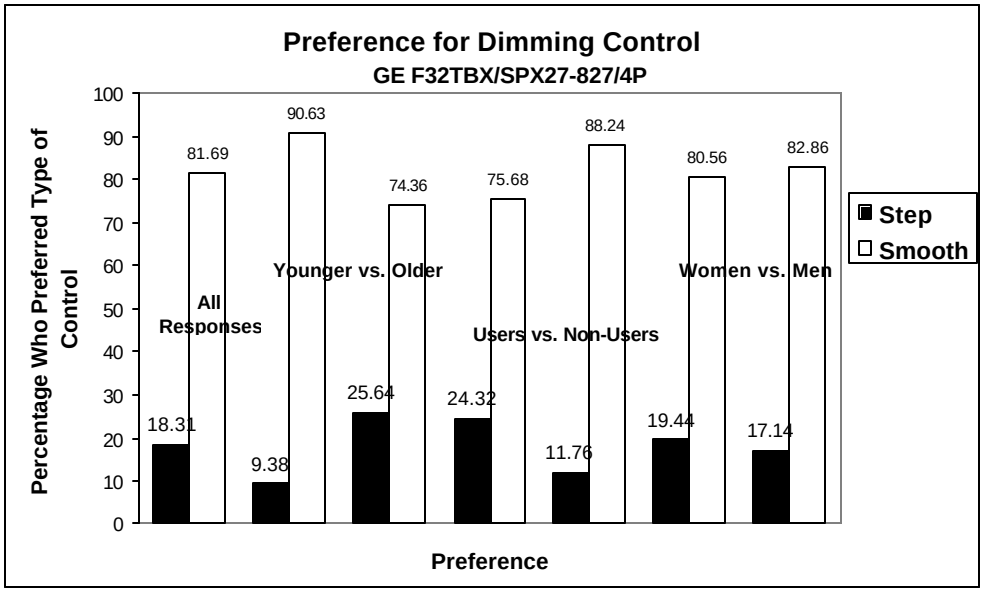


Figure 4.4-2 Percentage of respondents who preferred each type of dimming control, by all respondents, by age, by CFL ownership, and by gender, results from focus group study.

4.4.1.2 Choice of CFL Lamps

The conclusion drawn from the laboratory light distribution measurement study is that the color and shape of the table lamp, i.e., the fixture, influences the amount of light reaching the work surface more than the lamp or the shade. Therefore, any of the CFL lamps tested during this study (GE 28 watt 2D plug-in CFL, GE 32 watt Twin BIAX (TBX) plug-in CFL, TCP 32 watt Spiral plug-in CFL) can be used in table lamp applications. However, it is worth noting that prior experience shows that using 2D or Circline-type CFLs can produce greater illuminance on the work surface. However, if the shade diameter is not large enough, the outline of the lamp becomes visible on the outside of the shade and results in reduced aesthetics.

4.4.1.3 CFL Lamp Lumen Output

A leading portable luminaire manufacturer commented that a minimum output of 1750 lumens is needed for the CFL lamp (equivalent to 100-watt incandescent). This was confirmed during the focus group study when a majority of participants found that a lamp output of approximately 1800 lumens is required for reading a newspaper located two feet from the base of the table lamp used in this study.

4.4.1.4 Choice of Colors for CFL Lamps

During the focus group study, the participants viewed a variety of CFLs with correlated color temperatures (CCTs) of 2700K, 3000K, 3500K, and 4100K. Although the most popular lamp color was 3500K, participants liked having the choice of colors. They thought CFLs offer a benefit of color choice not possible with incandescent lamps. Some respondents very much liked the opportunity to vary the color of the lamps to fit changing decor and lighting moods. Based on this, it is interesting to consider why screw-base CFLs are available almost exclusively with a CCT of 2700K.

In addition, a leading portable luminaire manufacturer commented that good color rendition is an important lamp characteristic, especially for the hospitality industry, because they invest a lot of money in choosing fabrics and paint colors for the rooms, and therefore, the lamps should not distort the colors.

4.4.1.5 Fast Warm-up

The consensus among focus group respondents was that any noticeable warm-up period for CFLs was too long. During this same focus group study the majority of the participants said that the warm-up time should be 20 seconds or less. A leading portable luminaire manufacturer also commented that quick start and warm-up is an important lamp characteristic.

4.4.1.6 Long Lamp Life

Although some of the respondents felt positively about the long lamp life characteristic, this was not a major motivator for quite a few people. Some of those who did responded positively to long life wanted some sort of life guarantee. Many have become very suspicious of any long-lasting claims. Many people (mostly men) did not mind changing burnt-out lamps. Most respondents were more concerned about price than lamp life.

4.4.2 Table Lamp Marketing Issues

4.4.2.1 Willingness to buy CFLs

Contrary to some past research that shows consumer resistance to compact fluorescent lamps, the findings of the direct-mail survey show that a representative sample of U.S. households has quite favorable feelings about CFLs in general, and the prospect of incorporating CFL technology into dedicated table or floor lamps in particular. When asked, "would you buy compact fluorescent lamps, 82.2% of all respondents replied affirmatively (see Figure 4.4-2), while only 8.9% would not buy. People who already

use CFLs in their homes are significantly more likely to respond affirmatively to the question, reaching a level of 92.9% (see Figure 4.4-3). However, when asked "have you ever used CFLs in your home, 41.7% replied affirmatively, while 54.4% had not used them.

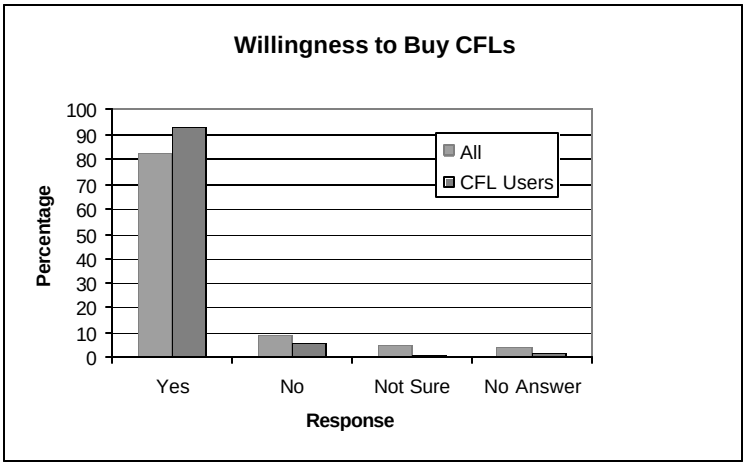


Figure 4.4-3 Willingness to buy CFLs, results from direct-mail survey

4.4.2.2 Willingness to buy dedicated CFL fixtures

When asked, "Would you buy a table or floor lamp that used only CFLs," 64.0% of all respondents answered affirmatively (see Figure 4.4-4). Among present CFL users, 67.2% would buy, and even among those who do not presently use CFLs, 61.1% were willing to buy a dedicated CFL table or floor lamp (see Figure 4.4-4).

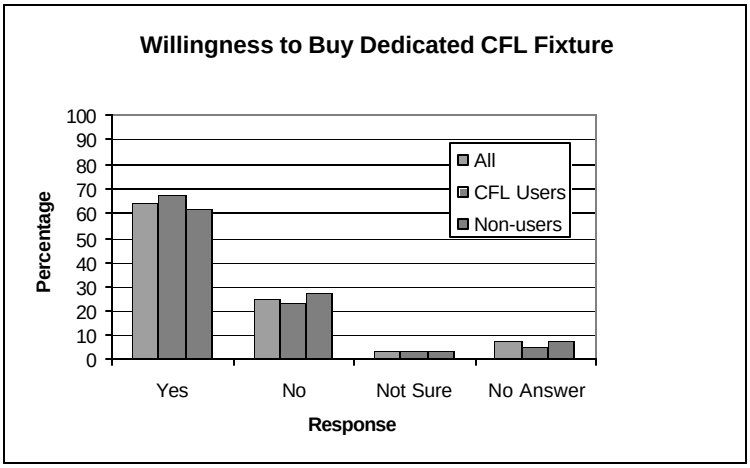


Figure 4.4-4 Willingness to buy dedicated CFL luminaire, results from direct-mail survey

4.4.2.3 Luminaire and Replacement Lamp Price

Most focus group and direct-mail survey respondents felt that the CFLs are costly. Several focus group respondents mentioned that when their children had broken a CFL, they did not replace it with another CFL because the lamps were so expensive. It was also mentioned during the focus group study that consumers like to stockpile bulbs, and the perceived high cost would limit stockpiling. This may be an issue where consumers need to be educated that they do not need to stockpile CFLs because they last much longer than incandescent lamps.

A majority of respondents from the two surveys felt that a dedicated CFL luminaire sounds expensive. The price for the most popular Cresswell/EMESS portable lamps is about $39. Volume falls off as the price rises to $49 and then falls off more rapidly after that.

The focus group study found that consumers like their luminaires and are anxious about changing to new ones. Therefore, it is suggested that areas in retail stores such as home centers, lighting stores, and hardware stores can be created for consumers to bring in their table lamps with screw-base sockets and have them converted to pin-base CFL sockets.

4.4.2.4 Consumer Education

The responses received from the lighting industry survey, comprised of fixture manufacturers, interior designers, and hospitality lighting specifiers, indicate that lack of consumer information regarding the benefits of CFLs is one of the main reasons for the low penetration of CFLs in residential applications. They also suggested that a consumer education campaign run by the DOE or a similar agency will increase the use of CFLs in residential applications. The focus group report also suggests a large marketing campaign is necessary to overcome purchasing inertia of consumers.

4.4.2.5 Market size for CFL lamps and dedicated CFL table or floor lamps

The responses received from the direct-mail survey show that nearly all respondents have portable fixtures in their bedrooms (90.4%) and living rooms (94.8%) and more than 61% have portable table or floor lamps in their family rooms and dens (Figure 4.4-5). However, people's use of CFLs in these areas are only 28.0% in their bedrooms, 23.5% in their living rooms, and 29.6% in their family rooms. These facts point to an opportunity to market both CFLs and dedicated CFL table or floor lamps for these living areas.

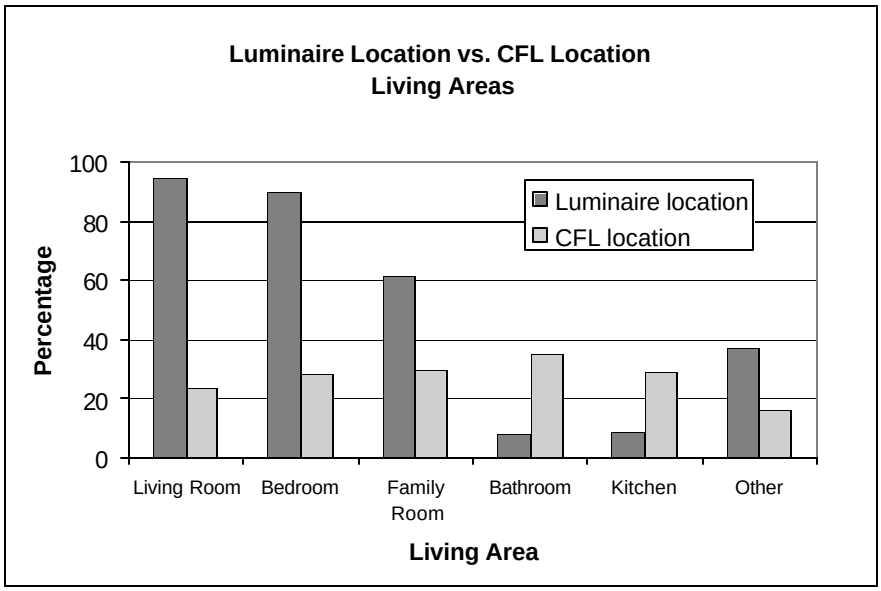


Figure 4.4-5 Locations of luminaire use, results from direct-mail survey

5 Conclusion

Our work has shown that it is quite feasible to produce dedicated CFL ballasts within the socket of a typical table or floor lamp. Application Specific Integrated Circuits (ASIC) are key to the success of such a product. Without the cost, size and control advantages provided by circuit integration, none of the customers' CTQ's would be achievable.

This program also included an investigation into end-users' attitudes toward CFL's, in order to gauge the potential for success for a product such as the BIAS. The results were positive, at least among those who were already integral CFL users. However, even non-CFL users showed a favorable attitude toward the color and features CFLs offered. This implies that when the high initial cost factor is mitigated, there would be less consumer resistance to CFLs use than was perhaps expected.

A major part of this study was devoted to the development of new robust ASIC technology which would be necessary to provide advanced ballast functionality when using low-cost ballast techniques such as GE Lighting's L-Comp topology. We have shown that the ASIC and ballast circuit does indeed provide all the functionality currently available commercially in integral CFLs. Additionally, functionality such as continuous dimming and no lamp/broken lamp protection, which are not usually included in current CFL offerings, are included for ease of use, energy savings and safety reasons.

6 Acknowledgements

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7 Appendix A: System Specification

7.1 GE CR&D						System Specification
26W, 120 Volt, LPF TBX Non-Amalgam, BIAS						
System Description						
Parameter	***Symbol***	***Conditions***	***Min***	***Nom***	***Max***	***Units***
Operating Voltage	Vin		108	120	132	V rms
Line Frequency				60		Hz
Operating Temperature Range		For 90% Lumen Output	5	25	50	C
CRI at full power			80	82	---	
Time to 90% Lumens			---	---	100	Sec
Starting Temperature		?		---	---	C
Starting Time		Rapid	---	---	1.5	Sec
Lumen Maintenance		@ 50% of Rated Life	---	85%		% initial
Power Factor	P.F.	base down at 120V, 25C	0.4	0.5	---	
THD(fund)	THD(fund)	base down at 120V, 25C				
Center Beam Candle Power		For Reflector Systems	---	N/A	---	
		For Reflector Systems	---	N/A	---	
Beam Spread				N/A		
Color Temperature at full power				2800		K
Target Cost		System Variable, FOB FGN	---	---	10	$
			Min	***Avg***	***Max***	
Lumens Base Down	(BD)		1710			Lumens
Lumens Base Up	(BU)		---	N/A	---	Lumens
Input Wattage (ballast)	Pin	base down at 120V, 25C	28	30	32	Watts
Input Current (ballast)	Iin	base down at 120V, 25C	---	0.485	0.550	A rms
Life (median)		base down at 120V, 25 C, 3hr/20min cycle	---	30,000	---	hours
System Starts			---	30,000	---	
nom is a population average, min and max are +/-3 ? limits for individual systems						
Regulatory						
Parameter		***Reference Document***	***Related Conditions***			
Radiated Emissions		CFR 47 Part 18.305				
Conducted Emissions		CFR 47 Part 18.307				
Transient Tolerance		ANSI/IEEE62.41				
Safety		UL 1993				
Performance Standard (FTC/IEC/EC/CSA)						

Recommended Application Space			
Shaded Lamp	? Yes	Open Air Fixture (Track)	? Yes
Enclosed Indoor	? Yes	Recessed Can (Open)	? Yes
Open Indoor	? Yes	Recessed Can (Closed)	? Yes
Bare Bulb (Base down)	? Yes	Enclosed Outdoor (Base Down)	? Yes

8 Appendix B: References

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