Detectability and printability of EUVL mask blank defects for the 32 nm HP node

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ABSTRACT

The readiness of a defect-free extreme ultraviolet lithography (EUVL) mask blank infrastructure is one of the main enablers for the insertion of EUVL technology into production. It is essential to have sufficient defect detection capability and understanding of defect printability to develop a defect-free EUVL mask blank infrastructure. The SEMATECH Mask Blank Development Center (MBDC) has been developing EUVL mask blanks with low defect densities with the Lasertec M1350 and M7360, the 1st and 2nd generations, respectively, of visible light EUVL mask blank inspection tools. Although the M7360 represents a significant improvement in our defect detection capability, it is time to start developing a 3rd generation tool for EUVL mask blank inspection. The goal of this tool is to detect all printable defects; therefore, understanding defect printability criteria is critical to this tool development.
In this paper, we will investigate the defect detectability of a 2nd generation blank inspection tool and a patterned EUVL mask inspection tool. We will also compare the ability of the inspection tools to detect programmed defects whose printability has been estimated from wafer printing results and actinic aerial images results.

Keywords: EUVL, EUV mask blank defect, EUV mask blank inspection, Defect printability

1. INTRODUCTION

A defect-free EUVL mask blank infrastructure is essential to inserting EUVL technology into high volume manufacturing (HVM). EUVL technology uses reflected EUV light from the patterned reticle to transfer the mask pattern to the wafer; therefore, defect-free reflective EUV mask blanks are critical for the technology. Particles on the EUV reflective multilayer (ML) surface are not the only problem, as embedded particles and pits under the ML on the substrate itself result in printable phase defects on the ML surface. Because surface particles can often be easily removed by standard cleaning processes, the phase error issue poses the greatest concern. In this paper, we focus only on these embedded substrate defects under the multilayer.
The SEMATECH MBDC has been developing defect-free multilayer deposition processes for several years using a state-of-the-art analytical tool set including the Lasertec M1350 and M7360 for mask blank inspection. [1],[2],[3] The Lasertec M7360, the worlds first 2nd generation EUV mask blank inspection tool, provides the MBDC with much improved inspection capability. [4],[5] Investigations of the capabilities of the M7360 are ongoing, and upgrades are in the planning stage to enhance its sensitivity. All activities are meant to drive the sensitivity specification necessary for detection on EUVL mask blanks for HVM EUVL blank manufacturing and patterned mask manufacturing. The same specification can also be used as a baseline to clarify the needs and the requirements of the 3rd generation EUV mask blank inspection tool currently in the planning stage for HVM of EUVL mask blanks. [6] The 3rd generation EUV mask blank inspection tool must detect all printable blank defects for EUVL HVM; therefore, studying the effects of small blank defects early will prepare the industry for success earlier. This activity is meant to augment and extend the knowledge of previous reports on the printability of ML embedded defects. [7],[8]
In this report, we summarize the detectability of embedded ML defects using the most sensitive EUVL mask blank inspection tool currently available (Lasertec M7360) and presents results on the printability of these embedded ML defects. The projected sensitivity specification for M7360 future upgrades and even for 3rd generation EUVL mask blank inspection tools can be projected based on our analysis.

2. EXPERIMENTAL

A test plate was fabricated with programmed embedded bumps, ML defects, and simple dense line patterns. In Figure 1, the entire test plate manufacturing procedure is illustrated. This particular test plate has only bump-type programmed embedded defects.

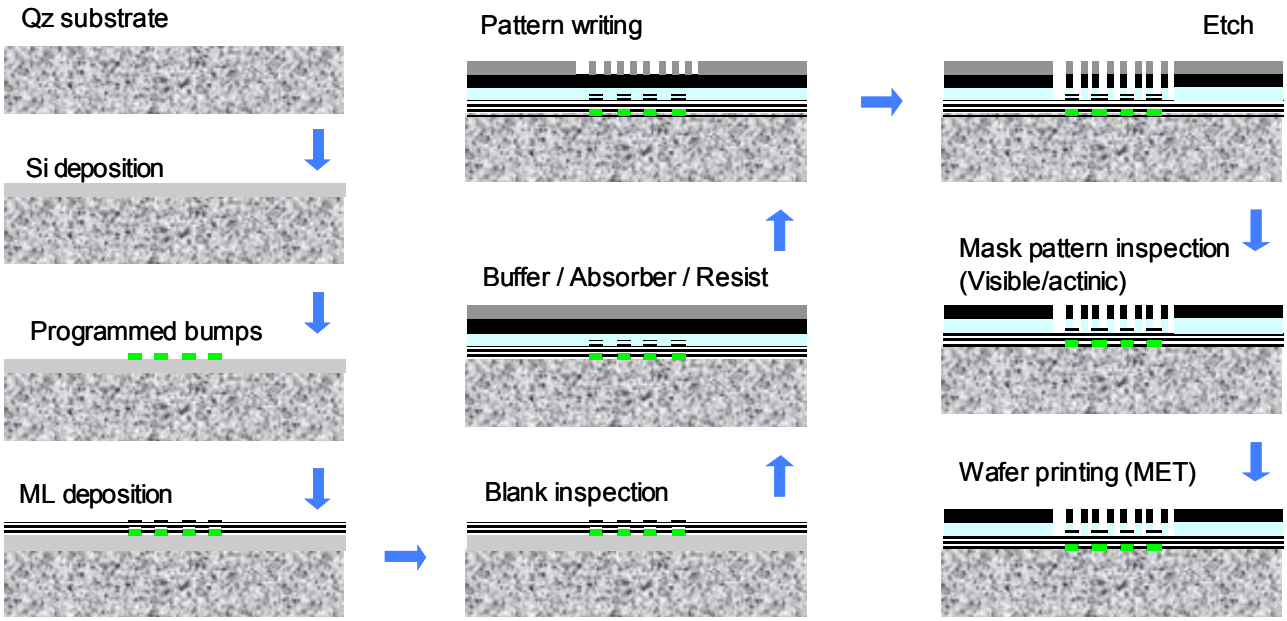

Figure 1: Entire manufacturing procedure for the programmed bump test plate.

2-1. Programmed bumps on EUVL mask blank

A 100 nm thick Si layer was deposited on a substrate. This was followed by fabricating 50 nm tall hydrogen silsesquioxane (HSQ) bumps using an e-beam pattern generation process. To mimic small (shallow), naturally occurring phase defects embedded in ML, a Mo/Si bi-layer was deposited and then a small portion of the Si layer was etched away. The process was then repeated 40 times. This deposition with etch smoothes the height of the bumps significantly. Finally, an 11 nm thick Si capping layer was deposited on the ML. The surface roughness of the final ML was measured using an atomic force microscope (AFM), and programmed defect sizes were also measured.

2-2. EUVL mask blank inspection with the Lasertec M7360

The Lasertec M7360 is a 2nd generation EUVL mask blank/substrate inspection tool operating at a 266 nm wavelength for enhanced resolution. It uses a confocal microscope to detect surface anomalies. The M7360 uses a laser power of 300 mW for ML inspections to prevent surface damage by the high laser power. For substrate inspections, the laser power is increased to 550 mW since no ML is present. The ultimate sensitivity of this tool with and without upgrades is still under investigation, but the test plate in this experiment was inspected using the current best recipe.

2-3. Absorber layer deposition and patterning

After blank inspection, a CrN buffer layer and a TaBN absorber layer were deposited on the test plate. Resist was also coated, and simple dense line patterns were generated on the embedded ML defect area. The test pattern was divided into two sections: 160 nm dense lines (1:1 pitch) and 225 nm dense lines. They correspond to 32 nm half pitch (HP) dense lines and 45 nm HP dense lines at wafer scale when printed with the SEMATECH/Berkeley 5X reduction EUVL

micro field exposure tool (MET). However, the same patterns represent 40 nm HP and 56 nm HP dense lines, respectively, when we consider the more common 4X reduction exposure conditions.

2-4. EUVL patterned mask inspection

In addition to the test pattern in the embedded defects area, an identical reference pattern was designed and patterned in a defect-free area to perform a die-to-die pattern inspection. The test plate was inspected using two state-of-the-art deep UV (DUV) pattern inspection tools using reflective light and an algorithm for reflective light inspections. Brief tool specifications are summarized in Table 1.

	Tool A	**Tool B**
Inspection wavelength (nm)	248	257
Inspection pixel size (nm)	62.5	72

Table 1: Wavelength and pixel size of the patterned mask inspection tools used.

2-5. Wafer print test at the SEMATECH/Berkeley MET

The wafer print test was performed using the SEMATECH/Berkeley MET at Lawrence Berkeley National Laboratory (LBNL) under annular illumination conditions. The defect printability was evaluated after resist develop processing by a scanning electron microscope (SEM).

2-6. Mask aerial image study at the SEMATECH/Berkeley actinic inspection tool (AIT)

The effect of ML embedded defects on the aerial test pattern image was assessed using the SEMATECH/Berkeley AIT at LBNL. This AIT is a unique, dedicated EUVL reticle inspection system operating on a bending magnet beam line at the LBNL Advanced Light Source (ALS). Aerial images from the mask were obtained to study substrate bump effects from absorber patterns on wafer critical dimension (CD) using the AIT's imaging mode, which uses a Fresnel zone plate lens to emulate a 0.25 numerical aperture (NA) EUVL stepper. Images were captured through focus with 0.8 □m steps corresponding to 50 nm on a 4X scanner. The background signal from the bright field area was used to accommodate illumination non-uniformity.

3. EXPERIMENTAL RESULTS

3.1. Programmed bumps on an EUVL mask blank

The programmed bumps are well formed and Gaussian shaped. AFM images and the size measured by the AFM are shown in both Table 2 and Figure 2. Bump heights ranged from 0.9 nm to 13.9 nm with widths (full width half maximum) ranging from 39 nm to 58 nm. Sphere equivalent volume diameter (SEVD) is the volume of imaginary sphere that has the same volume with a defect. The SEVD of those programmed defects ranged from 20 nm to 50 nm. The surface roughness of the final ML blank was 0.85 Å.

Defect Row	A	B	C	D	E	F	G	H	I	J	K	L
Height (nm)	13.9	13.1	11.9	9.7	8.2	7.2	6.1	5.4	4.0	3.5	2.4	0.9
FWHM (nm)	54.7	55.7	57.6	55.6	56.6	55.7	56.6	48.8	47.8	44.9	48.8	39.1

Table 2: Heights and widths (FWHM) of programmed embedded defects

3.2. Inspection results with the Lasertec M7360

The programmed bump ML plate was then inspected with the Lasertec M7360, and the results are shown as a dot graph in Figure 3 (each dot represents one defect at that location). The M7360 can detect with over 95% of capture efficiency embedded ML defects as small as 29 nm in SEVD that are actually 0.9 nm high and 48 nm wide. The mean

pixel for this size defect is over 3. If we consider smaller pixels, we can estimate that the M7360 can detect a defect 3.5 nm high and 45 nm wide. Based on the simulation, this size defect will have a 1.5% image contrast at 266 nm wavelength. As the 1st generation EUVL mask blank inspection tool, the Lasertec M1350 can detect defects with an image contrast below 1; consequently, we believe that this 2nd generation tool will also demonstrate more improved sensitivity after some upgrades. [6]

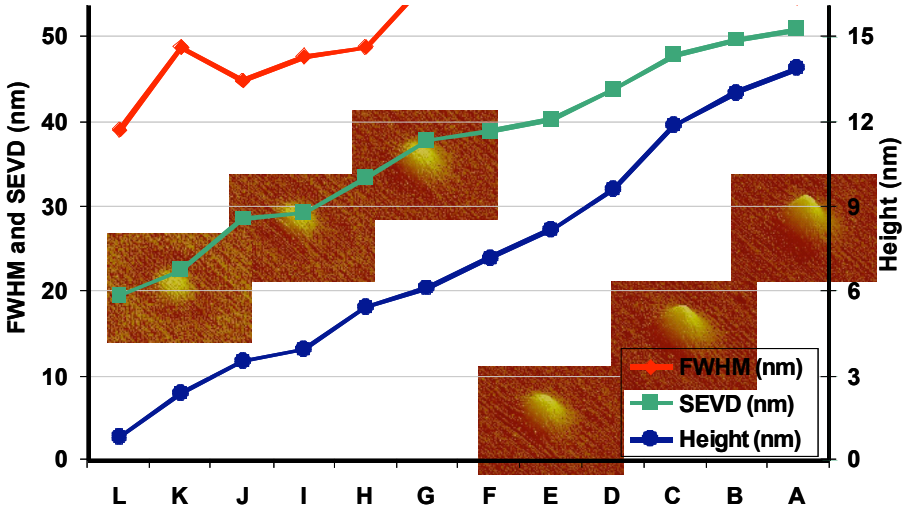

Figure 2: The size of the programmed embedded ML blank defects. The AFM images of defects are also shown: columns A, C, E, G, I, and K, from right to left. The heights, widths (in FWHM), and SEVDs are shown.

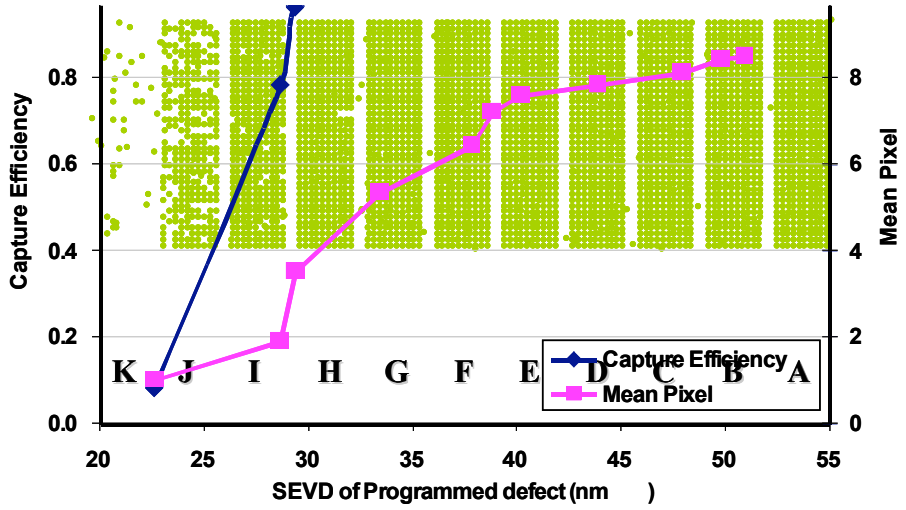

Figure 3: The result map of M7360 inspection (dot arrays). M7360 shows a high capture efficiency (CE) down to column I defects (29 nm SEVD, 4.0 nm high, and 47.8 nm wide) with a mean pixel over 3.

3.3. Post-patterning inspections with patterned reticle inspection tools

Simple dense line (160 nm and 225 nm) patterns were generated on the embedded ML defect area, and the patterned test plate was inspected with state-of-the-art patterned mask inspection tools. Only die-to-die inspection was performed with reflective light and an algorithm for reflective light inspections. Because current patterned mask inspection tools do not provide a special capability for EUVL patterned masks, the recipe we used was not well optimized for EUVL patterned masks. Irrespective of these conditions, the inspectability was actually quite good as the mask ran without catastrophic errors even in the 160 nm dense line pattern area. Due to the anti-reflective coating (ARC) layer, sufficient image contrast was obtained for 225 nm dense lines but still more resolution is required for 160 nm dense lines. (Figure 4) Some real defects that may have been generated during the test plate manufacturing process were detected successfully. (Figure 4) However, neither tool could detect any programmed embedded defects, even the largest ones (13.9 nm high) in column A.

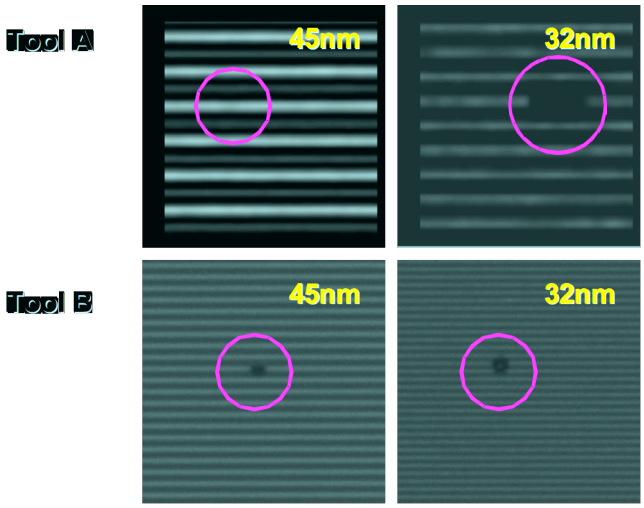

Figure 4: Some real defects on the test plate. The images from two DUV inspection tools show sufficient image contrast for the 225 nm dense lines thanks to the effects of the ARC.

3.4. Wafer print test at the SEMATECH/Berkeley MET

Smaller defects than column F, 39 nm SEVD (7.2 nm high and 55.7 nm wide), showed almost no effect on the wafer pattern for the 45 nm HP pattern. The same was true for smaller defects than column H defects, 33 nm SEVD (5.4 nm high and 48.8 nm wide) for the 32 nm HP pattern. In Figure 5, wafer SEM images are shown.
However, assessing the printability of the embedded programmed defects was problematic because the pattern fidelity was poor even though a resist that previously showed good resolution was selected. The line width roughness (LWR) of the resist pattern was too large to evaluate the printability of the programmed defects. The LWR of the 45 nm HP pattern averaged 6.3 nm, which is 14% of the nominal line CD. For the 32 nm HP patterns, the LWR was 7.8 nm, 28% of the nominal pattern CD. Therefore, it was difficult to assess defect printability at a level determined by 10% CD variation with respect to nominal. This part of the experiment should be rerun with a better quality resist.

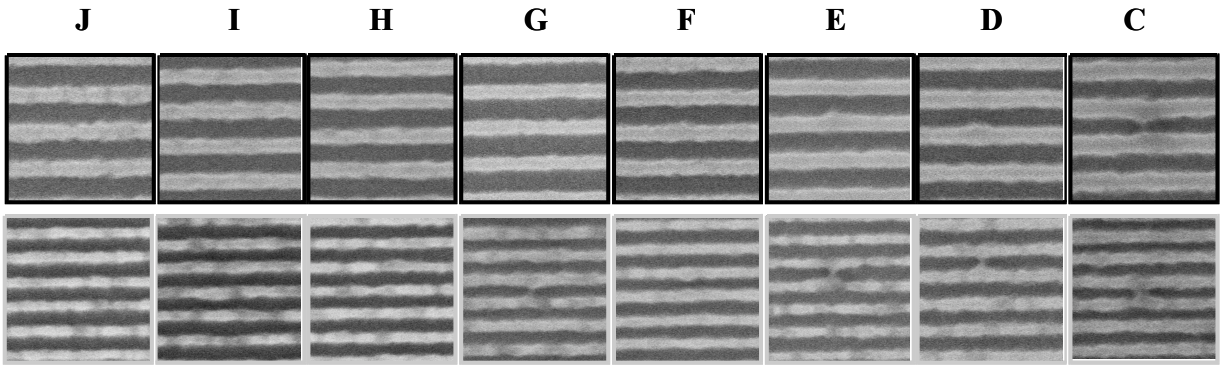

Figure 5: Wafer SEM images at the defect locations. Upper row images show each defect in the 45 nm HP pattern and lower row images for the 32 nm HP pattern.

3.5. Mask aerial image inspection at the SEMATECH/Berkeley AIT

We also investigated the programmed defects buried under the EUVL ML with the actinic light inspection tool at the ALS. The AIT could detect the programmed embedded defects well. Degradation of the aerial image was seen down to column L defects (0.9 nm high and 39 nm wide) for both 160 nm and 225 nm dense line areas. The images are shown in Figure 6. Bright intrusions or bridges are the absorber pattern markers used for locating an embedded programmed defect; these programmed defects can be seen in the lower left area relative to the absorber patterns. We also confirmed that the programmed embedded defects generate phase errors rather than amplitude errors; therefore, these defects produce larger image contrast under defocus conditions (Figure 7).

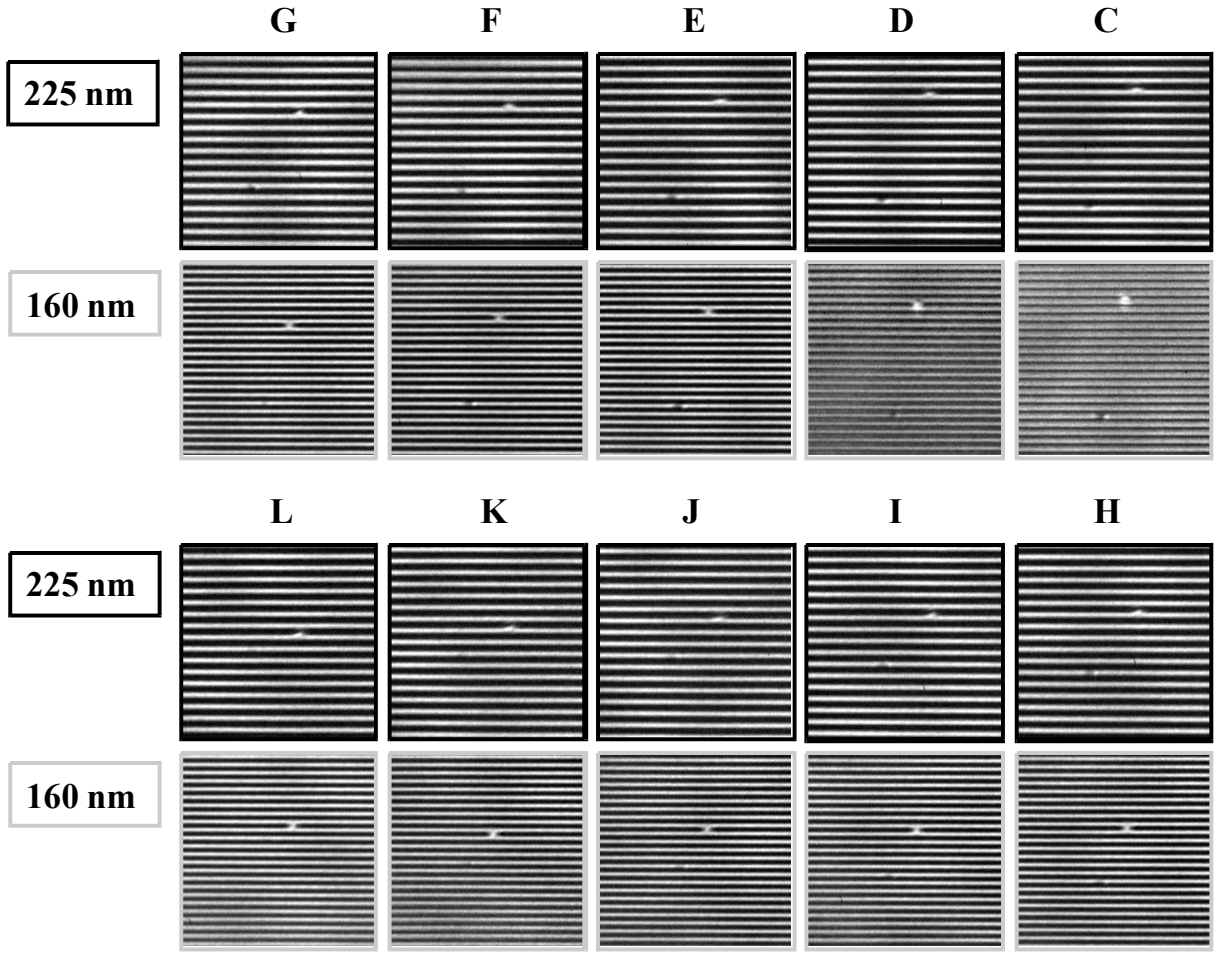

Figure 6: Actinic inspection tool images of the programmed embedded defect from each column. Upper row images are from 225 nm dense lines and lower row images from 160 nm dense lines. A white bridge or intrusion is an absorber layer pattern marker used for locating the nearby embedded defect. A programmed embedded defect can be seen below and to the left of the marker.

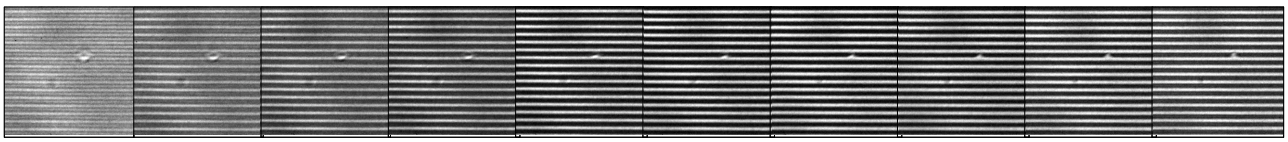

Figure 7: Column J defects in 225 nm dense lines with various focus offsets. Defect image contrast varies depending on focus, which also means that programmed embedded defects are well formed as phase defects.

4. DISCUSSION

Although we could not determine the printability of an embedded ML blank defect directly from the wafer printing results due to comparably large LWRs in the wafer pattern, we evaluated the effect of the programmed defects on the mask pattern aerial image with the AIT. We extracted aerial images from the image taken at actinic wavelength and estimated the effect of the programmed embedded defects on the mask pattern aerial image. We calculated CD variations caused by the embedded defects. □CD/CD values are plotted for 225 nm and 160 nm dense lines in Figure 8. CD variations in the 160 nm dense lines were usually larger than those in the 225 nm dense lines. It is reasonable to believe that the same defect size will affect smaller patterns to a greater extent. The defect proximity effect between

the line and space is known to be one of the strongest contributors to CD variation, but we could not measure the exact defect location in this test. The large fluctuation of CD variation values in Figure 8 may correspond to the exact defect location between the pattern line and space.

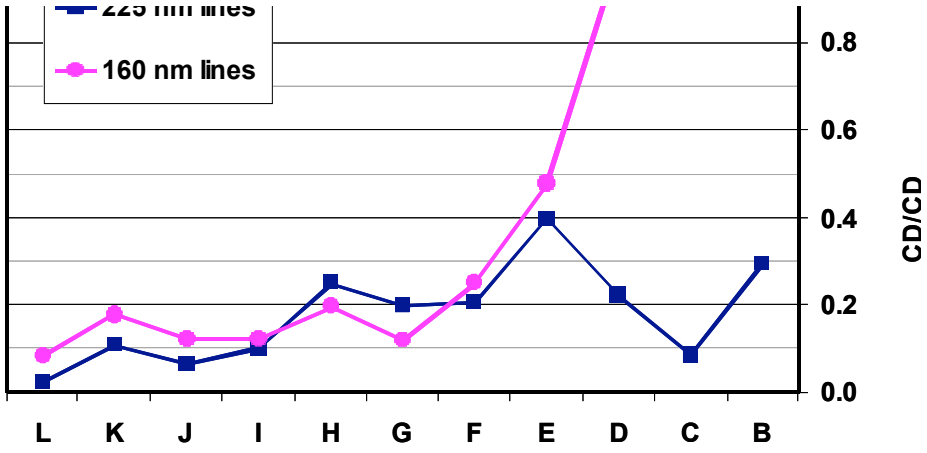

Figure 8: The CD variation caused by the embedded ML blank defects. CD/CD values are plotted showing that the CD variation in 160 nm dense line is usually larger than that for 225 nm lines.

If we agree that embedded ML defects adversely affect pattern CDs when the aerial image deformation exceeds 10% of its nominal value, then column H defects would be the smallest printed defects in the 225 nm dense patterns (56 nm on wafer) and the column K defects would be the smallest printed defects in the 160 nm dense patterns (40 nm on wafer). For the 32 nm HP node, we can estimate that a defect smaller than column K might affect the pattern on the wafer even though we were not able to prove it empirically in this experiment due to the resist process.

5. CONCLUSIONS

We fabricated a programmed embedded bump defect EUVL blank plate and inspected it with the Lasertec M7360. We also generated some test patterns on those programmed defects to compare the detectability of the M7360 and the printability of the embedded defects. The programmed defects had a well formed Gaussian shape ranging from 0.9 nm to 13.9 nm high. The current result of the Lasertec M7360 showed that it can detect defects down to column J, which is 28 nm in SEVD (3.5 nm high and 44.9 nm wide). We expect that the tool will have more capability after undergoing additional upgrades. The wafer printing result with the SEMATECH/Berkeley MET was not sufficient to evaluate defect printability because of a large LWR in the resist pattern. However, we estimated the defect printability using aerial images from the SEMATECH/Berkeley AIT. The results lead us to conclude that an embedded ML defect less than 1 nm high will affect the aerial image of 32 nm wafer patterns. Additional tests with an improved EUV resist should be run to verify this assertion. We summarize the detectability of the Lasertec M7360 and the printability of the embedded ML blank defects based on the AIT aerial image analysis in Figure 9. Solid lines represent the value based on the experimental data and simulated image contrast values at a 266 nm wavelength (M7360), while dashed lines show results of the simulations. The M7360 seems to have adequate capability for EUVL mask blank development at 45 nm HP node specifications. Even though there are incremental improvement possibilities with the M7360, a 3rd generation EUVL mask blank inspection tool will be required for HVM at the 32 nm HP node and beyond.

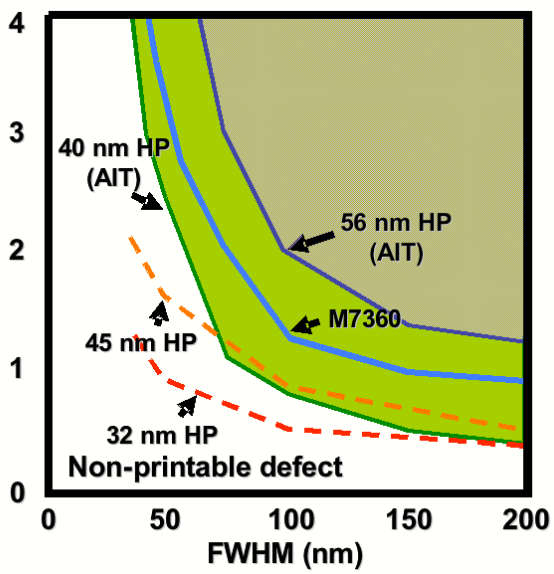

Figure 9: Summarized results of the EUVL mask blank defect printability compared with the detectability of the Lasertec M7360. Dashed lines represent the simulation results for 45 nm HP and 32 nm HP nodes.

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