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A Miniaturized mW Thermoelectric Generator For NW Objectives: Continuous, Autonomous, Reliable Power For Decades

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Abstract

We have built and tested a miniaturized, thermoelectric power source that can provide in excess of 450μW of power in a system size of 4.3cc, for a power density of 107μW/cc, which is denser than any system of this size previously reported. The system operates on 150mW of thermal input, which for this system was simulated with a resistive heater, but in application would be provided by a 0.4g source of ^{238}Pu located at the center of the device. Output power from this device, while optimized for efficiency, was not optimized for form of the power output, and so the maximum power was delivered at only 41mV. An upconverter to 2.7V was developed concurrently with the power source to bring the voltage up to a usable level for microelectronics.

Contents

Background

The development of small, efficient power sources for long duration has been a subject of active research for the past 40 years.[1] Small power systems that have been based on harvesting of chemical[2], thermal[3], optical[4], and mechanical[5] ambient energy have all been built and tested. Practical application of these devices has been limited by low conversion efficiencies and inefficient coupling to the harvested source. To overcome these limitations, systems that relied on nuclear fuel for hot side thermal energy were developed with significant efficiencies up to 8%. These systems were quite large, however, often in the 100cc to 1liter volumes, principally due to the thermal and radiation shielding needed to achieve high efficiency. Efforts to miniaturize these thermal harvesting systems, most notably for pacemaker implants[6], met with some success, but carried fuel loadings high enough to require significant shielding. Therefore, to significantly shrink the systems below these sizes, the size of the nuclear heat source must be reduced to reduce the radiation shielding requirements, and the heat capture efficiency must be increased to reduce the need for thermal insulation.

The goal for this research project was to develop a miniaturized (<1cc total system volume) thermoelectric generator capable of generating 1mW power from a 100mW radioisotopic source (either ^{238}Pu or ^{241}Am). Thermoelectric generators convert the heat flux associated with a temperature difference into electrical work. Dissimilar materials generate a voltage difference between a hot source and a cold sink. The voltage and power generated by such a device is a direct function of the temperature difference achieved, the thermal power available, and the efficiency of the converter device. To achieve good thermal gradients, the converter materials should have low thermal conductivity. For an efficient thermal converter, most of the heat flux must pass through the converter and not be lost to parasitic heat loss paths.

To achieve this, the program was developed along the lines of modeling and simulation to predict heat transfer, followed by fabrication to verify and refine the model. All testing with the thermoelectrics was done with a heat source simulant, a resistive heater, rather than with actual radioisotopes, due to the difficulty in working with such material on a tight time schedule. The heat from an isotopic source would be equivalent to the heat from a resistive source, with only the additional caveats of the radiation induced degradation of the

device in the actual isotopic source. The radiation effects on thermoelectric materials have been studied extensively in the literature, with no adverse effects until very high fluences were reported.

Initial literature investigations into the long-term effects of radiation on bismuth telluride revealed that little contemporary research was being performed on the subject outside of Russia and the former Soviet Union[7,8]. Due to the difficulty of obtaining these sources, they were not consulted for this work. Domestic research into the subject was largely performed in the 1960's, with the primary reference sources for our current effort stemming from this time[9,10].

The first work, by Kilp and Mitchell, evaluates the effects of thermal and fast neutrons on Bi_2Te_3 materials by exposing them to radiation from a test reactor. The total neutron dosage to the material was on the scale of ~10^{19} fast neutrons and ~10^{18} thermal neutrons (energies < 0.4 eV). As expected, material exposure to neutron radiation resulted in an increase in the electrical resistivity of the samples. The resistivity began to increase after exposure to an integrated flux of ~$0.2x10^{-19}$ neutrons. The Seebeck coefficient and thermal conductivity of the sample was not tested for the Bi_2Te_3 material, however it was the first indication that fairly large neutron fluxes were required to begin material degradation.

The second work, by Corelli and Frost, had a similar methodology to the first and also exposed Bi_2Te_3 materials to test reactor radiation. Typical neutron exposures for this effort were $1.5x10^{20}$ thermal neutrons/cm^2 (energies < 1MeV) and $1.6x10^{19}$ fast neutrons/cm^2. Unlike the prior work, cadmium was used to shield some of the tested materials from thermal neutrons in order to differentiate between the effects of differing neutron energies on the material properties. In general, those samples that were shielded from thermal neutrons had marginally less material degradation. The reported increase in the electrical resistivity was on the order of 1.2-5 times the pre-irradiated value. The Seebeck coefficient for Bi_2Te_3 was found to increase by 5-20% after exposure. A surprising note was the change from p-type Bi_2Te_3 to n-type after radiation exposure, further this change was found to be reversible after annealing. The authors of the study were not confident of an explanation for this observation, though they posited the trapping of charge carriers by Frenkel defects. This discussion notwithstanding, additional radiation testing on the

assembled prototypes using an external radiation source were pursued and reported below which simulated the effects of a 10 year operational life with a ^{238}Pu source in the device.

The project also had efforts to develop a thin film counterpart to the BiTe materials, to increase the number of layers of BiTe material used and thereby increase the operating voltage of the source. Concurrently, electronic means to upconvert the voltage from the device to a voltage sufficient to operating integrated circuits was undertaken. Both of these efforts are reported in subsequent sections. Since modeling was the thrust that first drove the design of the device, however, it will be discussed first.

Modeling and Simulation

We have developed a simple numerical model to predict the electrical and thermal performance of the mini-RTG. The goals of the modeling effort were (1) to predict performance metrics such as efficiency, power output, open-circuit and load voltages, heat source temperature, thermal gradients, etc… and (2) to evaluate and guide the design as the project progressed.

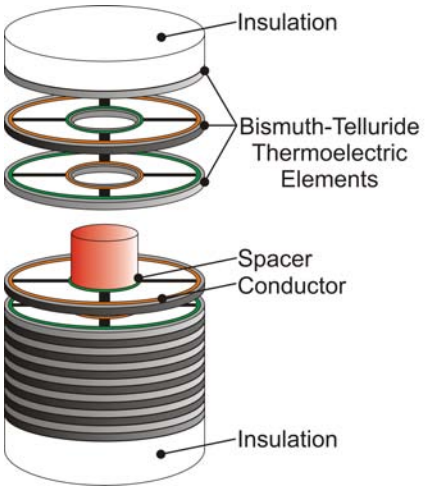

Figure 1: Exploded view of mini-RTG (device container not shown)

The model is a simple 1D approximation that couples the thermal and electrical behaviors through an iterative process. Thermoelectrical coupling is critical because heat transfer through TE circuits is not by conduction only. Thermal energy is also transported by Peltier, Joule, and Thompson heats that arise when current flows through a TE material. As a result, the thermal and electrical characteristics of the device are not independent and must be solved simultaneously. Although commercial FEM multi-physics packages, such as ANSYS, are capable of solving 3D TE problems, we chose a 1D approach to facilitate simple geometric permutations and to provide insight through examination of the governing equations of the system.

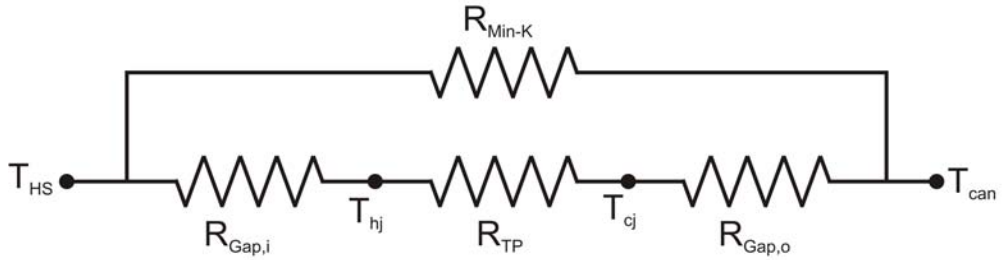

Figure 2: General thermal resistance network

Figure 1 shows an exploded view of the spoked TE elements surrounding the heat source along with the Kapton spacers, gold plated copper conductors, and Min-K end caps. All of the free space between the TE element and within the pockets created by the spokes is occupied by ambient air. The stainless device container is not shown.

The first step in developing the model was to discretize the actual geometry, shown in figure 1, into a network of thermal resistances. In general, the thermal resistance network is described in Figure 2 where $R_{Gap,i}$ is the gas gap and contact resistance between the heat source and thermopile, $R_{Gap,o}$ is the gas gap and contact resistance between the thermopile and container, R_{Min-K} is a parallel combination of the two Min-K end caps, R_{TP} is the thermopile, and T_{HS} and T_{Can} are the temperatures of the heat source and outer stainless container respectively. T_{hj} and T_{cj} are the temperatures at the hot and cold junctions of the thermopile.

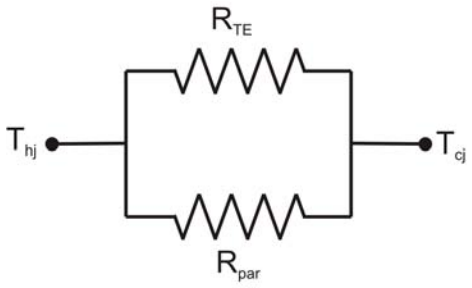

Figure 3: Thermal resistance network of the thermopile

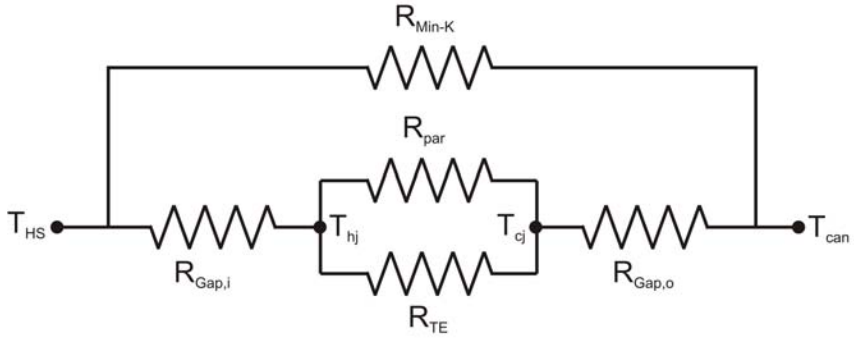

Figure 4: Total thermal resistance network

R_{TP} can be further descretized, as shown in Figure 3, where R_{TE} is the thermal resistance of the TE spokes, and R_{par} accounts for all parasitic conductive losses that bypass the TE spokes i.e. the gas/Kapton/Cu layer between TE elements, the gas pocket between spokes for each TE element, and the TE material at the inner and outer support rings that is not part of the spoke.

Substituting Figure 3 into Figure 2 gives the total 1D thermal resistance network in simplified form as shown in Figure 4. This formulation reasonably neglects all radiative and convective losses due to the low temperature gradients and small confined spaces within the mini-RTG.

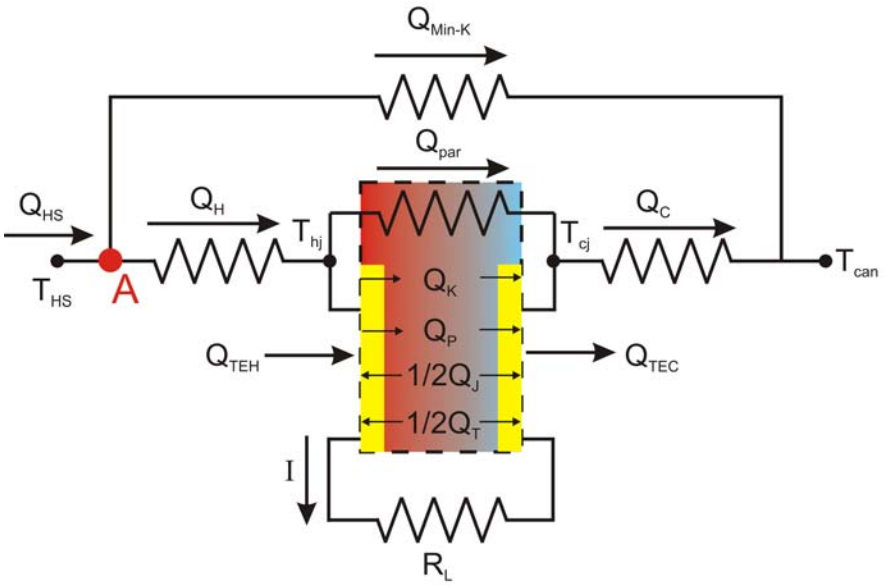

Figure 5: Heat flow for mini-RTG

Figure 5 show heat flowing through the various thermal resistors along with heat flowing due to thermoelectric effects within the TE material, where Q_K is conduction through the TE material, Q_P is Peltier heat, Q_J is Joule heat, and Q_T is Thompson heat. A steady-state energy balance at location A yields the relationship between heat generated by the heat source Q_{HS} and heat flowing through the thermopile Q_H and insulation $Q_{Min\text{-}K}$.

(1) $Q_{HS} = Q_H + Q_{Min\text{-}K}$

Similarly, a steady-state energy balance around the thermopile, defined by the dashed box, shows that the difference between heat entering the thermopile, Q_H, and exiting, Q_C, is equal to the power generated, IV_L, by the TE elements.

(2) $IV_L = Q_H - Q_C$

The power generated by the thermopile can also be expressed as the difference between the thermoelectric heats at the hot, Q_{TEH}, and cold, Q_{TEC}, junctions of the thermopile.

(3) $IV_L = Q_{TEH} - Q_{TEC}$

An energy balance of the thermoelectric heating within the yellow boxes in figure 5 gives the following expressions where Q_{CRH} and Q_{CRC} are the heats generated by current flowing through the electrical contact resistance at the hot and cold junctions, Q_J is Joule heating, Q_T is Thompson heating, and Q_{PH} and Q_{PC} are the Peltier heats at the hot and cold junctions.

(4) $Q_{TEH} = Q_{PH} - Q_{CRH} - \frac{1}{2}Q_J - \frac{1}{2}Q_T$

(5) $Q_{TEC} = Q_{PC} - Q_{CRC} - \frac{1}{2}Q_J - \frac{1}{2}Q_T$

Additionally, an energy balance at the hot and cold junctions yields the following alternative expressions for the thermoelectric heats.

(6) $Q_{TEH} = Q_H - Q_K - Q_{par}$

(7) $Q_{TEC} = Q_C - Q_K - Q_{par}$

The Peltier heats at the hot and cold junctions are given by the following equations where, N_C is the number of thermocouples, I is the current flowing through the TE material, α_H and α_C are the Seebeck coefficients at the hot and cold junctions, and T_H and T_C are is the junction temperatures.

(8) $Q_{PH} = N_C I \alpha_H T_H$

(9) $Q_{PC} = N_C I \alpha_C T_C$

The heats associated with current flowing though the electrical contacts and interconnects are given by the following equations where R_{CH} and R_{CC} are the electrical resistance per contact at the hot and cold junctions.

(10) $Q_{CRH} = N_C I^2 R_{CH}$

(11) $Q_{CRC} = N_C I^2 R_{CC}$

The Joule and Thompson heats are given by the following equations where R_{TE} is the electrical resistance of the TE material and V_P is the thermopile voltage.

(12) $Q_J = I^2 R_{TE}$

(13) $Q_T = N_C I(\alpha_H T_H - \alpha_C T_C) + \frac{1}{2} I V_P$

The current flowing through the thermopile can be defined by the following equation where R_L is the load resistance and V_L is the load voltage.

(14) $I = (V_P - V_L)/R_P$

V_P is then eliminated from equation (13) using (14) and equations (8-13) are substituted into (4) and (5) resulting in the following expressions for Q_{TEH} and Q_{TEC}:

(15) $Q_{TEH} = \frac{1}{2} N_C I(\alpha_H T_H + \alpha_C T_C) + \frac{1}{2} I V_L + \frac{1}{2} N_C I^2 (R_{CC} - R_{CH})$

(16) $Q_{TEC} = \frac{1}{2} N_C I(\alpha_H T_H + \alpha_C T_C) - \frac{1}{2} I V_L + \frac{1}{2} N_C I^2 (R_{CC} - R_{CH})$

At this point, the thermoelectrical coupling of this system is evident and the thermoelectric heats must now be coupled to the heat flowing from the heat source. The heat flowing into the thermopile, Q_H, can now be expressed as the heat flowing though the thermal resistance between the heat source and thermopile.

(17) $Q_H = 1/R_{Gap,i} (T_{HS} - T_{hj})$

The heat flowing through the thermopile by conduction, Q_K, is defined as follows:

(18) $Q_K = 1/R_{TP} (T_{hj} - T_{cj})$

Heat rejected by the thermopile, Q_C, is expressed as heat flowing through the thermal resistance between the thermopile and stainless steel container. The thermal resistance of the container is neglected and is assumed to be at the ambient temperature T_{amb}.

(19) $$Q_C = 1/R_{Gap,o} (T_{cj} - T_{amb})$$

An expression describing the temperature of the heat source, T_{HS}, can now be derived from the preceding equations. Solving equation (18) for T_{hj} and (19) for T_{cj}, substituting both expressions into equation (17), and solving for T_{HS} gives the following relationship:

(20) $$T_{HS} = Q_H R_{Gap,i} + Q_K R_{TP} + Q_C R_{Gap,o} + T_{amb}$$

Solving equation (6) for Q_K and substituting into equations (7) and (20) gives the following expressions:

(21) $$Q_{TEC} = Q_C - Q_H + Q_{TEH}$$

(22) $$T_{HS} = Q_H R_{Gap,i} + Q_H R_{TP} - Q_{TEH} R_{TP} - Q_{par} R_{TP} + Q_C R_{Gap,o} + T_{amb}$$

Equation (21) is then solved for Q_C and substituted into equation (22). Simplifying the result gives an expression for T_{HS} that is dependent on both thermal and electrical phenomena.

(23) $$T_{HS} = Q_H (R_{Gap,i} + R_{TP} R_{Gap,o}) - Q_{TEH} (R_{TP} + R_{Gap,o}) + Q_{TEC} R_{Gap,o} - Q_{par} R_{TP} + T_{amb}$$

With this set of equations established, we now describe the numerical procedure used to solve for the thermal and electrical performance the open and closed circuit condition. The open circuit solution will not be discussed since it is simply a matter of solving the 1D resistance network for the temperature nodes and calculating V_{oc} using the equation (24).

(24) $$V_p = N_C \int_{T_{cj}}^{T_{hj}} (\alpha_p - \alpha_n) dT$$

Closed-Circuit Solution Procedure:

Solve for V_{oc} as described above

Guess the load voltage $V_{load} = V_{oc}$

Guess the current flow

$I = V_{oc}/(R_{pile} + R_{load})$ if using a matched load

$I = (V_{oc}-V_{reg})/R_{pile}$ if using a regulated voltage

Guess a value for $T_{HS} = T_{amb} + 10K$ (T_{amb} is assumed to be known)

Check convergence $T_{HS} - T_{iter} < .0001K$

Initial guess for $T_{iter} = T_{amb}$

Calculate Q_{Min-K}

Calculate Q_H using equation (1)

Calculate Q_C using equation (2)

Use current previous iteration or initial guess if first iteration

Use V_{load} from previous iteration or initial guess if first iteration

Calculate the hot and cold junction temperatures

$T_{hj} = T_{HS} - Q_H R_{Gap,i}$

$T_{cj} = T_{amb} + Q_C R_{Gap,o}$

Calculate V_p using equation (24)

Calculate load voltage

$V_{load} = IR_{pile}$ if using a matched load

$V_{load} = V_{reg}$ if using a regulated voltage

Calculate the thermoelectric heats using equations (15) and (16)

Calculate electrical power generation using equation (3)

Perform check using IV_{load}

Calculate new T_{HS} using equation (23)

Calculate new current flow

$I = V_{oc}/(R_{pile} + R_{load})$ if using a matched load

$I = (V_{oc}-V_{reg})/R_{pile}$ if using a regulated voltage

Return to step 5 and repeat until convergence criteria is met

The solution contains all necessary information for determining heat flow, thermal gradients, electrical performance, efficiency, and power density.

Fabrication and Performance:

The fabrication of the micro thermoelectric generator underwent large design changes from the original design that was proposed at the start of the project. The first generation device, which was proposed based upon previous work in thermoelectric microscale devices, involved the use of lithographic techniques to pattern the thermoelectric n and p legs of the device over a thin silicon nitride membrane. The membrane was subsequently released in a potassium hydroxide (KOH) solution after protecting the thermoelectric legs with a polymeric coating. The electrical layout of this device was an arrangement of junctions that terminated on the periphery of the device, with a released silicon nitride membrane supporting the center terminations of the couples.

The first materials used in fabrication of the thermoelectric junctions were sputtered metal layers of chromel and constantan for the couples. This sputtered material was to be replaced by sputtered bismuth telluride (BiTe) layers once the process for low stress, high quality BiTe was developed in another part of this project. Realizing the sputtered BiTe materials proved difficult, however, and combined with the issues of heat flow in this design, caused a fundamental shift in the design and fabrication of the device.

It was thought that this arrangement would allow for heat from a source at the center of the device to flow radially through the legs and be rejected into the silicon periphery frame supporting the silicon nitride membrane. Modeling and subsequent testing showed that the heat flux would not flow down the legs of the thermocouples, and instead radiative loss through the top and bottom surfaces of the silicon nitride membrane would dominate. With no heat moving down the legs, the temperature of the center of the membrane did not go above ambient, and no power was generated from this device.

Realization of the issues of heat loss from the top and bottom of the membrane, coupled with difficulties in realizing a thin sputtered film of BiTe materials caused a re-evaluation of the design of the device. Bismuth telluride couples were far superior in performance to chrome constantan at the relatively low temperature gradients expected for the device, and so means of procuring and processing bulk specimens of this material were found. Since the heat flux needed to be down the legs of the thermoelectric devices, anywhere that was

not thermoelectric legs needed to be well insulated thermally. Since thermal insulation consumed system volume with only minor improvements to performance, we realized that, below a certain system size, that the traditional thermoelectric design where the thermocouples are all parallel to one another, and good thermal insulation forces the heat to move down the legs would not be inefficient and consume tremendous volume for a small device. Instead, a radial arrangement, similar to what was suggested for the silicon based device, could capture the majority of the radiated heat from the source and force the heat down the thermoelectric legs.

Another realization of the first device was that, in addition to the need for using bismuth telluride to maximize the voltage generated at low thermal gradient, that there were no means to pattern the bismuth telluride into the pattern needed for the device. To fabricate the wagon wheels in BiTe, substrates of hot pressed polycrystalline BiTe were cut from a boule. These rough cut substrates were ground down to approximately 8 mils (200 μm) thick, and then were mechanically machined using continuous wire electrical discharge milling (EDM). Because of the semiconductor nature of the n BiTe and, more importantly, the p type BiTe materials, a very low EDM rate, on the order of only 10 mils/minute (250μm/min) was used to cut the structures.

In the case of the radial design, modeling indicated that only a minimal number of legs could be used. If too many legs connected the hot center of the device to the cold side, the heat flux would be high enough to keep the hot side temperature too low to be useful. If, however, too few couples were used, there would not be enough couples to build up sufficient voltage. As a design compromise, a total of 4 radial legs, arranged like spokes on a wheel, were used. These legs were initiated and terminated on a circular structural support. The whole of the assembly has the appearance of a wagon wheel, with each of the legs acting as a spoke, and the inner and outer hubs providing connection between the legs. Since each wheel structure is monolithically made from a single material, the change from p to n type material is accomplished by stacking opposing materials up around a central shaft.

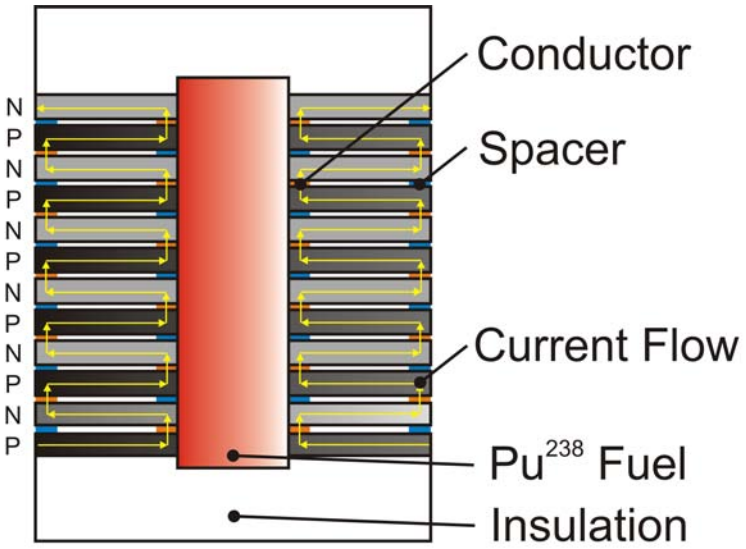

Figure 6: Schematic layout of the electrical connections between layers in the stacked RTG.

Electrical connections between layers were made using opposing gold coated copper rings and insulating rings of Kapton. This method forces the generated current down the legs of the device, and connects each stack pair serially from top to bottom. A schematic cross section of this device is shown in Figure 6. In the second prototype, unmodified BiTe materials were pressed directly against the gold coated copper rings. This was found to be a higher resistance than was acceptable, and so the contacting surfaces (the inner and outer ring of the wheels) were sputtered clean for 10 minutes using an in-situ Kaufmann source prior to sputtering a 1 µm thick gold layer. This coating reduced the internal resistance of the assembled system to less than one ohm.

Figure 7: The first radial design

For the second revision device, a total of 22 individual p and n type layers, stacked up with interleaved gold coated copper and Kapton spacers. For this design, the width of the thermoelectric legs was left at 1mm, allowing for significant structural robustness, but at a cost of increased heat flux from the central hot side source to the cold side external sheath. The external structure was fabricated in polycarbonate, and was an open structure, to allow tabs connecting the top and bottom thermoelectrics to be accessed from the side of the device. The test volume of this second device was approximately 8cc, but much of this volume was wasted, and was removed in the next revision. A source simulant, in this case a thermal surface mount resistor encased in a stainless steel container and packed with thermally conductive material, was used in place of the radioactive material. Current was passed through the resistor at the appropriate

rate to dissipate the same power that would be generated from a radioisotopic source of the same size as the outer stainless steel casing, inclusive of the volume of the casing itself. A picture of this device is shown in Figure 7.

This device was the first to produce power, but the power output of the device was minimal, with only 10mW produced from the device for 150mW input power, for a conversion efficiency of only 0.007%. Since the upper and lower faces of the thermoelectric stack were in contact with the polycarbonate, and although polycarbonate has a reasonably low thermal conductivity (0.2 W/m-K), modeling quickly showed that the significant fraction of the heat generated in the source was still escaping through the end faces of the device, rather than in the radial direction. In order to improve the efficiency of the device, the top and bottom faces needed to be well insulated thermally.

Removal of heat loss from the top and the bottom of the stack was accomplished with a 5mm thick layer of aerogel material (thermal conductivity: 27mW/m-K) on the top and bottom faces of the device. The disks of aerogel were precut and inserted into a redesigned, smaller volume (4.3cc) outer casing. The simulant heat source and the thermoelectric washers were then stacked up on the top of the aerogel disk to the final height. Lastly, a top layer of aerogel, with the electrical leads from the thermal simulant source threaded through the center of the disk, was inserted on top of the simulant and thermoelectric stack. A threaded cap and compression cone was added on top of this, and the stack was compressed until the electrical resistivity of the stack was reduced to approximately an ohm, indicating good electrical connection between the various layers of the stack. A picture of the completed third generation device is included in Figure 8. In this figure, the gold radial tabs that contact the top and bottom layer of the

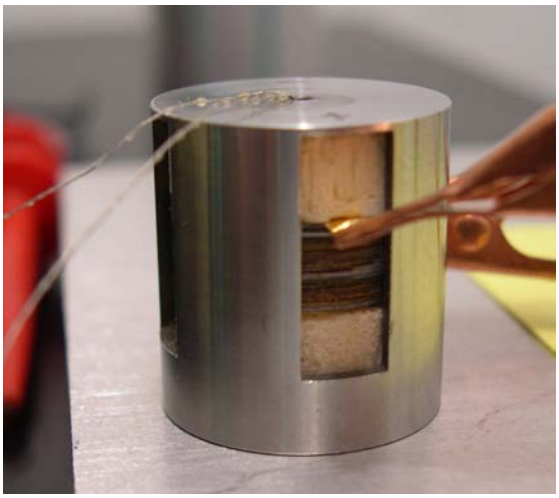

Figure 8: v3 prototype, showing aerogel insulation above and below the TE stack. Electrical leads to the heater exit from the top of the device.

thermoelectric stack, the leads to the electrical heat source, and the top and bottom aerogel insulation can be clearly seen.

This device performed quite well, with 338µW of power being generated in 4.3cc under an external matched load of ~1 ohm, or 78µW/cc, which was higher than any small radioisotopic source reported in the literature.[11] This performance represents a thermal to electrical conversion efficiency of 0.23%. Power performance vs. voltage for this device is shown in Figure 9. Lifetime for this device was also measured, with the device showing less than 1% loss in power over a test time of 80 days. Most of this loss is speculated to be change in the output heat of the simulant source over time, as the resistor degrades and increases its resistance, lowering the overall thermal power output of this source. At the end of this 80 days of testing, the equivalent energy density of the device (measured in watts of power produced for a given number of hours in a given volume) was 151 W-hr/l, approximately equivalent to the energy density of an alkaline battery. If this test was extended to the one year mark, the energy density would be approximately 700 W-hr/l, approximately equal in energy density to the best primary batteries available currently (that can operate on this timescale). At 10 years of life, the approximate equivalent energy density would be 6500 W-hr/l, an order of magnitude more dense than the best battery.

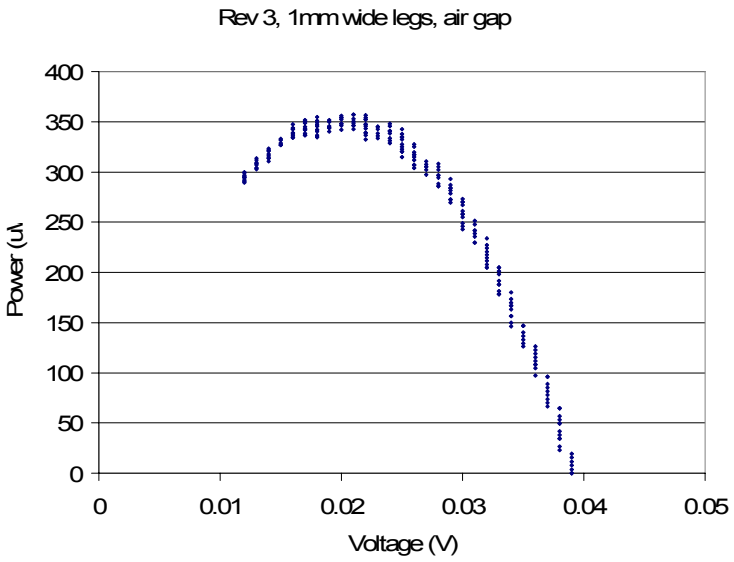

Figure 9: Power/voltage curve for the rev 3 RTG. Maximum power is delivered at 21mV and 338µW.

One of the major remaining problems with this device, however, was the loaded voltage at which the device was delivering this power. For the third revision device, the load voltage was only 21mV, well below the needed voltage for operation of any useful electronics. Since the device consisted of 4 sets of thermoelectric legs that were connected in parallel (increasing the current of the device, but not the voltage), the next revision to the device was to separate each of these legs from the hubs and reconnect them serially, thereby quadrupling the voltage, and quartering the current. Under this configuration, the device would deliver 80mV under load, which would still be too low for most devices.. Consequently an effort in low power, low voltage upconversion was taken on in the second year of the project. The results of this effort are discussed in another section of this report. A picture of the quartered thermoelectric elements is shown in Figure 10, prior to their assembly into the device. The development of this device was halted prior to assembly of these quartered materials into a functional device for test.

Figure 10: TE stack after quartering to change from parallel to serial electrical connection. This increases the output voltage by 4, and decreases the output current by 4.

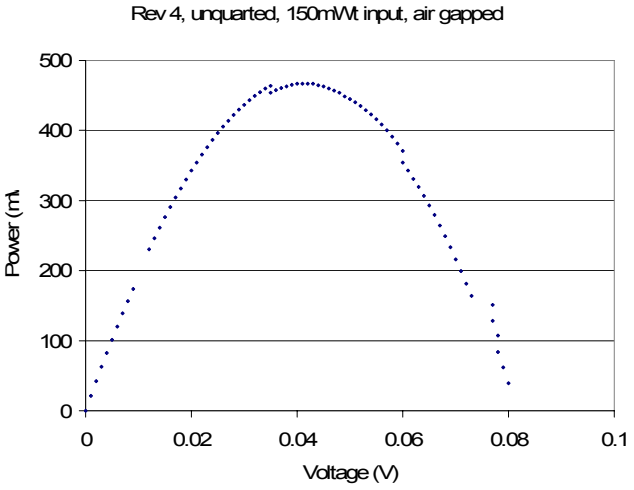

Figure 11: Power curve of v4 device, showing ~450µW power output at 40mV.

The final version of this device was constructed along the same lines, with a change in the width of the legs from 1mm to 0.5mm in width (which decreased the thermal heat flow down the legs by 50%, resulting in an increase in hot side temperature and resultant increase in potential under load). Testing of these elements in the assembly described above resulted in an increase in power from 338µW to 426µW (see the power curve in Figure 11, approximately 100µW below the expected

performance for this device. Simulations of this last assembly indicated that the most likely place for this loss of power was in inefficient heat coupling between the hot side of the thermoelectric legs and the heat source itself. Operating voltage was increased from 21mV to 40mV, however, indicating that the expected rejection of some of the heat flux out through the legs was achieved.

The final (unrealized) configuration of the device would be a quartered set of elements, serially wired, with 0.5mm wide legs. These would be assembled around a simulant heat source with good thermal contact between the heat source and the hot side of the elements. If the operating environment could also be changed from ambient air to 40 Torr of Xe gas, the simulations indicate that such a configuration would be capable of reaching close to 2mW of power with a load operating voltage of 250mV. Under these conditions, the efficiency of the upconverter could reach 3V with a 70% efficiency, resulting in a final delivered power of 1.4mW in 4.3cc at 3V under load, with a total power density of 230μW/cc.

Radiation Testing

While literature indicated that high fluences of neutrons could cause material degradation to the thermoelectrics, the radiation level of these studies was relatively high compared to the expected dose from our source. Our ^{238}Pu oxide source, of approximate mass of 0.33 grams, was expected to emit ~1417 neutrons/sec. This would result in a total 10-year neutron dose of ~4.47×10^{11}, with a 2 MeV average energy and a Maxwellian distribution peak at 0.7 MeV. To verify generator performance, the decision was made to expose the Bi_2Te_3 materials to at least a 10-year radiation dose to determine the resulting level of material degradation.

Sandia National Laboratories has several facilities designed for radiation testing of systems and materials. One such facility possesses a ^{252}Cf source which was decided to be appropriate for testing. The fission neutrons for ^{252}Cf have a broad energy spectrum peaked at ~1.5 MeV, but extending up to 13 MeV. This source was NIST calibrated in a report on 2/19/93 to emit 2.24×10^7 neutrons/sec. Using the reported ^{252}Cf decay half-life of 2.638 years, it was calculated that the neutron emission rate at the time of testing was approximately 3% of the calibrated rate, or 6.62×10^5 neutrons/sec. This would require a total generator exposure of 7.8 days to reach an effective 10-year radiation dose.

Scheduling the testing facilities for such a long time would disruptive to operations, and so the decision was made to co-locate the generator with the ^{252}Cf source in its storage tube. The source's storage tube consists of a brass tube, sheathed in lexan and steel, that has been sunk into the ground to provide for safe, long-term storage. Once placed in the storage tube, the generator would be directly next to the neutron source. One unaccounted for result of this test setup is an increase in the generator's exposure to moderated neutrons.

A traditional radiation exposure is done in a large open air room on a test apparatus that is suspended over a large sunken pit. The reason for this is that neutron interaction with solid matter surrounding the test setup may redirect the neutrons, resulting in a greater neutron flux and a larger dispersion of energies incident on the test material. In the setup that we used, the solid matter surrounding the source is maximized in order to minimize radiation exposure to the surrounding environment; as such the generator was exposed to a high level of moderated neutrons that could not be accounted for in our studies. The total radiation exposure of the generator lasted for 10.8 days, exposing the generator to at least $4.92x10^{10}$ neutrons/steradian, or the equivalent of a 13.8 year dose from a ^{238}Pu oxide source.

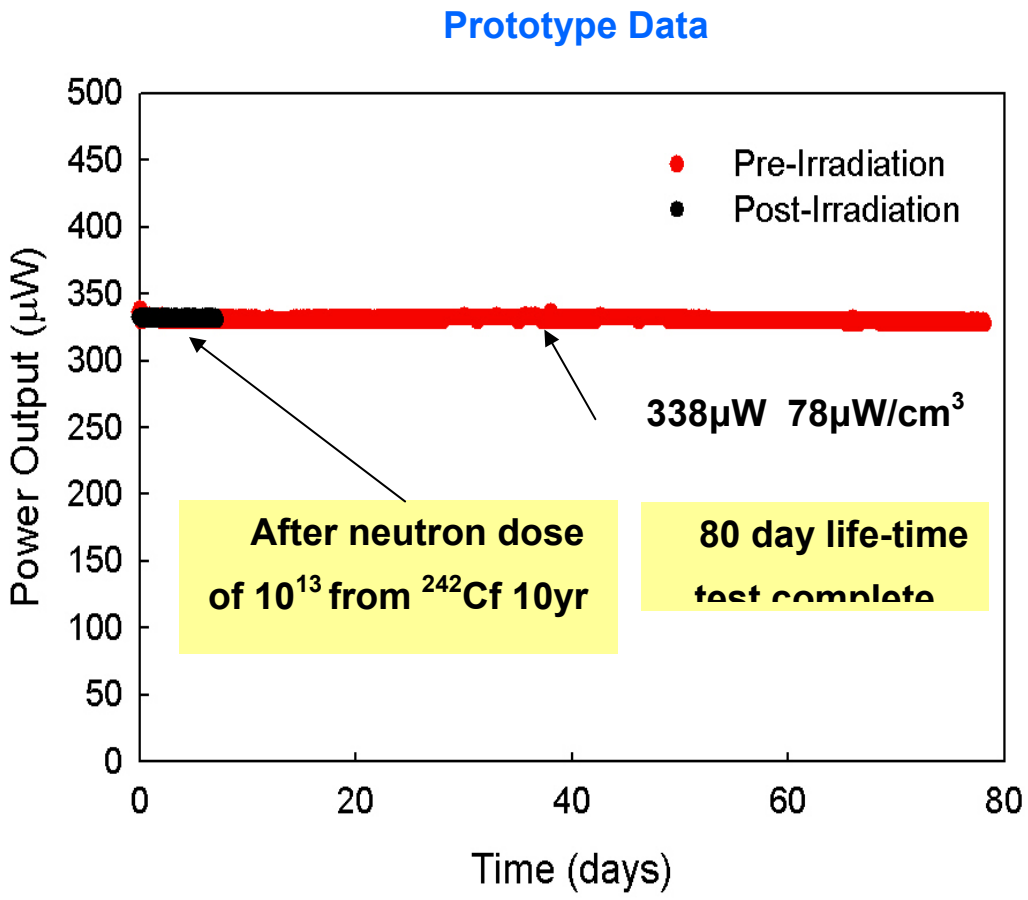

Figure 12: Lifetime data prior to (red) and after (black) 1E13 neutron dose (equivalent to 10 years) of ^{252}Cf.

After exposure to neutron radiation, the generator was removed from the source storage site, and was checked within the same day by a radiation technician. At the time of measurement neither the generator nor its stainless steel can produced radiation in excess of the background level. This indicated that neither the stainless steel nor the thermoelectric materials underwent activation during the test.

Once returned to the lab, the generator was tested for performance degradation. Figure 12 shows a graph of power output vs. time before exposure and after the radiation exposure. Although the test after exposure was not run to the 80 day mark, initial indications were the material was identical after neutron radiation exposure.

Recall, however, that this performance was achieved at very low voltages, below those necessary to support operation of most microelectronics. A means of increasing the voltage of the system was needed, and was pursued along two independent paths. The first

was a materials method, where depositing thin films of BiTe material on Kapton would allow for the stacking of many more layers. Increased number of layers equated to increased numbers of junctions, which would allow for a higher voltage operation (at reduced current, due to the higher series resistance of the circuit). The other method involved a direct, low voltage electronics upconversion system that would be applied directly to the low voltage output of the generator. Both of these systems are discussed in the next sections.

Film Growth and Microstructure

Although previous work on thin film depositions of BiTe materials has been reported in the literature[12 13], none have reported thick (20μm) thick films, which was the target for this application. We began work with a sputter target with nominal composition of Bi_2Te_3. Since the application would ultimately require thicknesses ~ 20 μm, considerable effort was spent reducing the residual stress of the sputter-deposited films by controlling the rf sputter power and the Ar pressure used during deposition. This is critically important to prevent spallation of thick films off the substrate. Conditions were successfully identified for negligible stress and most experiments were performed on films > 4 μm thick, which based on the information from the literature above, far and away represent the thickest

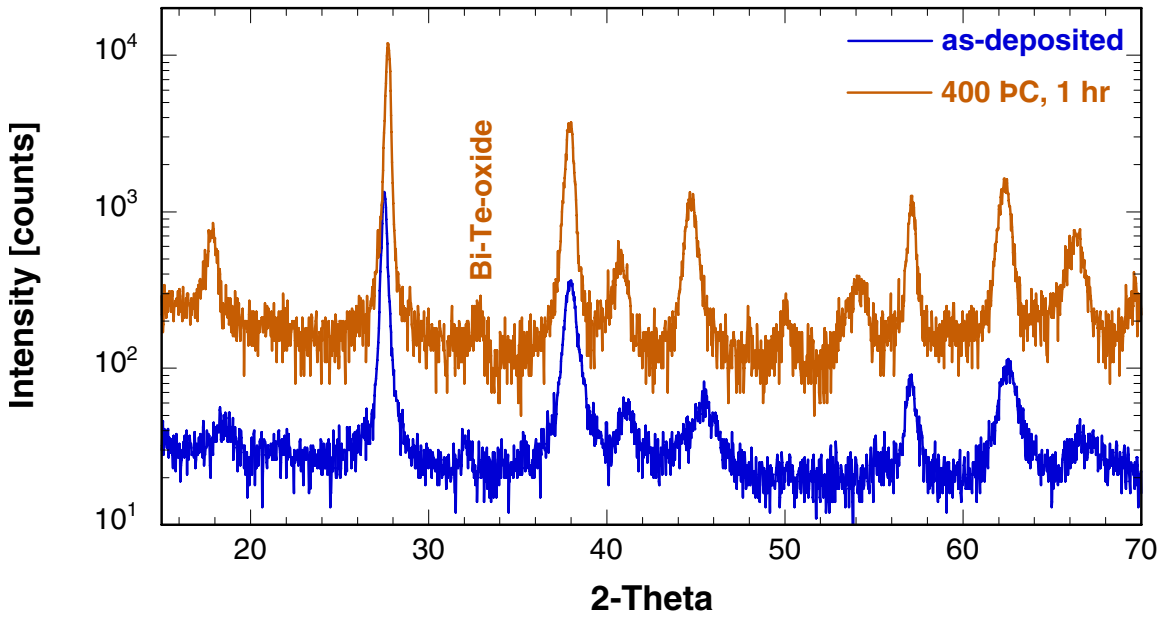

Figure 13: XRD of Bi2Te3 films on kapton as-deposited near room temperature and following 1 hour at 400 ˚C in forming gas.

BiTe films grown and studied. RBS measurements showed that our nominal target composition used under these conditions yielded films with composition Bi(36)Te(64), which is slightly Bi-rich and therefore should be somewhat n-type.

We performed annealing studies of these films deposited onto Kapton using x-ray diffraction (XRD) to identify crystalline phase formation. Anneals were for temperatures up to 400 ˚C for one hour in forming gas. In this range, the only identifiable phase is Bi_2Te_3. Figure 13 plots the XRD spectra for 6 µm thick films both as-deposited and following the 400 ˚C anneal. Many of the Bi_2Te_3 diffraction peaks are present in the as-grown sample, which barely reaches 50 ˚C during rf sputter deposition. As expected, these peaks grow somewhat in size with increasing temperature. In addition, the rest of the peaks also are detectable with 400 ˚C annealing. These diffraction spectra prove that these Bi_2Te_3 are polycrystalline with no preferred orientations. Finally, note the presence of a small peak near 32.6˚ that begins to appear in the annealed sample. This peak correlates with the presence of some BiTeO phase. Oxide phases will have a deleterious effect on thermopower and electrical conductivity.

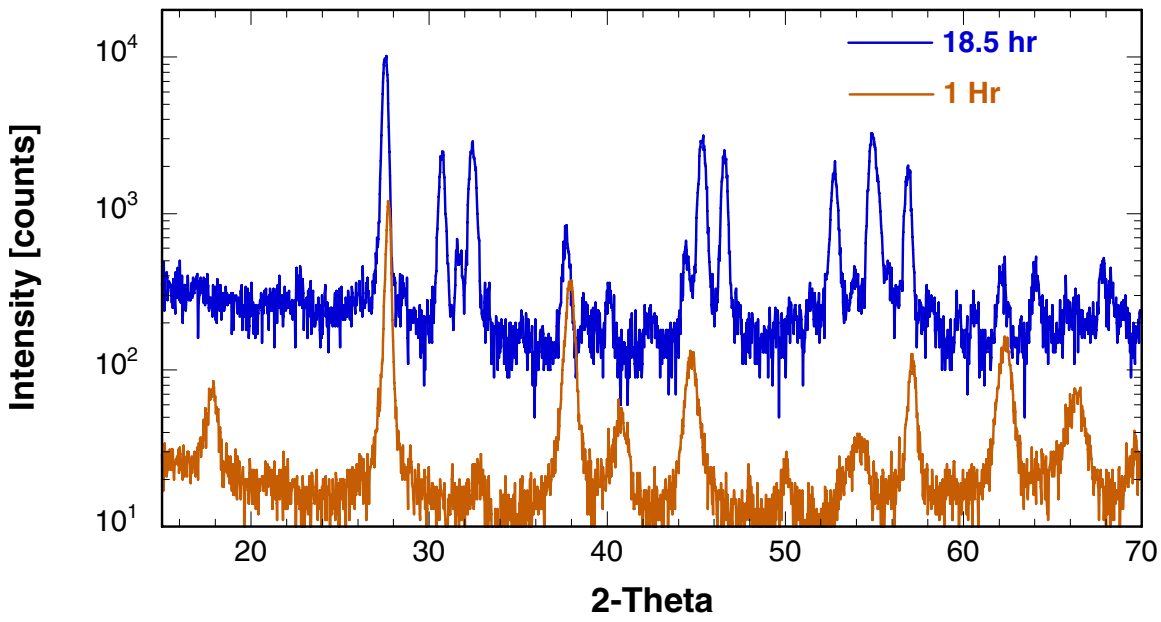

Figure 14: XRD of Bi2Te3 films on Kapton following anneals at 400 ˚C in forming gas for 1 and 18.5 hours.

To further explore the nature of the oxide formation, we annealed another sample at 400 ˚C for 18.5 hours (overnight), also in forming gas. The 1 and 18.5 hour anneals are directly compared in Figure 14. Many of the Bi_2Te_3 peaks are now smaller in size, and many new BiTe-oxide peaks now are present. Clearly, much of the film has oxidized.

Since these anneals are performed in forming gas, the question arises: where does the oxygen come from? The only source of oxygen in the furnace during these anneals is from the kapton substrate itself. We hypothesize that kapton degradation occurs at these temperatures and that all thermal crystallization anneals have to be done at temperatures < 400 ˚C.

To test this, we performed a series of anneals on pure Kapton alone, without a film present. The substrates, usually either 1 or 3 mil thick (~ 25 or 75 µm), lay flat on the furnace sample holder. However, even for temperatures above 200 ˚C, the ends of the substrate tape would begin to curl up, suggesting the presence of stress. Since there was no film on top of the substrates, this could only come about by changes in the kapton itself, most likely degradation.

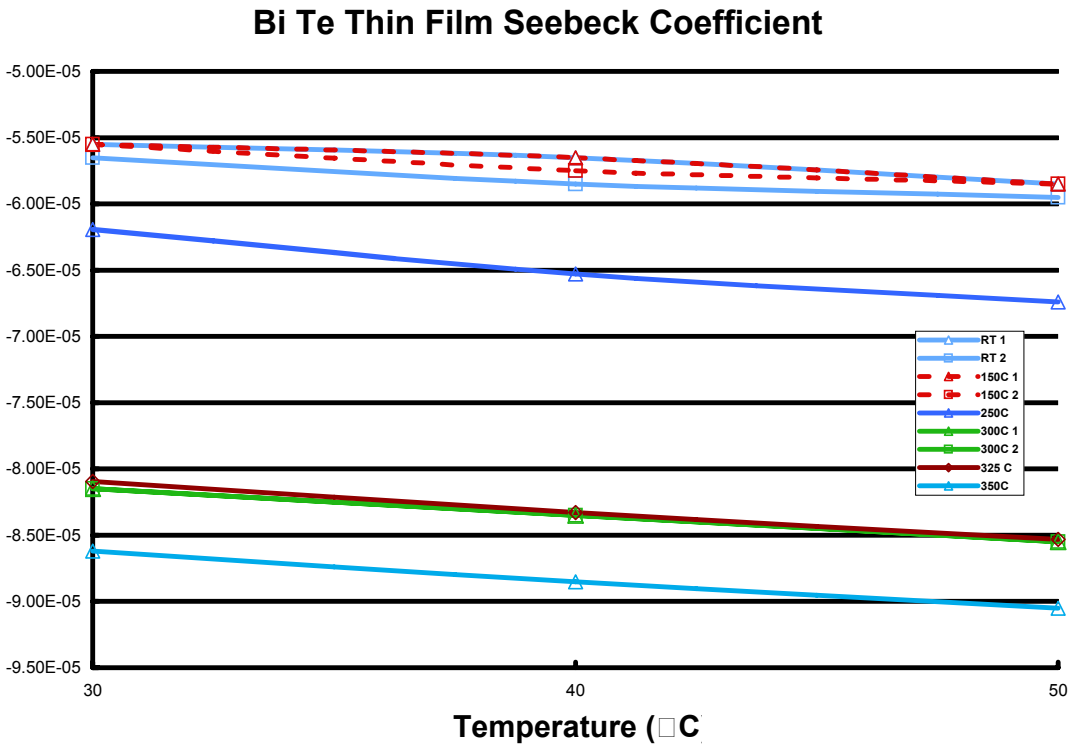

Figure 15 Seebeck coefficient for 6 µm thick Bi(36)Te(64) films grown on Kapton and annealed to various temperatures. The y axis is in units of ohm-cm.

This experiment was followed by a few anneals with 6 µm thick Bi_2Te_3 films on the kapton surface. A repeat of the 400 ˚C, 1 hour anneal described above resulted in a weight loss of 0.3% from a 1 mil thick kapton substrate. In addition, observation of the sample inside the furnace while at high temperature showed the tape to be curved concave up with respect to the film. However, after the sample cooled to room-temperature, the tape curved almost equally in the opposite direction. These changes in curvature note the large differences that must exist in the thermal coefficients of expansion between kapton and Bi_2Te_3. Clearly, between stresses induced by thermal expansion differences, and degradation of kapton due to high temperatures, which in turn apparently leads to the generation of oxygen that loads into the film, temperatures near 400 ˚C cannot be used for the crystallization of Bi_2Te_3 films on kapton.

Additional annealing studies were performed for Bi_2Te_3 films on kapton at 200 – 250 ˚C. Even at only 200 ˚C for two hours resulted in causing the kapton to measurably curl and lose mass. Ultimately, the conclusion of the annealing studies of Bi_2Te_3 films on kapton is that temperatures cannot really be raised to sufficiently crystallize the films without causing degradation of the substrate. Furthermore, such kapton degradation releases oxygen that essentially poisons the thermoelectric properties of the films.

Seebeck coefficient measurements show that these Te-rich films are indeed n-type conductors. Figure 15 shows the Seebeck coefficients as a function of temperature for films annealed at temperatures ranging from room-temperature to 350 ˚C. All the films show a similar functionality with temperature, with the Seebeck coefficients slightly increasing with increasing temperature. In general, the Seebeck coefficient increased with increasing annealing temperature.

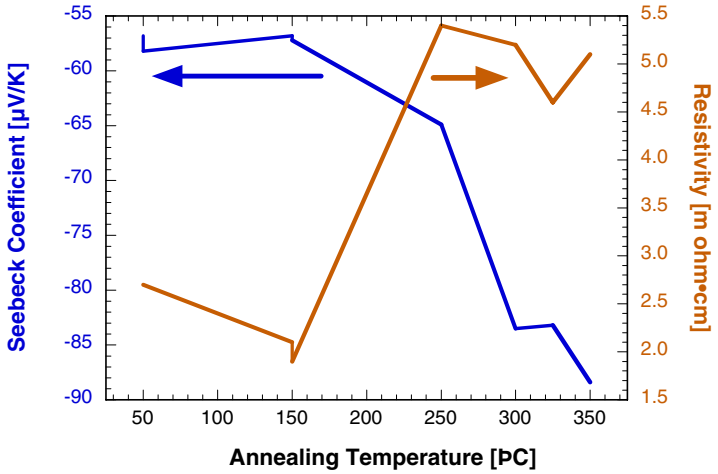

Figure 16: Seebeck coefficient and film resistivity as a function of annealing temperature in forming gas for 1 hour.

Figure 16 summarizes the Seebeck and film resistivity measurements as a function of annealing temperature. It is obvious that some major event occurs above 150 ˚C that has a deleterious effect on the film resistivity. Indeed, these results are contradictory taken by themselves. While it is expected that the Seebeck coefficients of a thermoelectric material will increase with improved crystallinity, as shown here, the film resistivity should decrease with grain growth. However, that is not what occurs. Instead, the film resisitivity increases with increasing annealing temperature. Of course, this correlates with the presence of insulating oxide material in the film. Unfortunately, in order to further improve the Seebeck coefficient, apparently higher annealing temperatures are necessary. However this will accelerate the degradation of the Kapton substrate and worsen the film oxide problem.

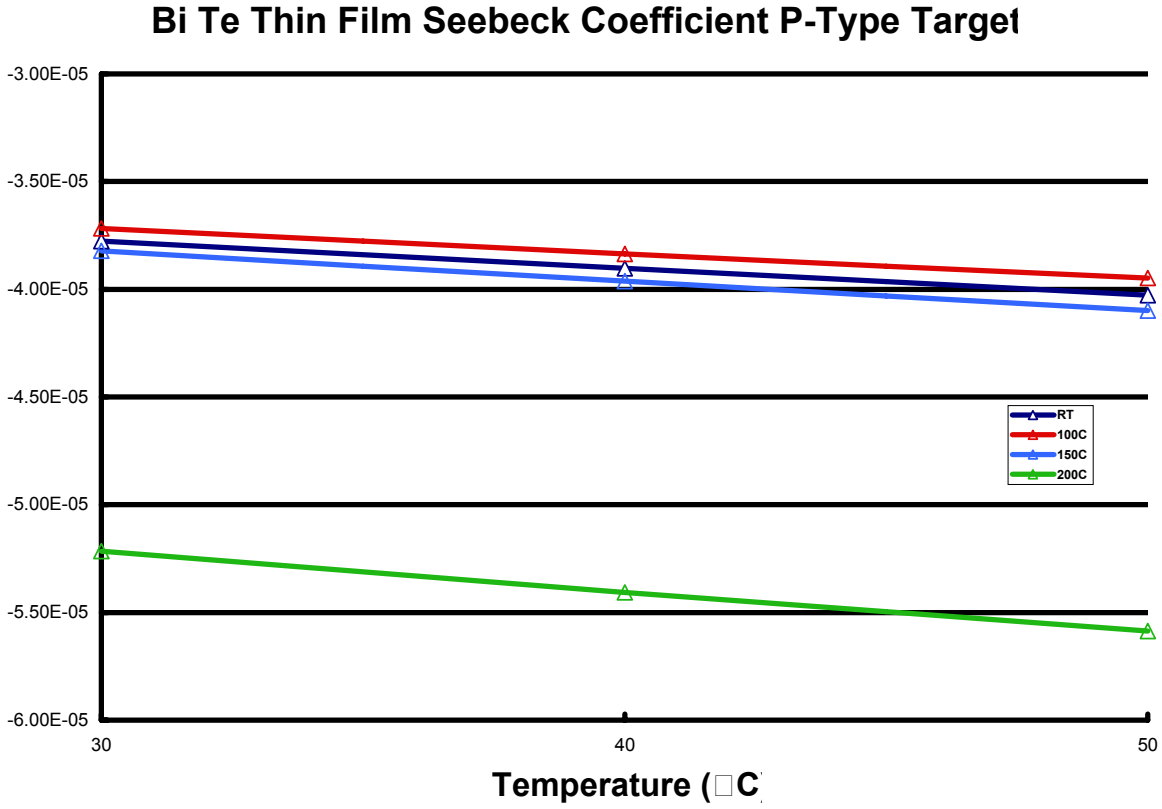

Figure 17 Seebeck coefficient for 6 µm thick Bi(48)Te(52) films grown on Kapton and annealed to various temperatures. The y axis is in units of ohm-cm.

We attempted to produce p-type BiTe films by self-doping, i.e. growing Bi-rich compounds, as opposed to adding in significant amounts of Sb. The resulting composition was Bi(48)Te(52), which compares as very p-type to the nominal 40-60 composition. Given that the n-type films showed significant oxidation when annealed to temperatures > 250 ˚C, these samples were limited to annealing temperatures ≤ 200 ˚C. Figure 17 shows the results for Seebeck measurements vs. temperature for various annealing temperatures. First, note that all of these films behave as n-type, not p-type, thermoelectrics. Second, similar to the earlier results, this coefficient increases with increasing annealing temperature, beginning with the 200 ˚C films. Third, not shown, are the resistivity results. While low for the as-grown and low temperature anneals, the film resisitivity increases by over an order-of-magnitude for the 1 hour anneal at 200 ˚C. So for the very film that shows the highest Seebeck value, the resistivity becomes too high. Not that it matters anyway, since the behavior was n- and not p-type. These results suggest that given our Kapton-forced annealing temperature limitations, we cannot achieve p-type conduction via self-doping, but likely require the use of chemical doping/substitutions, such as Sb for Te.

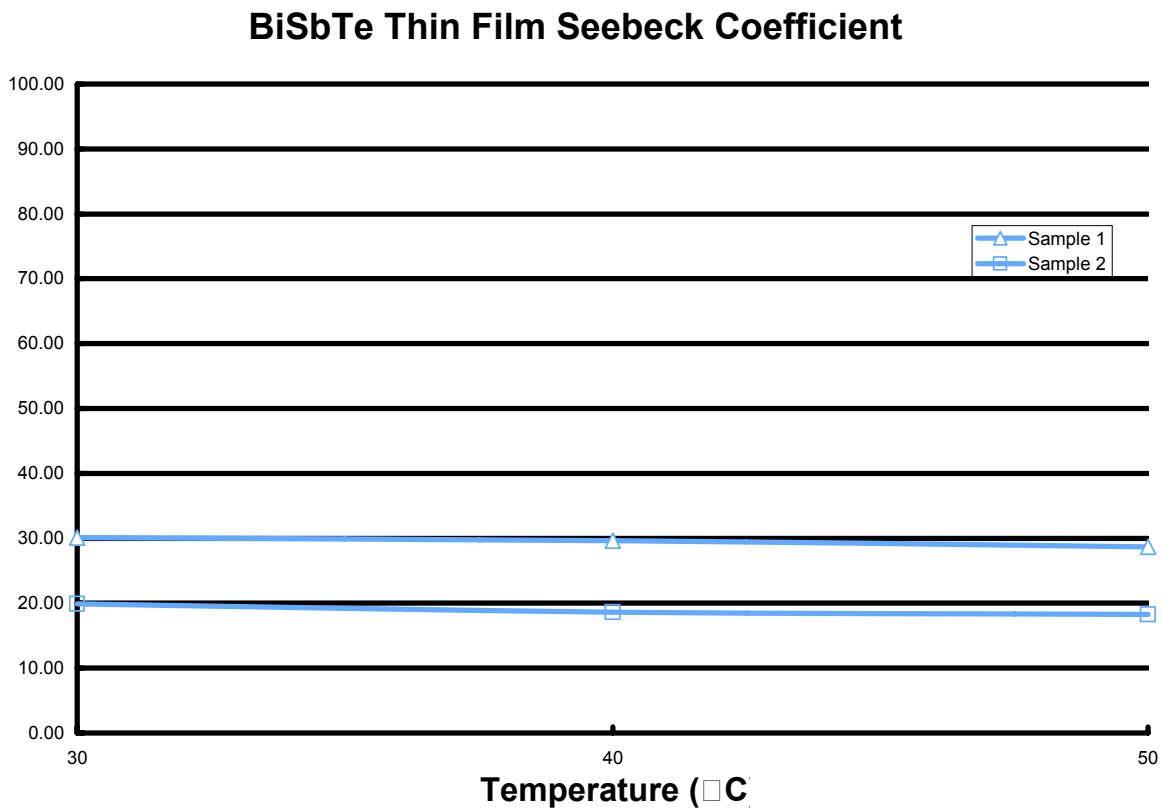

Figure 18. Seebeck coefficient for 6.7 µm thick Bi(11.8)Sb(35.3)Te(60) films (nominal composition) as-deposited on Kapton with no annealing. The y axis is in units of µV/K.

Therefore, we attempted to utilize chemical doping to force p-type behavior. Films with nominal composition of Bi(11.8)Sb(35.3)Te(60) were grown to a thickness of 6.7 µm on Kapton. The precise composition is unknown, and therefore we expect that the thermoelectric measurements can definitely be improved further. Two films measured, both as-deposited, were p-type, however, the Seebeck coefficients were low. These results are shown as a function of temperature in Figure 18.

It is likely that the Seebeck coefficient can be greatly improved by optimizing the BiSbTe composition, and that the resisitivity of these films can be kept low by avoiding thermal annealing above 150 ˚C on Kapton substrates.

Voltage Upconversion

The MicroTEG device requires voltage up-conversion to maximize energy density and provide a usable power to most commercially available electronics. A market search was performed on commercial off-the-shelf (COTS) boost converters to see if one was available

that would utilize the targeted 160 mV output of the boost converter with a total power of roughly 1 mW. Most COTS DC converters are designed to work with typical battery voltage inputs, and no boost converters were found that advertised operation with an input voltage much below 0.5 V. Even boost converters that just provide timing signals for external MOSFET switches could not be configured in a manner that would allow for an input voltage on the order of 100 mV.

It was decided that a custom solution would be required. A MathCAD based first order simulation showed that a switching frequency of 85 kHz with appropriate passive components would produce a 3.0 V or better output. Initial efforts were NOT designed to be autonomous or self starting. Success with early experimentation and a new definition of project success forced a path to a self sustaining but not self-starting solution. This would mean that a voltage on the order of 3 V would be required to jump-start the circuit into self-sustaining mode when an input voltage was present.

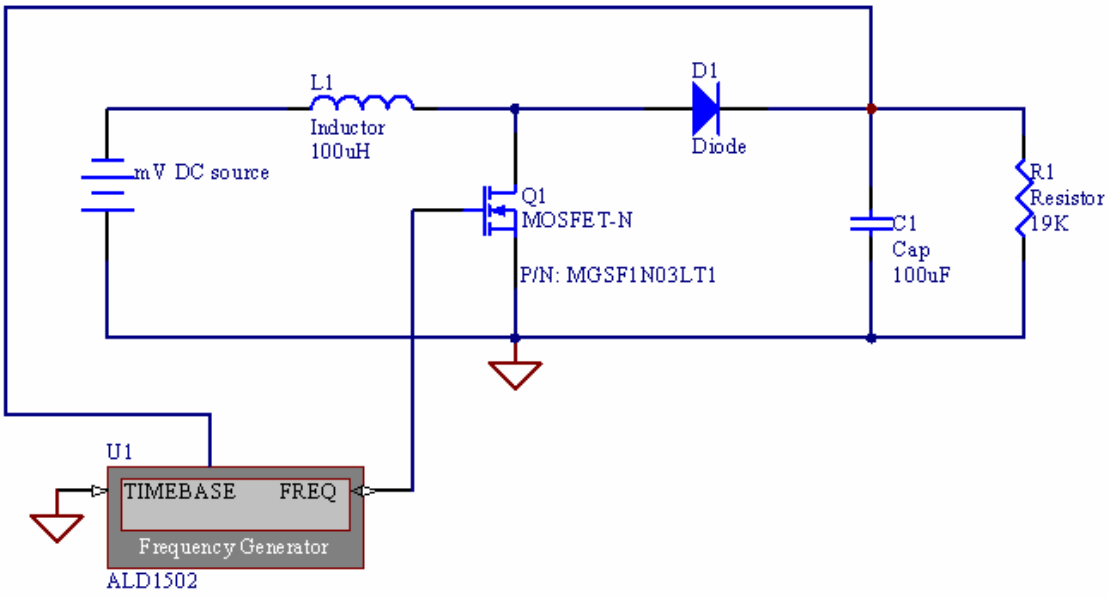

Figure 18: Circuit configuration for upconversion of the output voltage of the TEG.

The final circuit is represented in Figure 19. The first MOSFET selected (IRF4905) had a specified drain-source resistance (R_{ds}) of less than 0.02 ohms and showed no difficulty operating with 160 mV across the drain. Unfortunately, this P-channel MOSFET had 3.4nF of gate capacitance and required complicated power hungry circuitry for fast gate switching. Any self sustaining circuit will require minimum capacitance for maximum efficiency, where the trade off for lower gate capacitance is typically higher drain-source resistance. For first order, the duty cycle adjusted power required to drive the gate capacitance during the switching times should be less than the power lost through R_{ds} during switch on times, and both power numbers should be minimized such that the R_{ds} is much less than the resistance of the power source. Switching times must be much less than the switching frequency. An N-channel MGSF1N03LT1 was the switch that best met our design criteria. It has only 140pF of gate capacitance and near 100 milliohms of drain source resistance.

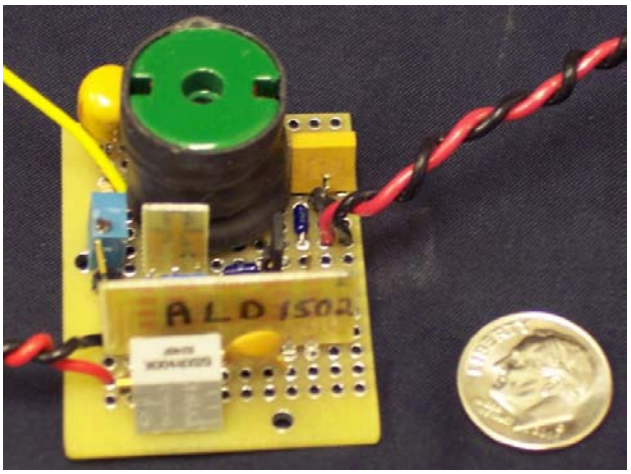

Figure 19: Initial self sustaining circuit, ~8cc of system volume

Much effort was spent trying to find the lowest DC resistance for a 100 uH inductor (0.018 ohms, green component in Figure 20), but it was later found that no measurable efficiency penalty was paid when using inductors with 0.2 ohms of resistance (orange component in Figure 21) which greatly reduced the physical size of the inductor. Some effort was also used to explore options for custom inductors that may help reduce size in future designs. The ALD1502 clock used in the boost converter circuit advertises 50 µA of operational current draw. With external passive timing components the timing circuit draws about twice that figure when generating a time base near 100 kHz. Note that a huge benefit of this particular part is that it offers time base and

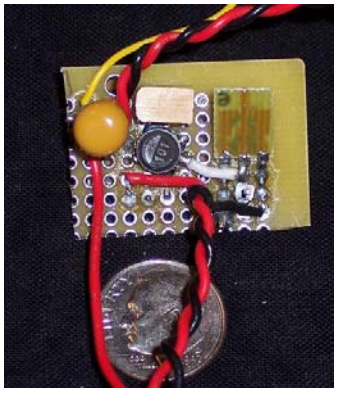

Figure 20: Final configuration of upconverter

duty cycle control in one package. The approximately 2 mA output source current is sufficient to drive the 140 pF gate capacitance to 3 V in 210 ns, which is roughly two orders of magnitude less than our switching frequencies.

Even with the rectification diode in place, the best data from the boost converter provided 75% of the input power in the form of rectified output power at 2.7 V. After powering the timing circuit from the output voltage, the available power to the load was 33% of the input power. With input power being near 1.14 mW, this means about 378 μW is available to our 19k ohm load (usable output power), 481 μW is needed for our clock circuit, and 256 μW is consumed in resistive, switching, and rectification losses. See Appendix A for information on increasing efficiency.

The goal of designing a self-sustaining boost converter to provide a battery-level voltage output for the MicroTEG energy harvester was met. Used with the MicroTEG source, the 378 μW of power available to a load would provide 66 W-hr to an electronic device over a 20 year span, and require a total volume of about ½ a C size battery. The circuits developed for this LDRD are simple and efficient. The benefit to having efficient boost conversion is an increase in energy density over series combinations of energy harvesting source devices. With the exception of the 100 μH inductor, all components could be fabricated on a single CMOS die, maximizing energy density calculations.

Summary and Conclusions

Significant progress in the miniaturization of a thermoelectric device was achieved through the realization that, at small enough dimensions, assembling the thermoelectric legs in a sparse radial design becomes more volume efficient than trying to insulate the system well enough to force the heat flow into a single direction linear heat flow. Minimizing the heat loss from above and below this radial design will result in much better performance, as will minimizing the amount of heat that can be lost through the thermoelectrics themselves, most notably by reducing their cross section. Even with all of these changes, the system will not have a sufficiently high number of couples to provide power at an unconverted voltage; the development of a small scale, monolithically integrated upconverter that can take the (relatively low) output load voltage of the device and convert it up to useful potentials will be required.

The final design of the device was capable of producing 467mW of power at 41mV in a 4.3cc system volume. This power, after 80 days of operation, was equivalent to the output power of an alkaline cell of approximately twice the size. Other improvements can be performed (such as further thinning of the TE elements, sealing the case and replacing the air with 40 torr Xe, and improving the thermal contact between the hot side of the TE and the heat source) can result in a generated power in excess of 1.3mWe. The final demonstrated performance, however, was 107μW/cc at approximately 0.3% efficiency, which exceeds any previously reported performance in terms of power density for a device of these dimensions.

Appendix A: Route to Higher Efficiency Upconversion

Possible path to overall 80% efficiency for the upconverter alone can be found if more of the parasitic capacitance can be removed. This can happen through the use of monolithically integrated transistors, which have a much lower gate capacitance than any devices that are discreet. A calculation of how this efficiency could be achieved is shown below.

For a typical test we had:

1.14 mW input power

160 mV with 7.15 mA

From this we get:

356 *u*W to a 19k ohm load (future useful power)

2.6 V with 137 *u*A

463 *u*W to our clock/PWM/MOSFET driver electronics

2.6 V with 178 *u*A

94.5 *u*W to output diode rectification

300 mV with 315 *u*A

226.5 *u*W to switching, inductive, capacitive, resistive losses in the circuit.

Overall, 72% efficient, with 31.3% of input power delivered to load.

What if we have a 100 *u*W clock/PWM/MOSFET driver?

This may be reasonable. Papers have demonstrated 10 *u*A clocks. This would leave approximately 20 *u*A to drive a MOSFET gate. We could maintain our current switching speed with a 30 pF gate capacitance in this case. Our 140 pF gate capacitance from our COTS MOSFET (MGSF1N03LT1) offers 0.125 ohms for Rds, or 0.5% of expected source DC resistance. A factor of 5 would have gate capacitance near 30 pF and Rds near 0.625 ohms, or 3% of expected source DC resistance. For I = 10 mA, DC loss would go from 1.25 *u*W to 6.25 *u*W – relatively insignificant considering the benefit of taking our 363 *u*W clock/driver to 100 *u*W.

This leaves us with:

714 *u*W to a 19k ohm load (future useful power)

2.6 V with 274 *u*A

100 *u*W to our clock/PWM/MOSFET driver electronics

2.6 V with 38.5 *u*A

94.5uW to output diode rectification

300 mV with 315 *u*A

231.5 *u*W to switching, inductive, capacitive, resistive losses in the circuit.

Which is still 72% efficient, but now with 62.6% of input power delivered to the load. If this is not sufficient, we would move to replacing the output diode. A switch here would need relatively straightforward characteristics. Even with a series resistance of 100 ohms (good for getting a gate capacitance near 5pF or so), this switch would dissipate 10uW of power at 315*u*A of current, and only drop 30mV (insignificant on the output, and 10x less than we currently drop across the diode). Driving the gate capacitance would require roughly 4*u*A, or 15*u*W of power. It would be expected that the existing clock circuit would serve as the time base, and delays could be obtained using another 10*u*W of power or so. Total power for the switch (driving + loss) is 35*u*W, or 1/3 of what we lose now.

Now we would have:

773.5 *u*W to a 19k ohm load (future useful power)

2.9 V with 267 *u*A

100 *u*W to our clock/PWM/MOSFET driver electronics

2.9 V with 34.5 *u*A

35 *u*W to output switch rectifier

30 mV with 301.5 *u*A (plus gate drive and time delays)

231.5 *u*W to switching, inductive, capacitive, resistive losses in the circuit.

This system is 76.6 efficient with 67.9% of input power delivered to load.

To go beyond this, we need a different set of components, or a different boost converter scheme. The inductive losses in our 100 *u*H inductors are near 10%. A smaller inductor would require a higher switching frequency (more power) and have us fighting DC resistance values (we currently have about 200 milliohms DC resistance in our inductor. We may be losing 100 *u*W in the inductor alone right now. This number may be difficult to reduce.

A zero current switching boost converter may have benefits in terms of improving switching noise. What may be difficult to analyze is what the penalty would be in terms of parasitic power the added capacitor and inductor will require to implement this scheme.

We may see a path to eliminating 50*u*W of switching noise only to find out that this required 40 *u*W of parasitic power. Not a good trade.

We are in the process of checking our output capacitor's leakage current. This could buy an additional 10 *u*W or more of power.

This means we may be stuck near 77% overall efficiency and 68% of input power to the load. How then can we get to 80% power to the load? MORE INPUT POWER.

If our circuit will consume on the order of 266 *u*W in operation, require an additional 100 *u*W for a time base and PWM, we use this as a reference. Having 1.5 mW of available power at 160 mV would let us deliver 75.6% of input power to a load. If we had 300 mV of voltage available on the input, we would reduce DC losses in the existing input portion of the circuit by half – taking just 66 *u*W away from these losses by reducing input current would leave you with a system that delivers 80% of input power to a load while providing for self sustaining operation.

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