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Reduction of Thermal Conductivity in Wafer-Bonded Silicon

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Abstract

Blocks of silicon up to 3-mm thick have been formed by directly bonding stacks of thin wafer chips. These stacks showed significant reductions in the thermal conductivity in the bonding direction. In each sample, the wafer chips were obtained by polishing a commercial wafer to as thin as 36 μm, followed by dicing. Stacks whose starting wafers were patterned with shallow dots showed greater reductions in thermal conductivity. Diluted-HF treatment of wafer chips prior to bonding led to the largest reduction of the effective thermal conductivity, by approximately a factor of 50. Theoretical modeling based on restricted conduction through the contacting dots and some conduction across the planar nanometer air gaps yielded fair agreement for samples fabricated without the HF treatment.

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Wafer bonding and fusion techniques have recently been utilized to create unique new material and device structures for a wide range of applications.[1-9] In this work, we will describe reductions in thermal conductivity in bulk silicon achieved by bonding a stack of thin wafers as illustrated in Fig. 1(a), in which numerous nanometer air gaps[10] in the bonded interface were used for impeding normal heat flow. Bulk materials with reduced thermal conductivity are of interest for a variety of thermoelectric, thermophotovoltaic or micro-electromechanical systems applications.

In each experimental run, a commercial one-side-polished, high-resistivity float-zone Si wafer of 500 μm thickness was used. [11] In some runs, the wafer was first patterned with a matrix of 3-μm-diameter dots on 50-μm centers and was etched to an estimated 10- to 20-nm depth by CF_4 reactive ion etching. The wafer was then polished from the backside to a thickness of no greater than 100 μm. (See column 6 of Table I.) This thin wafer is not only easily conformable (favorable for wafer bonding[1, 9]) but also allows more layers of nanometer air gaps per unit thickness (favorable for high thermal impedance). The polished wafer was then saw-cut into numerous 6.0 x 7.5 mm rectangular chips (dimensions conveniently chosen to fit into an existing graphite container for wafer bonding). The Si chips were then thoroughly cleaned in a procedure that included a Radio Corporation of America (RCA) process (of a cleaning solution of H_2O, H_2O_2, and NH_4OH) and a final methanol immersion rinse. The native oxide formed after the RCA process was left in place for all but two experimental runs. For Samples 5 and 6, a diluted (5 to 10 percent) HF dip was used for the oxide removal prior to the final methanol rinse.

The chips were then picked from the methanol bath and assembled wet on a quartz pedestal.[9, 12] The chip stack was then ready for bonding by heat treatment in an argon atmosphere. For bonding with pressure application (for all samples except 2 and 5), the chip stack was placed in the slot of a graphite container, topped by some graphite shims and a graphite plug for a tight fit into a thick-wall quartz cylinder.[3] The loaded chip stack was then placed in a quartz tube in a furnace, which was constantly purged by an ultra-high-purity argon flow. The system was first heated to approximately 50 C for a two hour baking, and then the temperature was raised to 500, 700, or 900 C, typically for 15 hours. These relatively low temperatures were used to minimize actual wafer fusion processes, which would likely increase thermal conductivity.

Thermal conductivity measurements were performed in the direction normal to the bonded interfaces. Thermal diffusivities were measured by a laser flash technique up to 1000 C in argon. Thermal conductivities were calculated by multiplying the thermal diffusivities by a constant silicon density of 2.33 gm/cm^3 and by the silicon specific heat of 0.169 cal/gm-C. Results of four wafer-bonded samples are shown in Fig. 2, where the measured thermal conductivity of a usual homogeneous bulk Si sample is also included for comparison. Table I summarizes all experimental runs, which are grouped for easier comparison of the varied experimental parameters.

Note that Sample 1, which had the thin native oxide left on and had been pressure-bonded, showed a relatively small decrease in thermal conductivity, as shown in Fig. 2. A larger decrease was measured in Sample 2, whose pressure-free bonding might have resulted in fewer and smaller points of contact between wafer chips. Samples with

patterned dots in between wafer chips generally showed still larger decreases in thermal conduction, as evident in Table I.

Table I also shows that Samples 5 and 6, whose chips had been treated in diluted HF prior to bonding, had significant reductions in thermal conduction when compared with similar but un-treated samples. In particular, Sample 6 showed a reduction in thermal conductivity by a factor of 50 as compared to the homogeneous bulk Si. This indicates that the removal of native oxide changed the surface chemical and structural properties for reduced bonding, although the exact details of the resultant atomic structure are unclear at this time.

To better understand the experimental results from basic heat transfer principles, an ideal model of the heat flow is developed, as illustrated in Fig. 1b and 1c, in which each bonded interface is characterized by a series of small contacting dots separated by laterally wide air gaps of nanometer thickness. Argon gas is likely present in these air gaps, since argon ambient was used both in wafer bonding and in the subsequent thermal conductivity measurement. For heat flow normal to the bonded interface, the structure can conduct either through the air gaps or through the small solid contact dots. Convection within the gap and radiation across the gap were not modeled because the combination of these effects was calculated to be less than 1% of the total heat flow. Since the air gaps have a much lower thermal conductivity, a large portion of the heat flows through the few widely spaced dots, where the extra path needed to constrict the heat flow to the dots and to spread the flow from the dots significantly increases the thermal resistance.

Here we consider an ideal case in which the contacting dots are arranged in a square matrix with a lattice constant l. A simple resistance network model is then used to analyze the effective thermal conductivity of each unit cell, as shown in Figs. 1(b) and 1(c). The total thermal resistance of the unit cell is given by[13]

$$R_{cell} = \frac{d+\delta}{k_{eff} l^2} = R_{si} + \frac{1}{R_d^{-1} + R_{gap}^{-1}} \quad (1)$$

where $R_{si} = \frac{d}{k_{si} l^2}$, $R_{gap} = \frac{\delta}{k_{rar}\left(l^2 - a^2\right)}$, d is the thickness of the silicon chip, δ is the gap thickness, a is the dot width, k_{rar} is the thermal conductivity of the argon gas, R_d is the thermal resistance due to the dot, and k_{eff} is the thermal conductivity of the unit cell. Since the conditions of $\frac{a}{l} \leq 0.5$ and $\frac{d}{l} > \frac{2.65}{\pi}$ are generally satisfied in our structures, we have[14]

$$R_d = 2R_s = \frac{2}{k_{Si} a}\left(0.47320 - 0.62075\frac{a}{l} + 0.1198\frac{a^3}{l^3}\right) \quad (2)$$

where the thermal resistance of the dot is neglected because of the small thickness of the dot, R_s is the spreading resistance, and the factor of 2 reflects equal contributions from constriction and spreading.

To evaluate k_{eff} using Eqs. (1) and (2), we use k_{Si} of bulk silicon, since the nominal dot dimension of three μm is considerably greater than the phonon mean free path.[15] However, a “rarefied gas” model must be applied to estimate k_{rar}, since the nanometer thickness of the gap is considerably smaller than the argon mean free path, and we have[16]

$$k_{\mathrm{rar}} = \frac{\delta}{\left(2\alpha^{-1} - 1\right)} \cdot \frac{1}{1 + \frac{4}{15}\frac{\delta}{\lambda}\frac{\alpha}{2-\alpha}} \cdot \frac{\gamma + 1}{\gamma - 1} P \sqrt{\frac{R}{8\pi M T}} \quad (3)$$

where α is the gas-surface thermal accommodation coefficient, R is the molar gas constant, M is the molecular weight, T is the absolute temperature, P is the pressure, λ is the mean free path, and γ is the ratio of specific heats. Reported values of α for argon gas at silicon surface range between 0.7 and 0.9.[17]

Figure 3 illustrates modeled k_{eff} for one set of experimental parameters with fabricated dots. The model generally yielded k_{eff} within a factor of 2 of the experimental values of Samples 3 and 4. For Sample 6, however, the modeled k_{eff} was 3 to 4 times the experimental values. This indicates that HF-treated surfaces may have smaller effective bonded area in each dot or a smaller number of dots contacting both silicon surfaces, since the native oxide left on the non-HF-treated surfaces of Samples 3 and 4 appear to have helped make more complete bonding over the entire area of each dot.

In conclusion, wafer bonding has been used for the first time for the reduction of thermal conductivity in bulk Si by a factor of 50. Since the nanometer air gaps in the wafer stacks are generally much smaller than optical wavelengths, relatively small reflections are expected for near-normal optical transmission. Electron tunneling through these thin gaps could also maintain some electrical conduction in the stacks.[18] The present wafer bonding technique holds considerable promise in applications where a reduction in thermal conductivity is required.

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Figure Captions

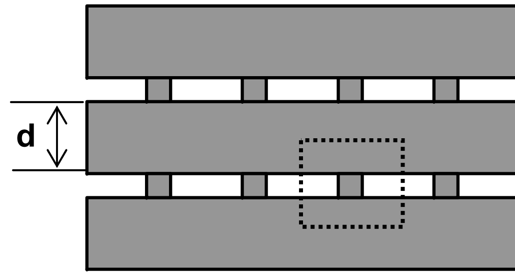
Fig.1 Schematic cross-sectional view of an idealized bonded wafer stack, (a), and the unit-cell modeling of its thermal conductivity, (b) and (c).

Fig. 2 (a) Experimentally measured thermal conductivity values of three wafer-bonded samples. Also plotted is the measured thermal conductivity of an ordinary homogeneous bulk silicon sample. (b) Expanded scale of Fig.2(a) showing measured low thermal conductivity of two wafer-bonded samples. Also plotted is the thermal conductivity of bulk silicon divided by 50.

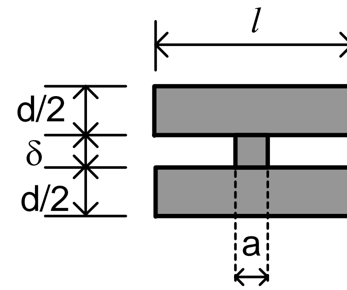
Fig.3 Modeled effective thermal conductivity of wafer-bonded silicon for one set of bonding parameters and several air-gap thicknesses. The bottom curve is for conduction through the contacting dots only.

Table I. Summary of the Experimental Runs

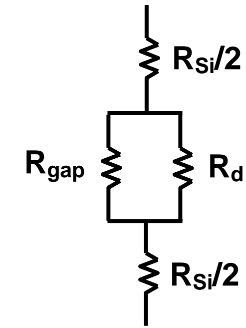
Sample	**Dot pattern**	**HF treatment**	**Pressured bonding**	**Temperature (C)**	**Average chip thickness (μm)**	**No. of chips**	***k* at 1000C (W/m-K)**
1			Yes	900	100	30	23.5
2				900	69	36	8.37
5		Yes		900	41	24	0.8
3	Yes		Yes	500	64	20	3.1
4	Yes		Yes	700	59	17	2.7
6	Yes	Yes	Yes	900	36	30	0.45



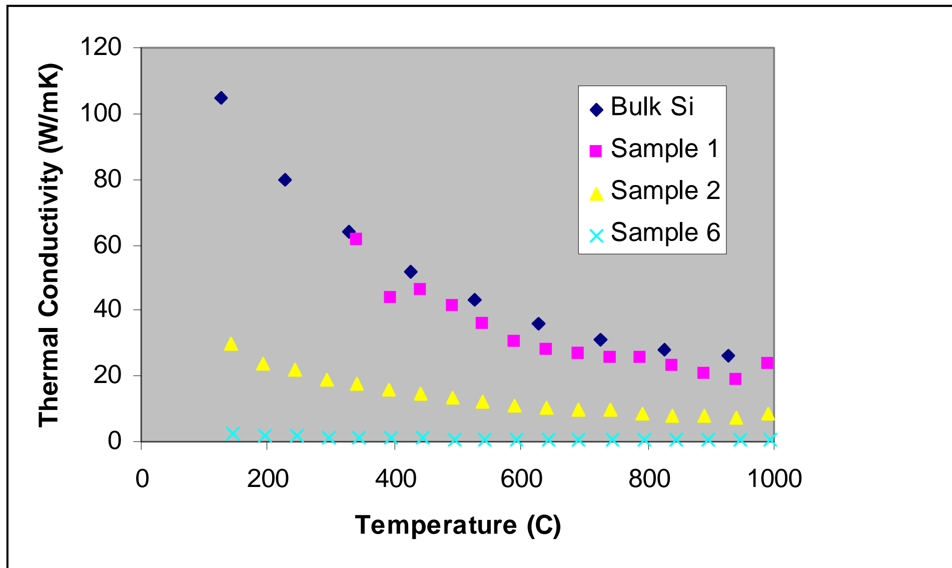
(a)



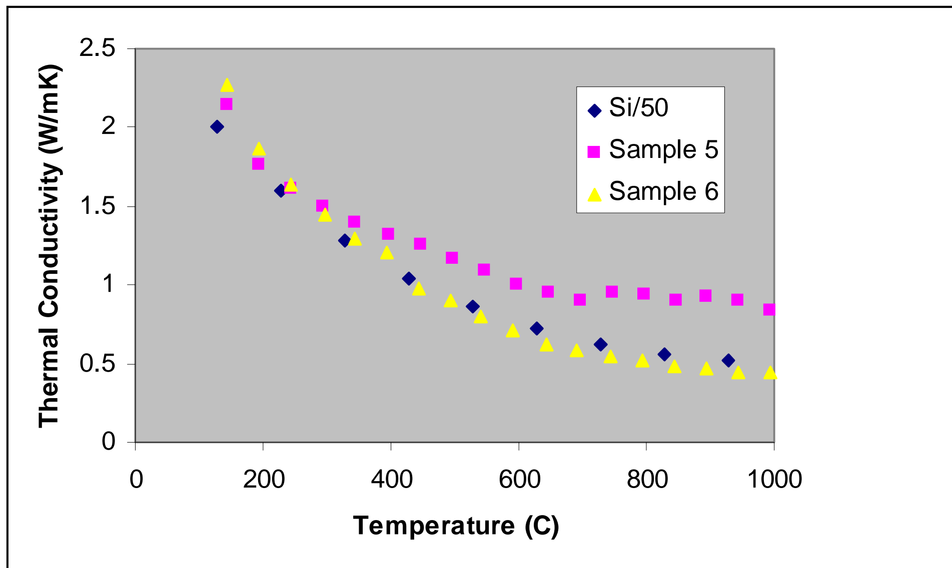
(b)



(c)



(a)



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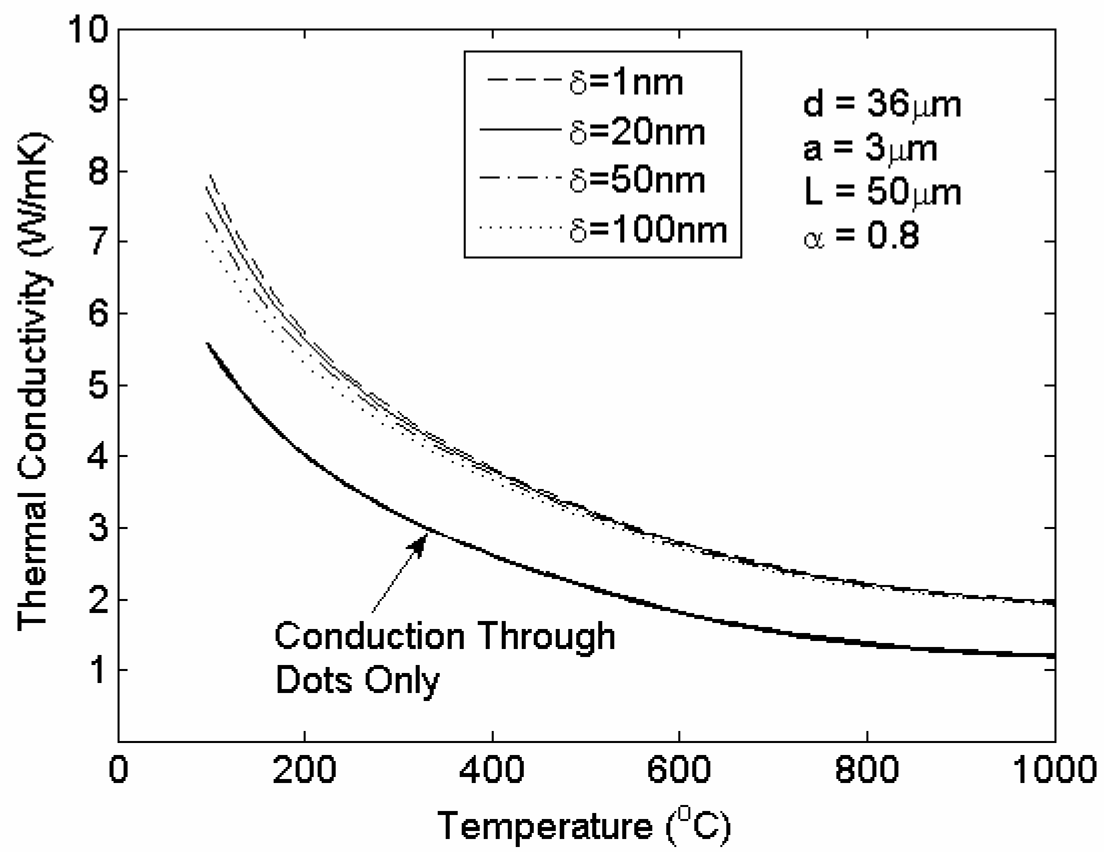
10
9
8
7
6
5
4
3
2
1
0
200
400
600
800
1000
Thermal Conductivity (W/mK)
Temperature (⁰C)
δ=1nm
δ=20nm
δ=50nm
δ=100nm
d = 36μm
a = 3μm
L = 50μm
α = 0.8
Conduction Through
Dots Only