

SANDIA REPORT

SAND2006-7112

Unlimited Release

Printed November 2006

Thermal Conductivity Measurements of SUMMIT™ V Polycrystalline Silicon

Leslie M. Phinney, Jaron D. Koppers, and Rebecca C. Clemens

Prepared by
Sandia National Laboratories
Albuquerque, New Mexico 87185 and Livermore, California 94550

Sandia is a multiprogram laboratory operated by Sandia Corporation,
a Lockheed Martin Company, for the United States Department of Energy's
National Nuclear Security Administration under Contract DE-AC04-94AL85000.

Approved for public release; further dissemination unlimited.

Issued by Sandia National Laboratories, operated for the United States Department of Energy by Sandia Corporation.

NOTICE: This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government, nor any agency thereof, nor any of their employees, nor any of their contractors, subcontractors, or their employees, make any warranty, express or implied, or assume any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represent that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government, any agency thereof, or any of their contractors or subcontractors. The views and opinions expressed herein do not necessarily state or reflect those of the United States Government, any agency thereof, or any of their contractors.

Printed in the United States of America. This report has been reproduced directly from the best available copy.

Available to DOE and DOE contractors from
U.S. Department of Energy
Office of Scientific and Technical Information
P.O. Box 62
Oak Ridge, TN 37831

Telephone: (865) 576-8401
Facsimile: (865) 576-5728
E-Mail: reports@adonis.osti.gov
Online ordering: <http://www.osti.gov/bridge>

Available to the public from
U.S. Department of Commerce
National Technical Information Service
5285 Port Royal Rd.
Springfield, VA 22161

Telephone: (800) 553-6847
Facsimile: (703) 605-6900
E-Mail: orders@ntis.fedworld.gov
Online order: <http://www.ntis.gov/help/ordermethods.asp?loc=7-4-0#online>



Thermal Conductivity Measurements of SUMMiT™ Polycrystalline Silicon

Leslie M. Phinney¹, Jaron D. Koppers¹, and Rebecca C. Clemens²
¹Engineering Sciences Center
²Surety Components and Instrumentation Center
Sandia National Laboratories
P.O. Box 5800 MS 0834
Albuquerque, New Mexico 87185-0834

Abstract

A capability for measuring the thermal conductivity of microelectromechanical systems (MEMS) materials using a steady state resistance technique was developed and used to measure the thermal conductivities of SUMMiT™ V layers. Thermal conductivities were measured over two temperature ranges: 100K to 350K and 293K to 575K in order to generate two data sets. The steady state resistance technique uses surface micromachined bridge structures fabricated using the standard SUMMiT fabrication process. Electrical resistance and resistivity data are reported for poly1-poly2 laminate, poly2, poly3, and poly4 polysilicon structural layers in the SUMMiT process from 83K to 575K. Thermal conductivity measurements for these polysilicon layers demonstrate for the first time that the thermal conductivity is a function of the particular SUMMiT layer. Also, the poly2 layer has a different variation in thermal conductivity as the temperature is decreased than the poly1-poly2 laminate, poly3, and poly4 layers. As the temperature increases above room temperature, the difference in thermal conductivity between the layers decreases.

ACKNOWLEDGMENTS

The authors thank Rosemarie Renn and Katie Francis for assistance during the design of the thermal conductivity test structures and the Microelectronics Development Lab staff for their efforts in fabricating the structures. We are also grateful for the assistance of Ted Parson in implementing the data acquisition system. We thank Blake Jakabowski and Ray Haltli for wire bonding and packaging samples for testing. We appreciate the efforts of Allen Gorby in providing general support for this project and especially for the work on the Janis cryostat, modifying it to be compatible with the samples and changing the modules between tests. We also acknowledge the contribution of Ed Piekos for his simulations of the test structures. Constructive peer reviews of this report were provided by Justin Serrano, Ed Piekos, and Michael Shaw.

CONTENTS

Acknowledgments	4
Contents	5
Figures.....	6
Table.....	7
Nomenclature	8
1. Introduction	11
2. Test Structure Design and Fabrication	13
2.1. SUMMiT V process	13
2.2. Test Structure Design	13
3. Experimental Layout and Methods	17
3.1. Steady State Resistance Technique	17
3.1.1. Model	17
3.1.2. Experimental Layout.....	19
3.2. Low Temperature Cryostat.....	21
3.2.1. Cryostat	21
3.2.2. LCC Package	21
3.2.3. Data Acquisition	22
3.3. High Temperature Cryostat	24
3.3.1. Cryostat	24
3.3.2. Alphaprobes Sample Holder	24
3.3.3. Data Acquisition	26
3.4. Data Analysis	27
3.4.1. Variation of Electrical Resistance.....	28
3.4.2. Calculation of Thermal Conductivity	29
3.4.3. Sensitivity Analysis	30
4. Thermal Conductivity Experimental Results	33
4.1. Electrical Resistance versus Temperature.....	33
4.2. Electrical Resistivity versus Temperature.....	34
4.3. Thermal Conductivity versus Temperature.....	34
4.4. Measurement Uncertainty	40
4.4.1. Experimental Uncertainty	40
4.4.2. Simulation of a Test Structure	41
5. Conclusions	45
5.1. Summary of Results	45
5.2. Recommendations for Continuation.....	45
6. References	47
Distribution.....	48

FIGURES

Figure 1:	Thermal conductivity data for polycrystalline silicon [2-5].	11
Figure 2:	Layers in the SUMMiT™ V Process, © 2003 Sandia National Laboratories.	13
Figure 3:	AutoCAD drawing of RS 485 module with thermal conductivity test structures along the upper and lower edges.	14
Figure 4:	Top and side views of thermal conductivity test structures: a) P1P2A b) P2A c) P3A and d) P4A. The side view of a test structure with an underlying via is identical to those shown above except the substrate directly under the beam is removed. The vertical scale of the side view is enlarged to improve visibility.	14
Figure 5:	Microscope image of RS485 module with wire bond connections to test structure bond pads.	15
Figure 6:	Microscope images of the thermal conductivity test structures after wire bonding: a) P1P2A b) P2A c) P3A and d) P4A.	15
Figure 7:	Work bench with thermal conductivity experiment equipment.	19
Figure 8:	Schematic of thermal conductivity experiment layout.	20
Figure 9:	Henriksen cryostat: a) exterior with A/B ribbon connector, b) exterior, and c) interior sample chamber holding a packaged die.	21
Figure 10:	Clockwise from upper left: LCC with die; back of empty LCC; front of empty LCC.	22
Figure 11:	Screen shot of the data acquisition software for the Henriksen cryostat.	23
Figure 12:	Janis cryostat: a) exterior, b) cold finger removed from the outer shroud with radiation shield around the sample area, and c) sample holder area with electrical wires for connection to Alphaprobes holder.	24
Figure 13:	Electrical connections to sample in Janis cryostat: a) Alphaprobes holder, b) top view of the holder with the lead numbers, and c) schematic of module with lead numbers next to corresponding probe locations on bond pads.	25
Figure 14:	Screen shot of the thermal conductivity data acquisition software for the Janis cryostat.	26
Figure 15:	Flowchart illustrating the data analysis procedure.	28
Figure 16:	Electrical resistance versus temperature for the P1P2A test structure on Die 1.	28
Figure 17:	Electrical resistance versus current at 293K for the P1P2A test structure on Die 1. The model line is the best fit from the data analysis MATLAB routine and corresponds to a thermal conductivity of 49.8 W/mK.	29
Figure 18:	Thermal conductivity vs. temperature for P1P2A test structure on Die 1.	30
Figure 19:	Percent change in thermal conductivity with variations in the thickness, width, length, and slope of resistance versus temperature.	31
Figure 20:	Electrical resistance versus temperature for the tested SUMMiT layers.	33
Figure 21:	Electrical resistivity versus temperature for the tested SUMMiT layers.	34
Figure 22:	Thermal conductivity data versus temperature for the temperature range 100K from 350K.	35
Figure 23:	Thermal conductivity data versus temperature for the temperature range 293K from 575K. Data was collected down to 83K to increase the overlap with the data from 100K to 300K.	36
Figure 24:	Thermal conductivity data versus temperature for P1P2 samples.	37
Figure 25:	Thermal conductivity data versus temperature for P2 samples.	37

Figure 26: Thermal conductivity data versus temperature for P3 samples.	38
Figure 27: Thermal conductivity data versus temperature for the P4 samples.	38
Figure 28: Thermal conductivity data versus temperature for four polysilicon layers.	39
Figure 29: Thermal conductivity versus temperature for averages of the measured data compared to existing thermal conductivity data.	40
Figure 30: Perceived thermal conductivity for poly4 and poly1-poly2 beams with a range of fillet radii.....	42
Figure 31: Comparison of temperature distributions for a poly4 beams with a square edge and with a 5 μm fillet at its attachment point.	43

TABLE

Table 1: Die and Test Structures Tested	16
---	----

NOMENCLATURE

Acronyms

ASC	Advanced Simulation and Computing
DAQ	Data Acquisition
DMM	Digital Multimeter
DMS	Discriminating Microswitches
DRIE	Deep Reactive Ion Etch
DUT	Device Under Test
GPIB	General Purpose Interface Bus
LCC	Leadless Chip Carrier
LN ₂	Liquid Nitrogen
LPCVD	Low Pressure Chemical Vapor Deposition
MEMS	Microelectromechanical Systems
P1P2	Laminate of the First (poly1) and Second (poly2) Polysilicon Structural Layers in the SUMMiT Process
P2	Second (poly2) Polysilicon Structural Layer in the SUMMiT Process
P3	Third (poly3) Polysilicon Structural Layer in the SUMMiT Process
P4	Fourth (poly4) Polysilicon Structural Layer in the SUMMiT Process
PECVD	Plasma Enhanced Chemical Vapor Deposition
RS	Reticle Set
SNL	Sandia National Laboratories
SUMMiT™	Sandia Ultra-planar Multilevel MEMS Technology
USB	Universal Serial Bus

Variables

A	surface area normal to direction
I	current
k	thermal conductivity
L	length
m	coefficient
q_F	conductive heat transfer rate
q_J	rate at which energy is generated by Joule heating
R	electrical resistance
R_0	electrical resistance at the equilibrium temperature
\bar{R}	average electrical resistance
t	thickness
T	temperature
T_0	equilibrium temperature
\bar{T}	average temperature
V	volume
V	voltage
w	width

x	direction
α	coefficient
ρ	electrical resistivity

1. INTRODUCTION

Microelectromechanical systems (MEMS) have been designed and developed for applications in the military and defense industries including optical switches, discriminating microswitches (DMS), non-volatile memory, and inertial sensors. In order to correctly predict the thermal, mechanical, and electrical performance of microdevices using numerical simulations, accurate material property data is essential. Material property data is also needed for the development and validation of material property models. The material property data needs to be measured over the entire temperature range applicable to a simulation, model, or device operation as the properties are usually a function of temperature.

One of the main fabrication processes for MEMS is sacrificial surface micromachining in which layers of structural and sacrificial material are sequentially deposited, patterned, and etched in order to build a microdevice. Sandia National Laboratories (SNL) developed a five-layer polycrystalline silicon surface micromachining process, SUMMiT™ V (Sandia Ultra-planar Multilevel MEMS Technology) [1]. The basic structural material in the SUMMiT V process is polycrystalline silicon (polysilicon). Polysilicon properties vary considerably with process variations that alter the microstructure and doping of the polysilicon. Available thermal conductivity data from the literature and SNL for several polysilicon samples is plotted as a function of temperature in Figure 1 [2-5]. The thermal conductivity data varies by almost an order of magnitude depending on the polysilicon fabrication process and measurement technique. The thermal conductivity data taken using SNL surface micromachined polysilicon (Manginell [5], red squares) has values that are at the high end of existing data and were taken for only one of the structural layers.

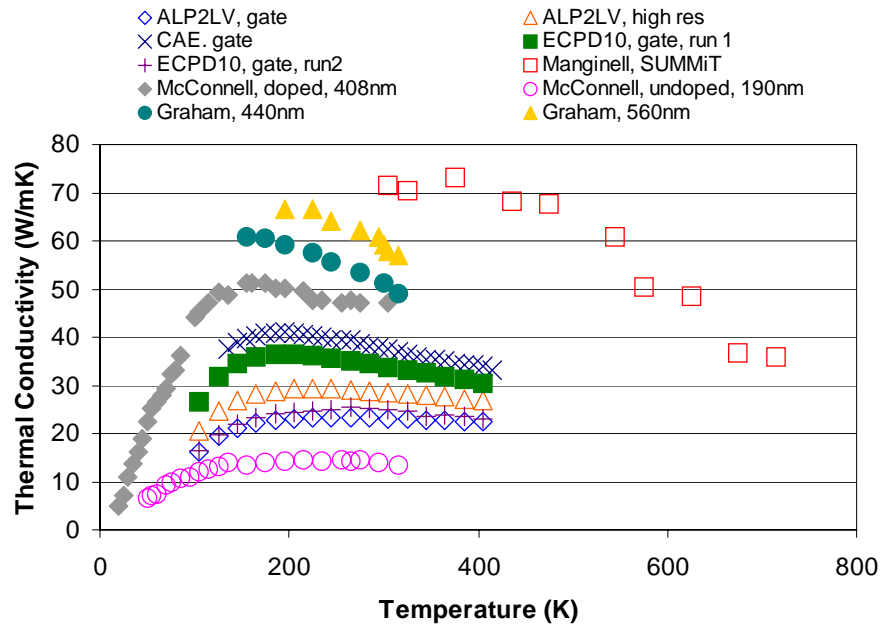


Figure 1: Thermal conductivity data for polycrystalline silicon [2-5].

This report documents the thermal conductivity measurements for SUMMiT V polycrystalline silicon in support of developing first principles models for thermal conductivities for MEMS simulations and MEMS device simulations. By measuring the thermal conductivity for SUMMiT V materials, computational models can be qualified against data for SUMMiT V materials and the data can be used as inputs to Advanced Simulation and Computing (ASC) codes such as the thermal code, Calore, and thermomechanical code, Calagio, to predict the performance of MEMS devices.

The specific deliverables for this project were:

1. Provide thermal conductivity data for SUMMiT V polycrystalline silicon at low temperatures for model validation, 100 K to 350 K.
2. Provide thermal conductivity data for SUMMiT V polycrystalline silicon at room temperature and above for model validation, 293 K to 575 K.

2. TEST STRUCTURE DESIGN AND FABRICATION

This section describes the test structure design and fabrication for thermal conductivity testing of the SUMMiT V polysilicon layers.

2.1. SUMMiT V process

The thermal conductivity test structures were fabricated using the SUMMiT™ V [1] process, in which there is a layer of polysilicon deposited on the substrate above the passivation and isolation layers and four polysilicon structural layers. The structural polysilicon layers are n-type, doped with phosphorous, and separated from the polysilicon on the substrate and each other by sacrificial layers consisting of silicon dioxide. The structural layers will be referred to as poly1, poly2, poly3, and poly4 with poly1 being closest to the substrate and poly4 being the furthest. Figure 2 illustrates the SUMMiT V layers and lists the nominal thickness values for the sacrificial and structural layers.

2.2. Test Structure Design

The thermal conductivity measurement test structures are 200 μm long and 10 μm wide beams fabricated from structural polysilicon layers in the SUMMiT V process. The test structures were fabricated on module 5 of Reticle Set (RS) 485 that is pictured in Figure 3 with the thermal conductivity test structures labeled. Four types of beams were fabricated: poly1-poly2 laminate (P1P2), poly2 (P2), poly3 (P3), and poly4 (P4) beams. Schematics of the top and side views of the thermal conductivity test structures are pictured in Figure 4. The nominal thicknesses of the test structures are 2.5 μm for P1P2, 1.5 μm for P2, 2.25 μm for P3, and 2.25 μm for P4.

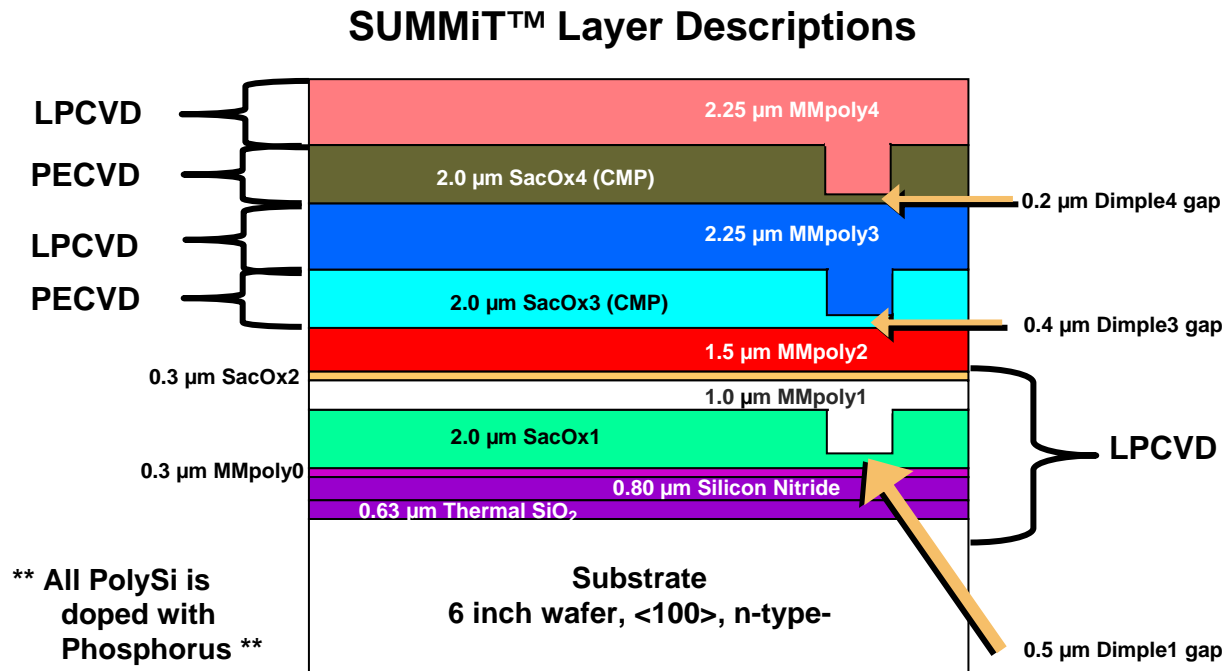


Figure 2: Layers in the SUMMiT™ V Process, © 2003 Sandia National Laboratories.

On the module, two of the beams from each layer were designed: one on the upper edge and one on the lower edge. The P3 and P4 test structures along the lower edge were designed with an underlying via produced with a Bosch DRIE (deep reactive ion etch) for improved thermal isolation. The test structures along the upper edge do not have an underlying Bosch hole and are labeled with an “A” following their layer designation: P1P2A, P2A, P3A, and P4A; whereas, the test structures designed on the side with Bosch holes are designated with the layer and a “B”: P1P2B, P2B, P3B, and P4B. Note that while the P1P2B and P2B test structures are on the lower edge and designated with a B, neither has a Bosch hole due to the need for a P2 layer to define a Bosch via. Only the P3B and P4B test structures have underlying Bosch holes, and the P4B are the ones for which data has been obtained. The majority of the P3B structures with Bosch holes appeared cracked during optical inspection so there was concern about their surviving the testing process and quality of the data that would be obtained.

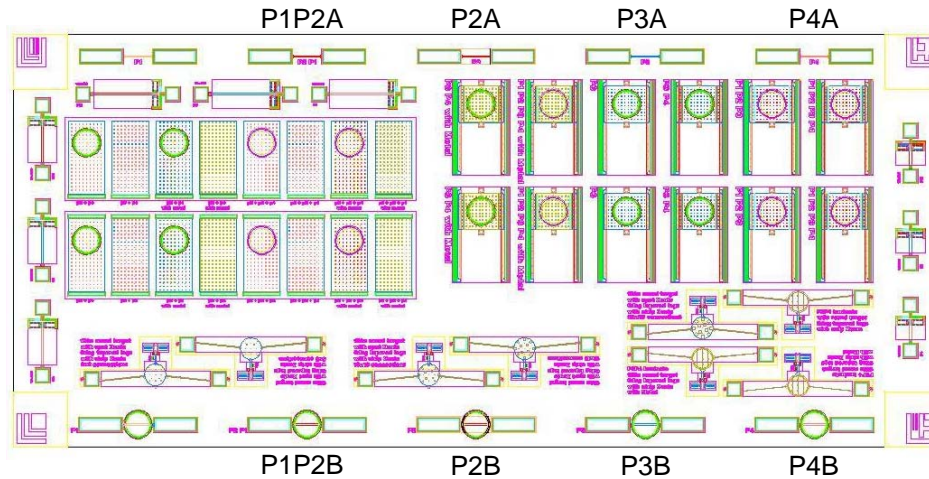


Figure 3: AutoCAD drawing of RS 485 module with thermal conductivity test structures along the upper and lower edges.



Figure 4: Top and side views of thermal conductivity test structures: a) P1P2A b) P2A c) P3A and d) P4A. The side view of a test structure with an underlying via is identical to those shown above except the substrate directly under the beam is removed. The vertical scale of the side view is enlarged to improve visibility.

The test structures have 5 μm radius fillets at the base of the beams where they connect to the bond pads. The fillets were added in an attempt to increase the survival rate of test structures through the Bosch and release process steps compared to an earlier design for which the yields were very low. Even with this design improvement, the yields for test structures with underlying Bosch holes were still low enough that it was decided for some of the modules not to have Bosch processing. In this case, the two beams designed with and without the Bosch via are essentially identical. Figure 5 is a microscope image of a module that did not have Bosch processing after wire bonding for testing in the low temperature Henriksen cryostat as will be discussed in Sect. 3.2.2, and Figure 6 shows individual test structures after wire bonding. Table 1 lists the tested modules and which test structures were tested on the module.

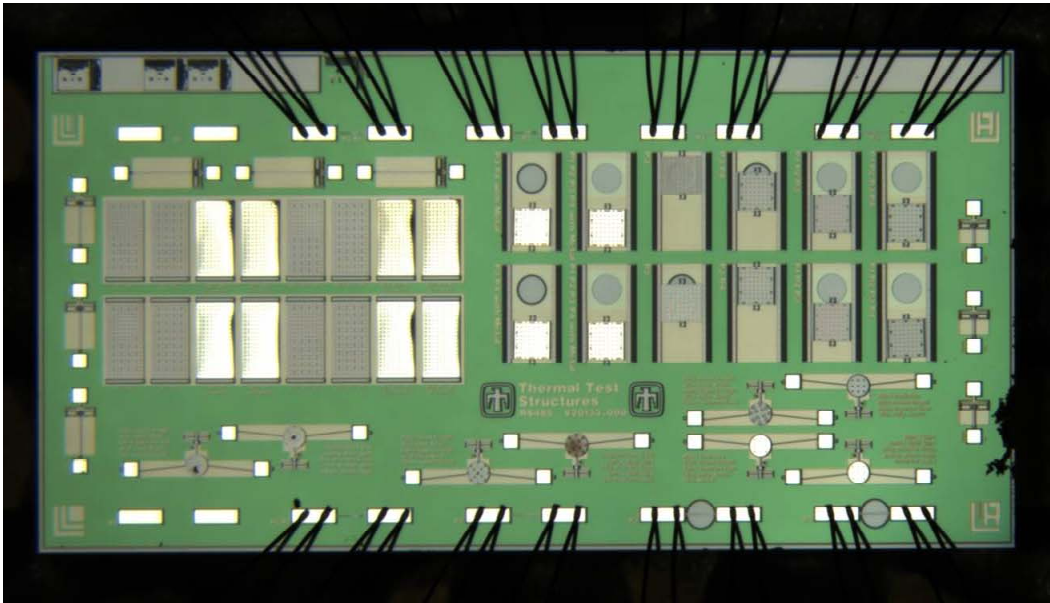


Figure 5: Microscope image of RS485 module with wire bond connections to test structure bond pads.

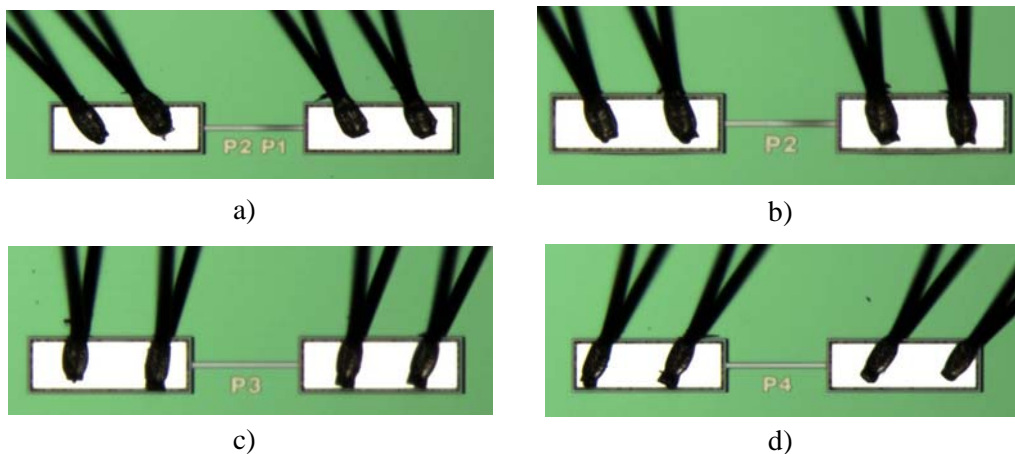


Figure 6: Microscope images of the thermal conductivity test structures after wire bonding: a) P1P2A b) P2A c) P3A and d) P4A.

Table 1: Die and Test Structures Tested

Cryostat	Die	Cycles	Test Structures							
			P1P2A	P1P2B	P2A	P2B	P3A	P3B	P4A	P4B
H	Die3	2	X	X	X	X	X	X	X	X
H	Die1B	1	X	X	X	X	X	X	X	B
J	Die1	1	X		X					
J	Die2	1			X			X		
J	Die37	2					X		X	
J	DieT	1	X							
J	Die3B	1			X	X				

H – Henriksen cryostat, J – Janis cryostat, X – Tested w/out Bosch; B – Tested w/ Bosch

3. EXPERIMENTAL LAYOUT AND METHODS

This section describes the steady state resistance method for measuring thermal conductivity. First, the theory of the model used to calculate the thermal conductivity from the measured electrical resistance is presented. Then, the experimental equipment and its layout are specified. The data acquisition system and experimental procedures are given. The final section discusses the data analysis methods.

3.1. Steady State Resistance Technique

A steady state resistance method was used to measure the thermal conductivities of the SUMMiT™ V layers with the fabricated test structures. In this technique, a four point probe measurement is made in which a DC current is sourced between the outer electrical connections and the DC voltage measured between the inner electrical connections. From the applied currents and measured voltages, the measured electrical resistance is calculated for a range of currents at each temperature. Assuming one dimensional heat transfer in the test structure with no losses except for conduction along the test structure, the thermal conductivity can be obtained from the electrical resistance as a function of current as described in Section 3.1.1. Section 3.1.2 discusses the experimental equipment and basic configuration for implementing the steady state resistance measurements. Two cryostats (temperature chambers) were used for measurements in this study, and particulars for the measurements in each chamber are provided in Sections 3.2 and 3.3.

3.1.1. Model

The steady state resistance technique has been used to measure the thermal conductivity of various materials with beam or bridge type test structures [6, 7] like those designed for the current study. This technique is based on the relationship between the electrical resistance distribution and the temperature distribution in the test structure [6, 7]. For a material whose electrical resistance increases with temperature, the electrical resistance measured across a test structure increases as the applied current is increased and the amount of Joule heating increases. If the energy removal from the test structure is high due to a high thermal conductivity of the material, the increase in electrical resistance is lower for a given current than for a material with a low thermal conductivity. Thus, the thermal conductivity of a material can be determined from the electrical resistance as a function of applied current.

The derivation of the model starts with Fourier's law, Equation 1, and the expression for Joule heating, Equation 2:

$$q_F = kA \frac{dT}{dx} \quad (1)$$

where q_F is the conductive heat transfer rate, k is thermal conductivity, A is the surface area normal to direction x , and T is the temperature, and

$$q_J = I^2 R \quad (2)$$

where q_J is the rate at which energy is generated by Joule heating, I is current, and R is electrical resistance. Using conservation of energy, Eqs. 1 and 2 are combined in an expression that relates the thermal conductivity to the resistance and current:

$$kV \frac{d^2 T}{dx^2} + I^2 R(T) = 0 \quad (3)$$

where V is the volume of the test structure and the electrical resistance, R , is a function of temperature T according to the relationship:

$$R(T) = R_0 [1 + \alpha(T - T_0)] \quad (4)$$

where R_0 and T_0 are the resistance and temperature at the equilibrium temperature, respectively, and α is a coefficient.

To solve Eq. 3, we assume steady state conditions for the test structure, no significant energy loss due to convection or radiation from the test structure to the environment, and that the test structure's bond pads are at the the heat sink temperature, T_0 . The resulting temperature distribution, $T(x)$, is given in Eq. 5 where $x = 0$ is at the beam center and $x = \pm L/2$ are at the ends of a beam of length L .

$$T(x) = T_0 - \frac{1}{\alpha} \left[1 - \frac{\cos(mx)}{\cos\left(\frac{mL}{2}\right)} \right] \quad (5)$$

The equation for m in Eq. 5 depends on the thermal conductivity k and is provided in Eq. 6:

$$m = \left(\frac{I^2 (R_0 \alpha)}{(wtL)k} \right)^{1/2} \quad (6)$$

where w is width, and t is thickness of the test structure. Since the coefficient m is a function of the slope of the resistance versus temperature curve, $slope = R_0 \alpha$, resistances in a temperature range must be obtained before the thermal conductivity values at a given temperature can be determined if a measured value of $R_0 \alpha$ is to be used in calculating the thermal conductivity. Integrating Eq. 5 along the length yields expressions for the average temperature, \bar{T} , and average electrical resistance, \bar{R} , for the test structure which are:

$$\bar{T} = T_0 - \frac{1}{\alpha} \left[1 - \frac{2}{mL} \tan\left(\frac{mL}{2}\right) \right] \text{ and} \quad (7)$$

$$\bar{R} = R_0 \left[\frac{2}{mL} \tan\left(\frac{mL}{2}\right) \right] \quad (8)$$

For a given test structure geometry and known linear variation of electrical resistance versus temperature, the thermal conductivity is the only unknown in Eq. 8 once the test structure electrical resistance is measured at a specific current. Thus, the thermal conductivity can be calculated from resistance measurements at a given temperature.

The steady state electrical resistance method for measuring the electrical resistance obtains a single, constant value for the thermal conductivity, k , of a test structure at a given temperature. It does not consider the variation of thermal conductivity in the test structure due to the temperature distribution in the test structure.

3.1.2. Experimental Layout

Figures 7 and 8 show the main components of the thermal conductivity experiment. The primary pieces of equipment include a cryostat, temperature controller, data acquisition computer, source meter, switching unit, digital multimeter, and liquid nitrogen dewar. More details on the experimental hardware are provided according the particular cryostat in Sections 3.2.1 and 3.3.1, one of which was used to collect the data set from 100K to 350K and the other to collect the data set from 293K to 575K. Also, the sample packaging and connections in the cryostat are described in Sections 3.2.2 and 3.3.2.

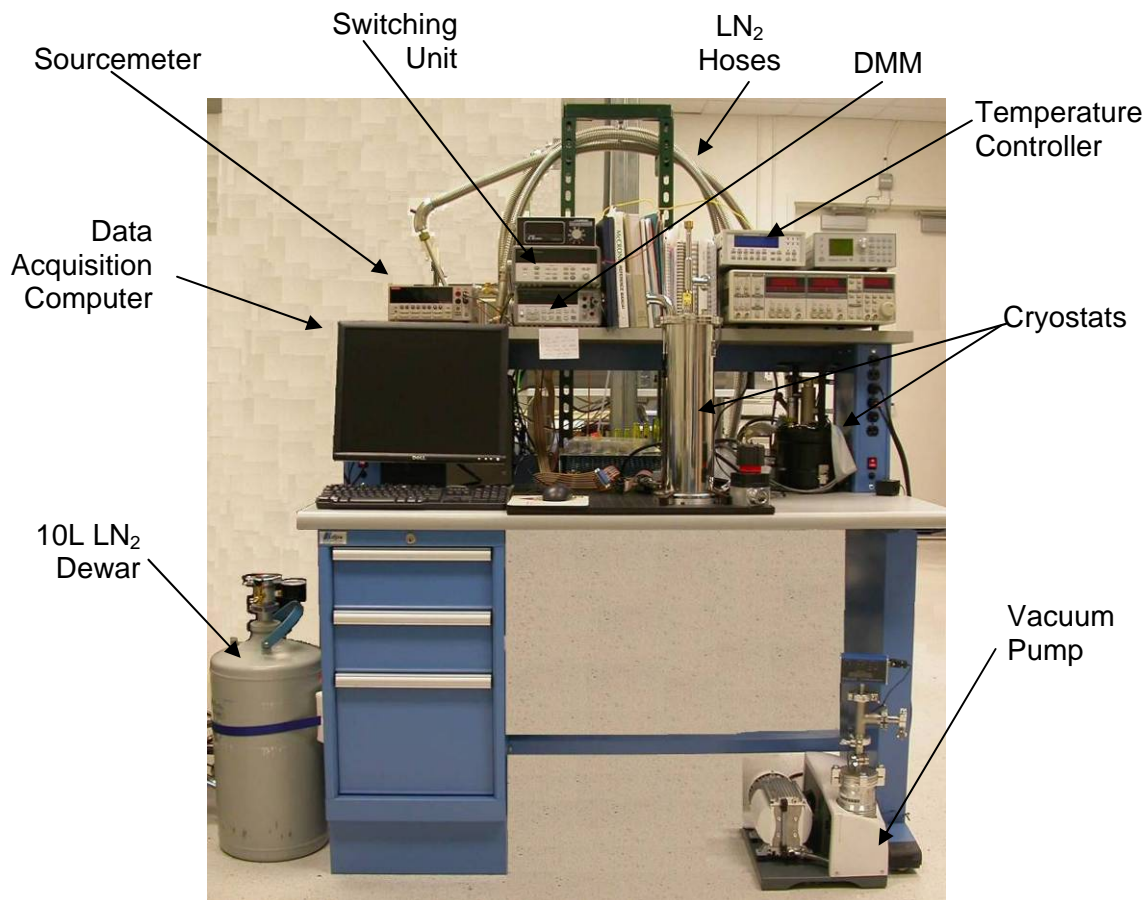


Figure 7: Work bench with thermal conductivity experiment equipment.

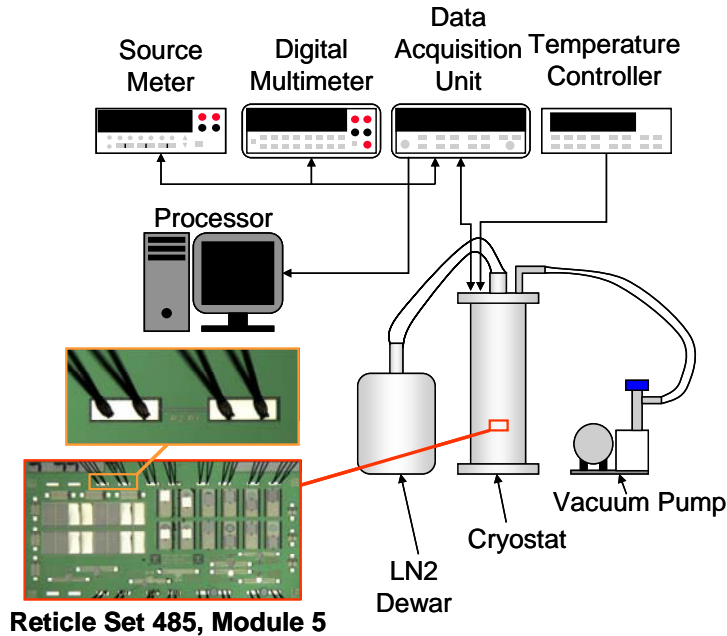


Figure 8: Schematic of thermal conductivity experiment layout.

For both cryostats, a sample is inserted into the cryostat at the beginning of a test. The equipment is then connected in the following order:

- 1) Electrical connections are made between the cryostat and the temperature controller and electronics for data acquisition.
- 2) The line from the vacuum pump to the cryostat is attached and the pump started. A cryostat is pumped down to a pressure below 1 mTorr before collecting data in order to minimize energy loss by convection from the test structures.
- 3) If low temperature testing is scheduled, the 10L LN₂ dewar is filled from an external supply (not pictured).
- 4) The 10L dewar is then attached to the cryostat by a LN₂ draw tube and hose.

Once the equipment is connected and turned on, the temperature controller is set to the desired temperature for the first measurement. After the target temperature and pressure are reached, a twenty minute temperature equilibration period is initiated. Upon completion of the temperature stabilization time, the data is collected using the data acquisition system as described in Sections 3.2.3 or 3.3.3.

3.2. Low Temperature Cryostat

3.2.1. Cryostat

The data set from 100K to 350K was collected using the Henriksen cryostat (Figure 9) which operates from 77K to 350K. The location on the cryostat into which the LN₂ hose is inserted is designated in Figures 9a and 9b. The cryostat is turned over and opened to show a sample in the cryostat in Figure 9c. The sample is held in place with a holder that is secured with four set screws. The sample and holder are then covered with a radiation shield and the bottom plate is attached via two hinged latches before the cryostat is turned over for testing.

3.2.2. LCC Package

Modules with intact test structures were wire bonded and packaged in a 68 pin Leadless Chip Carrier (LCC) for testing in the Henriksen cryostat (Figure 10). Two leads connect to the bond pads on each side of each test structure for four point probe measurements. Data is recordable from all eight test structures (P1P2 A and B, P2 A and B, P3 A and B, and P4 A and B) during a test. Wire bonds are connected to only two sides of the LCC package so that only two ribbon connectors are needed to convey electrical signals to and from the sample in the cryostat.

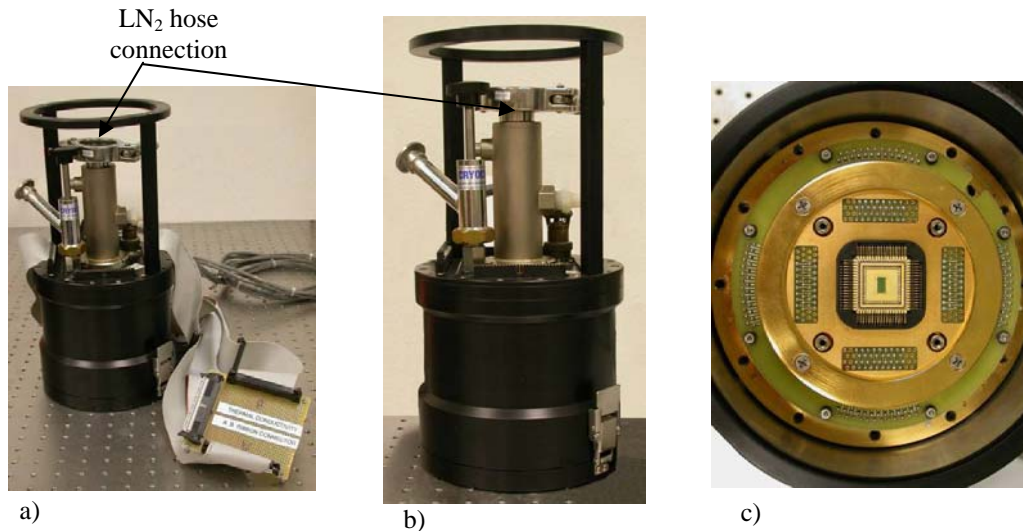


Figure 9: Henriksen cryostat: a) exterior with A/B ribbon connector, b) exterior, and c) interior sample chamber holding a packaged die.

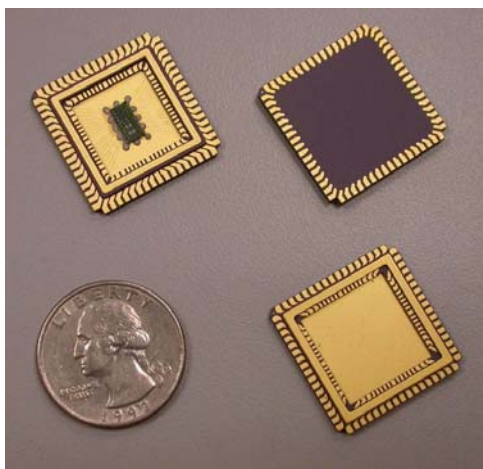


Figure 10: Clockwise from upper left: LCC with die; back of empty LCC; front of empty LCC.

3.2.3. Data Acquisition

3.2.3.1. Hardware

The equipment for thermal conductivity testing using the Henriksen cryostat consists of an Agilent 34401A Digital Multimeter (DMM), an Agilent 34970A Data Acquisition (DAQ) switching unit with two 20-channel multiplexer cards, a Keithley 2400 source meter, a Cryo-Con34 temperature controller, an A/B cable from each side of the device under test (DUT) leading to a circuit board combining the “A” and “B” sides to the connection with the DAQ, and a personal computer with a USB General Purpose Interface Bus (GPIB) connection.

3.2.3.2. Software

The data acquisition software for thermal conductivity testing is a LabView 7.1 executable program that sequences through the test structures at different current settings and saves the data to a file in a comma delimited (.csv) format. Figure 11 is a screen shot of the LabView data acquisition program for thermal conductivity testing using the Henriksen cryostat. The program is used to collect and record the data after the cryostat has stabilized and maintained a set temperature level for 20 minutes.

Resistance values were measured for each test structure prior to testing and are consistent with values calculated from the test structure geometries and electrical resistivity data in the literature. At room temperature, the resistance for P1P2, P3 and P4 test structures are between 180 Ω and 250 Ω ; the resistance of P2 structures is around 440 Ω . Before initiating data collection at a given temperature, the resistance can be measured by selecting the “Run” button in the Resistance Test box, verifying that the test structures and connections are in good working order.

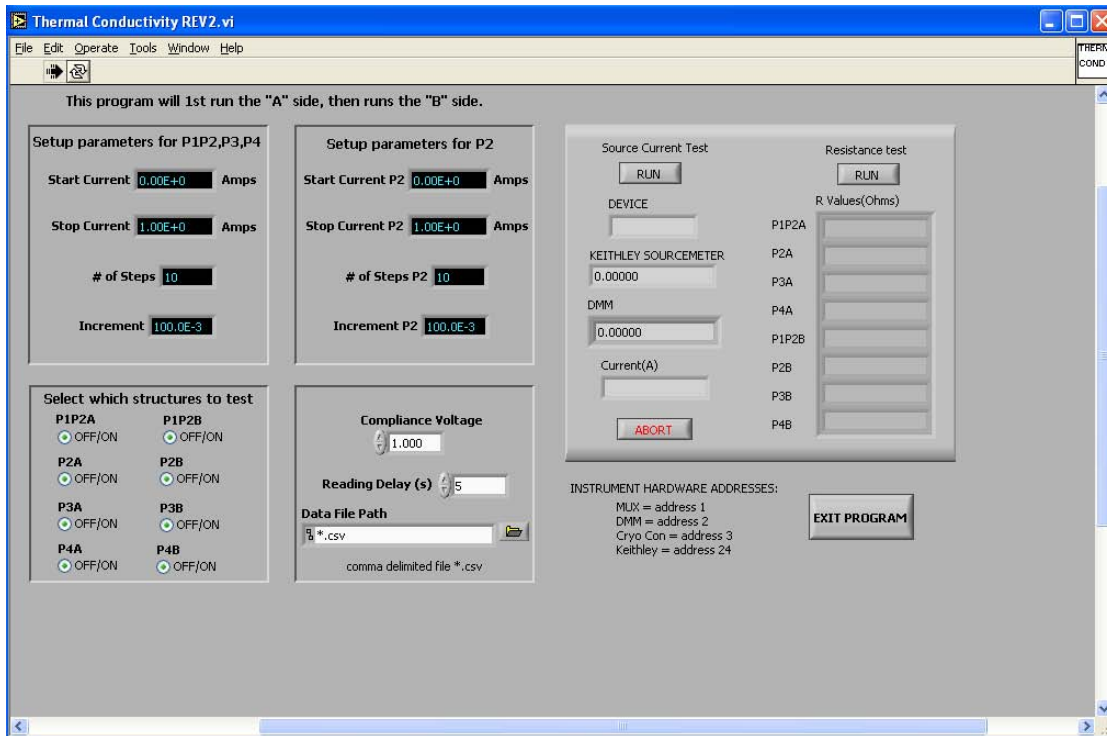


Figure 11: Screen shot of the data acquisition software for the Henriksen cryostat.

Prior to collecting data, the operator sets the following LabView parameters: which structures to test, stop current (in amps) for each type of structure, number of steps to reach the stop current, and the data file path (directory and file name where data is to be saved). For the tests, the stop currents are in the milliamp range so users need to enter the stop currents such as 2 mA as 2.0E-3 or 0.002 since the program is written for stop current inputs in amps.

Typical stop current values are 3.3 mA for P1P2, P3 and P4 structures and 2.0 mA for P2 structures. Hardcoded into the program is a 1 mA data recording step for each structure in order to provide a consistent current value for each structure for determining the temperature dependence of the resistance which is used in the data analysis process. The current increment values are automatically calculated by the program from the selected current limits and number of steps. Generally, they are at 0.1 mA or 0.2 mA per step.

Preset levels include the start current at 0 A; the compliance voltage at 1 Volt (to minimize the risk of damage to structures if current levels are accidentally set too high); and the reading delay at 5 seconds (to provide adequate time for the voltage to stabilize at each step).

To start the test, the Source Current Test “Run” button is selected. During testing, the program displays which structure (device) is being tested, the current being applied, and the voltage level registered by both the Keithley and Agilent meters. Measurements are recorded by the DAQ system from 0 mA up to the stop current at the specified current increments and then from the stop current back down to 0 mA. The program allows testing to be stopped, if necessary, by selecting the Abort button. This allows an operator to end a test if a device is exhibiting suspect voltage levels.

3.3. High Temperature Cryostat

3.3.1. Cryostat

The data set from 293K to 575K was collected using the Janis cryostat, pictured in Figure 12, which has temperature specifications of 77K to 700K. The exterior of the Janis cryostat is pictured in Figure 12a. The cold finger is removed from the outer shroud and pictured in Figure 12b. Note that there is a secondary radiation shield surrounding the sample connection area at the end of the cold finger. Figure 12c is a picture of the copper plate at the end of the cold finger with the radiation shield removed. The wires that connect to the pins on the Alphaprobes holder and enable the electrical connections with the source meter and multimeter, described in the next section, are clearly visible in Figure 12c. A thermocouple was connected to the back of the copper plate behind the sample location in order to provide temperature measurements closer to the sample than those obtained for the temperature controller thermocouple which is at the base of the copper sample holder plate.

3.3.2. Alphaprobes Sample Holder

The Alphaprobes sample holder pictured in Figure 13 has 40 lead pins connected to 40 probes. Each probe is aligned so it makes electrical contact with the corresponding die bond pad on a module. Two leads connect to the bond pads on each side of each test structure for four point probe measurements. Figures 13b and 13c specify the bond pad location corresponding to a given pin on the Alphaprobes holder.

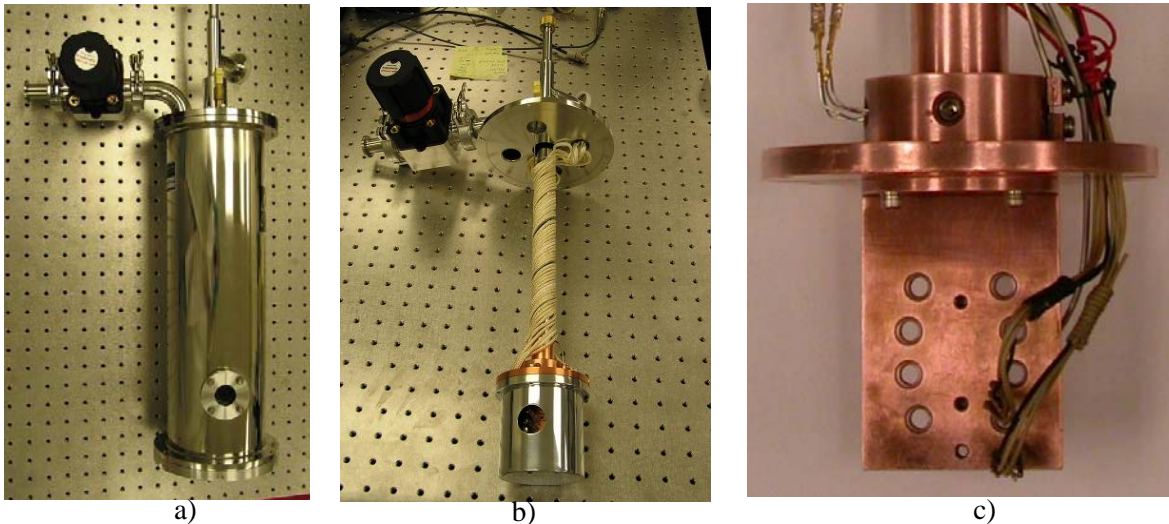


Figure 12: Janis cryostat: a) exterior, b) cold finger removed from the outer shroud with radiation shield around the sample area, and c) sample holder area with electrical wires for connection to Alphaprobes holder.

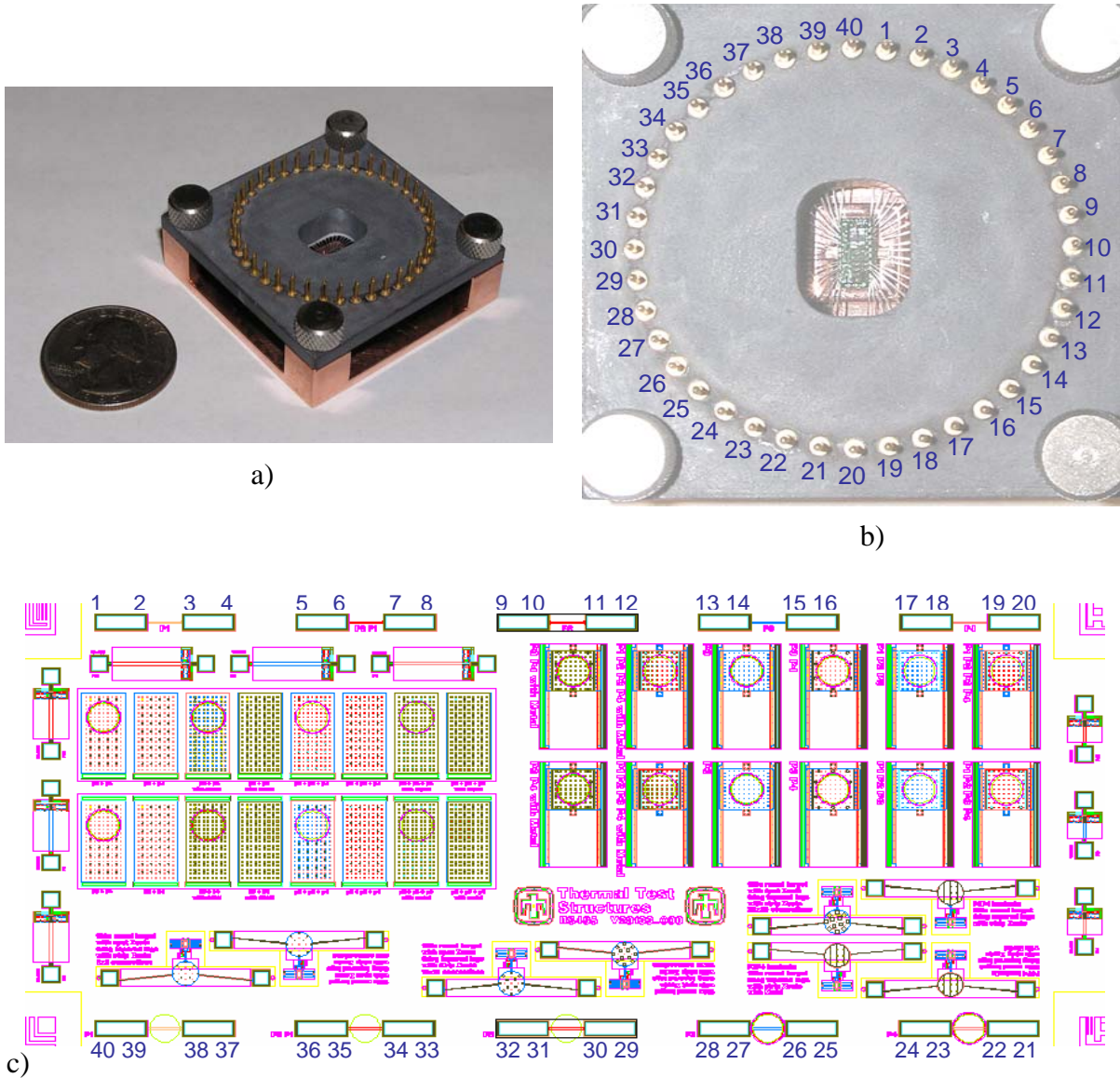


Figure 13: Electrical connections to sample in Janis cryostat: a) Alphaprobes holder, b) top view of the holder with the lead numbers, and c) schematic of module with lead numbers next to corresponding probe locations on bond pads.

Only two structures can be tested at a time due to wiring constraints in the Janis cryostat. After an intact sample is secured in the holder and the electrical connections are made to the pins for the two structures to be tested, resistance tests are performed to verify that good electrical connections have been made. After a testing cycle is completed for those two structures, the cryostat must be opened in order to switch the test structures to be tested. Two different structures are connected for the next test, either on the same die or on a new sample. Typically, a new sample is used as the quality of the electrical connections for a sample which has undergone testing up to 575K were not of sufficient quality for the next test.

3.3.3. Data Acquisition

3.3.3.1. Hardware

The equipment for thermal conductivity testing using the Janis cryostat consists of an Agilent 34401A DMM, an Agilent 34970A DAQ switching unit with two 20 channel multiplexer cards, a Keithley 2400 source meter, a Lakeshore 331 temperature controller, an Omega MDSSi8 series thermocouple reader, and a PC with a USB GPIB connection.

3.3.3.2. Software

The software for the thermal conductivity testing is a LabView 7.1 executable program that sequences through the devices at different current settings and saves the data to a file in a comma delimited file format similar to the program for the Henriksen cryostat. Figure 14 is a screen shot of the LabView data acquisition program for thermal conductivity testing using the Janis cryostat. The data acquisition program is used to collect and record the data after the cryostat has stabilized and maintained a set temperature level for 20 minutes.

Prior to collecting data, the operator sets the following parameters in the LabView program: selecting and labeling which two structures are to be tested, stop current (in amps) for each structure, number of steps to reach the stop current, and the data file path (directory and file name where data is to be saved). The current increment values are automatically calculated by the program from the selected current limits and number of steps. For the tests, the stop currents are in the milliamp range so users need to enter the stop currents such as 2 mA as 2.0E-3 or 0.002 since the program is written for stop current inputs in amps.

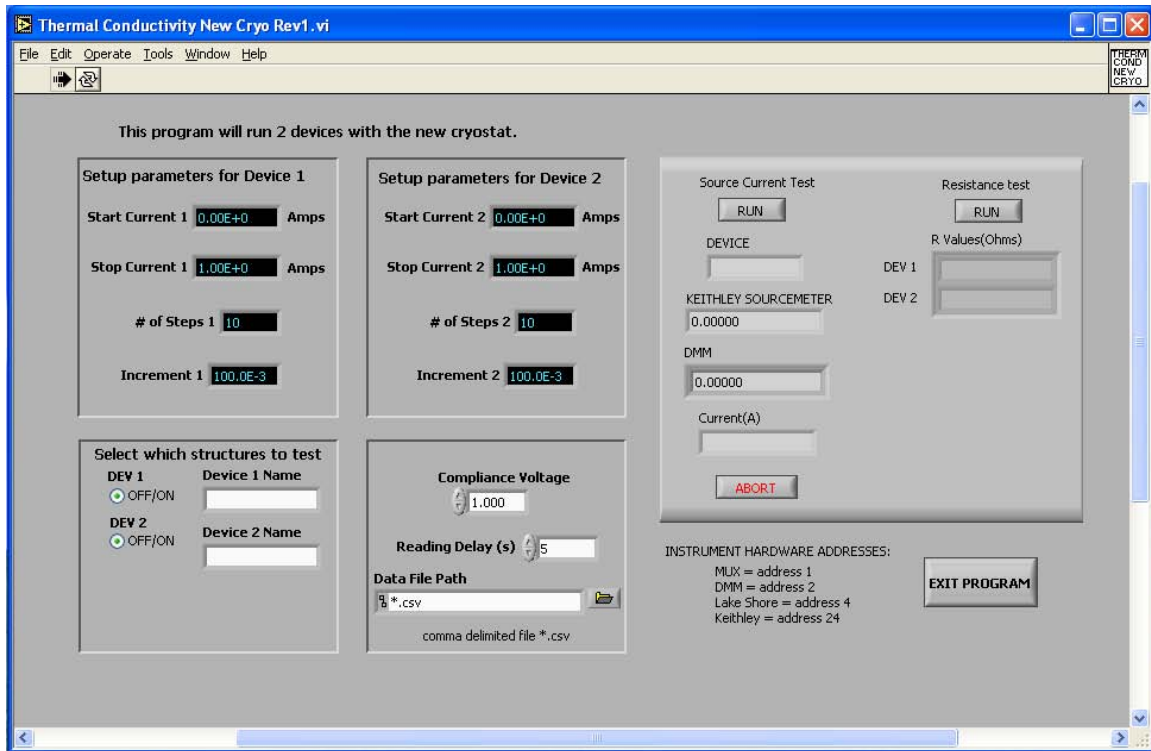


Figure 14: Screen shot of the thermal conductivity data acquisition software for the Janis cryostat.

The stop current values are set so the measured voltage across a test structure does not exceed 1 Volt. Since the electrical resistance of the test structures increases as the temperatures increases, the voltage at the maximum current is monitored and decreased as necessary. Typically, stop current values for P1P2, P3 and P4 structures are set at 3.3 mA at temperatures between 85 K and 555 K, and 3.0 mA at 575 K to keep the maximum voltage below 1 Volt. P2 structures are stopped at 2.0 mA at temperatures between 85 K and 415 K, at 1.8 mA between 415 K and 555 K, and at 1.6 mA at 575 K.

Hardcoded into this program also is a 1 mA step for each structure to provide a consistent current value for each structure for determining the temperature dependence of the resistance which is used in the data analysis process. Preset levels include the start current at 0 A, compliance voltage at 1 Volt, and reading delay at 5 seconds.

To start the test, the Source Current Test “Run” button is selected. During testing, the program displays which structure (device) is being tested, the current being applied, and the voltage level registered by both the Keithley and Agilent meters. Measurements are recorded by the DAQ system from 0 mA up to the stop current at the specified current increments and then from the stop current back down to 0 mA. The program allows testing to be stopped, if necessary, by selecting the Abort button. This allows the test operator to end a test if a device is exhibiting suspect voltage levels.

3.4. Data Analysis

Figure 15 shows the steps involved in data collection and processing for the steady state resistance technique, based on the theory discussed in Section 3.1.1. The resistance versus temperature curve slope is determined and utilized for the determination of the thermal conductivities. Since this is a key parameter in calculating the thermal conductivity, the data analysis is performed once data has been collected over the entire temperature range. In cases where thermal conductivity is calculated prior to collecting data over the entire temperature range, a value for the slope of the electrical resistance versus temperature is entered into the data analysis program based on previous measurements. A MATLAB routine was created to complete the data analysis.

3.4.2. Calculation of Thermal Conductivity

Using the value of the electrical resistance versus temperature slope for each layer, we calculate the value of m from Equation 6 for each data set. When only one of the test structures for a given layer is tested for a module, the value of the electrical resistance for that test structure is used to compute m . When analyzing the data from a module for which both the A and B test structures for a particular layer are tested on the module, the slope used to calculate m for that layer is the average of the slopes from the two test structures. In this illustrative example, the slope from Fig. 16 is used for the data analysis. In order to calculate the thermal conductivity, the simplex method for solving nonlinear equations was implemented to correlate the measured data points to the average resistance from the model in Eq. 8. The plot of resistance versus current in Figure 17 contains model results and measured data. In this case, the calculated thermal conductivity was 49.8 W/mK. The steeper the curve of the resistance versus current, the lower the thermal conductivity value, while the more gradual the curve the higher the thermal conductivity value. The thermal conductivity is calculated for each of the test structures for which data was collected at a given temperature. Figure 18 displays thermal conductivity values calculated at all of the data collection temperatures for the P1P2A test structure on Die 1. The calculation of thermal conductivity is repeated for all of the tested structures on a module and the results provided in Section 4.

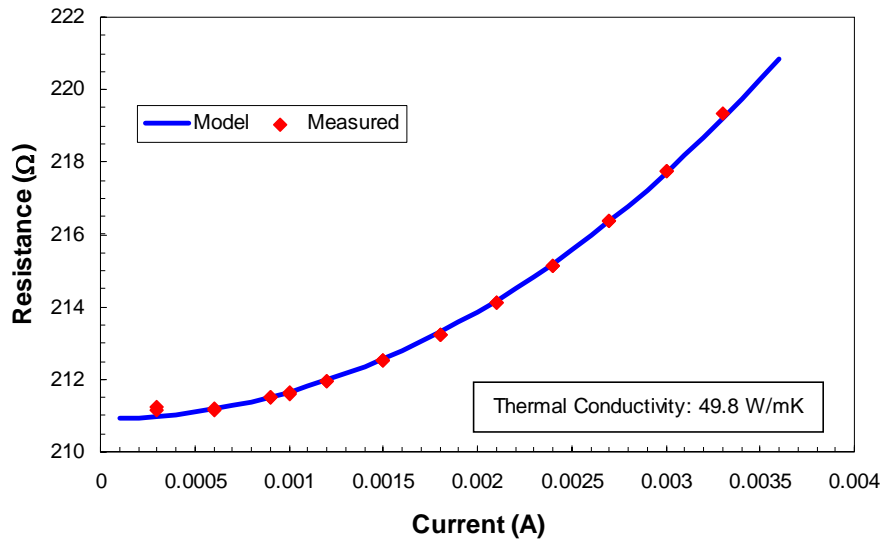


Figure 17: Electrical resistance versus current at 293K for the P1P2A test structure on Die 1. The model line is the best fit from the data analysis MATLAB routine and corresponds to a thermal conductivity of 49.8 W/mK.

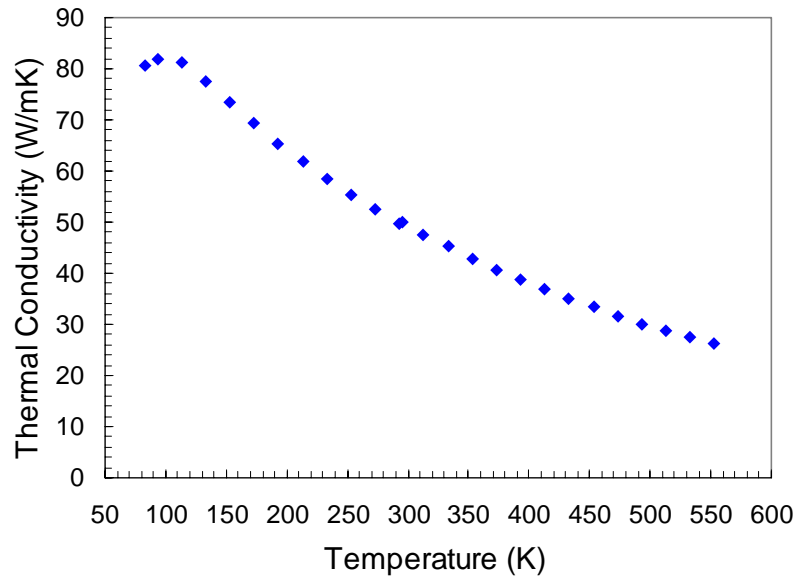


Figure 18: Thermal conductivity vs. temperature for P1P2A test structure on Die 1.

3.4.3. Sensitivity Analysis

A sensitivity analysis was conducted for the calculation of thermal conductivity. The analysis indicated that for Eqs. 6 and 8 a change in the $(R_0\alpha)$ term or length, L , resulted in a near linear change in the thermal conductivity while a change in the thickness, t , or width, w , resulted in a nonlinear change in thermal conductivity, as illustrated in Figure 19. The similarity in response for w and t , and the $(R_0\alpha)$ term and L , are because the paired variables are linearly proportional. Similarly, the variation in the response is a result of the inverse relationship of (wt) and $(R_0\alpha L)$ evident in Eqs. 6 and 8.

Estimates of the expected variation in these variables provide insight into the impact of the sensitivity of the thermal conductivity calculation to these variables. The length is known accurately to within $\pm 0.5\%$. The widths of SUMMiT structures are known to be 0.1-0.15 μm per side less than the designed value, leading to 1-1.5% difference in the width. A $\pm 0.1 \mu\text{m}$ variation in thickness corresponds to 6.7% for the P2 layer and 4.4% for the P1P2, P3, and P4 layers. When examining the electrical resistance versus temperature slope data, the P1P2, P3, and P4 layers have minimum and maximum values that are $\pm 1\text{-}3\%$ from the average value. The minimum and maximum values in the P2 slope are $\pm 3\text{-}6\%$ from the average. Combining these estimates with the sensitivity analysis results predicts that the P2 thermal conductivity data is more sensitive and likely to have more variation compared to the P1P2, P3, and P4 data due to its being thinner and having a higher percentage change in the electrical resistance versus temperature slope. Also, it is expected that variations in the thickness and slope of the electrical resistance versus temperature curve have a larger effect on the thermal conductivity calculation due to larger variations in these values than in the length and width.

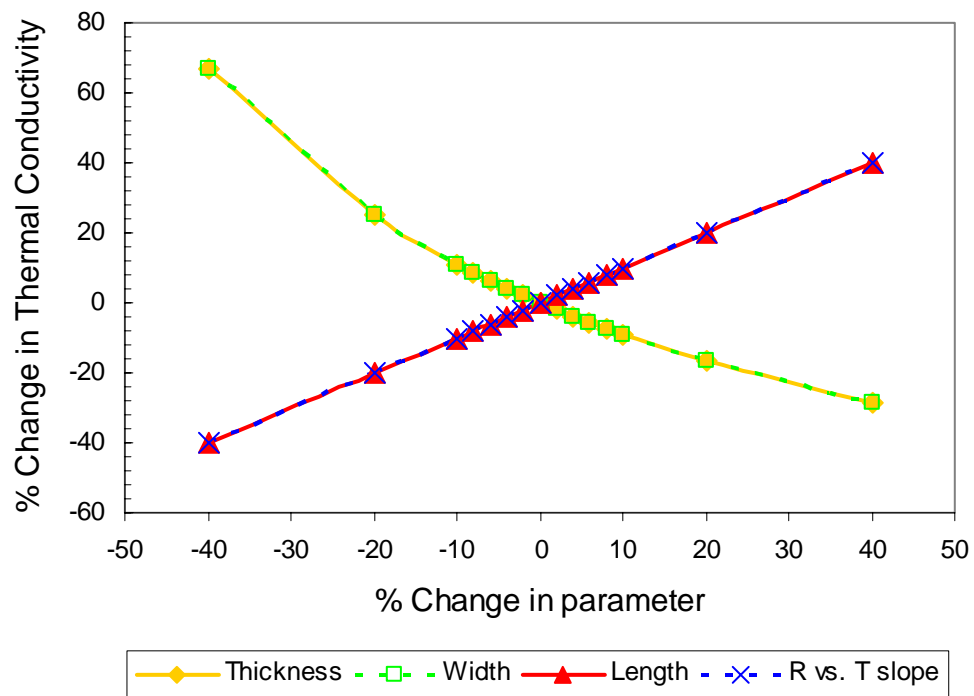


Figure 19: Percent change in thermal conductivity with variations in the thickness, width, length, and slope of resistance versus temperature

4. THERMAL CONDUCTIVITY EXPERIMENTAL RESULTS

This section presents the experimental results from the research project to measure thermal conductivities of SUMMiT™ V layers. Since the steady state resistance technique is an electrically based method, temperature dependant electrical resistance and resistivity are measured during the process and these results are presented. The thermal conductivity data obtained due to the data analysis are then plotted versus temperature for each temperature range, for each layer, in a graph summarizing the thermal conductivity data, and then in a graph in which they are compared to previously available thermal conductivity data.

4.1. Electrical Resistance versus Temperature

Figure 20 graphs the electrical resistance as a function of temperature for the P1P1, P2, P3, and P4 SUMMiT layers and specifies the equations for the best linear fit of the data. As discussed in Section 3, the voltage measured by the digital multimeter is recorded at a current of 1 mA twice at a given temperature, once as the current is being increased to the maximum value and again when it is being decreased. The recorded current and voltage values are used to calculate the electrical resistance. As seen in Figure 20, the electrical resistances for all layers increase with temperature as expected. The electrical resistances for the P1P2 and P4 layers are very close (within 3%) to each other. The electrical resistance of the P3 layer is approximately 10% lower than that for the P1P2 and P4 layers, while the P2 layer has the highest electrical resistance. This is due both to the geometrical effect due to the P2 test structures having the smallest cross sectional areas since their thicknesses are the lowest, 1.5 μm , and due to differences in the doping.

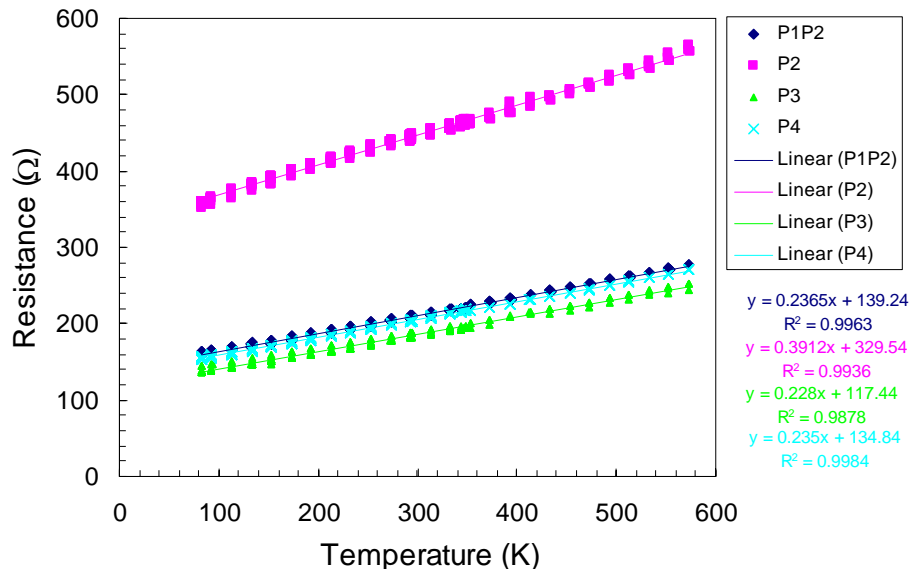


Figure 20: Electrical resistance versus temperature for the tested SUMMiT layers.

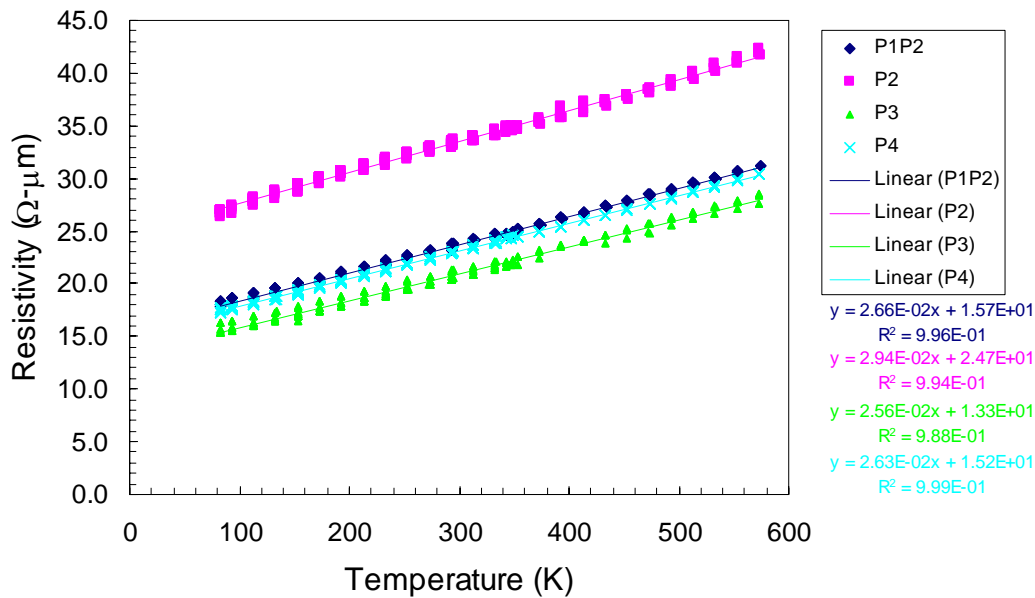


Figure 21: Electrical resistivity versus temperature for the tested SUMMiT layers.

4.2. Electrical Resistivity versus Temperature

Figure 21 graphs the electrical resistivities as a function of temperature for the P1P1, P2, P3, and P4 SUMMiT layers and specifies the equations for the best linear fit of the data. The electrical resistivities are calculated from the measured electrical resistances in Figure 20 according to the equation $\rho = R (A/L)$ where ρ is the electrical resistivity, R the electrical resistance, A the cross sectional area, and L the length. The cross sectional area A is the product of the thickness, t , and the width, w . The width and length of the four test structures are 10 μm and 200 μm , respectively. The thickness for the P2 test structure is 1.5 μm , and the P1P2, P3, and P4 test structures are 2.25 μm thick. The P1P2 thickness is a measured value for the RS 485 run. As seen in Figure 21, the electrical resistivity for all layers increases with temperature like the electrical resistance. Since the difference in area between the test structures for the layers is accounted for in the electrical resistivity unlike the electrical resistance, the P2 values are closer to the P1P2, P4, and P3 values. The P2 electrical resistivity is still significantly higher than the P1P2, P4, and P3 values due to lower doping as is apparent in Figure 21.

4.3. Thermal Conductivity versus Temperature

The thermal conductivity is graphed as a function of temperature for the SUMMiT V P1P2, P2, P3, and P4 polysilicon layers in Figure 22 for the temperature range from 100K to 350K. These measurements were conducted using the Henriksen cryostat as described in Section 3.2. The lowest temperature measurements actually are at 83K as the chamber was operational below 100K. As the temperature decreases from 350K, the thermal conductivities increase. The four layers do not exhibit identical thermal conductivities which is significant as previous SNL thermal conductivity data was measured for a single layer. The dependence with temperature for

the P2 layer also differs from that of P1P2, P3, and P4 layers. Below 233K, the thermal conductivity of the P2 layer plateaus and then decreases. Although the P1P2, P3, and P4 behave similarly as a function of temperature, the thermal conductivities of the P1P2, P3, and P4 layers continue to increase with decreasing temperature until 93K and then decrease. The P1P2 thermal conductivities are lower than the P4 which are slightly lower than the P3.

Figure 23 graphs the thermal conductivity as a function of temperature for the SUMMiT V P1P2, P2, P3, and P4 polysilicon layers for a temperature range including 293K to 575K. These measurements were conducted using the Janis cryostat as described in Section 3.3. Since the Janis cryostat was capable of operating with liquid nitrogen, the lowest temperature measurements were at 83K, providing overlap with the data set from 100K to 350K obtained in the Henriksen cryostat. Data obtained in both cryostats are available for comparison over the temperature range from 83K to 350K. Good agreement exists for the data collected in the two cryostats with similar trends observed in Figure 23 and Figure 22. As the temperature increases above 350K, the thermal conductivities continue to decrease. Additionally, the difference in the thermal conductivity data for the four layers decreases at higher temperatures.

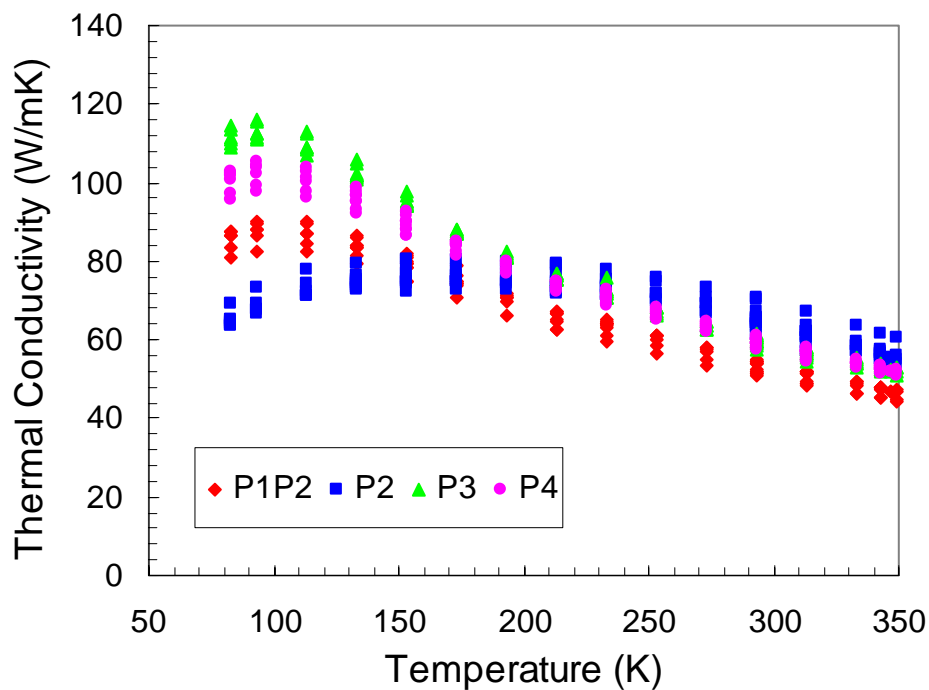


Figure 22: Thermal conductivity data versus temperature for the temperature range 100K from 350K.

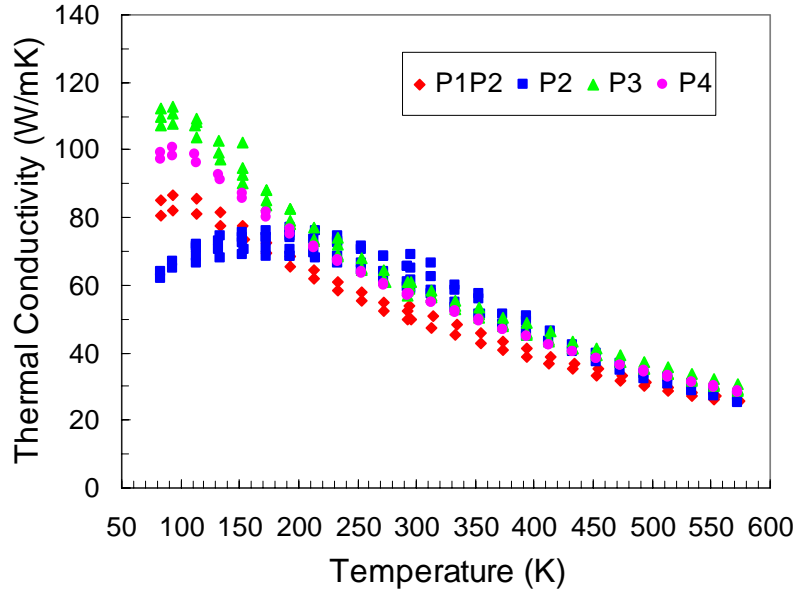


Figure 23: Thermal conductivity data versus temperature for the temperature range 293K from 575K. Data was collected down to 83K to increase the overlap with the data from 100K to 300K.

Figures 24-27 plot the thermal conductivity as a function of temperature for each of the P1P2, P2, P3, and P4 test structures with the data from both cryostats on a single graph. The die and test structure for the data is specified. Also, on Figs. 24-27 are the empirical fits to the data for each of layers that are given in Eqs. 9-16 in which the T is in Kelvin. Figs. 24-27 clearly show the consistency and reasonable agreement between the data taken using the Henriksen and Janis cryostats. The P2 data has the largest spread between highest and lowest data points, around 20% from minimum to maximum value, at low temperatures. The experimental measurements were performed twice for Die 3 in the Henriksen cryostat and Die 37 in the Janis cryostat and the measurement repeatability with the same test structure was good within $\pm 5\%$ for Die 3 and $\pm 3\%$ for Die 37. The number of samples tested is small due to the limited number of testable samples and time required to complete the tests. Much of the testing time is determined by the temperature stabilization periods. The effect of the Bosch isolation hole under a P4 test structure could not be clearly distinguished due to the experimental uncertainty indicating that an intact substrate does not significantly increase the heat transfer from a P4 test structure.

$$\text{P1P2: } k = 2.281774 \cdot 10^{-5} T^3 - 1.099149 \cdot 10^{-2} T^2 + 1.518364 T + 21.77175 \text{ for } 83\text{K} \leq T \leq 173\text{K} \quad (9)$$

$$k = 6.842156 \cdot 10^3 T^{-6.124836e-3} - 6.555521 \cdot 10^3 \text{ for } 173\text{K} \leq T \leq 573\text{K} \quad (10)$$

$$\text{P2: } k = 2.009513 \cdot 10^{-6} T^3 - 2.079541 \cdot 10^{-3} T^2 + 0.5446507 T + 33.04350 \text{ for } 83\text{K} \leq T \leq 333\text{K} \quad (11)$$

$$k = 1.047025 \cdot 10^3 T^{-0.1229262} - 454.6325 \text{ for } 333\text{K} \leq T \leq 573\text{K} \quad (12)$$

$$\text{P3: } k = 2.532847 \cdot 10^{-5} T^3 - 1.200034 \cdot 10^{-2} T^2 + 1.505219 T + 54.53700 \text{ for } 83\text{K} \leq T \leq 193\text{K} \quad (13)$$

$$k = 750.7730 T^{-0.1416520} - 275.8501 \text{ for } 193\text{K} \leq T \leq 573\text{K} \quad (14)$$

$$\text{P4: } k = 2.615225 \cdot 10^{-5} T^3 - 1.220266 \cdot 10^{-2} T^2 + 1.594555 T + 35.62111 \text{ for } 83\text{K} \leq T \leq 193\text{K} \quad (15)$$

$$k = 5.858570 \cdot 10^3 T^{-8.139494e-3} - 5.535406 \cdot 10^3 \text{ for } 193\text{K} \leq T \leq 573\text{K} \quad (16)$$

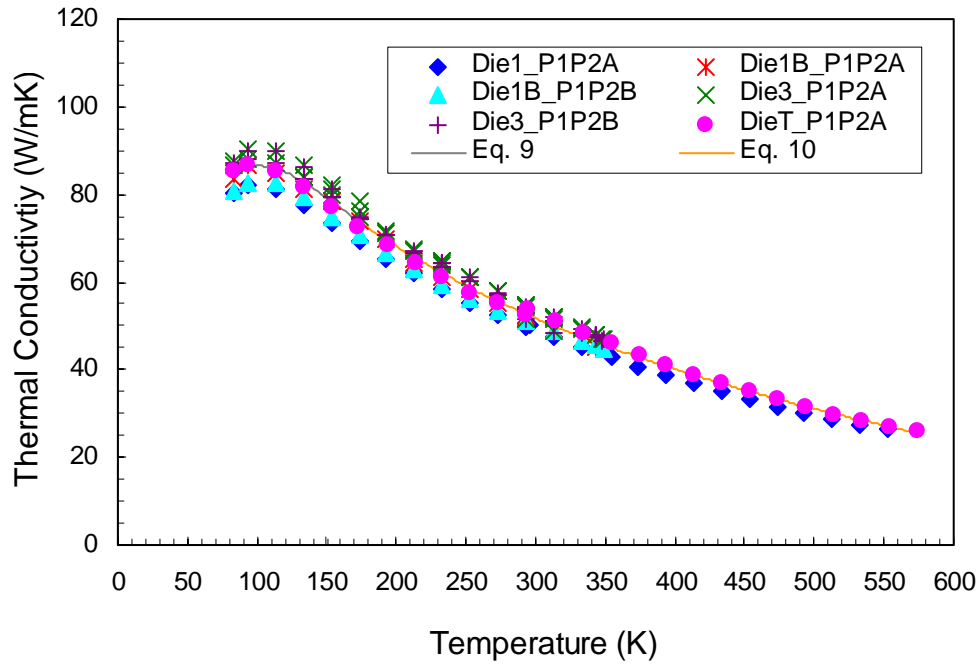


Figure 24: Thermal conductivity data versus temperature for P1P2 samples.

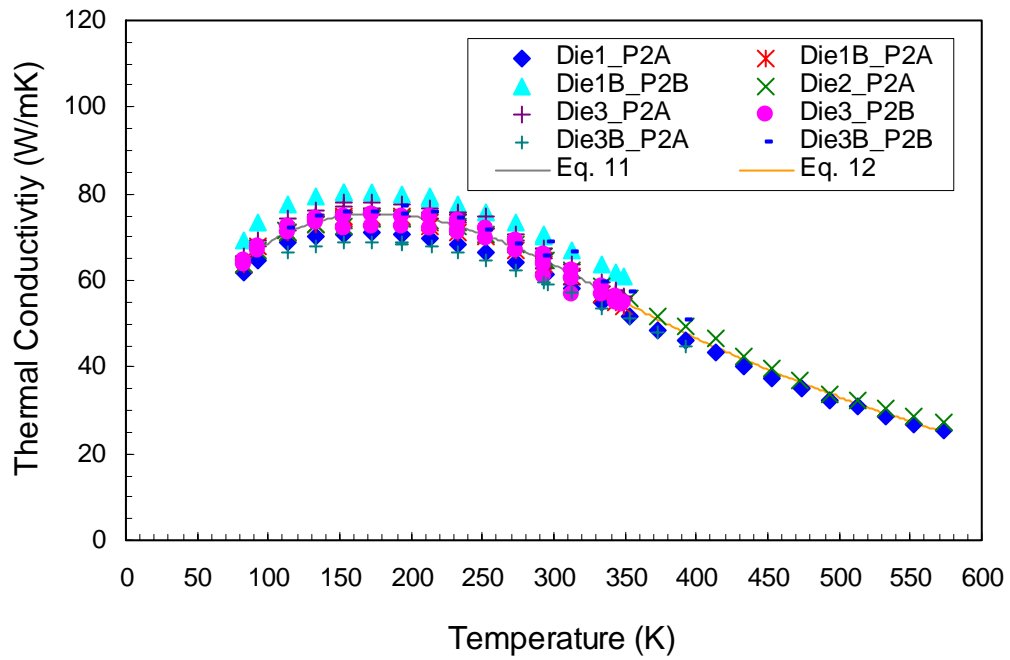


Figure 25: Thermal conductivity data versus temperature for P2 samples.

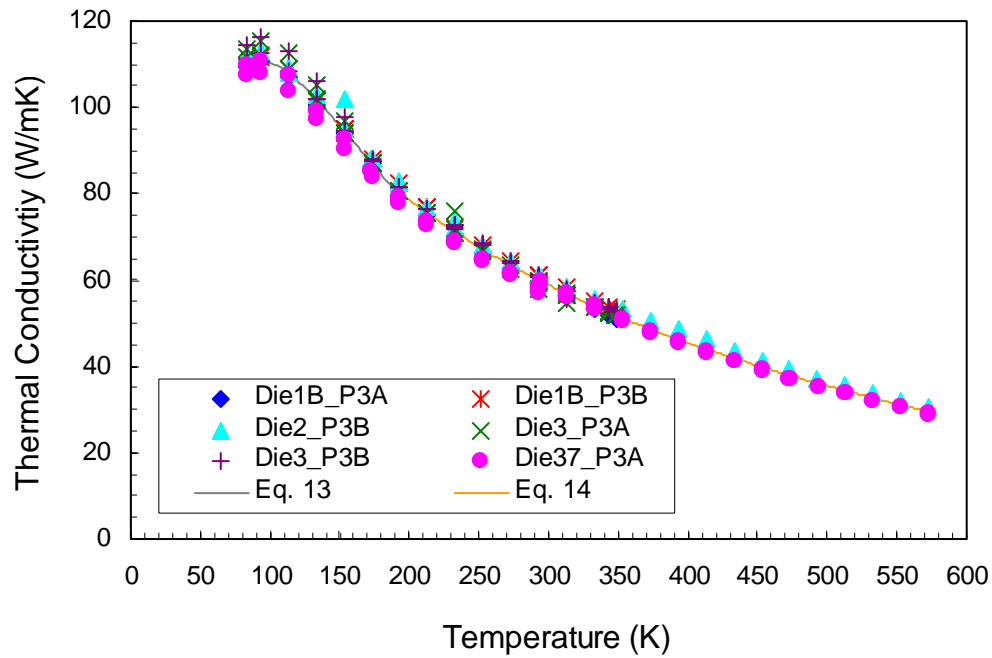


Figure 26: Thermal conductivity data versus temperature for P3 samples.

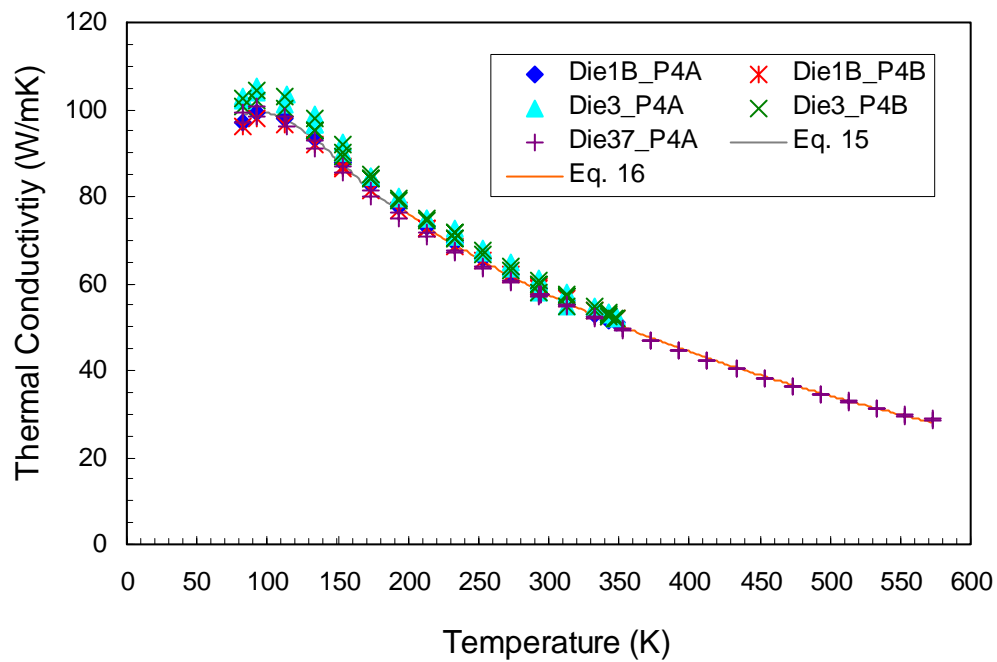


Figure 27: Thermal conductivity data versus temperature for the P4 samples.

Figure 28 summarizes all of the thermal conductivity data for the P1P2, P2, P3, and P4 SUMMiT layers. The current measurements are the first reported data establishing that the thermal conductivity is a function of each particular SUMMiT layer. Also, the P2 layer has a different variation in thermal conductivity from the P1P2, P3, and P4 layers as the temperature is decreased. As the temperature increases above room temperature, the difference in thermal conductivity for the layers decreases.

Figure 29 shows the measured P1P2, P2, P3, and P4 data comparing the existing thermal conductivity data that was presented in Section 1. Above 300K, the current data lies in the range of previously existing data although below the previously measured SNL data. At lower temperatures, the current data is higher than other measurements. Further work is needed to understand these differences.

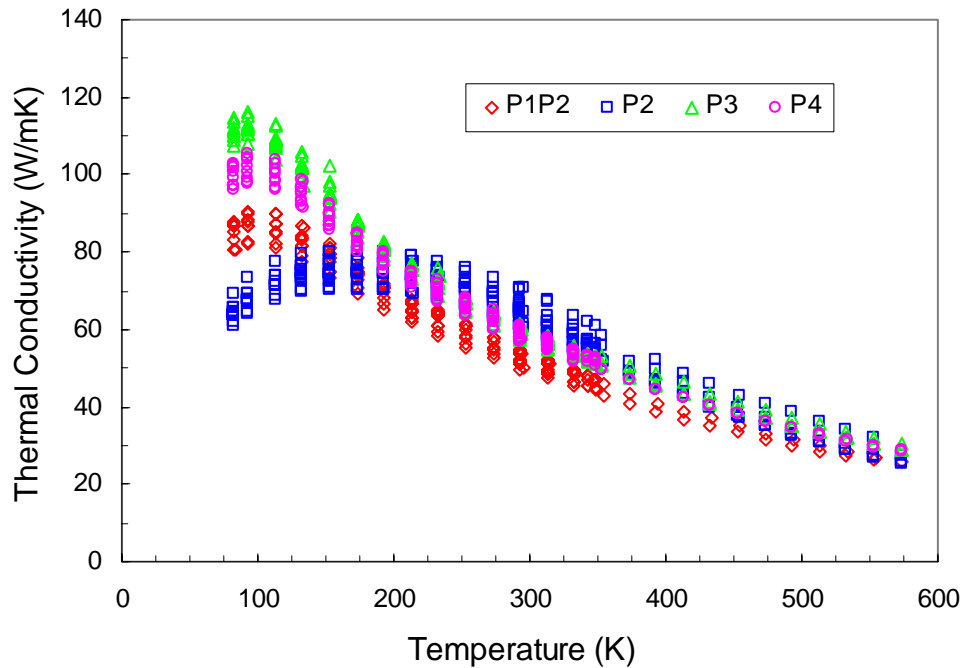


Figure 28: Thermal conductivity data versus temperature for four polysilicon layers.

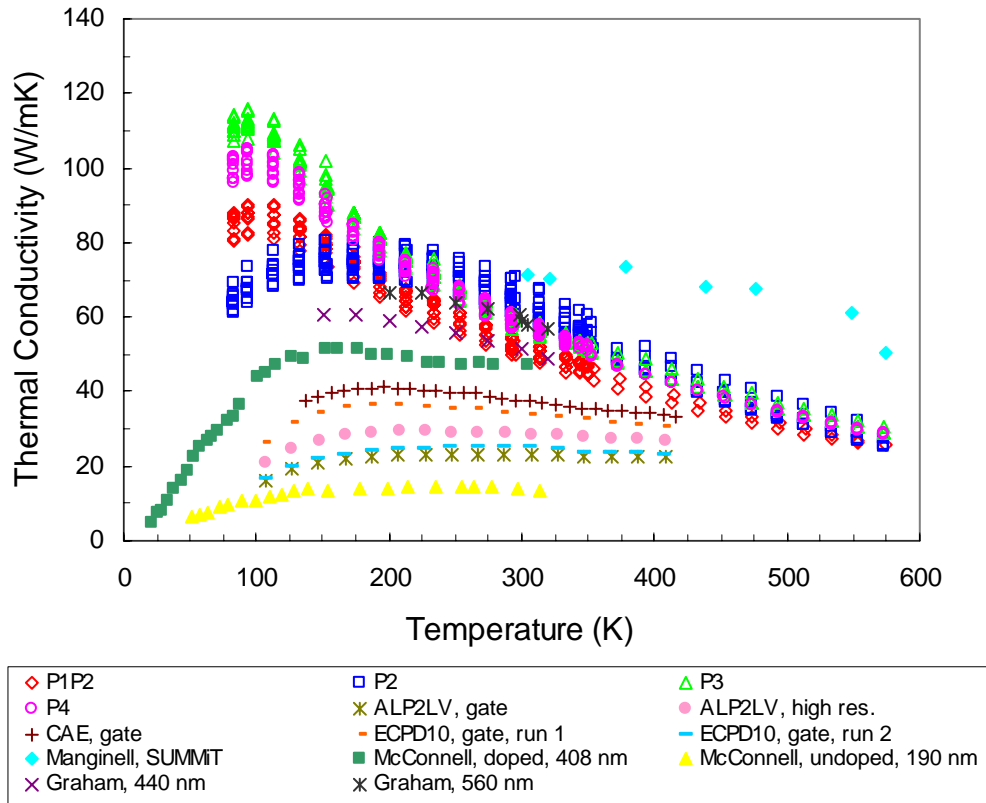


Figure 29: Thermal conductivity versus temperature for averages of the measured data compared to existing thermal conductivity data.

4.4. Measurement Uncertainty

Due to the limited number of samples and long test times, the thermal conductivity data presented in this report has limited statistics for quantifying measurement uncertainty. This section discusses model assumptions and experimental conditions contributing to uncertainty in the thermal conductivity so readers can assess the data. Simulations of the test structure were performed to investigate the impact of fillets on the test structure. The effect of bond pad heating is also discussed.

4.4.1. Experimental Uncertainty

A small number of samples and long test times limited the experimental data collected. For two dice, the data was collected twice with the same die. In the Henriksen cryostat, Die 3 was tested twice over the temperature range from 83K to 349K. The agreement for the thermal conductivity measured at a given temperature was $\pm 4\%$ for P1P2, $\pm 5\%$ for P2, $\pm 5\%$ for P3, and $\pm 5\%$ for P4. In the Janis cryostat, Die 37 was tested twice with the agreement for the P3A test structure being $\pm 3\%$ and for the P4A being $\pm 2.5\%$. When all of the data collected for a given

layer is examined the spread of the minimum to the maximum from the average is $\pm 6\%$ for P1P2, $\pm 10\%$ for P2, $\pm 7\%$ for P3, and $\pm 5\%$ for P4.

The data analysis model assumes one dimensional conduction with no losses due to convection or radiation from the beam and calculates a constant k for the test structure. Since the cryostats are evacuated to less than a 1 mTorr prior to collecting data, the assumption of no heat loss from the beam to the environment is considered reasonable and unlikely to contribute significantly to uncertainty in the measurement.

The presence of a temperature distribution in the test structure subject to an applied current raises two issues in the thermal conductivity data: 1) the actual temperature at which the thermal conductivity is determined and 2) the effect of considering the thermal conductivity as constant instead of temperature dependant in the data analysis. In order to calculate the thermal conductivity at a chamber temperature, data is collected at a range of currents and the temperature distribution in the test structure at these currents varies. For example, for the P1P2, P3, and P4 samples, the applied currents range from 0.3 mA to 3.3 mA at 293K. At currents at or below 1.5 mA the maximum temperature in the test structure is 9K and average temperature 6K above the chamber temperature. At the highest current, 3.3 mA, the maximum temperature is 43K and average temperature 23K above the chamber temperature. Thus, the test structure temperature is above the chamber temperature although by increasing amounts as the current is increased. The maximum current in the test was selected so the average temperature in a test structure would not exceed 30K. Since the thermal conductivity is calculated by fitting to the data at all currents, an optimal correction for the temperature of the test structure is not clear. The data reported in this section are plotted as a function of the chamber temperature and are not corrected to reflect the increase in the test structure during the test. When examining the regions of steepest slope in the thermal conductivity data, the k can vary by up to 15% over a 30K temperature range. An iterative data analysis procedure that considers the temperature dependence of the thermal conductivity could be used. It would need development effort and require more computation time than the current technique.

As discussed in Section 3.4.3 the thermal conductivity calculation is sensitive to variations in the length, width, thickness, and electrical resistance versus temperature slope values. In particular, variations in the thickness and slope of the electrical resistance are expected to have more impact than the other variables.

4.4.2. Simulation of a Test Structure

To further assess weaknesses inherent to the one-dimensional solution used to recover thermal conductivity from the measured resistance, simulations of the test structure were performed using the ASC/SIERRA application Calore. In particular, the simulations were undertaken to determine the effect of the fillets added for structural reasons where the beam meets its anchor. The simulation results also provide insight into the effects of bond pad heating on the assumption of constant temperature at the edges of the test structure.

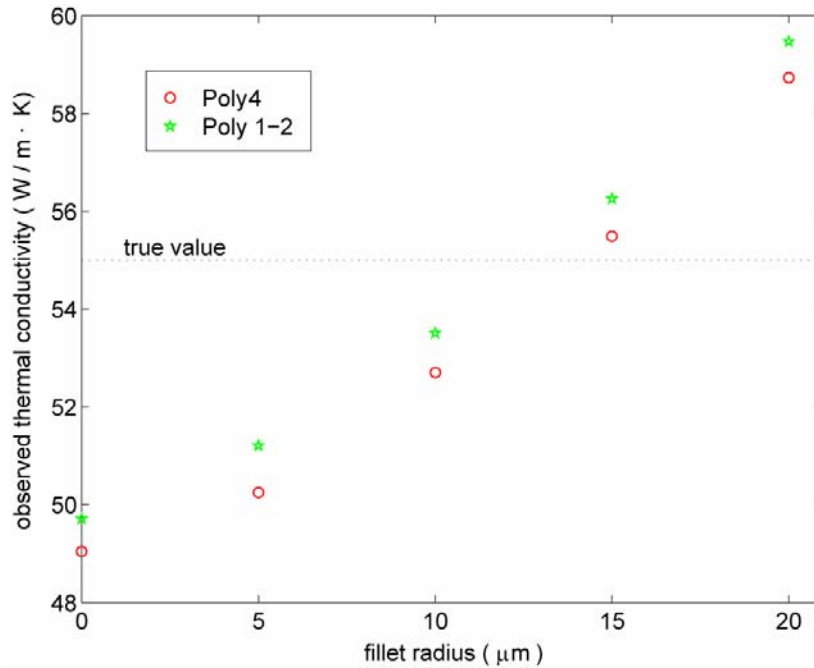


Figure 30: Perceived thermal conductivity for poly4 and poly1-poly2 beams with a range of fillet radii.

All simulations were performed with a fixed thermal conductivity of 55 W/m·K and a resistivity versus temperature slope of 0.0263 $\Omega \cdot \mu\text{m}/\text{K}$. The observed resistivity was calculated by dividing the observed voltage by the specified current and the perceived thermal conductivity was recovered from a series of simulations using the same MATLAB script used to process the measured data.

The results of a series of simulations performed for a range of fillet sizes are shown in Figure 30. From this figure, it may be observed that beams with a small fillet yield an observed thermal conductivity that is actually closer to the true value than beams with square ends. This result is contrary to the intuitive expectation that the square-edged beam would more closely reflect the one-dimensional structure assumed in the MATLAB script.

The physical reason for this discrepancy may be discerned by comparing the temperature distribution for a square-edged beam to that of a 5 μm fillet case. Such distributions are presented in Figure 31. From this figure, it can be observed that, contrary to the assumption contained in the one dimensional model, the temperature does not immediately reach the substrate temperature at the beam end; because the anchor is some distance above the substrate, it warms slightly. The fillet helps to combat the warming of the anchor by spreading the heat to a larger area at the attachment point. The larger bias observed in Figure 30 for the poly4 beam than for the poly1-poly2 beam reflects its larger distance from the substrate. As the fillet radius increases past a certain value, which varies depending on distance from the substrate, the perceived thermal conductivity increases above the true value. This is a consequence of a larger portion of the beam having a cross section larger than the nominal value used in the analytical solution. Based on the simulation results, for the test structures with a 5 μm fillet like those in the current study, bond pad heating may contribute to up to 10% underprediction of the thermal

conductivity. New test structures with larger fillets have been designed to further examine this phenomena.

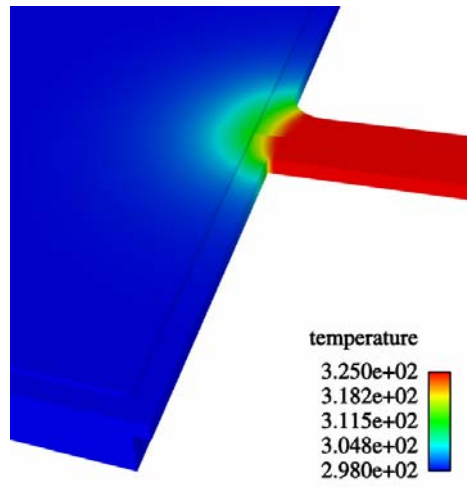


Figure 31: Comparison of temperature distributions for a poly4 beams with a square edge and with a 5 μm fillet at its attachment point.

5. CONCLUSIONS

5.1. Summary of Results

A capability for measuring the thermal conductivity of MEMS materials using a steady state resistance technique was developed. This effort involved obtaining and setting up the necessary equipment, designing test structures for fabrication, conducting the required operational reviews, and developing the data acquisition system. The thermal conductivities of SUMMiT™ V layers were measured using the developed capability. Thermal conductivities were measured over in two cryostats over two temperature ranges: 100K to 350K and 293K to 575K in order to generate two data sets. These measurements of thermal conductivity for poly1-poly2 laminate, poly2, poly3, and poly4 polysilicon structural layers in the SUMMiT V process establish for the first time that the thermal conductivity is a function of the particular SUMMiT layer. At 293K, the average thermal conductivity \pm the spread of the data collected of the P1P2, P2, P3, and P4 layers are 52.4 W/mK \pm 5%, 64.4 W/mK \pm 10%, 59.8 W/mK \pm 4%, and 58.8 W/mK \pm 3%, respectively. The poly2 layer has a different variation in thermal conductivity than the poly1-poly2 laminate, poly3, and poly4 layers as the temperature is decreased. Below 233K, the thermal conductivity of the P2 layer plateaus and then decreases. The thermal conductivities of the P1P2, P3, and P4 layers continue to increase with decreasing temperature until 93K and then decrease. The P1P2 thermal conductivities are lower than the P4 which are slightly lower than the P3. As the temperature increases above room temperature, the difference in thermal conductivity between the layers decreases. The agreement between the data collected in the two cryostats is reasonable. A simulation of a test structure indicates that bond pad heating likely contributes to the measured thermal conductivities being up to 10% lower than actual values. Additionally, electrical resistance and resistivity data are reported for poly1-poly2 laminate, poly2, poly3, and poly4 polysilicon structural layers in the SUMMiT process from 83K to 575K.

5.2. Recommendations for Continuation

This study provided thermal conductivity data as a function of temperature for SNL SUMMiT layers for device simulations and model validation; however, the measured data is insufficient to fully explain all of the observed trends. In order to validate first principles thermal conductivity models, an ideal data set would be for a range of polycrystalline silicon microstructures and doping values. Also, the polysilicon films should be well characterized so that the distribution of grain sizes and orientations are available to the modeling efforts. Thus, it is recommended that thermal conductivities be measured for polysilicon test structures for various microstructures and doping that are well characterized. Testing additional SUMMiT samples, including test structures with varying lengths and widths, will improve the data statistics and uncertainty quantification. Testing the samples designed with larger fillets will provide additional data to evaluate the effects of bond pad heating on the measurement accuracy. The impact of interfaces on thermal transport is important in micromachined structures due to the prevalence of laminated layers in MEMS devices and could be investigated with laminated thermal conductivity test structures.

6. REFERENCES

- [1] Sniegowski, J. J., and de Boer, M. P., 2000, "IC-Compatible Polysilicon Surface Micromachining," *Annual Review of Material Science*, 30, pp. 299-333.
- [2] von Arx, M., Paul, O., and Baltes, H., 2000, "Process-Dependent Thin-Film Thermal Conductivities for Thermal CMOS MEMS," *Journal of Microelectromechanical Systems*, 9, pp. 136-145.
- [3] McConnell, A. D, Uma, S., and Goodson, K. E., 2001, "Thermal Conductivity of Doped Polysilicon Layers," *Journal of Microelectromechanical Systems*, 10, pp. 360-369.
- [4] Piekos, E. S., Graham, Jr., S., and Wong, C. C., 2004, "Multiscale Thermal Transport," Sandia National Laboratories report, SAND2004-0531, printed February.
- [5] Manginell, R. P., 1997, "Polycrystalline-Silicon Microbridge Combustible Gas Sensor," University of New Mexico Ph.D. thesis.
- [6] Tai, Y. C., Mastrangelo, C. H., and Muller, R. S., 1998, "Thermal Conductivity of Heavily Doped Low-Pressure Chemical Vapor Deposited Polycrystalline Silicon Films," *Journal of Applied Physics*, 63, pp. 1442-1447.
- [7] Shojaei-Zadeh, S., Zhang, S., Liu, W., Yang, Y., Sadeghipour, S. M., and Asheghi, M., 2004, "Thermal Characterization of Thin Film Cu Interconnects for the Next Generation of Microelectronic Devices," *ITherm 2004 Proceedings: The Ninth Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems*, Las Vegas, Nevada, pp. 575-583.

DISTRIBUTION

1	MS0437	Gerald Sleaf	12910
1	MS0824	T. Y. Chu	1500
1	MS0824	Wahid Hermina	1510
1	MS0826	Michail Gallis	1513
1	MS0826	Edward Piekos	1513
1	MS0826	John Torczynski	1513
1	MS0826	C. Channy Wong	1513
1	MS0834	Daniel Rader	1513
8	MS0834	Leslie Phinney	1513
1	MS0834	Justin Serrano	1513
1	MS0836	Joel Lash	1514
1	MS0847	James Redmond	1526
1	MS1064	Rebecca Clemens	2614
1	MS1064	Stephen Lott	2614
1	MS1069	Michael Baker	1749-2
1	MS1069	Mark Platzbecker	1749-1
1	MS1070	Jaron Koppers	1526
1	MS1080	Michael Shaw	1749
1	MS1411	Edmund Webb III	1814
1	MS9405	Silvie Aubry	8776
2	MS9018	Central Technical Files	8944
2	MS0899	Technical Library	4536