PEP-II TRANSVERSE FEEDBACK ELECTRONICS UPGRADE*

J. Weber, M. Chin, L. Doolittle, LBNL, Berkeley, CA 94720, U.S.A.

R. Akre, SLAC, Stanford, CA 94309, U.S.A.

Abstract

The PEP-II *B* Factory at the Stanford Linear Accelerator Center (SLAC) requires an upgrade of the transverse feedback system electronics. The new electronics require 12-bit resolution and a minimum sampling rate of 238 Msps. A Field Programmable Gate Array (FPGA) is used to implement the feedback algorithm. The FPGA also contains an embedded PowerPC 405 (PPC-405) processor to run control system interface software for data retrieval, diagnostics, and system monitoring. The design of this system is based on the Xilinx® ML300 Development Platform, a circuit board set containing an FPGA with an embedded processor, a large memory bank, and other peripherals. This paper discusses the design of a digital feedback system based on an FPGA with an embedded processor. Discussion will include specifications, component selection, and integration with the ML300 design.

INTRODUCTION

The digital components of the existing PEP-II transverse feedback (TFB) electronics consist of a pickup-to-kicker timing delay and circuitry for changing the sign and gain of the feedback for a given bunch. This circuitry is implemented using 8-bit converters sampling at 476 megasamples per second (Msps) and a fast ECL RAM array with EClips ECL logic[1]. Using the improvements in Analog to Digital Converter (ADC), Digital to Analog Converter (DAC), and FPGA technologies, this system will be upgraded to an FPGA-based system with greater resolution, expanded diagnostic capability, and an embedded control system interface. The new system uses 12-bit ADCs and DACs, 128 MB Double Data Rate (DDR) RAM, and an FPGA with an embedded processor.

However, as the density and complexity of circuit boards increases, the challenges of designing and simulating the system also become increasingly difficult. One method to minimize development time and failure risk is to begin with a vendor designed demo board that contains many of the desired system components. Using this methodology, LBNL designed a new digital delay module for the PEP-II transverse feedback system based on the Xilinx® ML300 Development Platform design.

DESIGN

Discussion of the design of the SLAC TFB Digital Delay Module will include system specifications, selection of major components, design strategy, and integration with the ML300 design. Figure 1 shows an overview of the PEP-II transverse feedback system. The new digital delay module electronics are shown in blue.
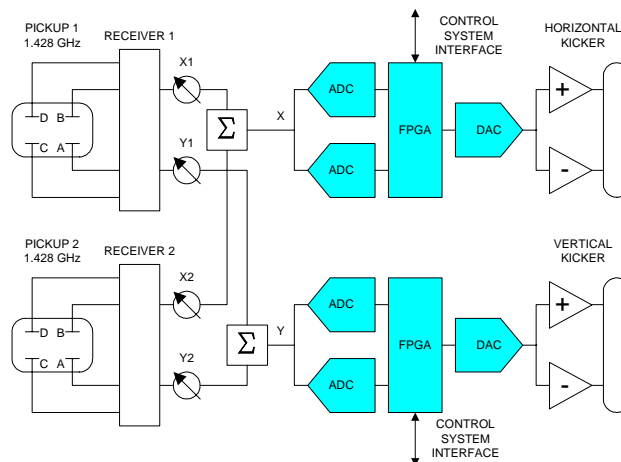

Figure 1: PEP-II Transverse Feedback System.

System Specifications

Requirements for the transverse feedback system electronics upgrade include 12-bit resolution and a 238 Msps minimum sampling rate. As in the current system, the new system provides delay and single bunch kick out capabilities. In addition, the new system includes deep memory for data capture and grow/damp diagnostics and an FPGA embedded processor for interfacing to the control system. A 119 MHz clock input, a cog pulse synchronized to the PEP-II orbit frequency, and X and Y axis position data are inputs. The outputs of the system apply the baseband correction signal to the horizontal and vertical stripline kickers[1]. Table 1 lists the specifications for the new SLAC TFB Digital Delay Module.

Table 1: Digital Delay Module Specifications

Parameter	Value
Sampling Rate	238 Msps
Resolution	12 bits
Input Impedance	50 Ω
Coupling	AC
Analog Bandwidth (3 dB)	32 kHz – 500 MHz
Input Amplitude (ADC)	+4.8 dBm
Output Amplitude (DAC)	+4.0 dBm
Signal to Noise and Distortion	> 55 dB
Spurious Free Dynamic Range	> 67 dB
External System Clock	119 MHz Sine Wave
Clock Input Amplitude	+7.0 dBm ±5%
Clock Phase Shift Range	> 90° (> 2.1 ns)
Clock Jitter	< 2 ps (Note 1)
System Memory (DDR RAM)	128 MB

Note 1: Jitter from external clock source not included.

Component Selection

The brains of the feedback system require a large FPGA with plenty of gates to handle the high speed feedback algorithm in logic while interfacing to the control system via the embedded processor. The Xilinx® Virtex-II Pro™ was chosen for this design because it was the most advanced and cost effective of the available FPGAs with embedded processors.

Besides the FPGA, the most critical components of this feedback system are the ADC and DAC. The 12-bit ADC with the greatest sampling rate was the Analog Devices AD9430 at 210 Msps. To meet the sampling rate requirement of 238 Msps, two ADCs were used sampling at 119 Msps 180 degrees out of phase. The Maxim MAX5886 DAC was chosen with 12-bit resolution and a sampling rate of 500 Msps, meeting both resolution and sampling rate requirements.

Design Strategy

This project called for an aggressive timeline to meet the operational needs of PEP-II. Once the main components of the system were chosen, we began to look for ways to reduce the development time. One idea was to start with a vendor designed FPGA demo board. In some cases, demo boards provide connectorized general purpose interfaces so that custom daughter boards can plug directly into the demo board. In other cases, schematics and layout files for the demo board are provided by the vendor allowing modification of the board itself for customization. Using part or all of a demo board design can significantly reduce the development effort of a new design.

Another important advantage of using a demo board is the reduction in Signal Integrity (SI) analysis effort. Simulating a complex high speed design using SI tools can be a daunting task, as these tools are expensive and complex. On the other hand, to not perform SI analysis on a new design can result in PCB design issues that can only be resolved by revising the PCB layout. By using a demo board design, designers can skip SI analysis with greater confidence or analyze only the customized portion of the design.

Of the several demo boards produced by various vendors using the Virtex-II Pro™ FPGA, the Xilinx® ML300 Development Platform contained the most features compatible with our specifications, including DDR RAM, an embedded processor, Ethernet, RS-232, and a CompactFlash drive. Xilinx® also provided all ML300 schematics, drawings, and design files on their website[3]. The ML300 documentation provided all the tools needed to modify a proven design to meet the needs of the SLAC TFB Digital Delay Module, shown in Figure 2. The SLAC TFB CPU Board was modified from the ML300 CPU Board design. In Figure 2, the yellow components remain from the ML300 CPU Board design and the green components were added.
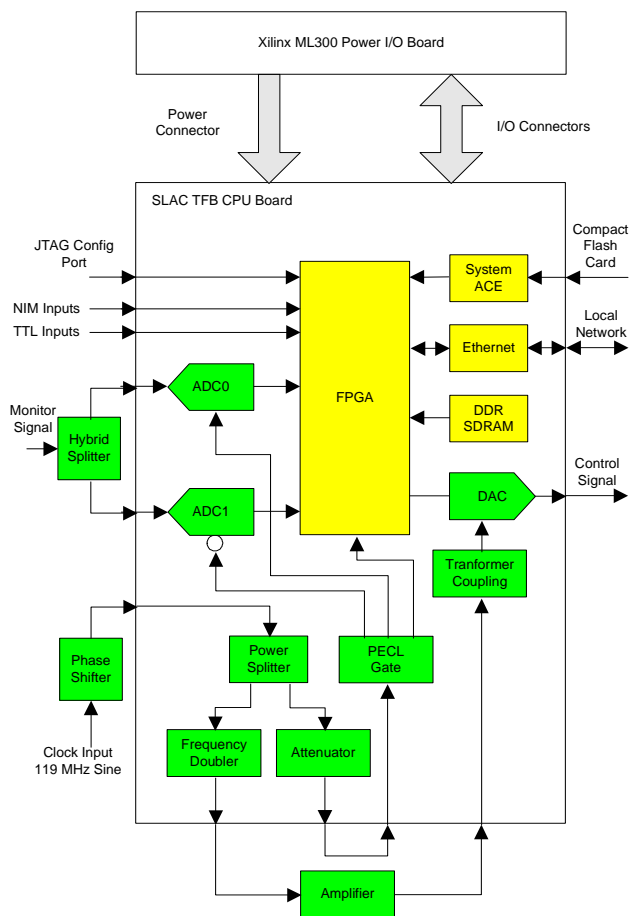

Figure 2: Transverse Feedback Digital Delay Module.

Demo Board Integration

There are several important steps to successfully modify a demo board design. First, designers must understand all components in the demo board system and their interconnections. Details such as board stack-up, plane layers, grounding, and form factor must be examined to eliminate conflicting design changes. The ML300 hardware consists of a 2 PCB set including the ML300 CPU Board and ML300 Power I/O Board. During this stage, we decided to use the ML300 Power I/O Board as is and modify only the ML300 CPU Board since it contains the FPGA.

The second step is to remove unwanted components from the design. During this process, schematic and layout engineers must work closely to ensure that components removed from the schematic and the layout match. The ML300 supports many interfaces that were not required for the transverse feedback design, so we removed features such as PCI Bus, Multi Gigabit Transceivers, CardBus, TFT Display, Touch Screen, Audio Codec, and PMC Connector support. The removal of these components and nets provided more than enough space for the components and nets we needed to add.

Finally, necessary components that were not included in the demo board design must be added. This process is very similar to the layout of a new design, except that the layout engineer must work around the remaining

components from the demo board design. For the SLAC TFB CPU Board design, ADCs, a DAC, clock circuitry, and general purpose digital inputs were added and interfaced to the FPGA as necessary.

TESTING

A major advantage of using the ML300 design was that the testing became much easier. Several example designs, consisting of both the FPGA "hardware" and the PPC-405 software to run the hardware, were provided with the ML300 to test components such as the Ethernet, RS-232, CompactFlash, and DDR RAM interfaces. These designs allowed us to quickly test many components of the system and focus on the performance of the analog components and the digital filter.
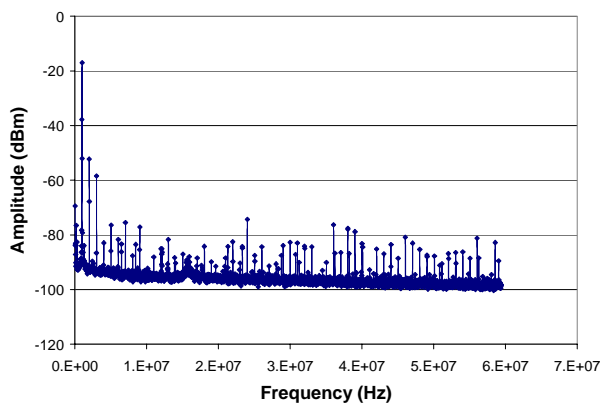

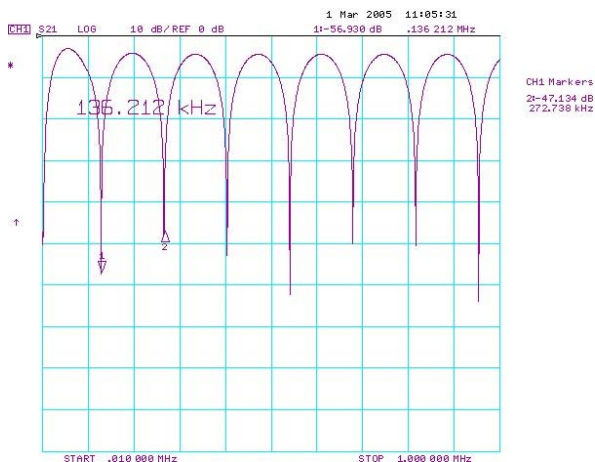Figure 3: SLAC TFB Digital Delay Module spectrum.

Figure 4: SLAC TFB Digital Delay Module filter.

Figure 3 shows the spectrum of the SLAC TFB Digital Delay Module for a 1 MHz Sine Wave input. This measurement is limited by the harmonics of the source stimulus, but gives a general idea of the noise floor and dynamic range of the system. Figure 4 shows the behavior of the digital filter over the range of 10 kHz to 1 MHz. The filter notches appear at intervals of the PEP-II orbit frequency of 136.3 kHz[2].

CONCLUSION

The benefits of basing this design on the ML300 were significant. Since the design files were available, we were able to maintain the layout of many major components and bypass SI analysis. This reduced the development such that we were able to build a prototype in less than six months. It also reduced the risk of board failure so that the first prototype hardware has been fully tested and performs to specifications, thus no revision of the board is required. The availability of demo software and drivers allowed for reduced testing effort, and allowed us to focus our testing effort on the analog portion of the design. In sum, starting with a demo board allowed us great savings in development and testing time and as a result we were able to quickly deliver a complete, fully tested feedback system.

The first two of four SLAC TFB Digital Delay Module Chassis have been delivered to SLAC and await installation and commissioning at PEP-II. The hardware of these systems has been fully tested and the control system interface and diagnostics support are in progress. This project should be completed in the next few months.

ACKNOWLEDGEMENTS

REFERENCES

[1] W. Barry, et al., "Design of the PEP-II Transverse Coupled-Bunch Feedback System", PAC'95, Dallas, TX, May, 1995, http://www.jacow.org.
[2] "PEP-II Conceptual Design Report", LBL-PUB-5379, SLAC-418, CALT-68-1869, UCRL-ID-114055, UC-IIRPA-93-01, June, 1993.
[3] Xilinx® ML300 Development Board documentation, http://www.xilinx.com/products/boards/ml300/index.htm.