

CIGSS Thin Film Solar Cells

Final Subcontract Report
11 October 2001—30 June 2005

N.G. Dhere
Florida Solar Energy Center
Cocoa, Florida

Subcontract Report
NREL/SR-520-39486
February 2006

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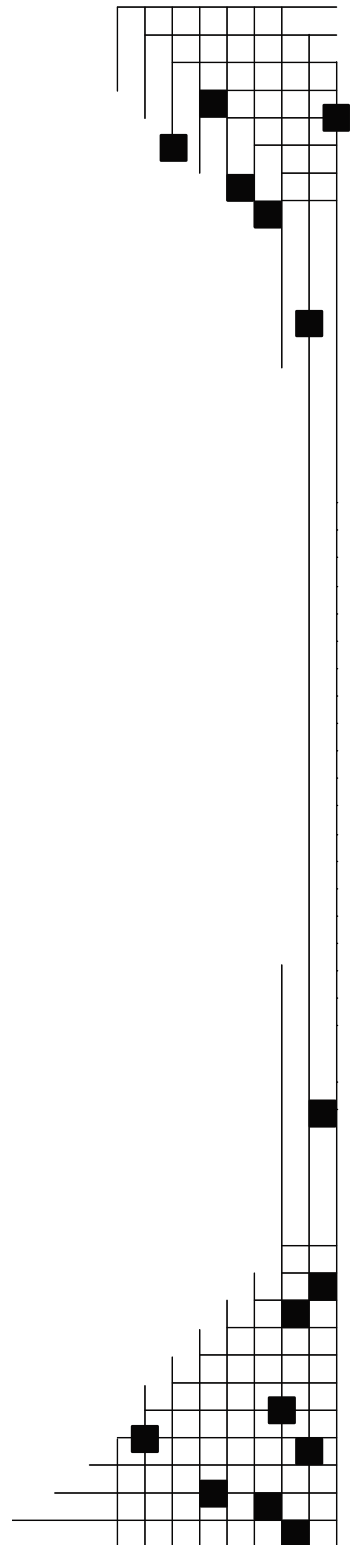
N.G. Dhere
*Florida Solar Energy Center
Cocoa, Florida*

NREL Technical Monitor: B. von Roedern
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National Renewable Energy Laboratory
1617 Cole Boulevard, Golden, Colorado 80401-3393
303-275-3000 • www.nrel.gov

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Introduction

I-III-VI₂ compounds are developing into a promising material to meet the energy requirement of the world. CuInSe₂ (CIS) and its alloy with Ga and S have shown long term stability and highest conversion efficiency of 19.5% [1]. Among the various ways of preparing CuIn_{1-x}Ga_xSe_{2-y}S_y (CIGSS)/CdS thin-film solar cells, co-evaporation and sputtering techniques are the most promising. Sputtering is an established process for very high-throughput manufacturing. ARCO Solar, now Shell Solar pioneered the work in CIS using sputtering technique [2,3]. The two stage process developed by ARCO Solar involved sputtering of a copper and indium layer on molybdenum coated glass as the first step. In the second step, the copper-indium layers were exposed to a selenium-bearing gas such as hydrogen selenide (H₂Se) mixed with argon. The hydrogen selenide breaks down and leaves selenium, which reacts and mixes with the copper and indium in such a way to produce very high-quality CIS absorber layer. Sputtering technology has the added advantage of being easily scaled up and promotes roll to roll production on flexible substrates. In the early 90's, a nontoxic selenization process was developed at the PV Materials Lab to avoid use of extremely toxic H₂Se gas. The two stage selenization process involved deposition of copper-indium layer with excess copper. The elemental stack was selenized by heating the substrate in the presence of selenium vapors obtained by thermally evaporating elemental selenium. Selenization of the copper-rich film helped improve adhesion with molybdenum back contact. The copper-rich film was further deposited with indium and re-selenized to produce an efficient thin-film CIS absorber [4]. The process was further modified and gallium concentration was optimized to produce cell with efficiency 9.02% [5]. As of now, CIGSS/CdS thin film solar cells are being prepared by rapid thermal processing and conventional selenization using diethylselenide (DESe) as selenium source [6,7] and H₂S as sulfur source [8], in combination with DC/RF magnetron sputtering and chemical bath deposition technique. Sulfurization of metallic precursors is a well-developed process to produce a high bandgap (1.55eV) absorber. Hahn-Meitner-Institut of Germany has developed a similar process using elemental sulfur [9]. A new selenization set-up for DESe was build and moved near the furnace to reduce the distance between the furnace and selenium source. Preliminary

experiments for selenization were carried out. X-ray diffraction and electron probe microanalysis have shown promising results. Experiments were carried out to establish optimum parameters for CuGa-In precursor deposition as well as selenization/sulfurization. A rapid thermal processing set-up was assembled. Preliminary experiments were carried out. ZnO/ZnO:Al deposition by RF magnetron sputtering and CdS deposition by chemical bath deposition (CBD) are being carried out on routine basis. CdS setup was modified to reduce the consumption of the solution as well as to heat the chemical bath uniformly [10].

Selenization/Sulfurization Furnace

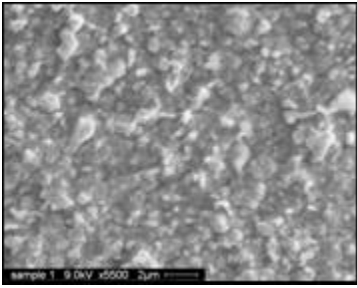
Three new temperature controllers from Eurotherm were procured. The necessary enclosure was procured and all three controllers along with an over-temperature controller have been properly installed in the enclosure while the enclosure itself was installed securely beneath the furnace. The controllers were connected to the selenization/sulfurization furnace and are being used to control the heat treatment process for the development of CIGSS thin films on glass and stainless steel substrates. The controllers were programmed with the requisite parameters and initially tested for time/temperature readings. The new temperature controller has reduced the temperature fluctuation during the process. A temperature ramp of 6 °C/ minute is being routinely used for selenization/sulfurization of the elemental stack because it led to the minimum error between the set values and the actual values. Experiments were carried out to establish selenization cycles in order to achieve complete selenization of the elemental stack. A series of experiments was performed for optimizing the heat treatment parameters such as temperature and soaking time to ensure complete selenization and formation of a device quality absorber.

Metallic precursors CuGa and indium were sputter-deposited on molybdenum coated glass substrate. Power and pressure for precursor deposition was kept the same in all experiments discussed here. The speed at which the substrates moved over the targets of each precursor layer was varied in order to obtain desired rates of depositions, total thicknesses of each layer and consequently the stoichiometric composition. As mentioned

in the Year 3 Annual Report, the substrate movement speed was controlled with a PC-controlled stepper motor using a LABVIEW program.

Experiment #1- To set initial parameters for selenization and sulfurization.

Metallic precursor - CuGa was deposited at linear speed of 0.048 cm/sec while indium was deposited at a linear speed of 0.021 cm/sec. The elemental stack was selenized at 400°C for 10 minutes and sulfurized at 475°C/20 minute in a single run. i:ZnO and ZnO:Al window bilayers were deposited using RF magnetron sputtering at 200 Watt at 0.048 cm/sec and 300 Watts at linear substrate movement speed of 0.006 cm/sec. Ni/Al contact fingers were deposited using a metal mask by electron beam evaporation.



EPMA: sample 1

Elem.	Cu	In	Ga	Se	S
At%	26.57	25.64	3.78	17.11	26.88

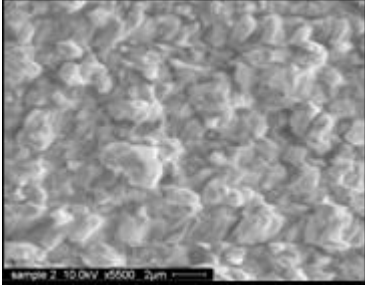
Figure 1: SEM micrograph

From SEM analysis (Fig. 1) it was seen that the grain size was very small and the grains were not faceted. EPMA analysis was carried out to check the stoichiometry and it was observed that the amount of selenium was comparatively lower than the sulfur amount. This indicated that there was not enough Se in the atmosphere or the temperature and soaking time were not adequate for completion of the reaction between metallic precursors and Se. Initially sulfur reacts with the unreacted Cu-Ga-In. It can also replace selenium because it is more reactive than selenium.

Sulfurization is considered as a bandgap engineering treatment. The open-circuit voltage V_{oc} mainly depends on the band gap in the space charge region. CIGS has a bandgap of 1.12 eV with Ga ~ 30 at% resulting in lower V_{oc} . Post sulfurization treatment leads to the formation of CIGSS or $CuIn_{1-x}Ga_xS_2$ layer with a wider bandgap of 1.55eV at the p-n junctions that helps in increasing the open circuit voltage (V_{oc}). During post

sulfurization treatment the sulfur atoms occupies already existing selenium vacancies, thereby reducing the compensating donor and also passivating the surface [11].

EPMA:Sample 2a with lower sheet resistance



Elem.	Cu	In	Ga	Se	S
At%	31.27	22.79	3.73	15.16	27.03

EPMA:Sample 2b with higher sheet resistance

Elem.	Cu	In	Ga	Se	S
At%	27.87	20.25	3.34	13.82	34.70

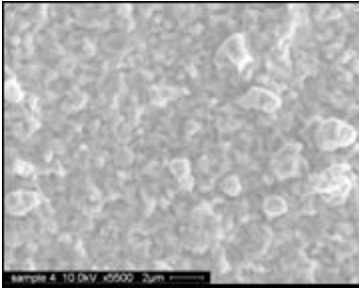
Figure 2: SEM micrograph of Sample 2

Experiment #2-The purpose of this experiment was to see if selenium incorporation increases in presence of sodium and excess copper.

Addition of controlled amount of sodium helps in growth kinetics of the chalcopyrite film resulting in crystalline film [12]. Two changes were made in this experiment. First the amount of CuGa was increased by reducing the substrate movement speed from 0.048 cm/sec to 0.04 cm/sec. Secondly small amount of sodium was added in the form of NaF layer. 3.4 mg of NaF was thermally evaporated onto the Mo surface. NaF melted and then evaporated at a current of 160-165 A. Calculations indicated that this amount corresponds to 60 to 120 Å. Some part of the film peeled off at Mo/CIGSS interface. Peeling was due to improper cleaning and probably due to NaF layer at the interface. The film was patchy, a part of it had sheet resistance of 250 Ω/□ while the other had 300 Ω/□. Sample 2a was from the lower sheet resistance region indicating more copper while Sample 2b was from the comparatively higher sheet resistance. Overall the film was copper-rich as Cu/In+Ga ration was > 1. The problem of incomplete selenization continued as the amount of Se in the films was consistently low.

Experiment #3 – To check the consistency of results in Experiment 2

EPMA: Sample 3a



Elem.	Cu	In	Ga	Se	S
At%	26.86	24.4	3.7	13.69	31.33

EPMA: Sample 3b

Elem.	Cu	In	Ga	Se	S
At%	27.94	21.52	3.53	12.85	34.14

Figure 3: SEM micrograph of Sample 3

A thin layer of NaF was deposited on the precursor layer instead of Mo layer as it was believed to be one of the potential reasons for peeling observed in Experiment 2. The film appeared uniform after the selenization cycle. SEM micrograph (Fig. 3) revealed well-developed, compact and distinct grains with sizes varying from 0.5 μm to 2 μm . It was again evident from EPMA analysis that the proportion of selenium was considerably lower than that of sulfur. After CdS chemical bath deposition on the absorber layer, a patchy morphology that was not discernible on earlier selenized/sulfurized films appeared. Another important observation was no peeling-off of the absorber film.



Figure 4a: Se/S treated and CdS deposited

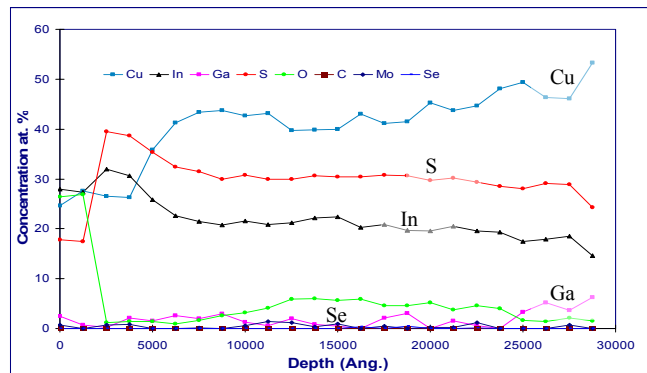


Figure 4b: AES depth profile

Experiment # 4 – To increase Se incorporation by supplying more selenium-containing vapor.

Some experiments were carried out at a higher Se pressure and a constant heating rate of 6°C/min so as to overcome selenium deficiency. Selenization was carried out at

400°C for 15 minutes so as to increase Se incorporation in the films. Selenization was followed by sulfurization at 475°C for 15 minutes. Sulfurization time was reduced as the intention was to have more Se than S in the films. Diluted DESe pressure was increased from earlier value of 30 Torr to 60 Torr in order to increase the amount of Se. The heat-treated film showed three patches with sheet resistance of 700 Ω/\square , 1000 Ω/\square and 1200 Ω/\square . Half of the sample was etched in 10% KCN and subsequently oxidized in equal quantities of H₂O₂ and 1% H₂SO₄. The remaining half was used as selenized/sulfurized without any surface treatment. Both the pieces were coated with CdS layer. As shown in the Figure 4a, the etched oxidized sample appears bluish purple while the other appears gray with three patches clearly visible. Though EPMA data was not available, it was observed from AES data that selenium incorporation was not significant.

Experiment #5 – To prevent indium loss if any, during selenization

An additional dwell was incorporated at 140°C for 30 minutes to prevent indium loss during selenization. Selenization and sulfurization were carried out with similar ramp of 6°C/min with temperature and dwell of 400°C for 15 minutes and 475°C for 15 minute respectively. Total pressure of DESe diluted in hydrogen was 60 Torr. During chemical bath deposition excessive thickness of CdS was deposited. The film showed yellow CdS patches all over the film. Also from AES it was observed that the amount of Se was less than that of S. Elemental depth profile of the absorber layer grown with these parameters is shown in Figure 5.

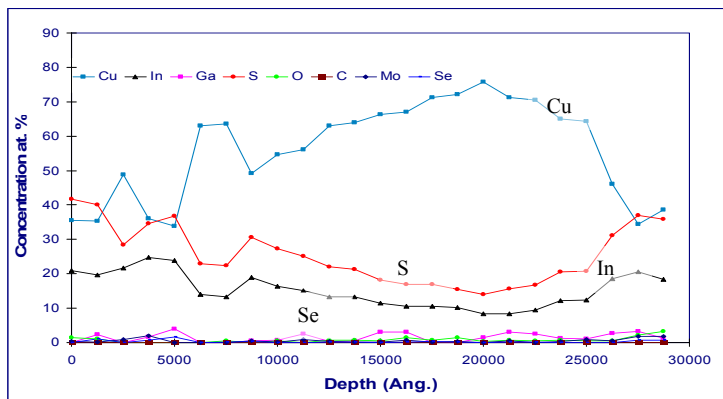
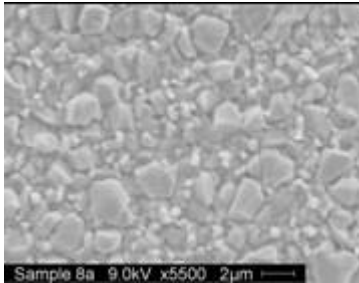


Figure 5: AES elemental depth profile

Experiment # 6 – To study the effect of excess copper

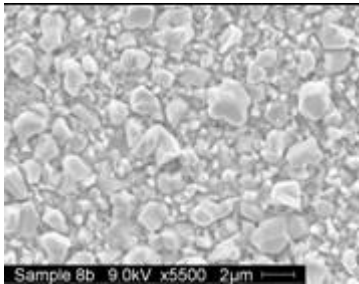
From the AES depth profile shown in Figure 5, it was seen that the amount of Se in the absorber film was very low even after increasing the amount of diluted DESe (from 30 Torr to 60 Torr). Therefore, selenization was carried out on the excess copper film. Indium layer deposited at substrate speed of 0.04329 cm/sec was sandwiched between two layers of CuGa deposited at substrate speeds of 0.06 and 0.138 cm/sec respectively. No NaF was added as the film had excess Cu. SEM micrograph is shown in Figure 6.. In all the experiments carried out so far, Se incorporation was found to be very less. Hence, further experiments were carried out for preparing selenide absorber layer.



EDS of etched film grown in Cu-rich composition

Elem.	Cu	In	Ga	Se
At%	22.16	22.16	5.05	49.58

Figure 6: SEM of sample grown in Cu-rich composition



EDS: sample with additional dwell and higher ramp

Elem.	Cu	In	Ga	Se
At%	22.86	24.93	3.16	47.82

Figure 7: SEM of sample with dwell of 140°C for 30 minutes and ramp of 20°C/minute

Experiment # 7- To study the effect of higher heating rate and dwell at lower temperature

In the following experiment, the deposition parameter and the maximum temperature for selenization were similar to the previous experiment, except that in this case a heating ramp of 20°C/minute and an additional dwell at 140°C for 30 minutes was

used. CdS, i:ZnO/ZnO:Al and Ni/Al contact fingers were deposited. During the measurement, it was realized that the Mo layer from absorber layer interface to the substrate had completely reacted even under the Cu_In-Ga layers, leaving no Mo back contact for efficiency measurement. The thickness of these films was measured using a thickness profilometer and was found to be 1.3 to 1.5 μm . This thickness was almost half of the value intended (2.75 μm). SEM of the absorber layer is shown in Figure 7.

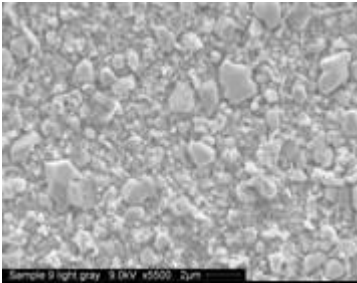


Figure 8a: SEM

EDS: from light gray patch

Elem.	Cu	In	Ga	Se
At%	22.49	21.19	5.38	49.13



Figure 8b: As deposited and Se treated

EDS: from murky gray patch

Elem.	Cu	In	Ga	Se
At%	21.25	22.71	4.24	50.54

Experiment #8- To optimize selenization time at maximum selenization temperature

This sample (Figure 8b) had a layer of NaF on top of metallic precursor layer. The sample was selenized at 400°C for 10 minutes. Diluted DESe pressure was maintained at 60 Torr. The sample showed a dark gray patch as seen in Figure 8b. The sheet resistance in this region was 40 - 60 Ω/\square and 150 to 200 Ω/\square in the remaining uniform gray region. The dark patch was believed to be that of non-reacted film. So the dwell time was increased to 15 minutes in the next experiment.

Another sample shown in Figure 9a-3 was selenized at 400°C/15 minutes and it showed a pattern after taking out from the furnace. The pattern remained after etching. The entire film turned dark on oxidation. The film also peeled off during CdS deposition (Figure 9a-2). SEM of the film is shown in Figure 9b. In both the films shown in Figure 8a and 9b, the thickness of the absorber layer was in the range of 1.3 to 1.5 μm . Due to

the lower thickness, Mo layer was completely reacted, as a result of which devices could not be prepared using the film.

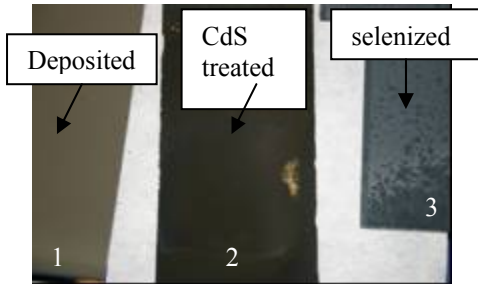


Figure 9a: 1- as deposited, 2- selenized and CdS treated, 3- selenized

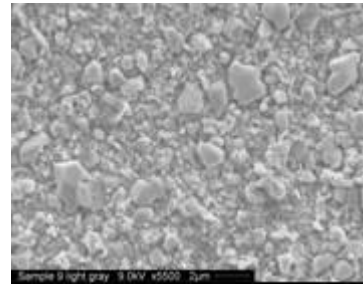


Figure 9b: SEM of absorber layer

Experiment # 9- Thickness of the absorber was doubled to prevent complete Mo reaction

In next experiment, the deposition timing was doubled so as to obtain higher thickness of the absorber film. As mentioned earlier, the thicknesses were in the range of 1.3 -1.5 μm so the deposition timing was doubled. CuGa was deposited in two layers; the first layer was deposited at a substrate speed of 0.03 cm/sec while the second layer was deposited at 0.07 cm/sec. An indium layer deposited at a substrate speed of 0.021 cm/sec was sandwiched between the two CuGa layers.



Figure 10a: Se/S treated

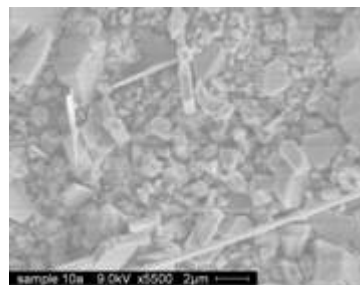


Figure 10b: SEM image

A 5 cm x 10 cm strip from this deposition was selenized at 400°C for 10 min and sulfurized at 475°C for 10 minute. 1% of DESe was used for selenization. The partial pressure of diluted DESe was 30 Torr. The temperature was ramped up at 20°C/min with

no intermediate dwell. The sample showed patches of dark and light gray area as seen in Figure 10a. Sheet resistance in the dark areas was $1.4 \text{ k}\Omega/\square$ and $1 \text{ k}\Omega/\square$ in the light gray areas. Overall the film was slightly copper-rich which was evident from the CuSe whiskers seen in the SEM micrograph (figure 10 b).

Experiment # 10- To study the effect of reduced ramp rate

In another experiment, the ramp rate was reduced to $6^\circ\text{C}/\text{minute}$. This sample showed a patch too as seen in Figure 10c. However, the film showed overall uniformity compared to the film shown in Figure 10a. The sheet resistance was 300 to $500 \Omega/\square$ and the thickness was 3.8 to $3.9 \mu\text{m}$. SEM image is shown in Figure 10d.



Figure 10c: Se/S treated sample 10b

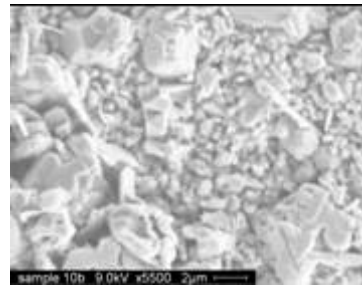


Figure 10d: SEM of sample 10b

The grain size varied from $<1 \mu\text{m}$ to $2 \mu\text{m}$ in all the samples. Sulfur quantity was higher in all the films. Cells were completed and efficiency was measured. The values obtained were not very attractive and it was inferred that the process needs to be modified to optimize the parameters to obtain good quality absorber.

Heterojunction Partner Layer, CBD CdS

Heterojunction partner CdS layers were satisfactorily deposited by chemical bath deposition on $10 \times 10 \text{ cm}^2$ CIGS2 samples. The CdS deposition set-up was modified to reduce the quantity as well as to ensure uniform heating of the solution. A 4000 ml beaker was used as a water bath while the reaction solution was prepared in a 1000 ml

beaker. Two samples of size 5 cm x 10 cm could be coated with a conformal layer of CdS in a single run.

Rapid thermal processing (RTP)

A Rapid Thermal Processing (RTP) unit has been designed, constructed and installed for preparation of CIGSS thin films on 10 cm x 15 cm substrates by selenization/ sulfurization of elemental precursors using the vacuum deposited selenium layer and $N_2:H_2S$ atmosphere. For RTP, selenium evaporation will be carried out by thermal evaporation in a separate setup. An optimized, minute amount of NaF was deposited to improve the morphological and electrical properties of the absorber.

The configuration and schematic are shown in Fig. 11 and 12 respectively. A quartz tube (ID = 15 cm) was mounted with a stainless steel flange assembly. Feedthroughs were mounted on the end flange for connection to a thermocouple which would monitor temperature. Viton rubber 'O' ring in a groove was used to form an air-tight seal between the hard surfaces of the flange and glass tube. The flange had two openings – a gas inlet (for H_2S and Se vapors) and an exhaust. A pair of high density infrared heaters (Research Inc., Model 5090), each with a bank of 5 T3-style quartz infrared halogen lamps directs energy onto the reaction tube where the substrate was kept. Each lamp is rated at 1200 Watts. The power to the lamps was controlled by a pair of single-phase (120V AC, 55 A) standalone SCR power controls (Research Inc., Model 5620). Each T3-style quartz halogen lamp radiates 90% energy in less than 1 second.

The two heater arrays have to be controlled independently so that the thermal gradient across the thickness of the substrate remains symmetrical during all RTP processing phases. This prevented the substrate from breaking and cracking.

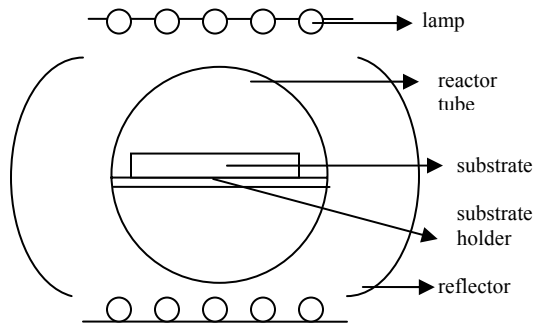


Figure 11: RTP System Configuration

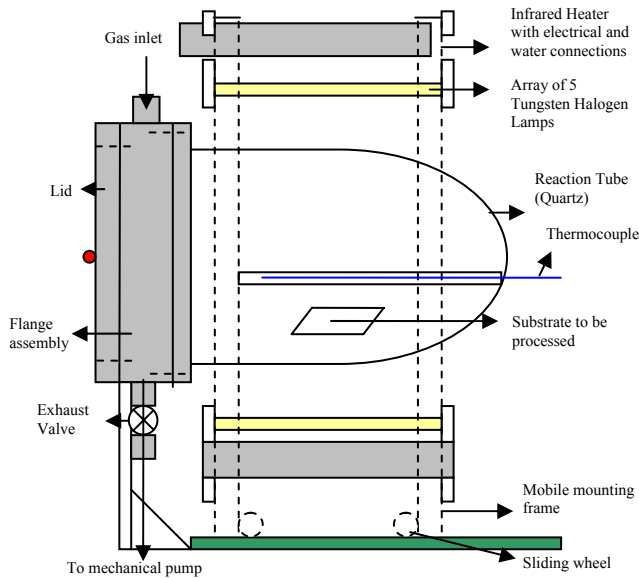


Figure 12: RTP Schematic

Each heater consists of a specular aluminum reflector that directs the infrared energy supplied by the lamps on to the substrate. Connections to supply required cooling water to the heater were provided. The heaters were mounted on a stand so as to face both the surfaces of the substrate. Two aluminum sheets with 95% reflectivity and measuring 30 cm x 30 cm x 0.05 cm each were formed into arcs and installed laterally on both sides of the quartz tube to reflect the heat back to the substrate during RTP. Circular reflective stainless steel sheets were placed within the quartz tube at both ends. A sliding

mechanism was provided to quickly move the heaters away from the reaction tube after the completion of the process for rapid cooling.

Experiments were carried out in order to determine the rate at which substrate temperatures would rise with the current setup. A mechanical pump was used to achieve a vacuum in the range of 10^{-3} Torr within the quartz tube. Cool water was circulated through each of the two infrared heaters at a rate of approximately 1.4 liter per minute per heater. The two power controllers for the infrared lamp arrays were switched to 'operate' mode. The power was raised to 100%. The temperature of the substrate was measured by means of a K-type chromel-alumel thermocouple. An initial temperature ramp of >6 °C per second and an average temperature ramp of 3.96 °C per second were obtained so that the temperature increase from 25 °C to 500 °C could be attained in 120 seconds at 100% power (Figure 13). The control power was slowly reduced and the power supply was switched off after reaching the temperature of 500 °C.

The next set of experiments was carried out to determine the fixed power to the two heaters for slowly reaching and maintaining a temperature of 500 °C. These initial experiments were carried out to model the behavior of the RTP setup with respect to the temperature-time profile obtained for a particular power setting. The ramps thus obtained were not as high as those required in RTP. Initially, the power was kept at 30% of the maximum. The temperature rose to 430 °C in 48 minutes and then remained stable. The power was then increased to 40%. Temperature rose to 500 °C in 2 minutes with a tendency to rise further. At this stage the power was switched off (Figure 14). In the subsequent experiment, it was found that when total lamp power was fixed at 35%, the substrate temperature rose to 500 °C in 52 minutes and remained stable (Figure 15). The results of these experiments are being used to maintain a given temperature during the desired interval after reaching that temperature at a very high rate using 100% power.

The following graphs show ramp rates for various power settings:

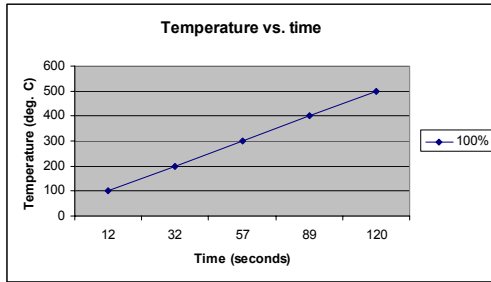


Figure 13: Plot of Temperature vs. time at 100% power

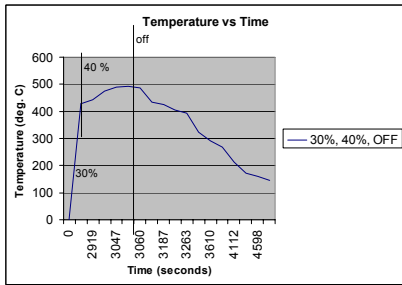


Figure 14: Plot of temperature vs. time for 30%, 40% and 0% power

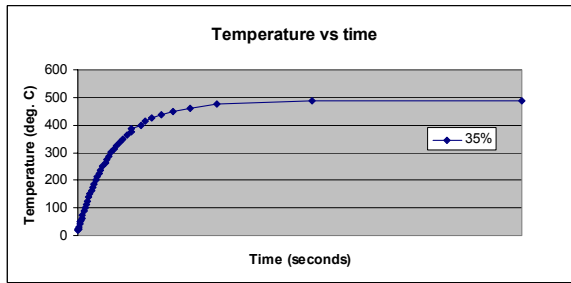


Figure 15: Plot of temperature vs. time for power fixed at 35% (constant)

Towards the end of the quarter, a high-purity, pyrolytic graphite custom-made tray (Fig. 16) was procured from Poco Graphite to hold a 10 cm x 10 cm sample at the center of the rapid thermal processing (RTP) quartz chamber. The graphite tray was designed in such a way that the sample could be kept in the tray. The graphite tray would rest on a larger quartz plate of size 14 cm x 14 cm x 0.31 cm.

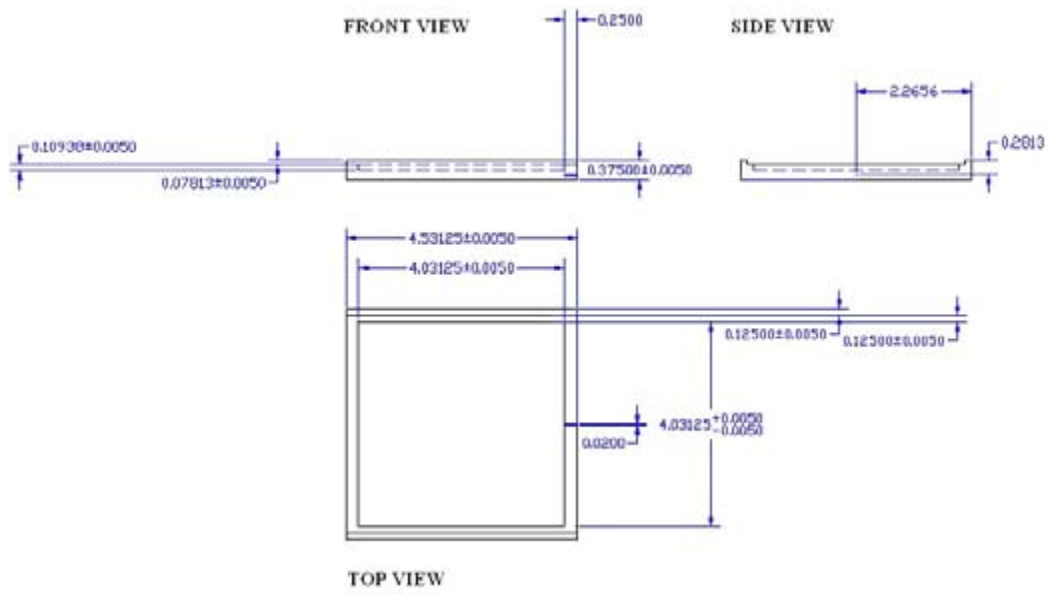


Figure 16: Mechanical drawing for custom-made graphite tray

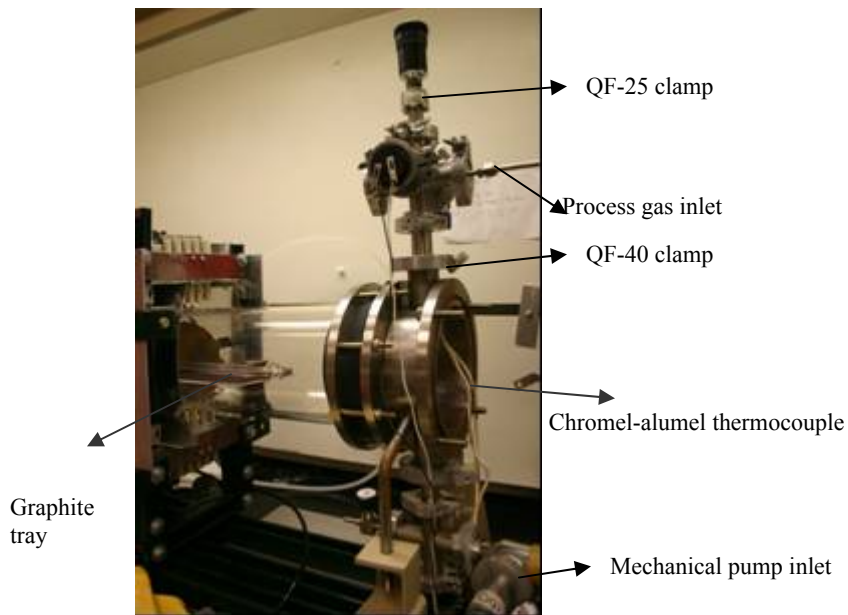


Figure 17: RTP Setup

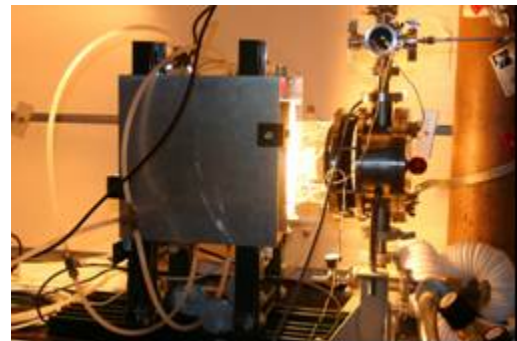


Figure 18: RTP setup during actual run

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14. ABSTRACT (Maximum 200 Words) This report describes the I-III-VI ₂ compounds that are developing into a promising material to meet the energy requirement of the world. CuInSe ₂ (CIS) and its alloy with Ga and S have shown long-term stability and highest conversion efficiency of 19.5%. Among the various ways of preparing CuIn _{1-x} Ga _x Se _{2-y} S _y (CIGSS)/CdS thin-film solar cells, co-evaporation and sputtering techniques are the most promising. Sputtering is an established process for very high-throughput manufacturing. ARCO Solar, now Shell Solar, pioneered the work in CIS using the sputtering technique. The two-stage process developed by ARCO Solar involved sputtering of a copper and indium layer on molybdenum-coated glass as the first step. In the second step, the copper-indium layers were exposed to a selenium-bearing gas such as hydrogen selenide (H ₂ Se) mixed with argon. The hydrogen selenide breaks down and leaves selenium, which reacts and mixes with the copper and indium in such a way to produce very high-quality CIS absorber layer. Sputtering technology has the added advantage of being easily scaled up and promotes roll-to-roll production on flexible substrates. Preliminary experiments were carried out. ZnO/ZnO:Al deposition by RF magnetron sputtering and CdS deposition by chemical-bath deposition are being carried out on a routine basis.								
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