Results from Irradiation Tests on D0 Run 2a Silicon Detectors at the Radiation Damage Facility at Fermilab

J. Gardner[1], C. Gerber[3], Z. Ke[4], S. Korjanevsky[2], A. Leflat[5], F. Lehner[6], R. Lipton[4], J. Lackey[4], M. Merkin[5], P. Rapidis[4], V. Rykalin[7], E. Shabalina[3], L. Spiegel[4], L. Stutte[4], B. Webber[4]

1 University of Kansas, Kansas City
2 Kansas State University, Manhattan, Kansas
3 University of Illinois at Chicago
4 Fermilab
5 Moscow State University
6 University of Zurich, Switzerland
7 Northern Illinois University, NICADD

Abstract

Several different spare modules of the D0 experiment Silicon Microstrip Tracker (SMT) have been irradiated at the Fermilab Booster Radiation Damage Facility (RDF). The total dose received was 2.1 MRads with a proton flux of $\sim 3 \cdot 10^{11}$ p/cm^2 sec. The irradiation was carried out in steps of 0.3 or 0.6 MRad, with several days between the steps to allow for annealing and measurements. The leakage currents and depletion voltages of the devices increased with dose, as expected from bulk radiation damage. The double sided, double metal devices showed worse degradation than the less complex detectors.

1. Introduction

Run 2 of the Fermilab Tevatron collider is now expected to accumulate an integrated luminosity of 15 fb-1. This is a factor of eight higher than the exposure anticipated when the D0 Run 2 detectors were designed. As the run progresses, radiation damage to the silicon will gradually degrade the signal to noise ratio of the detectors, and well before 15 fb-1 is accumulated, the SMT will have to be replaced. The purpose of these studies was to determine the radiation lifetime of the "as built" D0 SMT detectors.

The measurements were made on detector sub-assemblies that didn't pass all of the strict acceptance tests for use in the SMT. However, for the selected devices, the performance of the silicon detector itself was not compromised by the deficiencies of the subassembly. Tested modules included:

-9-chip ladders (double sided) small stereo angle (2°, barrel layers 2,4)
-14-chip (double sided) wedge shaped large stereo angle (15°, F disks)
-6-chip ladders (double sided double metal) 90°detector, (inner barrel layers 1,3)
-3-chip ladders (single sided) (outer barrel layers 1,3)

Figure 1a is a photo of a 3-chip ladder. The ladder is made up of two silicon strip sensors, wire bonded together in the middle, with readout electronics covering the left two-thirds of the left half of the pair. Visible are 3 SVXII [reference 1] readout chips attached to the HDI (High Density Interconnect) hybrid. This is a single sided detector. Figure 1 b shows the double metal, double-sided 6-chip ladder, constructed from a single piece of silicon from a 6" wafer. This sensor has p-implanted strips running lengthwise on the ohmic side of the silicon, and n-implanted strips at 90° on the front side. The triangular pattern on the sensor marks where the n-side metal readout strips (across the short dimension of the sensor) are attached to a second layer of metal strips that take the signals to the SVXII chips. Each surface of this double-sided detector is read out with 3 SVXII chips. Figure 2a is a 9-chip, double-sided detector (single metal) with 4 SVXII chips visible on the ohmic side, and 5 more chips on the junction side. Finally, figure 2b shows the F Wedge detector (double sided, single metal), with 8 chips visible on the junction side, and 6-chips on the ohmic side. Whole subassemblies such as these were irradiated in the RDF beam line of the Fermilab booster. A future D0 note will describe this new facility.

For the irradiation, the samples were mounted inside a temperature controlled box attached to a moving table. The half width of the beam is nominally about 0.6 cm in both dimensions, so in order to irradiate the samples uniformly, the box was moved through the beam in ½ cm steps. The beam intensity was stable down to about 3E11 per spill. A repetition rate of 3 seconds was used, corresponding to a flux of about 3E11/cm2-sec.

Figure 1a 3-Chip Ladder (single sided)

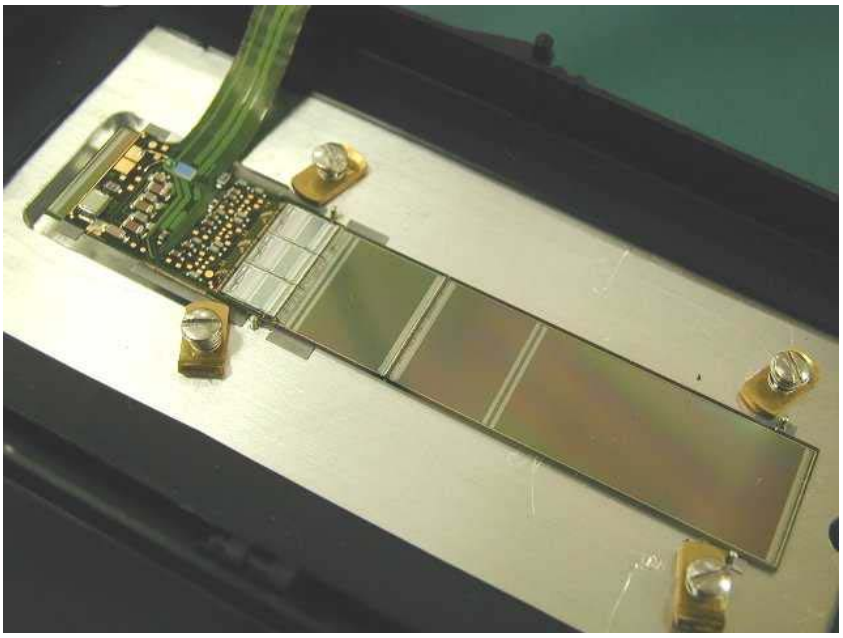


Figure 1b 6-Chip Ladder (double sided, double metal)

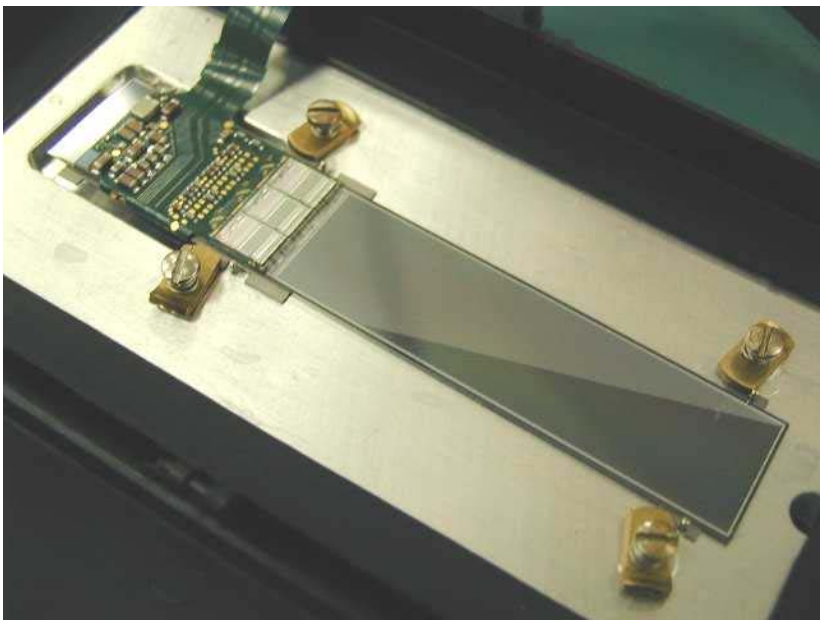


Figure 2a 9-Chip Ladder (Double Sided, single metal)

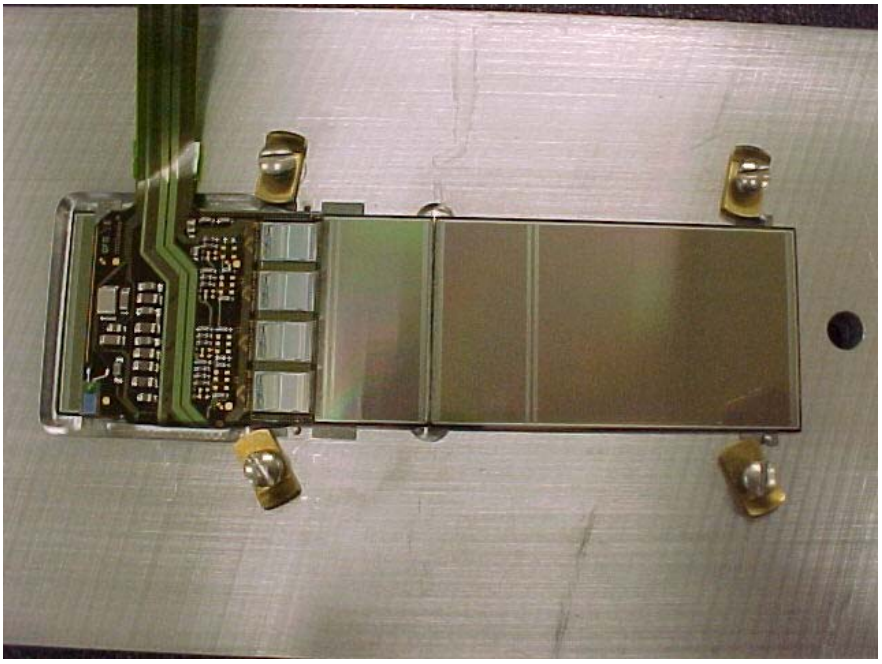
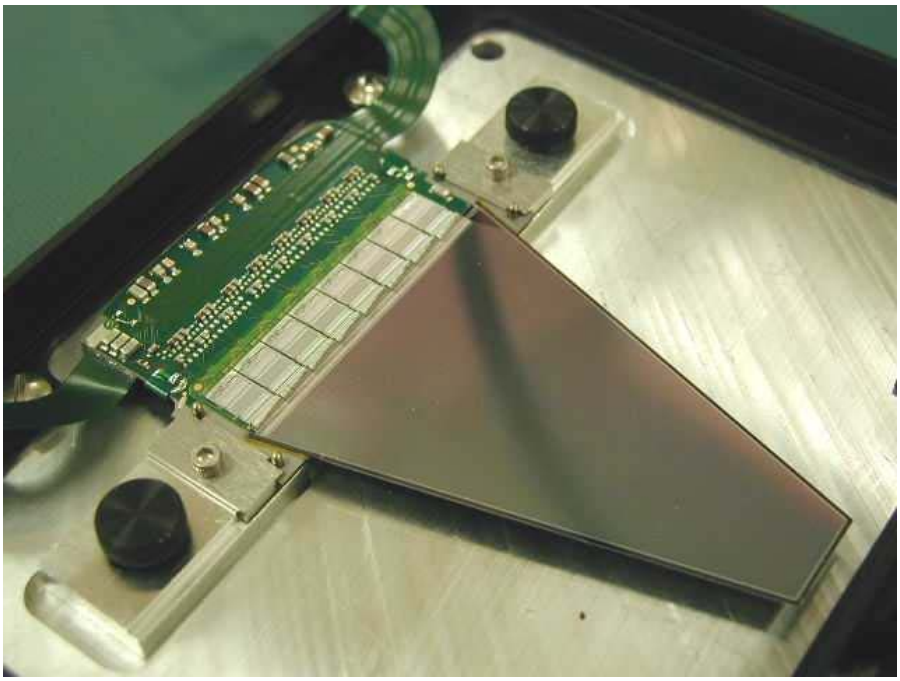


Figure 2b 14-Chip F Wedge (double sided, single metal)



2. The results of the measurements

After each irradiation the following measurements were made:

- Depletion voltage
- Leakage current
- Average noise
- Number of noisy channels
- Stability of the leakage currents versus time

The samples were irradiated at 5° C at RDF and then were kept at 5° C for about two days (until there was an access into RDF to remove them). Then they were taken to SiDet (Silicon Detector Lab at Fermilab) where they were kept at room temperature for about 40 hours. This was done to avoid the short-term charge up effects in the detectors due to the intense radiation, and to allow for short-term annealing of the samples. Afterwards they were stored in the "burn-in" test rack [reference 2] at SiDet which was kept at 7° C in a dry atmosphere. The first test was to measure the depletion voltage, so the subassemblies were removed one at a time and put on the laser test stand [reference 3] for 1-2 hours (at room temperature). Some other quick measurements at temperatures of +15° C and -5° C were also made, but the detectors spent most of their time at 7° C in the burn-in test stand. When the SVXII chips are powered, there is a temperature gradient across the sensor, so all of the quoted temperatures have some variation across the silicon, in addition to an uncertainty in the temperature measurement itself. A best guess is that the temperature is accurate to about plus or minus three degrees.

2.1 Depletion Voltage Measurements

A near infrared laser with a wavelength of 1063 nm was used to generate a signal in the silicon. The light was guided with a flexible fiber to strike the top surface of the detector, where most of the light passed between the aluminum readout strips and into the bulk of the silicon. The attenuation length of this light was measured [reference 2] to be about 206 μm in our silicon, so there was some light going through the entire 300 μm thick device. The charge induced on the readout strips in the illuminated area was measured as a function of applied bias voltage. The resulting curves typically have a linear portion, where the width of the depleted region is proportional to voltage, and a plateau region, corresponding to a fully depleted junction. For this paper, the depletion voltage is defined as the intersection of a straight line fitted to the linear region and a straight line fitted to the plateau region. [reference 6, 11]. Figure 3 and Table 1 show the resulting depletion voltages of the detectors versus exposed dose. In all the figures, the serial number of the particular detector that was measured is usually given. The first digit of the serial number is the number of SVXII chips that are mounted on the detector, and identifies the type of detectors used. For example, detector 6418 is the 6-chip (90° double sided, double metal) device. An exception to this numbering scheme is FW-239, which is the 14-chip (double sided, single metal) wedge shaped detector.

Figure 3 Depletion voltage vs. accumulated dose.

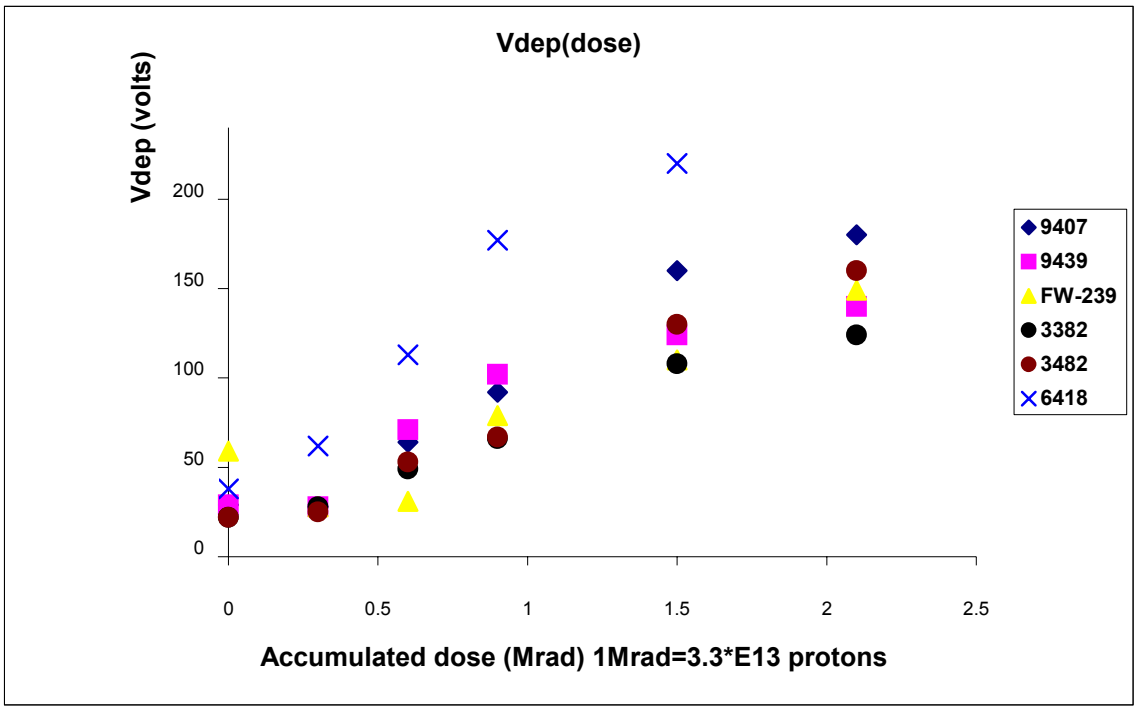


Table 1.

N of the detector	Number of SVXII chips	Vd before irradiation (volt)	Vd after 2.1 MRad (volt)	Ratio Vd before/Vd after
9407	9	29 ± 3	180 ± 30	6.2
9439	9	29 ± 3	140 ± 25	4.8
FW-239	14	59 ± 6	149 ± 25	2.5
3382	3	22 ± 3	124 ± 20	5.6
3482	3	22 ± 3	160 ± 25	7.3
6418	6	38 ± 4	Not found	

After an irradiation dose of 0.3 - 0.5 MRad we observed the well-known phenomena of type inversion - the transition from n-type to p-type bulk material. It is most clearly seen in figure 3 for the F-wedge detector, which started with a high initial depletion voltage of about 60V. The rise in depletion voltage with dose has roughly the same slope for all detector types, except for the 6-chip silicon ladder, which has a much steeper rise. The final bias voltage, which is necessary to deplete the F-wedge, 3-chip and 9-chip devices after a dose of 2.1 MRad, is within the range of 120-170V. This means that we also will probably be able to deplete these module types in the inner layer of the D0 SMT after exposure to 4-5 fb^{-1} [reference 4].

The different behavior of the depletion voltage for the 6-chip ladder is not understood. There was a significant difference in the construction of this sensor, since it was manufactured on a 6" wafer basis with a "double metal" buildup on the n side. Nominally, the first layer outside of the bulk silicon is about 1.1μ m of grown SiO2, etched down to 3000 A between the heavily doped strips in the bulk silicon and the aluminum readout strips (first metal). On the double metal side, an additional 3 μm of SiO2 is deposited by the PECVD process (Plasma Enhanced Chemical Vapor Deposition) to electrically insulate the first metal from the second metal layer. Both surfaces are then covered with a few μm of SILOX (~96%SiO2, ~4% P2O5) by the CVD process (Chemical Vapor Deposition).

To track down whether the anomalous depletion voltages of the 6-chip ladder was a feature of the bulk silicon, or a feature of the processing that builds up all the layers, measurements were made on the "test structure diodes" that were built into each of the 6" wafers. These diodes are simple devices with a single layer of metal on each surface. No anomalies were seen in the depletion voltages of the test structures after irradiation [reference 7]. So radiation damage to the bulk silicon is ruled out as the source of the differences in behavior of the 6-chip detector. We are left to conclude that either presence of the extra layer of SiO2 between the two metal patterns, or the processing involved in depositing the extra layer, makes the device more easily degraded by irradiation.

The measured pulse height of the illuminated strips versus applied voltage is shown in Fig.4 for 3-chip ladder and in Fig.5 for a 9-chip ladder. The plots contain both non-irradiated and irradiated detector measurements. After irradiation, the 3-chip and 9-chip ladders reached a plateau as the bias voltage was raised and we were able to determine the depletion voltage in the same way as before irradiation. The charge collection curve for the irradiated 6-chip ladder did not saturate as shown in Figure 6, and therefore the detector was not fully depleted after irradiation. To estimate the loss of the collected charge of the irradiated 6-chip ladder due to under-depletion, attempts were made to keep the laser light constant when comparing the response of the irradiated sample (6418) to a non-irradiated one. This measurement showed that 70% of the charge was collected by the irradiated ladder at the maximum possible operational voltage of 160-170V. Further increase of the bias voltage produced an unacceptable noise level.

Figure 4 Charge collection in 3-chip detector

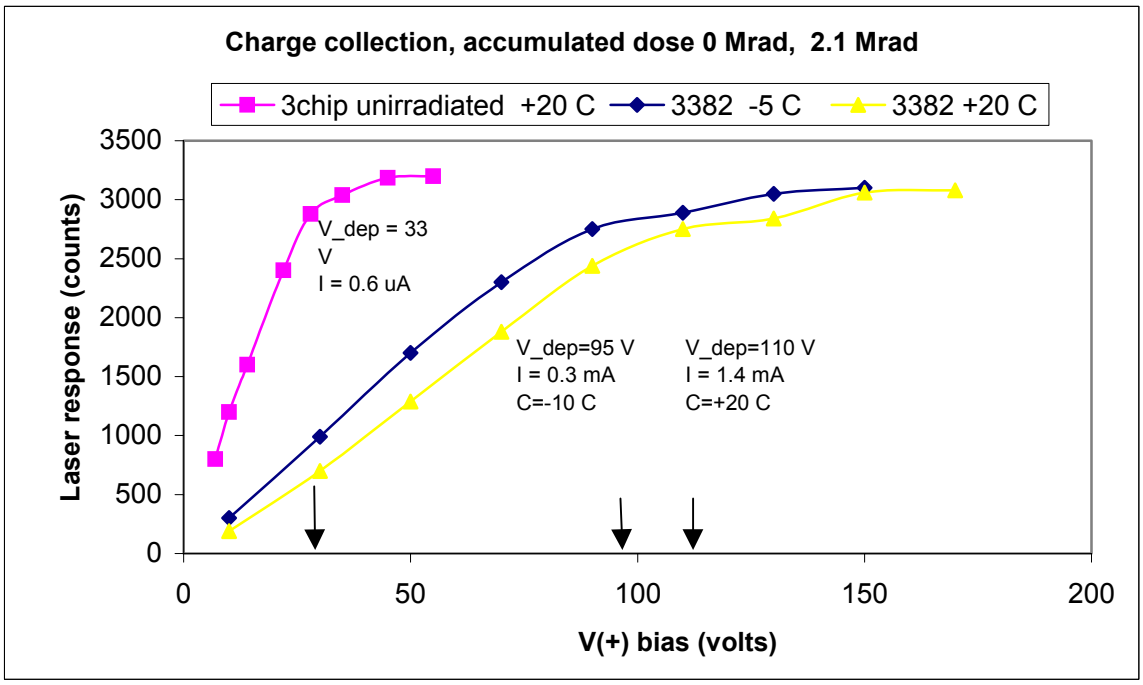


Figure 5 Charge collection in 9-chip detector

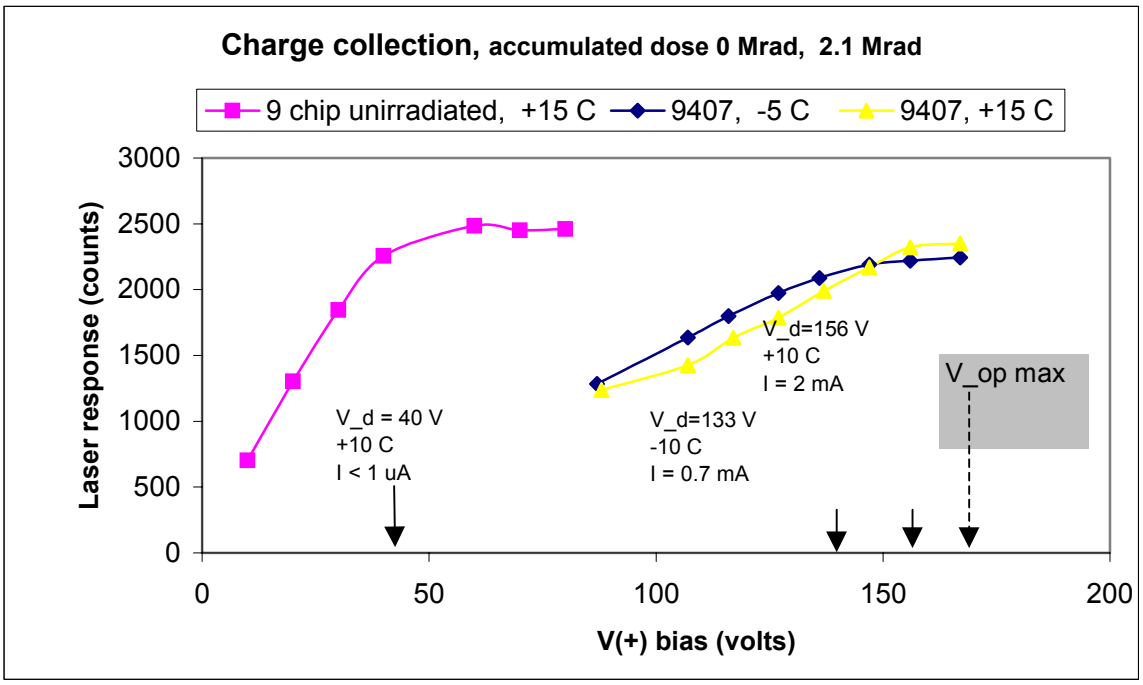
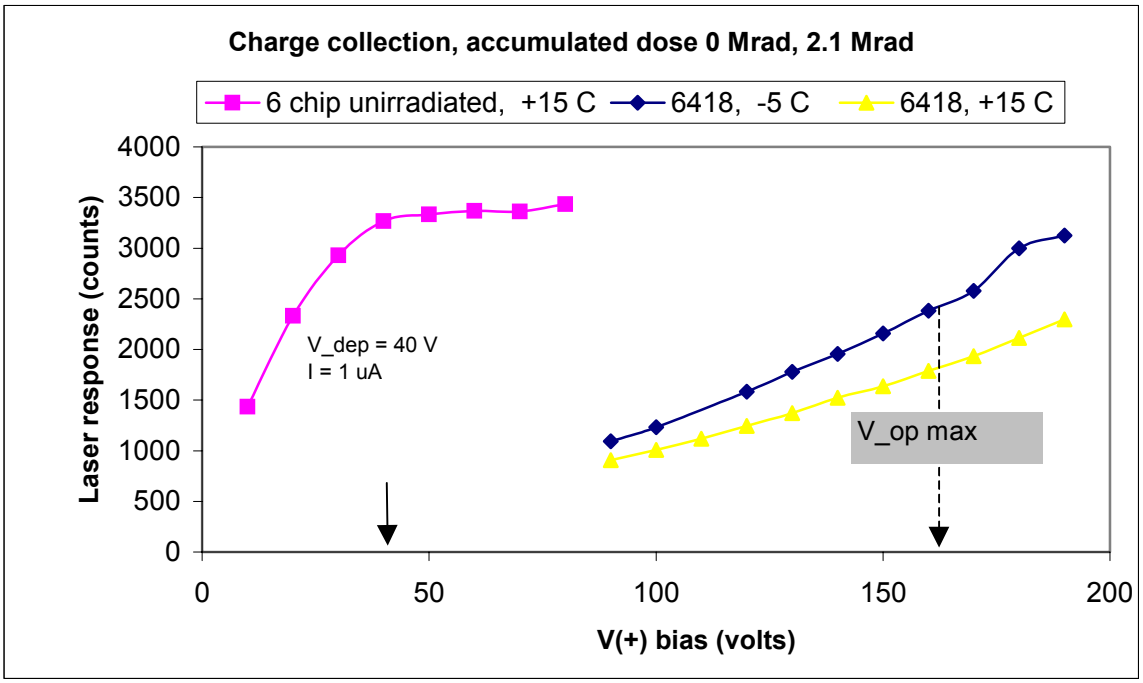


Figure 6 Charge collection in 6-chip detector



2.2 Leakage current

After about 5 more days of annealing at 7° C, leakage currents and detector noise were measured in the burn-in test stand. The same readout system was used that had been used for the extensive burn-in tests of all the modules that were put into the SMT. Aluminum plates in the burn-in rack were kept cool by circulating water at 3°C. The detector subassemblies were attached to the aluminum plates to sink the heat from the SVX chips when they were powered. The temperature of the SVX chips on the 9-chip ladder rose to 20° C, but the silicon itself remained close to 7° C.

The expected leakage current after irradiation can be calculated using the formula $I=I_0+\alpha\cdot Vol\cdot\Phi$, where I_0 denotes the leakage current before irradiation, α is the radiation damage coefficient, which is typically $3\text{-}4\cdot10^{-17}$A/cm at room temperature, Vol is the active volume of the detector, and Φ is the exposure fluence [reference 4]. Based on the known value of α we find an expected leakage current after 2.1 MRad of 17-23 $\mu A/cm^2$ at 7°C.

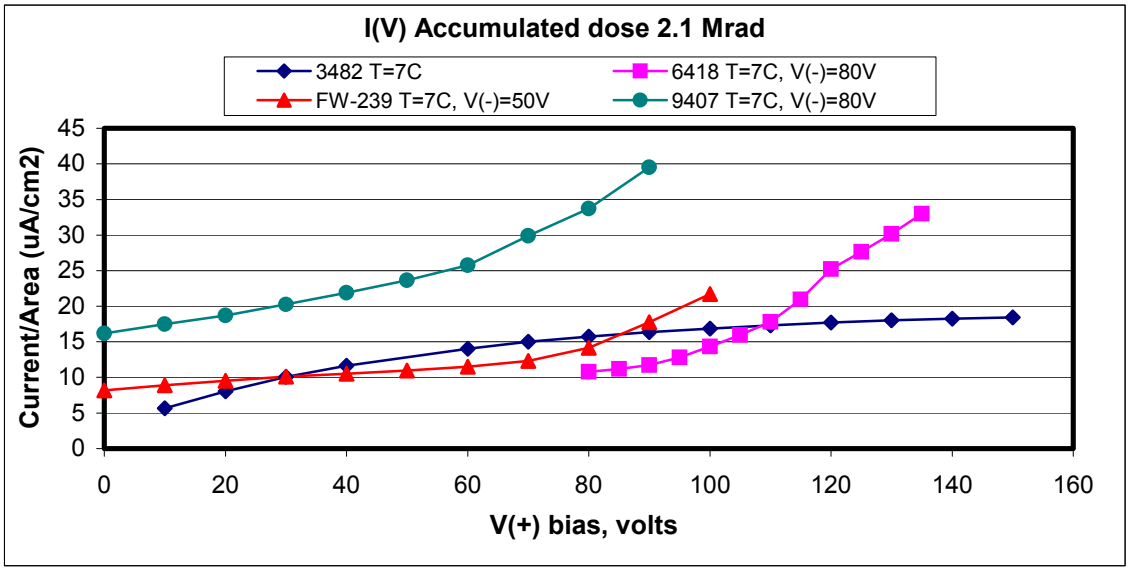
The measured leakage currents, normalized to the silicon area, after 2.1 MRad are shown in Fig. 7 as a function of the applied positive bias. The measured values are in fair agreement with the expected 17-23 $\mu A/cm^2$ at 7°C, indicating that short term annealing took place. Note that all double-sided detectors received an additional reverse (negative)

bias voltage of 50V or 80V on the p-side, so that the total potential across the detector is given by the sum of the two bias voltages on the two sides.

The single sided 3-chip detectors showed no sign of breakdown up to 150V. The double sided detectors without double metal (9-chip and 14-chip) have approximately the same area-normalized leakage current at full depletion, but seemed to be gently breaking down at about 140-150 Volts. The double-sided double metal detectors (6-chip), which could not be fully depleted, showed breakdown at a total voltage of about 180 Volts.

One consequence of the increased leakage currents of the detectors after irradiation is a higher shot noise. The shot noise contribution for a RC-CR shaper can be approximately calculated by $Q^2_{shot}=12\cdot I_{strip}\cdot\tau$ with I_{strip} being the strip currents in nA and τ the shaping time in ns [reference 8]. A calculation based on the expected leakage current increase after irradiation yields a shot noise contribution of ~2000e at T=20C, which is significantly reduced to ~1100e if the temperature of the silicon is lowered to T=7C. For a minimum ionizing particle traversing 300μ of silicon, about 24,000e is expected.

Figure 7 Leakage current



2.3 Average noise

The average noise of the different detector types after each individual irradiation step was measured in the burn-in test stand. Figure 8 shows the measured noise in ADC counts for the p side of all detector types after each step. The average noise on each detector side is the mean of the gaussian fit of the random noise distribution of all channels of a ladder. We used the same download parameters in the SVXII chip as in the real experiment where a minimum ionizing particle is expected to have the most probable charge of 26 ADC counts [reference 12]. The bias voltages were set for full depletion, (except for 6418, which could not be fully depleted after 2.1 Mrad). A clear increase in noise with higher fluence was observed, rising from a level of 1.5-2.5 ADC counts before irradiation to 3.0-3.5 ADC counts after 2.1 MRad. The largest relative increase of noise (by a factor of 2.3) is seen for the F-wedge detector, but the absolute value of its noise is similar to that for other modules after irradiation. The average noise for double-sided ladders goes up by 80% and for the single-sided detector by 40%. Based on the leakage current expectations at a temperature of 7° C, about 0.7-0.8 ADC counts of the ~1-1.5 count increase can be solely attributed to shot noise due to larger leakage currents. Other noise sources that may contribute to the noise increase with increased dose are discussed in reference 9.

Figure 8 Average noise on p side (at operating voltage)

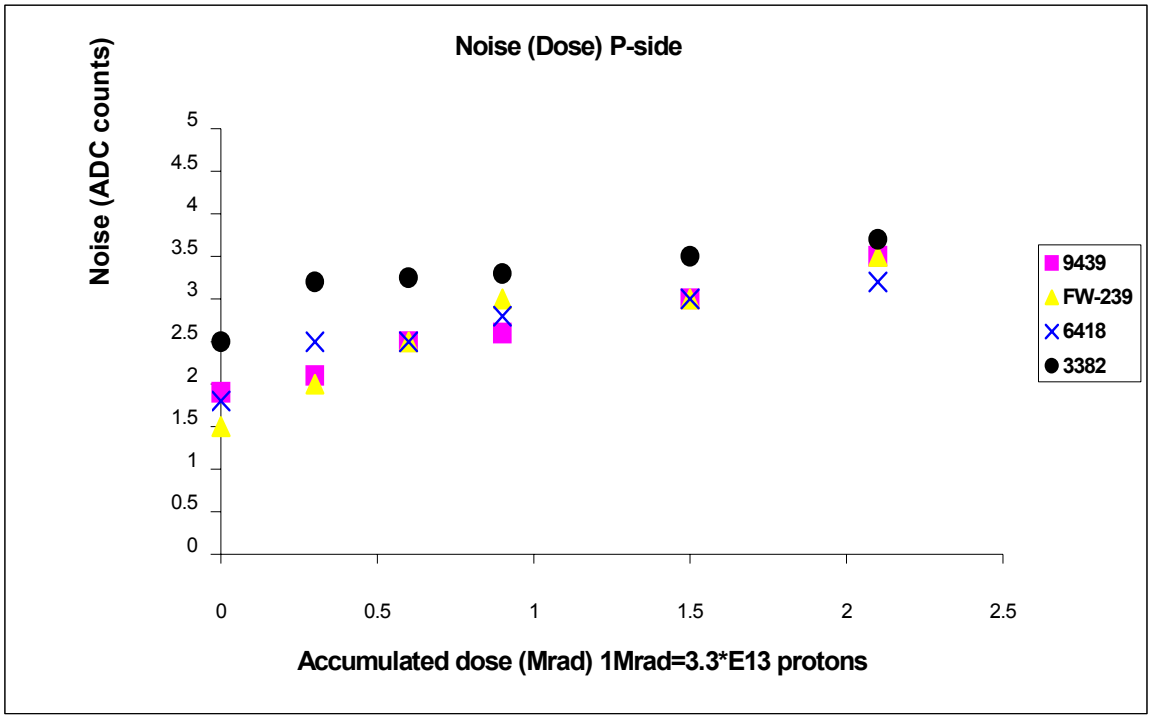


Figure 9 shows a similar plot for the n-side noise, where similar increases of about 70% are seen for the majority of tested modules. However, the noise on the n-side of the 6-chip detector increases with dose by a factor of 2.8 and reaches the highest absolute value of 5 ADC counts. This is reminiscent of previous observations of micro-discharges [reference 10] in the 6-chip ladders. Figures 10 shows noise versus bias voltage, after 2.1 Mrads, for the different sides of the 9-chip detectors at two different temperatures.

Figure 9 Average noise on n side (at operating voltage)

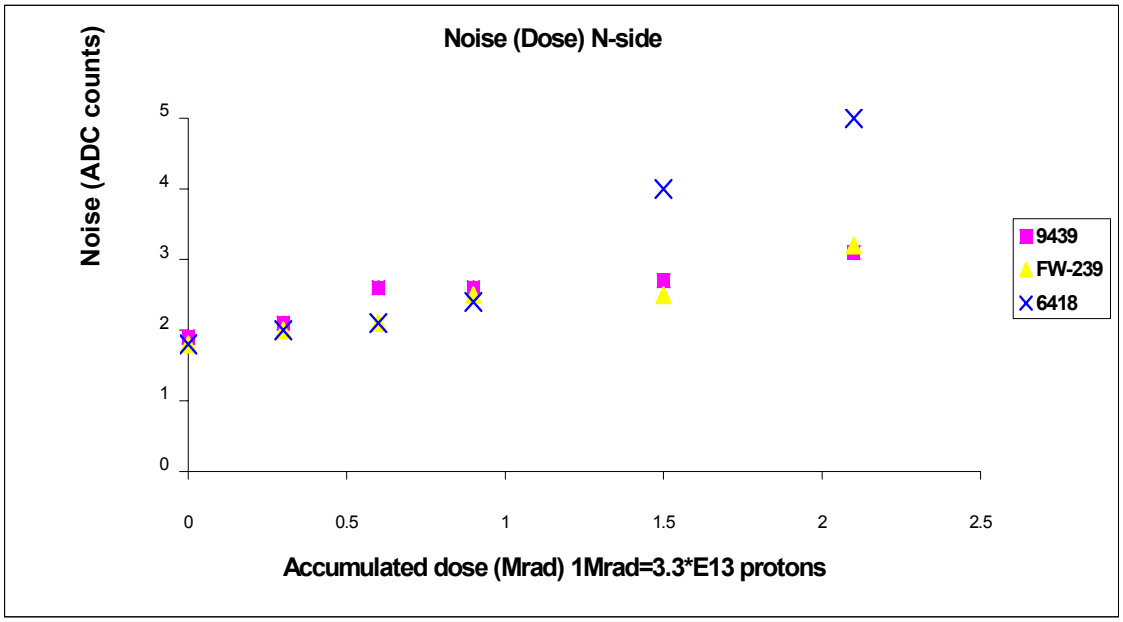
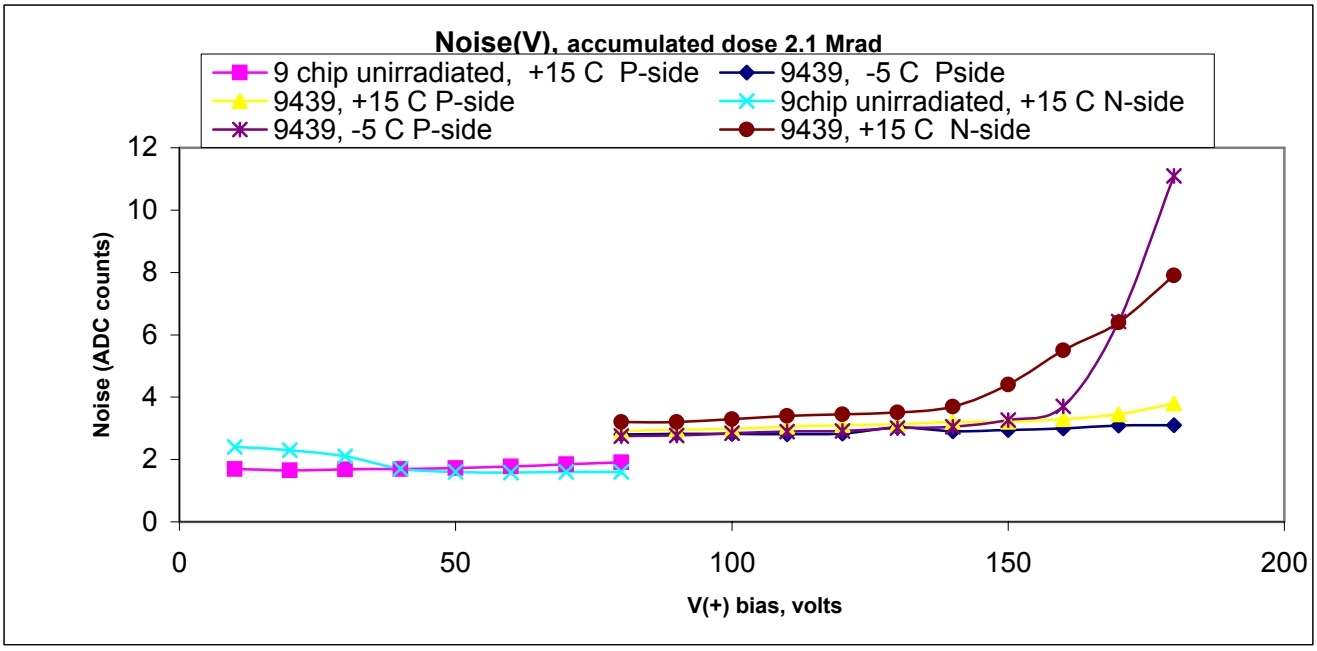


Figure 10 Noise versus voltage in 9-chip detector



2.4 Number of Noisy Channels

The number of noisy channels also comes from measurements in the burn-in test stand. Channel random noise was defined as sigma of the gaussian fit of the channel pedestal distribution after common mode subtraction. If channel random noise exceeded 6 ADC counts the channel was labeled as noisy. This value corresponds to approximately a four sigma deviation from the mean random noise of the normal channels. This definition of a noisy channel, based on the average random noise of the non-irradiated detector, was retained after irradiation. The number of noisy channels rose significantly after 1.5 MRad. The most dramatic increase was for the 6-chip ladder (n-side) Fig 11, as would be expected, since the corresponding average noise increased to 5 ADC counts, very close to the defined "noisy" threshold. However, the number of noisy channels dropped to an acceptable level just one month after the last exposure, as is shown in Fig. 12.

Figure 11 Noisy Channels

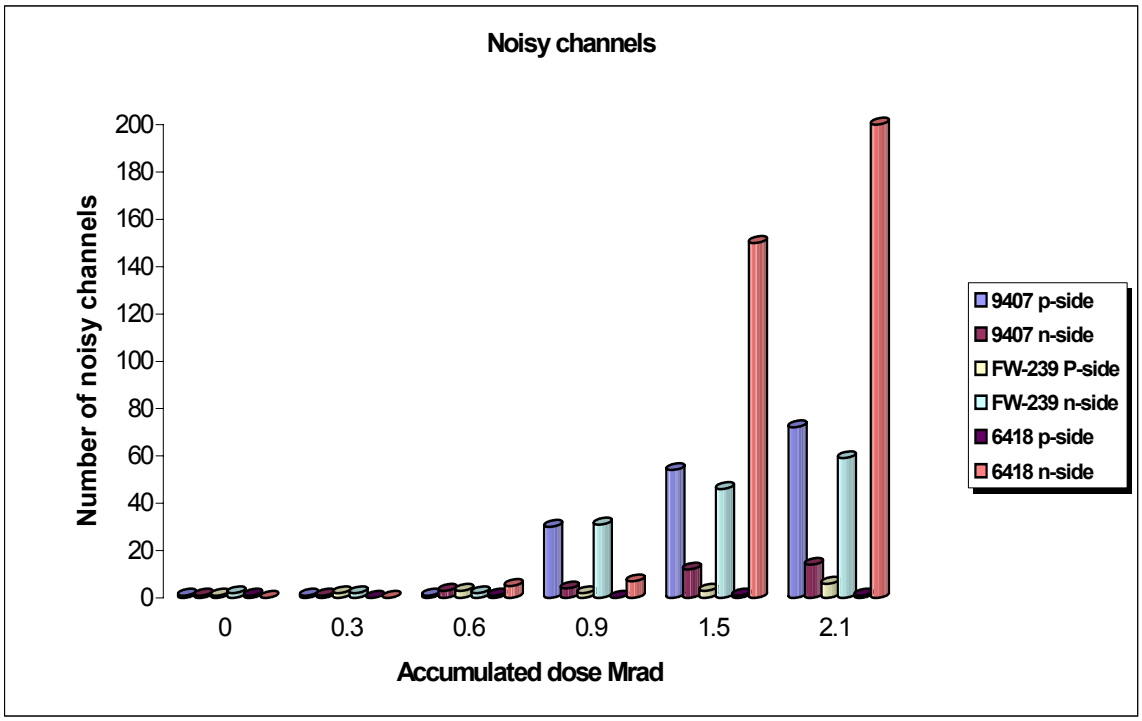
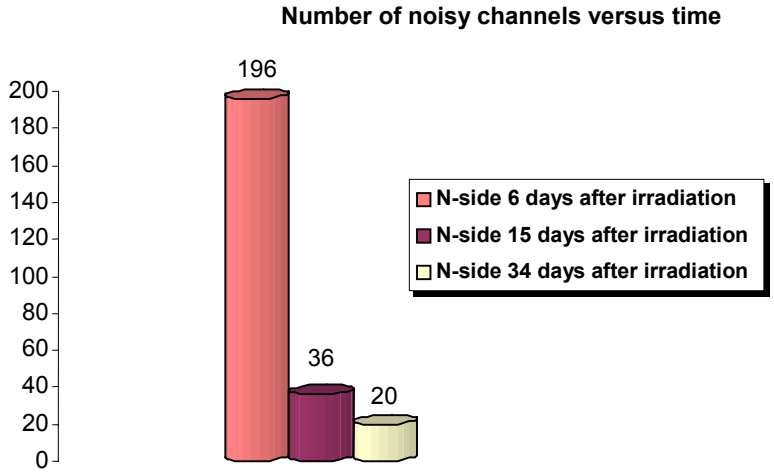


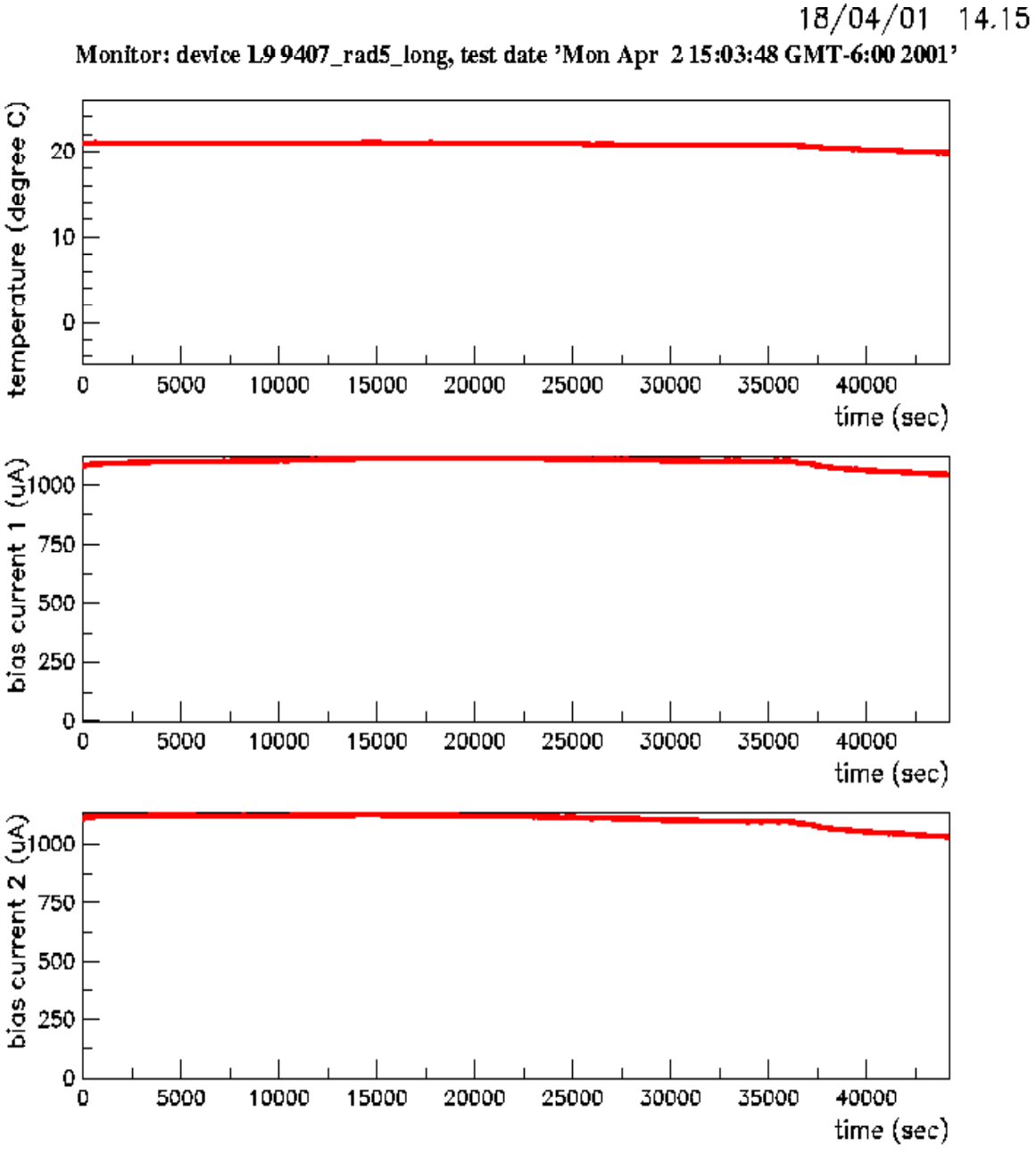
Figure 12 Noisy channel decrease in 6-chip detector



We measured the stability of the total leakage current of all the detectors during a 15 hour period. These measurements were done for all detectors after 2.1 MRad irradiation.

Figure 13 shows the temperature measured on the hybrid and the leakage current of the 9-chip detector versus time. Other detectors showed similar behavior. The leakage current decreased slightly following the decrease of temperature as expected.

Figure 13 Stability of current and temperature



3. Conclusions

Irradiation studies up to a total dose of 2.1 MRad have been done on some Run 2a SMT modules. Depletion voltage, average noise, number of noisy channels and stability of the leakage currents were measured. The depletion voltage increases as expected for 3- and 9-chip ladders. The double sided, double metal (6-chip) module could not reach full depletion after irradiation. For this detector (operated under-depleted), only about 70% of the expected charge was collected after 2.1 Mrad at the highest possible operation voltage. There is a large uncertainty in projecting these measurements to obtain an expected lifetime for the SMT detector since 2.1 MRad in our measurements was obtained in a few minutes while the inner layers of SMT will collect a similar dose in two years.

There is quite a spread in leakage currents, but they hover around the expected 17-23 $\mu A/cm^2$ at 7°C after 2.1 MRad.

A clear increase of average noise with higher fluence has been observed, rising on the p-side by a factor of two after 2.1 Mrad. The noise on the n-side exhibited a similar increase for the 9-chip ladder and the F-wedge.

The most dramatic increase of the number of noisy channels after irradiation was observed in the 6-chip ladder (n-side). However, this number dropped by a factor of ten after one month. The increase in n-side noise with dose for the 6-chip detectors was consistent with previous observations of micro-discharges.

During stability measurements all detectors behaved similarly, and no anomalies were seen during the 15 hour test.

References:

1. A Beginners Guide to the SVXIIE, Fermilab-TM-1892, October 1996
2. D0 Note 3841, Electrical Production Testing of the D0 Silicon Microstrip Tracker Detector Modules
3. Fermilab TM 1849 Pulsed LASER for Testing Silicon Strip Detectors, Mario Vaz, Selcuk Cihjangir, Petros Rapidis, July 1993
4. Conversion of the integrated luminosity into the radiation dose accumulated by SMT is discussed in "New Leakage current, noise and depletion voltage expectations for Run II b" by Frank Lehner, D0 Note 3959
5. RD 48 Status Report, CERN/LHCC 2000-009
6. Alessandro Boffini, 9th Vienna Conference on Instrumentation VCI 2001, Feb. 19-23
7. Sara Lager, Master Thesis, in preparation
8. H. Spieler IEEE Trans. Nucl. Sci. NS-32, 419 (1985)
9. S.M. SZE, Physics of Semiconductor Devices, Second Edition 1981, p.111
10. F. Lehner, D0 note 3804
11. F.Rizatdinova D0 note 3832, Laser test of silicon detectors at D0
12. M.T.Roco, D0 note 3405 Analysis of SMT Beam Tests Data