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A 5KV, 3MHz Solid-state Modulator Based on the DSRD Switch for an Ultra-fast Beam Kicker

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ABSTRACT

A solid-state modulator is being developed at the SLAC National Accelerator Laboratory for ultra-fast broadband beam deflection. The modulator design is based on an opening switch topology that uses Drift Step Recovery Diodes (DSRDs) as the opening switches. The modulator provides nano-second length pulses into a 50 Ω load, i.e. a strip line kicker. The rise and fall time of the kicker is primarily determined by the switching characteristic of the DSRD and has been measured as approximately 1.5ns with a 5kV output voltage. A pumping circuit for the DSRD kicker has been developed to drive 200A through the DSRD with a 3MHz repetition rate.

Index Terms – **DSRD, modulator, solid-state, nanosecond**

1 INTRODUCTION

Many fast switching, high power applications benefit from solid state switches to achieve higher system performance, reliability and lifetime requirements. At MW power levels and nanosecond time scales, solid state options are limited. One option, the Drift Step Recovery Diode (DSRD) has been demonstrated as capable of blocking thousands of volts and switching in nanosecond to sub-nanosecond ranges [1-6].

As a diode, the DSRD is implemented in opening switch topologies. In this mode, the DSRD operates much like a normal step recovery diode [7]. During forward conduction, charge is stored near the *pin* junctions in the form of minority carriers. During recovery, this charge is swept away and the depletion region is restored very quickly. The turn off transient occurs precisely when the extracted charge is equal to the pumped charge and the DSRD is switched off.

The DSRD has a very precise doping gradient to carefully control the distribution of minority carriers under pulsed conditions. This doping gradient maintains high switching speeds even under large current densities. When used as an opening switch, the DSRD can exhibit switching speeds close to the theoretical limit of silicon even at high voltage [6]. Voltage rise rates > $2 \cdot 10^{12}$(v/s) can be achieved with DSRD arrays under specific conditions.

To take the greatest advantage of the doping gradient, charge must be pumped into and then extracted from the DSRD under pulsed conditions. The specific DSRD package used in this project was designed and built at Ioffe Physical Institute and was specifically designed for peak recovery currents of 200A. This paper discusses a modulator built to resonantly pump the DSRD and create 200A recovery currents under which the DSRD opens creating 5kV pulses on a 50Ω load.

2 PULSE MODULATOR CIRCUIT

The 5kV modulator was built as a precursor to a 10kV ultra-fast pulser for a 50Ω stripline beam kicker. The pulser was designed for high frequency operation over short bursts with a fast rise and fall time. The modulator performance goals are summarized in Table 1.

Table 1: Modulator demonstration performance goals for driving an ultra-fast stripline beam kicker. The 5kV modulator would form half of the 10kV system.

Output voltage	5 kV
Burst repetition rate	3 MHz
Pulses per burst	30
Macro repetition rate	5 Hz
Flattop pulse length	4 ns
Risetime	1 ns
Falltime	~ 1 ns
Load impedance	50 Ω

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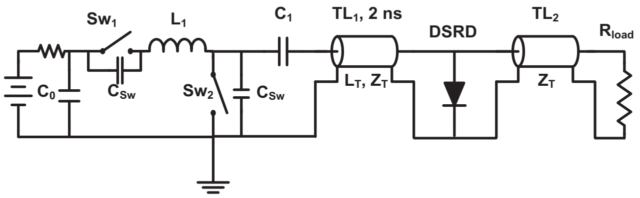

Figure 1. 5 kV modulator circuit diagram. The circuit is designed to pump the DSRD and create a 200A peak recovery current precisely when the DSRD is depleted of charge. The circuit parameters are shown in Table 2.

Table 2: Modulator circuit parameters. L$_1$ and C$_1$ were specifically chosen to create proper resonant circuit impedances. Parasitic switch capacitance C$_{Sw}$ was significant enough to be included in the analysis of the circuit.

C_0	12 μF
C_{Sw}	400 pF
L_1	300 nH
C_1	1.88 nF
L_T	90 nH
Z_T	50 Ω
R_L	50 Ω

While the output pulse risetime is determined by the switching characteristics of the DSRD, a 200A recovery current must be generated by the modulator pumping circuit. A circuit diagram of the 5kV DSRD modulator is shown in Figure 1. The circuit operates in 3 distinct stages.

Stage 1 occurs when switch S$_{W1}$ is actively closed and capacitor C$_1$ is charged through the path: L$_1$, C$_1$, TL$_1$, DSRD. Capacitive voltage doubling is observed on capacitor C$_1$. During this stage the DSRD functions as low impedance, but in fact is storing charge near its *pin* junctions, as previously mentioned.

Stage 2 begins when switch Sw$_1$ is actively opened and switch S$_{W2}$ is actively closed. This event is closely tied to when zero current is flowing through inductor L$_1$ to minimized voltage transients due to stored energy in the inductor. During stage 2, capacitor C$_1$ is shunted to ground through the path: TL$_1$, C$_1$, DSRD. During this stage the DSRD behaves as low impedance until the instant when stored charge is depleted and the DSRD abruptly turns off.

Stage 3 begins when the DSRD opens and current commutates from the DSRD to the output transmission line TL$_2$. At this moment transmission line TL$_1$ releases its stored energy in the form of a pulse transmitted to the matched 50Ω load through TL$_2$. The duration of the pulse is approximately twice the electrical length the transmission line TL$_1$, 4 ns.

The magnitude of the peak recovery current is determined by the impedance of stage two, Z$_2$ and the peak voltage on capacitor C$_1$. The stage 2 impedance is expressed by equation (1), where R$_{Sw2}$ is the on-state resistance of switch 2. In order to minimize the added switch resistance and reduce the peak voltage observed by a single device, an array of MOSFETs were used: 2 in series by 4 in parallel. This circuit used 16 total DE475-102N21A Power MOSFETs.

$$Z_2 = \sqrt{\frac{L_{TL1}}{C_1}} + R_{Sw2} \tag{1}$$

A picture of the fully constructed pumping circuit is shown in Figure 2. Identical low inductance MOSFET arrays were used for both switch 1 and switch 2. These arrays take up the bulk of the physical space of the modulator. Inductor L$_1$ is an air core helical inductor. Ceramic capacitors were used for low loss and high stability at high frequency for both the energy storage capacitance C$_0$, and the resonant pumping capacitor C$_1$.

High voltage isolation was needed for the gate connections of the MOSFET arrays. This was accomplished by isolating the trigger signal from each gate driver through a high voltage isolation pulse transformer. The trigger signal for both switches, Sw1 and Sw2, were amplified on the low voltage side of isolation from a trigger generator and distributed to the MOSFET gate drivers at high voltage.

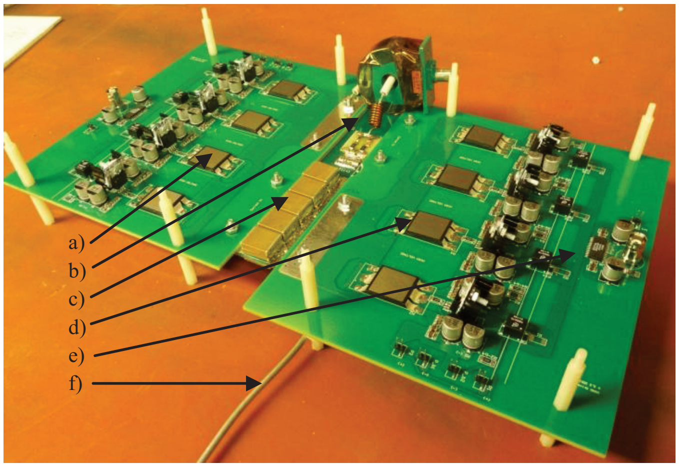

Figure 1. The 5kV pumping circuit. Shown are a)Sw$_1$array, b)L$_1$, c)energy storage capacitors, d)Sw$_2$ array, e)transformer isolated trigger circuit, f)TL$_1$ The DSRD is connected to the end of transmission line TL$_1$ outside of the picture range.

3 TESTS

Tests were performed on the described circuit under a range of charge voltages. Charge voltage was used to vary the pumping current and thus amplitude of the output voltage pulse. The charge voltage was increased up to the point at which Sw$_1$ and Sw$_2$ were over-stressed by voltage. Careful timing of stages 1 and 2 was accomplished by observing the time of zero current through inductance L$_1$. The load voltage was measured with a 50Ω high voltage, high frequency attenuator.

Generally charging was limited to 1kV or less. This was because during stage 2, voltage across Sw_1 was observed to oscillate about the charge voltage with amplitude equal to two times the charge voltage. This oscillation was produced by the LCL circuit formed between the storage capacitance, the switch parasitic capacitance and inductance L_1. On several occasions, MOSFET arrays failed due to overvoltage.

3.1 High Voltage

The DSRD modulator was tested up to 200A, with 5kV delivered to a 50Ω load. Single shot 5kV output pulses were formed with a charge voltage of about 1kV. Figure 3 shows a measured single shot output pulse at 5kV. The 10-90% rise time of the pulse was 1.5 ns. The pulse width (FWHM) was 4.7ns. After the voltage pulse, the voltage at the 50Ω load remained very low demonstrating low residual power in the circuit elements downstream of Sw_2.

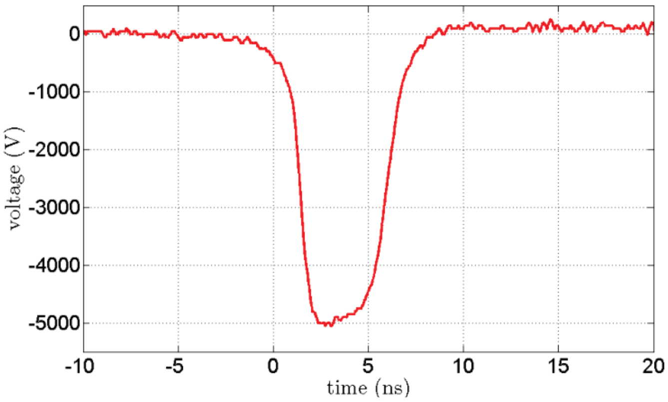

Figure 2. A single 5kV pulse formed by the DSRD modulator.

3.2 High Frequency

The modulator was also tested with a repetition rate of 3MHz for 30 pulse bursts. Figure 4 shows measured 3MHz bursts. In Figure 4a, the amplitude of the first pulse was 4kV. The pulse train was stable, but contained some pulse to pulse droop. The droop was caused by the use of a 1μF energy storage capacitor used during this shot rather than a 12μF capacitor.

In Figure 4b, the amplitude of the first pulse was 4.75kV. The pulse train became highly unstable from shot to shot. It was discovered that the pumping circuit was susceptible to oscillations which would cause MOSFETs to turn on when operated above a certain threshold. This resulted in oscillations on capacitor C_1 which created unpredictable pumping currents through the DSRD. The output voltage pulses became erratic in time and magnitude under this mode of operation.

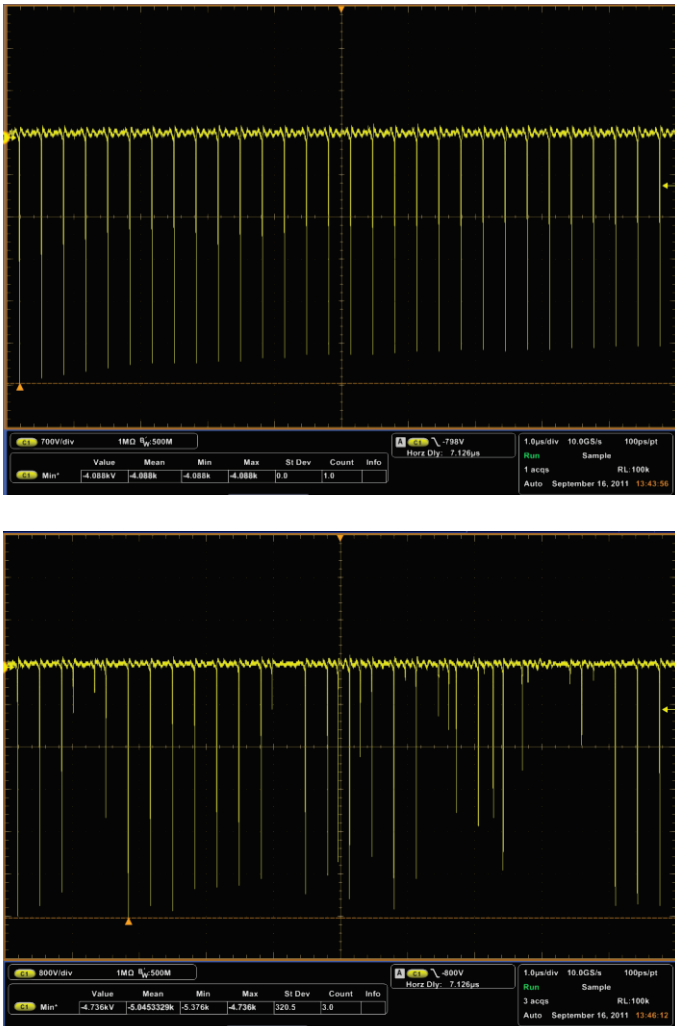

Figure 3. 3MHz pulse train data taken with the DSRD modulator. a) With an output voltage of 4kV, the pulse train was consistent with the pumping current. b) When the output voltage was increased to near 5kV, oscillations in the pumping circuit created erratic output voltage pulses.

4 STATUS

5kV pulses with a 1.5ns risetime have been formed with the DSRD and a 200A pumping circuit. 3MHz, 30 pulse bursts were demonstrated at 4kV, corresponding with a pumping current of 160A. Above 4kV, the pumping circuit has exhibited instability due to oscillations which cause the output voltage to become erratic.

Work is on-going to make the pumping circuit more robust. Filters are being added to the circuit to dampen out post-pulse oscillations. Also, improvements to the MOSFET arrays are being made to further de-stress components and ensure reliable MOSFET gate signals.

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