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TRIPLE-COINCIDENCE WITH AUTOMATIC CHANCE COINCIDENCE CORRECTION*

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*Research carried out under the auspices of U. S. Nuclear Regulatory Commission.

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ABSTRACT

The chance coincidences in a triple-coincidence circuit are of two types - partially correlated and entirely uncorrelated. Their relative importance depends on source strength and source and detector geometry so that the total chance correction cannot, in general, be calculated. The system to be described makes use of several delays and straightforward integrated circuit logic to provide independent evaluation of the two components of the chance coincidence rate.

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In coincidence counting measurements, it is often necessary to make corrections for chance coincidences. In two-fold coincidence systems, these corrections can be made analytically, if the singles counting rates are known and constant and if the coincidence resolving time is known. If the average counting rates are not constant in time, as is the case with decaying sources or pulsed accelerators, one generally has recourse to one of several techniques[1,2,3] for simultaneously measuring the "chance" and the "true-plus-chance" rates. Although differing in detailed execution, these systems all introduce a delay in one input which is long compared to the coincidence resolving time to eliminate all "true" coincidences, and then count both with and without this added delay in the same or in similar coincidence circuits.

Triple coincidence systems, however, present a somewhat different problem because, even with constant average counting rates and known resolving time, the chance rate cannot, in general, be determined analytically. This is due to the fact that the chance coincidences are composed of a mixture, in undefined proportions, of entirely uncorrelated and partially correlated signals. The partially correlated events $C_{2,1}$ are those in which two of the three inputs are in "true" coincidence whereas the third input, by chance, occurs within the resolving time, whereas the entirely uncorrelated events C_3 are those in which all three inputs arrive, by chance, within the resolving time. The relative importance of $C_{2,1}$ and C_3 depends on the source strength (C_3 varies as the cube of the source strength while $C_{2,1}$ varies as the square) and also on the geometry of the source-detector arrangement, since some of the double coincidences may be the result of particles or gamma rays scattering between two detectors.

The problem of triple-coincidence accidental evaluation came up recently in an apparatus designed to assay fissionable material by detecting neutron induced fission. The neutron-irradiated sample is surrounded by three large plastic scintillators, the fission signature being gamma-ray cascades from fission products and/or fission neutrons triggering all three scintillation counters simultaneously. Some of the samples are mixed with various amounts of thorium which produces a high background of paired gamma rays which contributes to both the C_3 and $C_{2,1}$ chance rates. The system to be described provides for the simultaneous evaluation of the true-plus-chance rate $(T + C_3 + C_{2,1})$ and the two components of the chance rate so that the true coincidence rate T can be unambiguously evaluated.

Each of three detectors fires a constant-fraction discriminator[4] which in turn triggers a monostable multivibrator. The monostable outputs are mixed in a three-input "and" circuit which generates an output whenever all three signals overlap. The durations of the monostable outputs (30 ns, in our case, to allow for neutron flight times) determine the coincidence resolving time. Each coincidence monostable triggers a delay (also about 30 ns), after which the original monostable is retriggered. This tail-chasing process continues, the number of cycles being monitored by three two-stage binary counters, until each input has produced a train of three gates. All of the three gate durations corresponding to a particular input are precisely equal because they are generated by the same monostable, after a delay which is long compared to the monostable recovery time. These gates will be referred to as G_0, G_1 and G_2 (see Fig. 1) with additional subscripts corresponding to the inputs 1, 2 or 3.

The true-plus-chance counting rate $(T + C_3 + C_{2,1})$ is determined by counting the overlaps of gates G_{01}, G_{02} and G_{03} (the earliest gates associated with each of the three inputs), so that:

$$G_{01} \times G_{02} \times G_{03} = T + C_3 + C_{2,1} \tag{1}$$

The chance component $C_{2,1}$ is determined by the "or" combination of three "and" gates $(G_{01} \times G_{02} \times G_{13})$, $(G_{11} \times G_{02} \times G_{03})$ and $(G_{01} \times G_{12} \times G_{03})$, respectively. It is necessary to generate coincidences with all three "true" binary pairs because, due to geometrical considerations, the two-fold true coincidence rates between the various detector pairs are not necessarily equal.

In addition to coincidences of the type $C_{2,1}$, each of the three "and" circuits also counts entirely uncorrelated events of the type C_3.

Therefore:

$$(G_{01} \times G_{02} \times G_{13})+(G_{11} \times G_{02} \times G_{03})+(G_{01} \times G_{12} \times G_{03}) = C_{2,1} + 3C_3 \ . \tag{2}$$

C_3 can be determined by any one of three combinations of gates G_0, G_1 and G_2 from the various inputs. To preserve circuit symmetry and to improve the statistical precision by counting more events, it was decided to count all three possibilities. Thus:

$$(G_{01} \times G_{12} \times G_{23})+(G_{11} \times G_{22} \times G_{03})+(G_{21} \times G_{02} \times G_{13}) = 3C_3 \quad . \tag{3}$$

It remains, now, to identify these variously labelled gates in terms of the three monostable output signals M_1, M_2 and M_3 and the three two-bit counters whose outputs are A, $\overline{A}$ and B, $\overline{B}$ with appropriate subscripts corresponding to the input number. G_{01}, for example, may be characterized by $(M_1 \times \overline{A}_1 \times \overline{B}_1)$, whereas G_{13} is $(M_3 \times A_3 \times \overline{B}_3)$.

The logic equations were transformed somewhat to take advantage of the MECL 10,000 series triple three-input NOR gates and the wired-OR feature available with emitter-coupled logic. The three time intervals (0,1,2) for each input are initially defined (see Fig. 1) as $\overline{A} \times \overline{B} = P$, A and B respectively. The threefold coincidence between the monostable outputs $(M_1 \times M_2 \times M_3)$ is implemented as $\overline{(\overline{M}_1 + \overline{M}_2 + \overline{M}_3)}$ using one three-input NOR gate. Equations (1), (2) and (3) were implemented in hardware as:

$$\overline{(\overline{M}_1 + \overline{M}_2 + \overline{M}_3)} \times \overline{(\overline{P}_1 + \overline{P}_2 + \overline{P}_3)} = T + C_3 + C_{2,1} \tag{4}$$

$$\overline{(\overline{M}_1 + \overline{M}_2 + \overline{M}_3)} \times [\overline{(\overline{P}_1 + \overline{P}_2 + \overline{A}_3)} + \overline{(\overline{P}_1 + \overline{A}_2 + \overline{P}_3)} + \overline{(\overline{A}_1 + \overline{P}_2 + \overline{P}_3)}] = C_{2,1} + 3C_3 \tag{5}$$

$$\overline{(\overline{M}_1 + \overline{M}_2 + \overline{M}_3)} \times [\overline{(\overline{P}_1 + \overline{A}_2 + \overline{B}_3)} + \overline{(\overline{P}_2 + \overline{A}_3 + \overline{B}_1)} + \overline{(\overline{P}_3 + \overline{A}_1 + \overline{B}_2)}] = 3C_3 \tag{6}$$

where each function in curved brackets was realized by a three-input NOR gate and where the OR functions inside the square brackets were realized by wiring the outputs of the three NOR circuits in parallel. The timing situation is such that all the routing conditions (P,A,B) are either initially established or set up during the delays between timing gates so that the resolving times for the overall logic functions are determined exclusively by the monostable durations M_1, M_2 and M_3.

The gate and delay monostables were all made up of MECL "D" type flip-flops, reset after an RC delay by an inverter (Fig. 2). Periods from 5 ns up can be realized with the MC10231 flip-flop. The ratio of period to recovery time is a function of the value of the timing pull-down resistor R and can easily be made greater than ten.

Performance

The system was tested in an arrangement where there was a substantial number of true double coincidences but no true triple coincidences. This was accomplished by connecting two of the inputs to two scintillation counters viewing the same Co^{60} source of coincident gamma rays and the third to a periodic pulse generator. Operating at singles counting rates at the three inputs between 200,000 and 300,000 counts per second, and with a true double coincidence rate between the two scintillation counters (corrected for chances) of about 10,000 counts per second, the following counts were recorded during a 20,000 second counting interval:

$$T + C_3 + C_{2,1} = 3,983,943 \quad (7)$$

$$C_{2,1} + 3C_3 = 5,860,320 \quad (8)$$

$$3C_3 = 2,902,690 \quad (9)$$

Subtracting 2/3 of (9) from (8), one obtains:

$$C_3 + C_{2,1} = 3,925,193$$

which differs from (7) by only 1.5%, confirming the fact, to reasonably good accuracy, that there are no true triple coincidences T.

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FIGURE CAPTIONS

1. Timing diagram showing an input signal, the corresponding gate waveform and the states of the counter flip-flops.

2. Circuit diagram showing the gate and delay monostables and the counter flip-flops. The flip-flops (rectangles) are MC10231 and the NOR gates are MC10102.

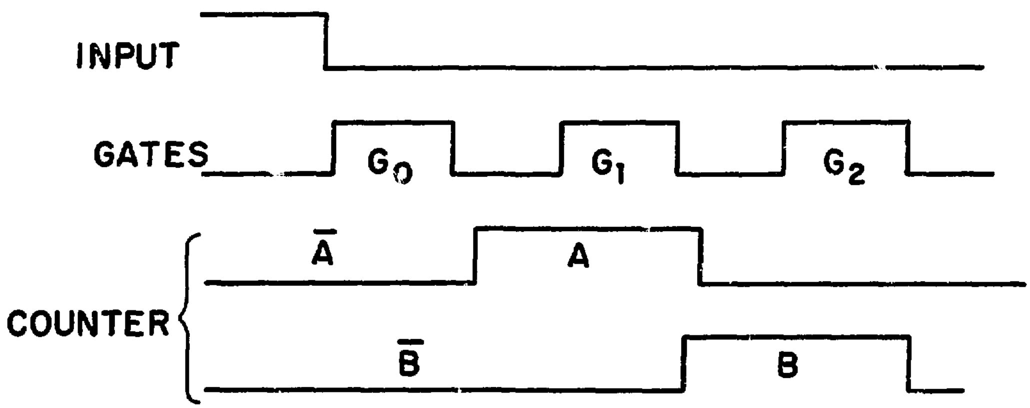
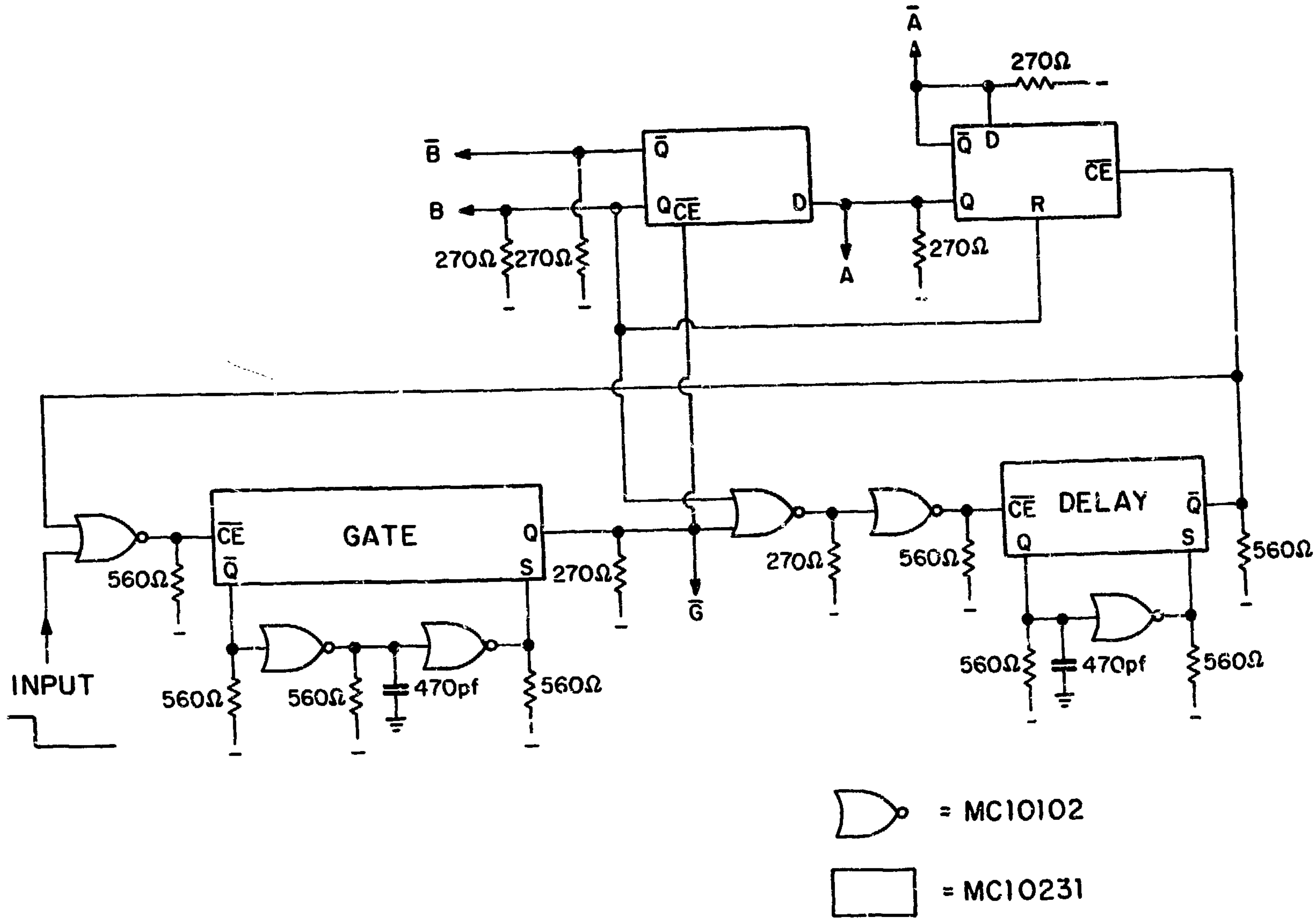


FIGURE 1



INPUT
GATE
DELAY
CE
Q
S
D
R
A
B
G
270Ω
560Ω
470pf
= MC10102
= MC10231

FIGURE 2