FUNCTIONAL DESCRIPTION OF THE EBR-II DIGITAL DATA ACQUISITION SYSTEM

by

J. M. Allen,* R. W. Hyndman, R. A. Call, E. W. Laird,
M. R. Tuck, and K. D. Tucker

EBR-II Project
Argonne National Laboratory
Argonne, Illinois - Idaho Falls, Idaho

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LIST OF SYMBOLS USED

Symbol	Definition
A/D	analog-to-digital
AIO	acknowledge input/output interrupt
BEI	Beehive Electrotech Inc.
bit	binary digit
byte	four bits
CALCOMP	Calcomp Inc.
CD	controller/digitizer
COC	character-oriented communications
CPU	central processing unit
DAS	digital data acquisition system
DC	device controller
DIO	direct input/output
DM	differential multiplexer
EBCDIC	extended binary coded-decimal interchange code
EIA	Electronics Industries Association
FET	field-effect transistor
HIO	halt input/output
I/O	input/output
LSB	least significant bit
MAC	MAC Panel, Inc.
MD	multiplexer/digitizer
MIOP	multiplexing input/output processor
MSB	most significant bit
PC	primary controller
RAD	rapid-access disk
SIO	start input/output
TDV	test device
TIO	test input/output
WD	write direct
XDS	Xerox Data Systems

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ABSTRACT

The EBR-II digital data acquisition system (DAS) is a Sigma 5 computer specifically configured to perform data acquisition and detailed on-line data reduction. The hardware description contained herein describes each of the major components and its interaction with the other system components. The description enables an understanding of the hardware, hardware interaction, and some of the considerations necessary for developing the system software.

I. GENERAL DESCRIPTION OF SYSTEM

The EBR-II digital data acquisition system (DAS) consists of a Xerox Data Systems (XDS) Sigma 5 digital-computer system with an associated analog-to-digital (A/D) front end and peripheral equipment. For simplicity, the system can be broken down into three major groups: (1) the A/D front end, (2) the Sigma 5 computer, and (3) peripheral input/output (I/O) equipment. Figure 1 shows a functional block diagram of the system.

Except for the source transducers, all equipment shown in the figure and listed below in this section is in the DAS room on the mezzanine floor of the EBR-II reactor building (Building 768). The patch panel, in the DAS room, is interfaced between the DAS and the EBR-II instrumentation. Three keyboard displays for use by the reactor operators are in the reactor control room.

Equipment for each group in Fig. 1 is listed in Tables I, II, and III. All equipment listed was furnished by XDS with the exception of the Calcomp

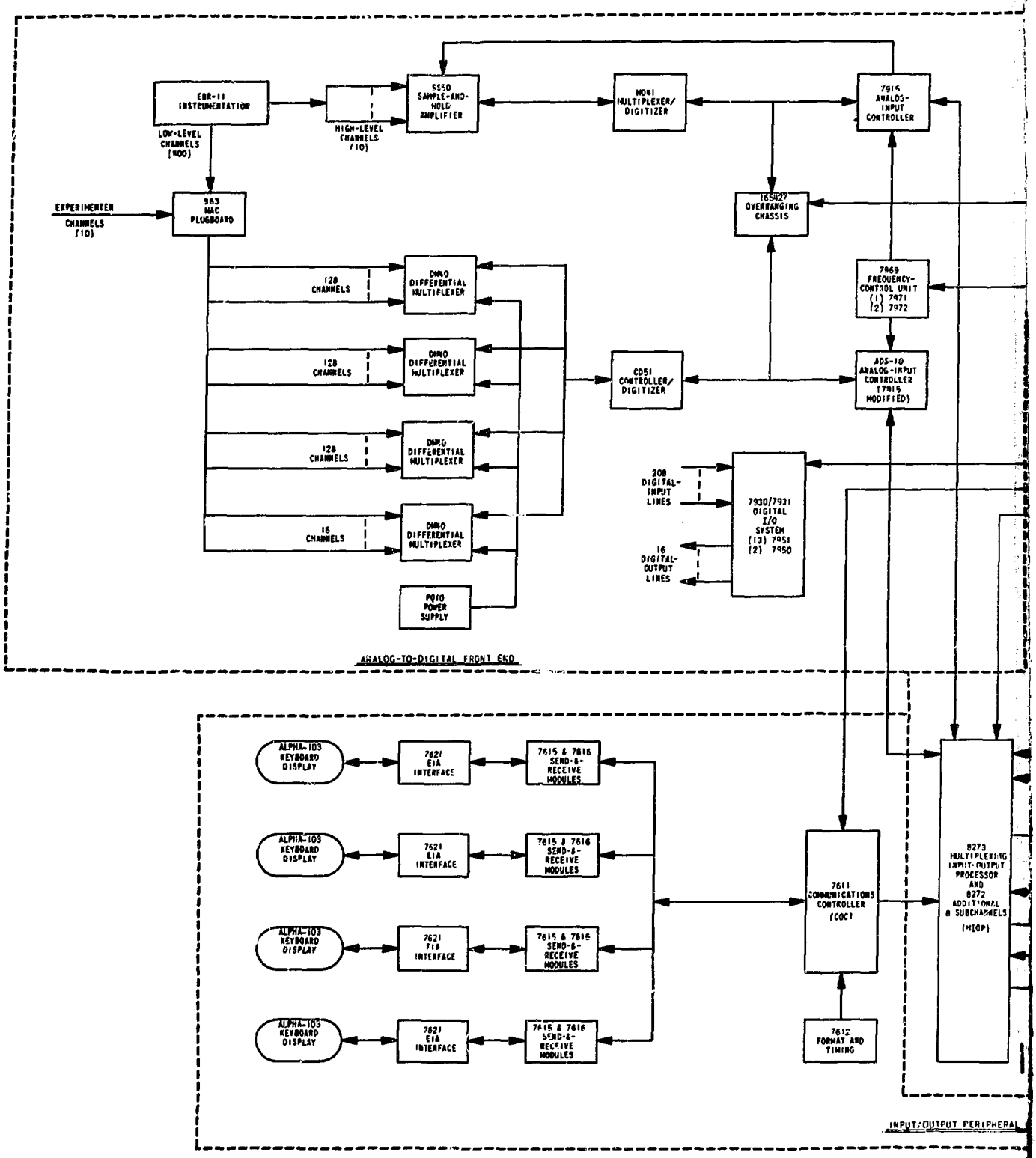

Fig. 1. EBR-II Digital Data Acq

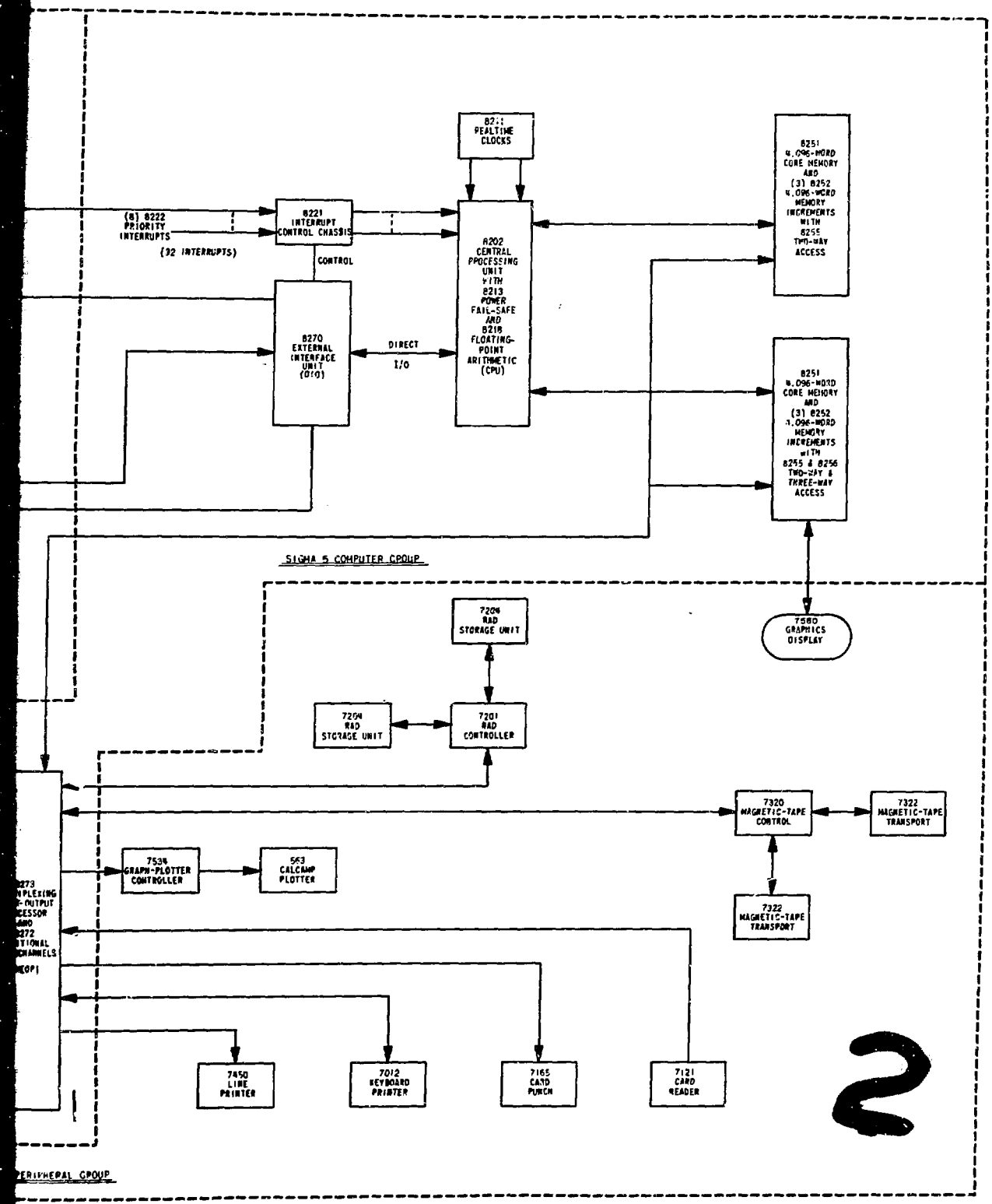
8221
REALTIME CLOCKS
(8) 8222 PRIORITY INTERRUPTS
(32 INTERRUPTS)
8221 INTERRUPT CONTROL CHASSIS
CONTROL
8270 EXTERNAL INTERFACE UNIT (0:0)
DIRECT I/O
8202 CENTRAL PROCESSING UNIT WITH 8213 POWER FAIL-SAFE AND 8218 FLOATING-POINT ARITHMETIC (CPU)
8251 4,096-WORD CORE MEMORY AND (3) 8252 4,096-WORD MEMORY INCREMENTS WITH 8255 TWO-WAY ACCESS
8251 4,096-WORD CORE MEMORY AND (3) 8252 4,096-WORD MEMORY INCREMENTS WITH 8255 & 8256 TWO-WAY & THREE-WAY ACCESS
SIGMA 5 COMPUTER GROUP
7560 GRAPHICS DISPLAY
7204 RAD STORAGE UNIT
7254 RAD STORAGE UNIT
7201 RAD CONTROLLER
7320 MAGNETIC-TAPE CONTROL
7322 MAGNETIC-TAPE TRANSPORT
7322 MAGNETIC-TAPE TRANSPORT
7536 GRAPH-PLOTTER CONTROLLER
563 CALCOMP PLOTTER
7450 LINE PRINTER
7012 KEYBOARD PRINTER
7165 CARD PUNCH
7121 CARD READER
PERIPHERAL GROUP

TABLE I. Equipment List for A/D Front End[1]

Quantity	Equipment	Model Number
1	MAC Plugboard (MAC)	938
4	Differential Multiplexers	DM40
1	Controller/Digitizer	CD51
1	Analog-input Controller	ADS-10
1	Sample-and-Hold Amplifier	SS50
1	Multiplexer/Digitizer	MD41
1	Overranging Chassis	165427
1	Analog-input Controller	7915
1	Basic Frequency Control	7969
1	Basic Program Control	7971
1	Programmable Frequency-source Unit	7972
1	Digital I/O Adapter	7930
1	Digital I/O Expansion Unit	7931
2	Eight Digital Storage I/O Outputs	7950
13	Sixteen Discrete Digital I/O Inputs	7951
1	Power Supply	PQ10

TABLE II. Equipment List for Computer Group[1]

Quantity	Equipment	Model Number
1	Sigma 5 Central Processing Unit (CPU)	8202
2	Realtime Clocks	8211
1	Power Fail-Safe	8213
1	Floating-point Arithmetic	8218
1	Memory Protection	8214
6	4K Memory-expansion Modules	8252
2	Two-way Memory-access Modules	8255
1	Three-way Memory-access Module	8256
1	Multiplexing I/O Processor	8273
1	External Direct Input/Output (DIO) Interface Feature	8270
8	Multiplexing I/O Processor Subchannels	8272
1	Interrupt Controller	8221
8	Priority Interrupts	8222

TABLE III. Equipment List for I/O Peripheral Group[1]

Quantity	Equipment	Model Number
1	Keyboard Printer and Controller	7012
1	Card Reader	7121
1	Card Punch	7165
2	Rapid-access-disk (RAD) Storage Units	7204
1	RAD Controller	7201
1	Magnetic-tape Controller	7320
2	Magnetic-tape Transports	7322
1	Buffered Line Printer	7450
1	Communications Controller	7611
1	Format-and-Timing Module	7612
4	Send Modules	7615
4	Receive Modules	7616
4	EIA Interface Modules	7621
4	Keyboard Displays (BEI)	ALPHA-103
1	Calcomp Plotter (Calcomp)	563
1	Graph-plotter Controller	7534
1	Graphics Display	7580

plotter, furnished by Calcomp, Inc. (CALCOMP); the keyboard displays, furnished by Beehive Electrotech Inc. (BEI); and the plugboard, furnished by MAC Panel, Inc (MAC). The signal inputs taken from the EBR-II instruments are classified in Table IV. The experimenter channels can have the input range of the low-level analog signals.

The 400 low-level analog channels and the 10 experimenter channels are connected to the plugboard from the cable-routing room. These channels are then jumpered, in the DAS room, from the upper half of the plugboard to the lower half. The analog signals from the plugboard as well as the high-level analog signals are routed to their respective multiplexers. After being multiplexed and digitized, the data are stored or processed in the computer and/or becomes output on the desired I/O equipment. The digital signals are put directly into the computer. Sixteen digital lines are available for output, and 208 for input.

II. DETAILED DESCRIPTION OF SYSTEM

The discussions in this section provide a brief insight into the functional operation of the various components of the DAS. Those functional units, such as interface units, which are integral parts of other units are not discussed. For example, the external interface unit (Model 8270) is not discussed because it is an integral part of the CPU and serves only as an interface between the digital I/O system and the CPU.

A. Analog-to-Digital (A/D) Front End

The A/D front end receives the high-level and low-level analog signals, multiplexes them, and digitizes them into digital format.

1. MAC Plugboard

The plugboard is in the wall between the cable-routing room and the DAS room. The 400 low-level channels and the 10 experimenter channels are taken from the cable-routing room and terminated in the upper half of the plugboard.

TABLE IV. Signal Classification

Type of Signal	Gain	Input Range
Digital	1	±0.5 V = false; ±3 V = true
High-level Analog	1	±10 V
Low-level Analog	1	±10 V
Low-level Analog	2	±5 V
Low-level Analog	4	±2.5 V
Low-level Analog	8	±1.25 V
Low-level Analog	16	±625.0 mV
Low-level Analog	32	±312.5 mV
Low-level Analog	64	±156.3 mV
Low-level Analog	128	±78.13 mV
Low-level Analog	256	±39.06 mV
Low-level Analog	512	±19.53 mV
Low-level Analog	1024	±9.77 mV
Low-level Analog	2048	±4.88 mV
Low-level Analog	4096	±2.44 mV

The upper half of the plugboard can accommodate up to 800 channels. These channels are jumpered to the lower half of the board with jumper cables. This method allows a great degree of flexibility in input to the computer. The lower half of the plugboard is connected directly to the low-level differential multiplexers (DM40).

2. Differential Multiplexer

Four DM40's comprise the low-level front end for the DAS. It is through these four units that the low-level analog plant parameters are put into the computer. Three of them accommodate 128 channels, and the fourth accommodates 16. A simplified block diagram of a DM40 is shown in Fig. 2.

The DM40's accept the input of the 400 analog channels from the plugboard. The circuits supply the necessary multiplexers, guard amplifiers, and, if desirable, passive data filtering. The multiplexed data are then fed into a programmable-gain differential amplifier whose output is multiplexed on a DM40 level (i.e., with other DM40's). The output of the DM40, still in analog form (and at $\pm$ 10V), is fed to the controller/digitizer (Model CD51).

Each channel input is fed through a pair of shielded input lines: a positive line, a negative line, and a shield. Field-effect transistor (FET) switches with very high impedance (>50 MΩ) and unity gain are connected to each side of the input lines.

The DM40 is isolated by floating the ground (i.e., the system is connected to ground at the transducer and in the CD51 controller/digitizer). As can be seen in Fig. 2, guard amplifiers are provided to drive the shield on both the backplane and switch modules. These amplifiers, by reducing the capacity to ground, minimize dielectric-absorption loss and maintain a high signal-to-noise ratio.

Multiplexing is accomplished by selecting FET switches with seven address bits. The data are stored and decoded by the address/store/decode logic, as shown in Fig. 2.

The differential amplifiers have programmable gains of X1, X8, X64, and X512, which are selected by two gain bits via the software. By combining these gains with the gains of the CD51, the gains and signal-input ranges listed in Table IV can be selected.

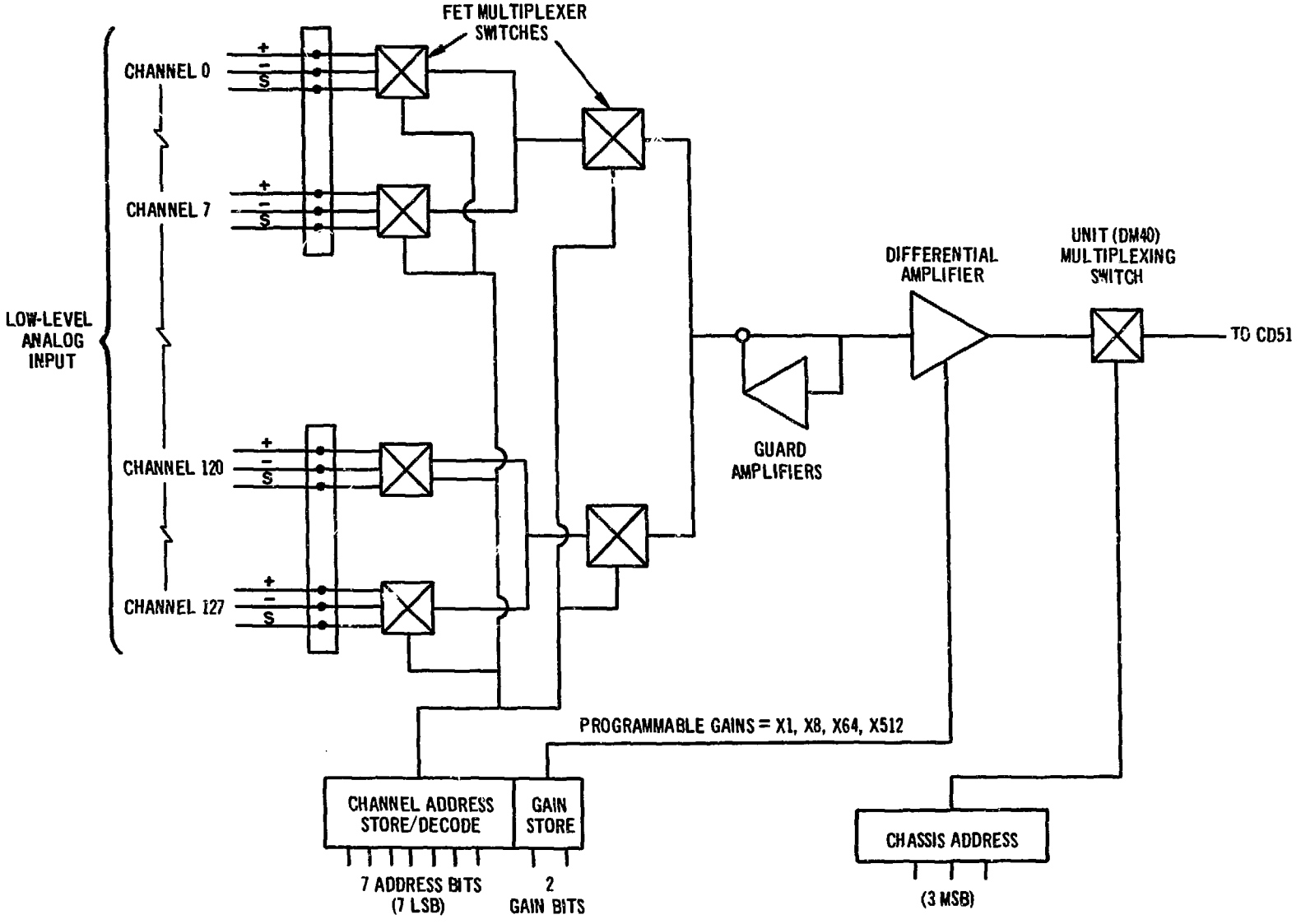

Fig. 2. Differential Multiplexer (Model DM40)

Input over-voltage protection for the FET switches is provided both by 1/8-A fuses and by diode clamping at ±12 V.

The maximum multiplexer speed, or sample rate, is 10,000 samples/sec in the sequential mode or 8500 samples/sec in the random mode. (Modes of operation will be explained later.)

3. Controller/Digitizer

The multiplexed ±10-V analog output signal from the DM40 is put into the controller/digitizer (Model CD51), where it is digitized into a 15-bit digital output. Besides digitizing, the CD51 also supplies control for the DM40 by providing a 10-bit channel address and two-bit gain control.

Digital output is sent to the analog-input controller (Model ADS-10), which also provides digital control signals to the CD51. A basic block diagram of the CD51 is shown in Fig. 3.

Briefly, the CD51 functions as follows: The sample amplifier continuously samples and tracks the ±10-V output of the DM40. With the isolation switch closed, the hold amplifier retains the tracking-voltage level on a capacitor. Acquisition time is 95 μsec. When the command is received to convert from analog to digital, the isolation switch opens and the A/D converter converts the voltage on the capacitor into a 15-bit digital format. Conversion time is 5 μsec. The sample-and-hold amplifiers have program-controlled gains of X1, X2, X4, and X8. Two gain bits are used for gain control.

The A/D converter uses the method of successive approximations to convert the analog data to the 15-bit digital format. Fourteen bits are used to provide the digital value, and one bit is used for a parity sign. Negative numbers are represented in two's complement form. The conversion coefficient is 10 V per 16,384 binary digits.

In the automatic mode, the address-and-gain logic receives digital control data from the ADS-10 and its control panel in the manual mode. Address-and-gain control bits are passed on to the DM40's. Internal gain control is provided to the CD51 by the ADS-10.

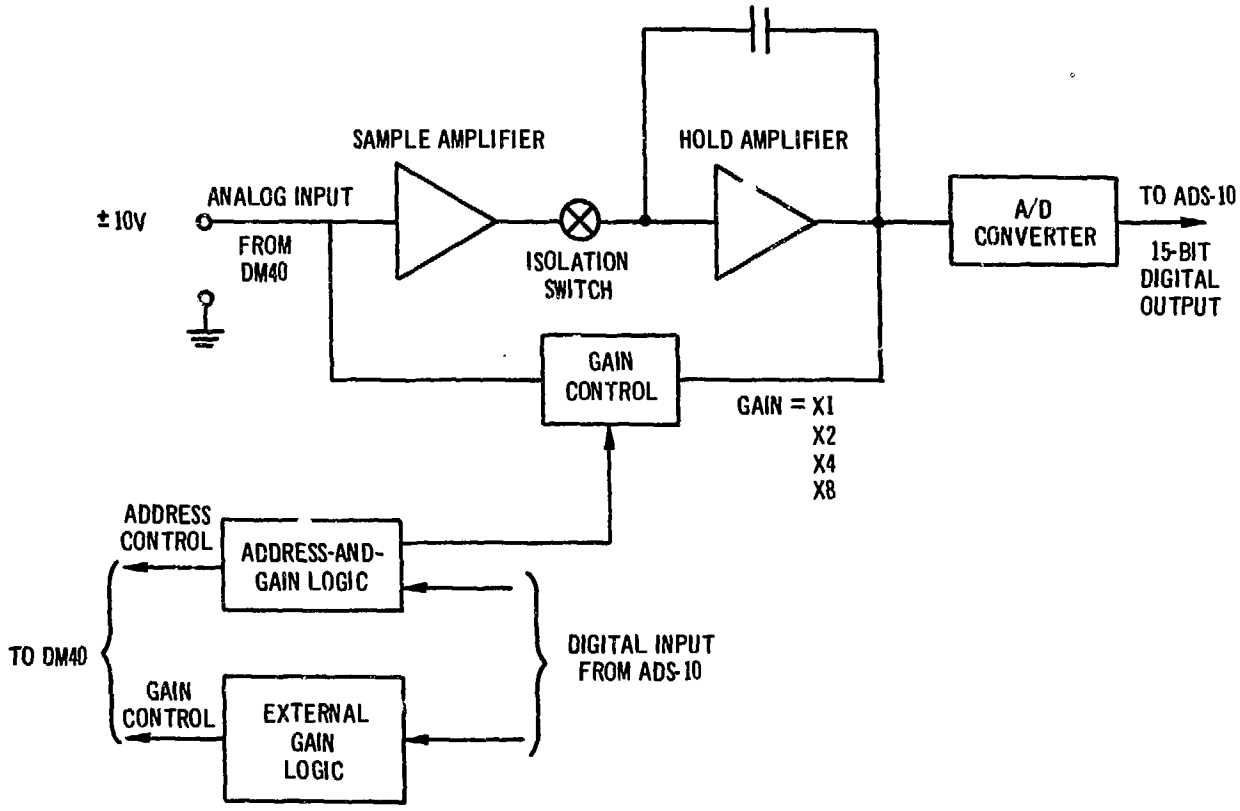

Fig. 3. Controller/Digitizer (Model CD51)

4. Simultaneous Sample and Hold

Up to this point, no discussion has been made of the 10 high-level (±10-V) channels. These channels are routed from the plant transducers to the cable-routing room and then directly to the sample-and-hold amplifier (Model SS50). They do not pass through the plugboard as did the low-level channels. The SS50 operates very similarly to the sample-and-hold amplifiers in the CD51 with two major exceptions: the SS50 can sample and hold all 10 channels simultaneously or hold a single channel or several channels in a sequential or random address pattern controlled by the software. Also, the SS50 does not process a programmable gain option. The gain is normally set at unity, but physical changing of resistors will provide additional gains of 0.1 and 10. The inputs corresponding to the three gains are ±0.10, ±10, and ±100 V.

The block diagram of the SS50 is shown in Fig. 4. Ten sample-and-hold amplifiers are provided, one for each high-level channel. The mode of operation (i.e., "simultaneous," etc.) is controlled by OR gates decoded from the software instructions. The analog output of the SS50 is sent to the multiplexer/digitizer (Model MD41) for processing.

5. Multiplexer/Digitizer

The MD41 is very similar to the CD51 controller/digitizer, the major differences being that the MD41 multiplexes and has no gain control. The MD41 has an acquisition time of 5 μsec and a conversion time of 25 μsec.

6. Overranging Chassis

The capability for interrupts when an overrange is detected is provided at the output of the CD51 for the low-level channels and at the output of the MD41 for the high-level channels. Overrange is defined as an input signal >±10 V for a digital value of 011111111111111 with a positive signal and for a digital value of 100000000000000 with a negative signal. An overrange from the CD51 will trigger the external interrupt X'66, whereas an overrange from the MD51 will trigger the external interrupt X'67.

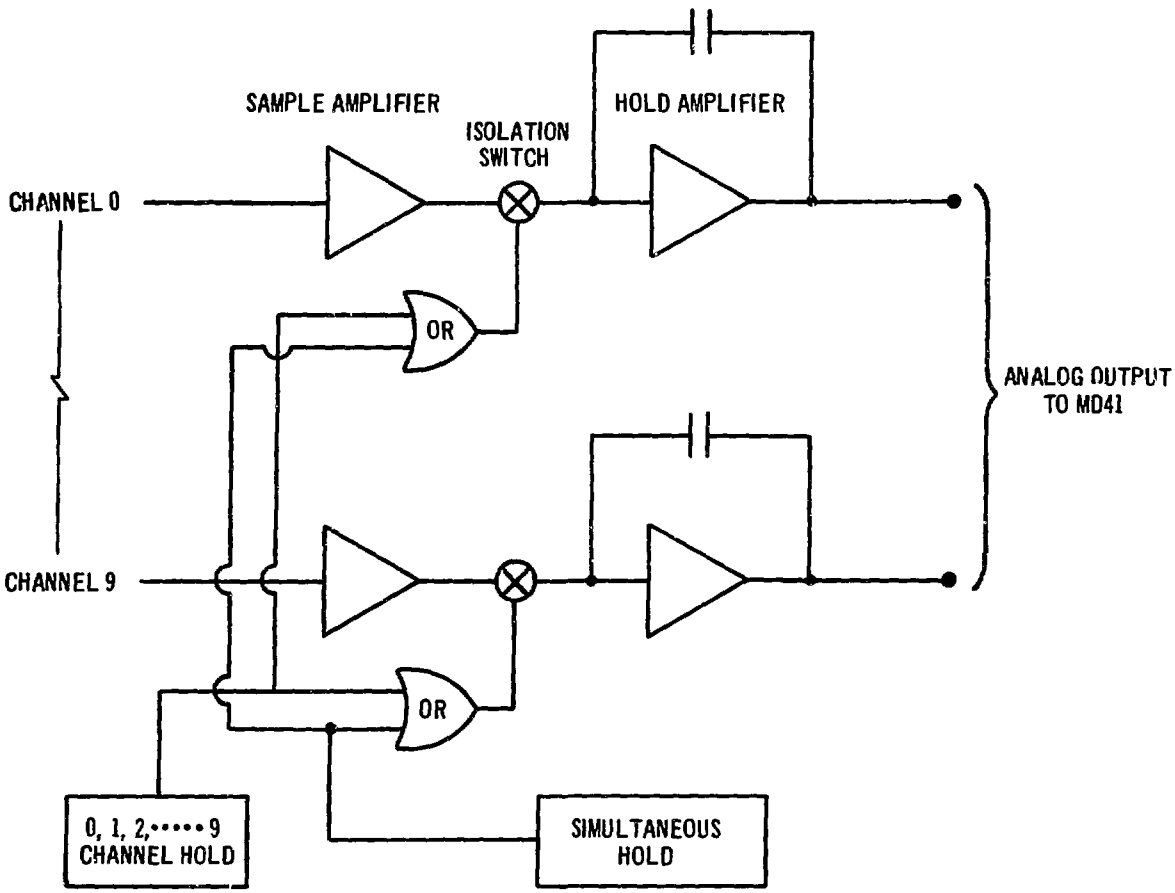

Fig. 4. Simultaneous Sample-and-Hold Amplifier (Model SS50)

7. Analog-input Controllers

Two analog-input controllers, one for each A/D converter, are incorporated into the DAS: the Model 7915, which controls the MD41 and high-level channels; and the Model ADS-10, which controls the CD51 and low-level channels. The ADS-10 is a modified 7915.

Basically, both the 7915 and the ADS-10 provide control and data paths for the multiplexers and A/D converters by communicating between the multiplexing input/output processor (MIOP) and the digitizers. Neither model requires control by the central processing unit (CPU) once CPU initiation has been started.

Each model has two basic modes of operation: random and sequential. In either of these modes, the controller can either be in the ready state, order in/out state, or data in/out state. In the random mode, the 7915 (or the ADS-10) receives addresses for each two bytes to be obtained from the MD41 (or the CD51) and stored in memory. In the sequential mode, each digitized result (2 bytes) is successively stored in higher positions in core without receiving new address instructions from the computer.

The basic difference between the Model 7915 and the Model ADS-10 is that the ADS-10 has had circuit modifications to enable it to address up to 1024 channels instead of 256 channels, the standard capability of the 7915. Because of these modifications, some of the seven combination operational modes of the 7915 could not be incorporated into the ADS-10 (see Table V).

Each model receives frequency and clock control from the frequency-control unit. Communications and data to and from the controllers are shown in Fig. 5. Each controller contains digital storage for A/D output and control logic for multiplexers, channels, and analog control such as control for the sample-and-hold amplifiers. As stated before, the ADS-10 has control logic and storage for 1024 channels, whereas the 7915 has logic and storage for 256 channels.

8. Frequency-control Unit

The frequency-control subsystem consists of the following three subunits:

TABLE V. Operational Modes of Model 7915 and Model ADS-10 Analog-input Controllers

Mode No.	Mode Description	Model 7915	Model ADS-10
1	Random, internally clocked, maximum rate	X	X
2	Random, externally clocked, 1 sample/clock	X	X
3	Random, externally clocked, burst mode on	X	
4	Sequential, internally clocked, maximum rate	X	X
5	Sequential, externally clocked, 1 sample/clock, same channel	X	
6	Sequential, externally clocked, 1 sample/clock, sequential channel	X	X
7	Sequential, externally clocked, burst sequential clock	X	

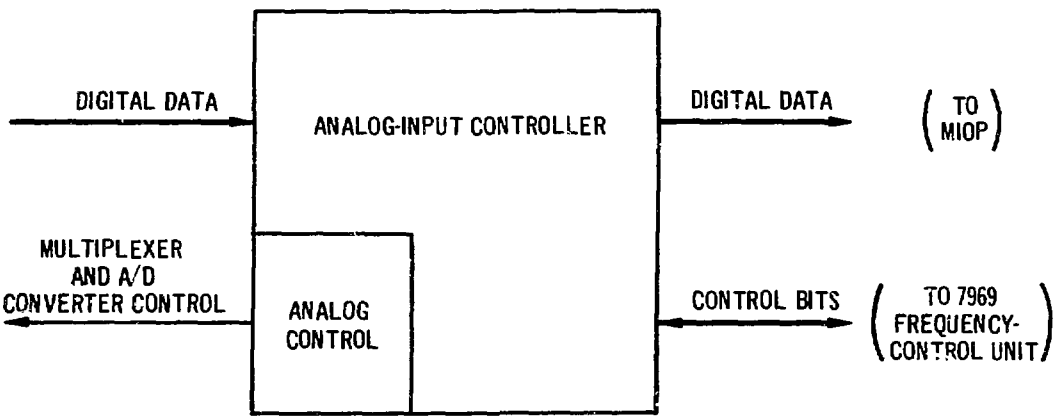

Fig. 5. Block Diagram of Analog-input Controller (Models 7915 and ADS-10)

a. Basic frequency unit (Model 7969)

b. Basic program-control unit (Model 7971)

c. Programmable frequency-source unit (Model 7972)

The primary purpose of the frequency-control subsystem is to furnish the front end with frequency control and clocking signals, such as sampling-rate control for the multiplexers. The subsystem is shown in Fig. 6.

The basic unit of the subsystem is the 7969, which contains the basic clock--a 1.6-MHz, crystal-controlled oscillator--and a frequency divider that provides master frequencies of f/2, f/4, f/8, f/16 f/32, f/64, and f/128 (where f is the basic frequency). These frequencies are selected by switches in the unit. The 7969 provides its clock pulses to the 7972, discussed below.

The basic program-control unit (7971) serves as an interface between the frequency-control subsystem and the direct input/output (DIO) interface. It also decodes the write-direct (WD) instructions. Its DIO response logic receives the address of the function strobe signal from the DIO and, after it has recognized the address, acknowledges the receipt to the CPU via the DIO. The decode logic of the 7971 decodes the WD statements in the software and sets the comparison register in the 7972.

The programmable frequency-source unit (7972) contains a 12-bit counter register and a comparator. The master frequency from the 7969 operates the counter in a free-running mode. The contents of the counter register are continuously compared with the contents of the comparison register, which has been set by the 7971. When the two registers are equal, the comparator resets the counter and enables a clock-pulse generator, which is the clock that is routed to the front end for control purposes. Clock-pulse frequency is 100 Hz to 25 kHz.

9. Digital Input/Output System

The digital input/output (I/O) system provides direct digital input and output to be used with the DAS. Digital input could be in the form of binary output from relays. Digital output could be provided to a digital-to-analog converter for control functions.

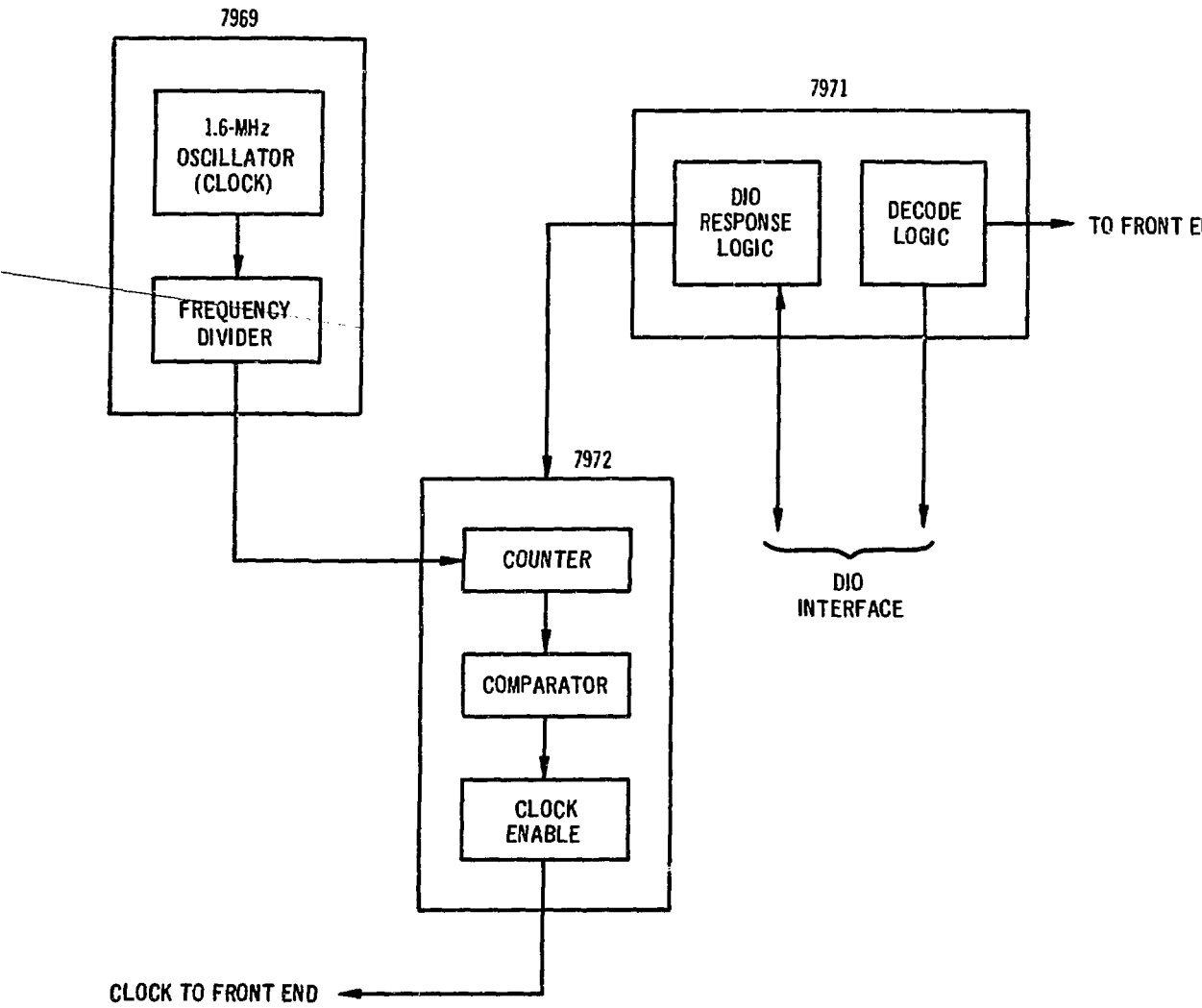

Fig. 6. Block Diagram of Frequency-control Subsystem

The system is made up of an I/O adapter (Model 7930), an I/O expander (Model 7931), two digital storage I/O units (Model 7950), and 13 digital-input units (Model 7951).

The I/O adapter (7930) is the basic unit of the system. It performs the following functions: (1) decodes addresses, (2) receives and sends data, and (3) responds to service requests from the CPU via the external DIO interface unit (Model 8270).

The digital I/O expander (7931) provides control capability by allowing an additional 16 positions of control to be incorporated into the 7930.

The total digital I/O system is capable of receiving signals from 208 digital-input lines from the external equipment. This input is brought in through the 13 digital-input units (7951), each of which is capabl of accepting 16 bits of digital input data. The total system is capable of providing 16 bits of digital output to external equipment. This output is provided by the two stored digital I/O units (7950), each of which is capable of storing eight bits of digital data.

Each channel or bit location is identical and responds to its own address. Unlike the digitized analog data, the direct digital data does not interface with the MIOP.

B. Sigma 5 Computer Group

The computer group consists of the equipment listed in Table II. The primary component of the group is the XDS Sigma 5 computer.

1. Sigma 5 CPU

The central processing unit (CPU) is the basic unit of the Sigma 5 computer. It controls program execution, performs arithmetic and logic functions, addresses core and private memory, retrieves and stores instructions and data, controls insertion and data flow between the core memory and other units of the system, and provides CPU timing. The various functions performed by the CPU are illustrated in Fig. 7.

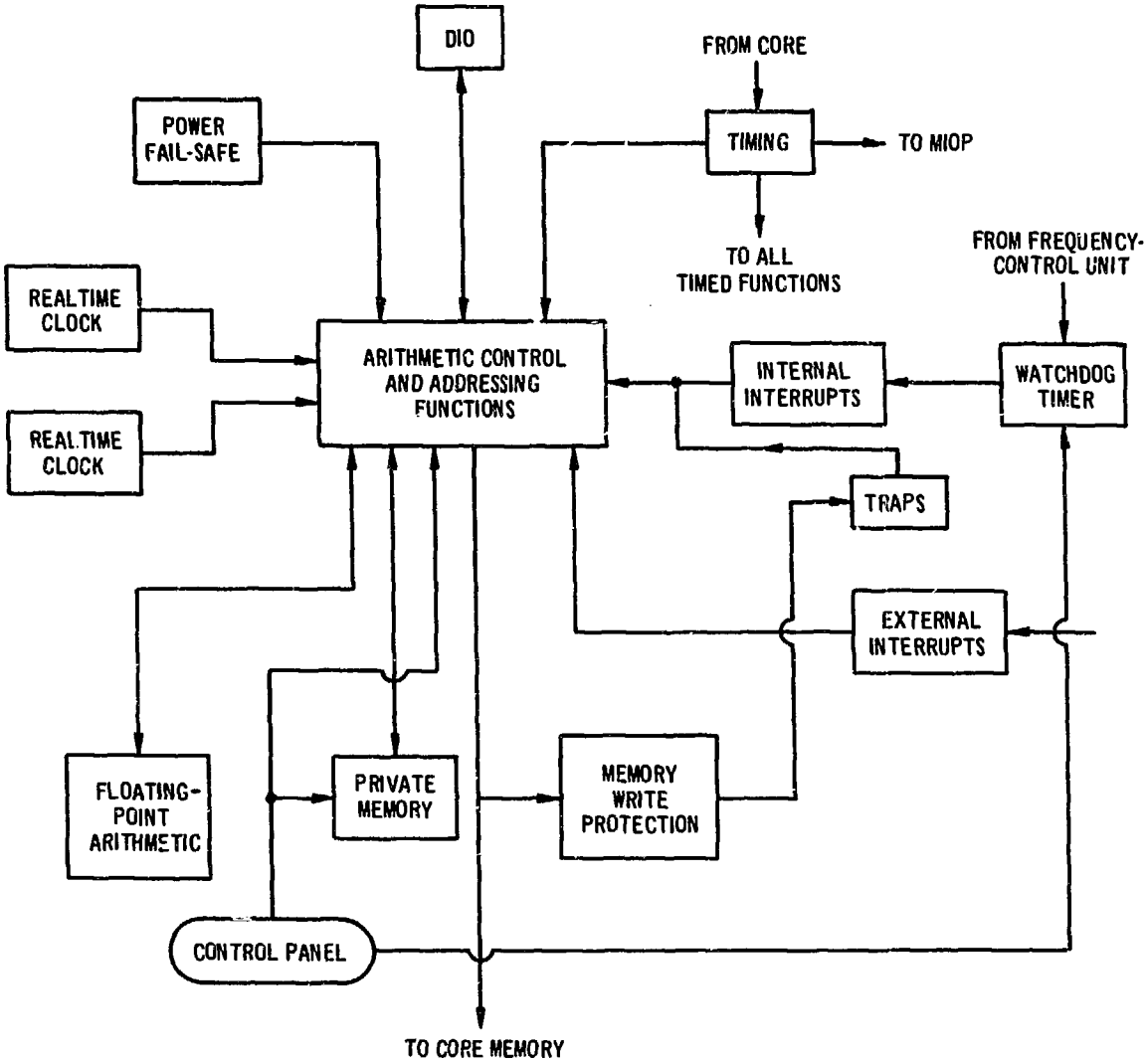

Fig. 7. Block Diagram of Central Processing Unit (CPU)

a. CPU Timing

CPU timing consists of: (1) internal timing provided by the CPU-clock generator and the oscillator clock generator, and (2) real-time clocking provided by two realtime clocks (Model 8211).

(i) Clock Generators. The CPU clock generator consists of three tapped delay lines. It provides both alternating-current (ac) and direct-current (dc) clocks for many different functions both internal and external to the CPU. For example, ac clocks are provided for triggering ac flipflops in the CPU and the floating-point arithmetic unit. Clocks are provided for preparation and execution of instructions at all times when operating in control-panel mode, interrupt/trap mode, and I/O mode.

The oscillator clock generator provides both a 1-MHz and a 16-kHz clock. The 1-MHz clock steps the watchdog timer (discussed in Sect. b, below), supplies the MIOP a signal for routing to device controllers, and is a source for interrupt gate clocks and other functions.

The 16-kHz clock is used in connection with interrupts of the realtime counter, which supplies the time-base selector.

(ii) Realtime Clocks. The two realtime clocks are basically a fixed-interrupt routine preset to trigger at a frequency specified by the time-base selector. Five different frequencies are available from the time-base selector: 8 kHz, 4kHz, 2kHz, 500 Hz, and 60 Hz. External control frequencies also may be used.

Realtime clocks are used for control operations, such as sampling-rate control.

b. Watchdog Timer

The watchdog timer monitors the program execution and provides a trap if the program does not periodically reach interruptable points in the program. It allows 42 msec between points; if this time limit is exceeded, a trap is initiated.

c. Interrupt and Trap Functions

The interrupt and trap functions cause the normal program execution to be interrupted. The difference between the interrupt and the trap is in the way they interrupt the program sequence. The interrupt allows the current instruction to be completed before interrupting. It also provides for returning to the point of the interrupt and continuing program execution. A trap will cause an immediate interruption of the program and the execution of a specified instruction. A trap is usually cause by an error in execution or in the software. Interrupts are usually controlled by clock or software and are assigned priorities. There are 13 internal interrupts and 32 external interrupts associated with the DAS.

d. Power Fail-Safe

The power fail-safe (Model 8213) option prevents loss of volatile (destroyable) information when power fails. The option consists of a power monitor and two interrupts: power-on and power-off. These two interrupts are assigned the highest priorities.

The power monitor initiates a power-off request when power decreases below a preset value. The power-off request activates the power-off interrupt. The CPU then has approximately 5 msec to finish the current instruction, store all volatile information in nonvolatile core locations, and then shut down the computer.

e. Floating-point Arithmetic

This unit (Model 8218) allows use of floating-point arithmetic on the Sigma 5. It is controlled by CPU clocks.

f. Private Memory

"Private memory," or "fast memory," consists of 32 registers in the CPU that are called "private" because only the CPU may gain access to them.

g. Memory Protection

Memory protection (Model 8214) allows program-controlled access to memory on a 512-word-block basis. It compares a two-bit write-lock code with a two-bit write-key code. The write key is contained in bits 34 and 35 of the program-status doubleword. Write-lock codes are contained in write-lock registers in memory.

2. Core Memory

The DAS core memory consists of two basic 4K memory modules (Model 8251), six 4K memory-expansion modules (Model 8252), two two-way memory-access modules (Model 8255), and one three-way memory-access module (Model 8256)--for a total memory of 32K. Half the memory (bank No. 1) has two-way access so the CPU and MIOP can both access memory. The other half (bank No. 2) has three-way access so the CPU, MIOP, and graphics unit can access memory. The graphics unit accesses bank No. 2 only. The priority of access is: (1) MIOP, (2) CPU, (3) graphics unit.

The core memory contains decoding for logic, ferrite magnetic cores for data storage, and various sensing and switching amplifiers for reading data into and out of the core.

The method of "interleaving" is used in the core to reduce the average access time for the memory. Interleaving is the practice of alternating addresses to different memory banks. This practice allows the next access to start before the previous access is completed. With interleaving, the memory cycle (a read and a write) is 635 nsec; without interleaving, the memory cycle is 635 nsec. Interleaving control is provided via the CPU control panel. Interleaving can not be used when using the graphics unit.

The memory has three modes of operation: (1) read-restore, (2) full-clear write, and (3) partial-clear write. A memory cycle in each mode consists of a read and write.

In the read-restore mode, the data are first loaded into a data register and then provided to the requestor. These same data are then restored in the original core location. In the full-clear write mode, the new data are loaded into a data register and then written into core as the restore portion of the read-restore mode discussed above. In the partial-clear write mode, one, two, or three bytes from the core are loaded into the

data register. The remaining byte or bytes are not used, but are replaced by a new byte or bytes from some external source. The total word (four bytes) is then rewritten into core.

During any mode of operation, odd parity is checked when data are read out of core and loaded into a data register. A parity error will cause a trap unless the override on the control panel is on.

3. Multiplexing Input/Output Processor (MIOP)

The MIOP (Model 8273) serves as the link between the core memory and the device controllers (DC's) that control the peripheral I/O equipment. By freeing the CPU from I/O tasks, the MIOP allows it to concentrate on program execution. Multiplexing is done on a device-controller (DC) level. This means that the two tape transports are not multiplexed individually; instead, the tape controller is multiplexed with the rapid-access-disk (RAD) controller and other peripheral devices. Various functions of the MIOP are shown schematically in Fig. 8.

Communication between the MIOP and CPU is accomplished on an IOP address line, three function-code lines that stipulate the operation to be performed (i.e., SIO, HIO, TIO, TDV, and AIO)*, and two condition-code lines that indicate to the CPU whether or not instructions have been recognized.

The MIOP responds to service requests from the CPU or the device controllers. In response to service requests from the device controllers, the MIOP performs the following service cycles:

a. data out
b. data in
c. order out
d. order in

C. Input/Output (I/O) Peripheral Group

The I/O group consists of the equipment listed in Table III. This group of equipment enters information into and obtains information from the computer. Information can be entered into the computer either by magnetic tape, punched cards, keyboard input, or the light gun on the graphics unit.

*See List of Symbols Used for definitions.

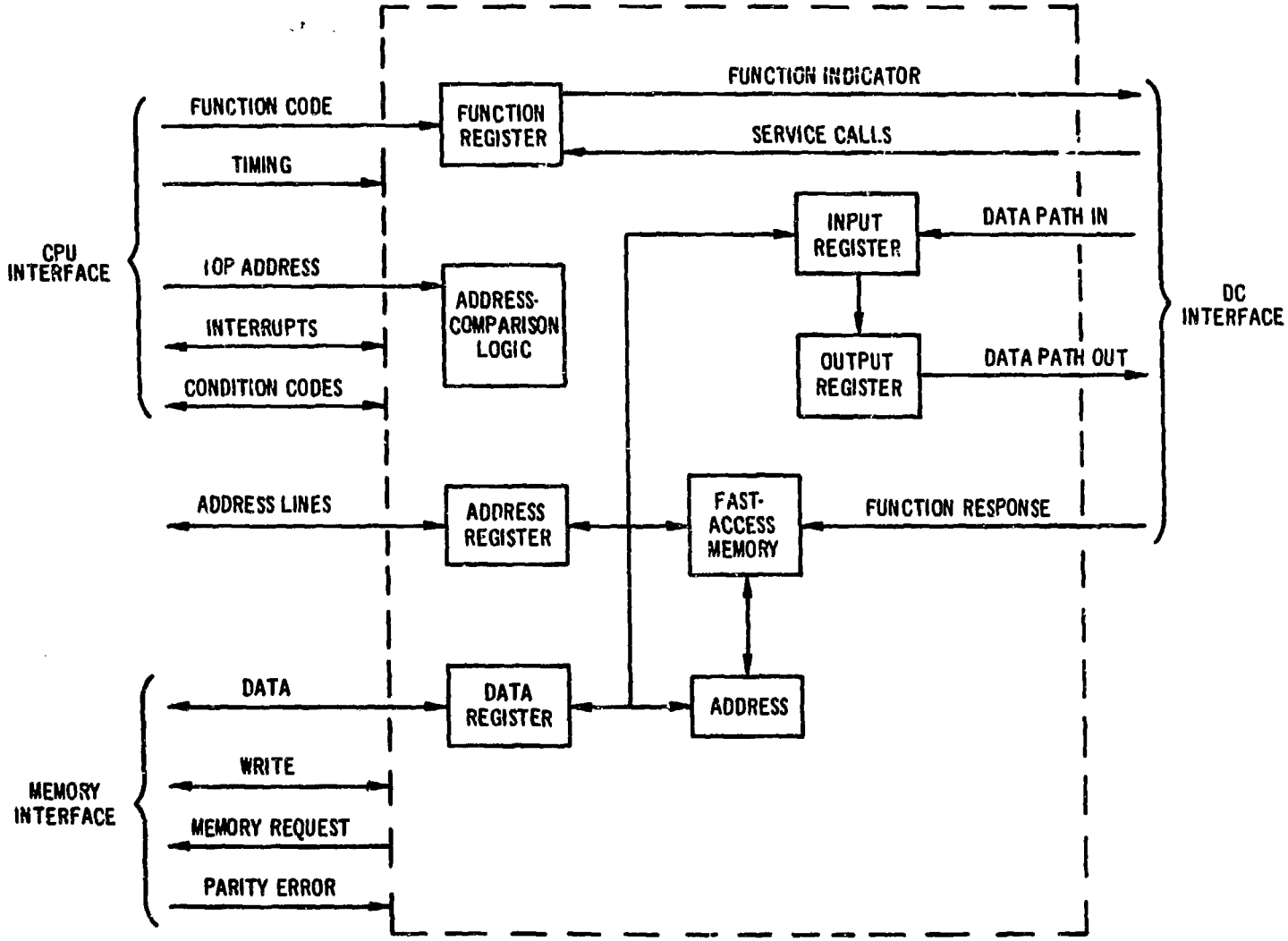

Fig. 8. Functions of Multiplexing Input/Output Processor

Information from the computer is printed on paper, punched into cards, or electronically displayed.

1. Keyboard Printer and Controller

The keyboard printer and controller (Model 7012) provides a means of direct communication between the operator/programmer and the computer via the MIOP. Operational messages, diagnostics, and other information is received and transmitted to and from the computer at a maximum rate of 10 characters/sec, using 62 alpha-numeric characters and symbols. As characters are put into the computer, one character at a time, they are also printed out on paper.

A device controller (DC) provides an interface between the MIOP and the keyboard printer. It receives and decodes addresses and instructions from the MIOP and transmits them to the keyboard printer.

2. Card Reader

The card reader (Model 7121) puts information into the computer via punched cards. It is capable of reading cards at a maximum rate of 200 cards/min in either binary or EBCDIC format. Automatic read-mode switching from binary to EBCDIC is possible; hence, reading of mixed decks is feasible. Cards are read in EBCDIC unless rows 1 and 2 in column 1 are punched. A photoelectric reader senses each 12-bit column and transfers the data to the MIOP as a series of bytes.

3. Card Punch

The card punch (Model 7165) provides punched-card output at a rate of 100 cards/min on standard 80-column cards in either binary or EBCDIC format. Punch-error detection is provided during stacking of punched cards. An error card is stacked higher than the normal cards, thereby providing easy identification of errors. Both the hopper and the stacker have 1000-card capacity. A device controller is provided as an interface between the punch and MIOP.

4. Rapid-access Disk (RAD) and Controller

Basically, the RAD provides the Sigma 5 with a large, high-speed disk storage. By storing all monitor, processor, and user program data, the RAD minimizes the amount of storage in the core. Data can be stored permanently or temporarily on the RAD. The system, as installed at EBR-II, has one controller and two storage units. Each RAD can be stored or retrieved by use of its unit address.

Each RAD storage unit (Model 7204) contains two disks rotating at 1774 rpm. Each side of a disk is used for data storage; hence, four surfaces are available for storage. Since each surface accommodates 128 tracks, each RAD storage unit contains 512 tracks of storage. Each track has its own floating read/write head; this arrangement reduces the access time to an average of 17 msec. Each storage unit has a three-megabyte capacity; thus, total capacity is six megabytes.

Write protection is available by use of 16 toggle switches, each inhibiting 32 tracks. The selection unit performs the signal conversion required to write on and read from the disk.

The RAD controller (Model 7201) selects the RAD storage unit dictated by the unit address. It interfaces with the MIOP, as do the other DC's. It stores data going from and coming into a 16-byte fast-access memory and then, upon command, sends it to the disk or to the MIOP.

5. Magnetic-tape Transport and Controller

The magnetic-tape system includes a controller (Model 7320) and two tape-transport units (Model 7322). Control of the tape system is similar to that of the RAD. The system reads and writes information on magnetic tape while interfaced with the MIOP. The tape system can write forward, read forward or reverse, space over records or files, erase, and rewind online or offline.

The information is stored in bytes on nine parallel tracks compatible with IBM-2400 format. Eight tracks are for data, and one is for parity information. The recording density is 800 bits/in. per track. Information can be transferred at 60,000 bytes/sec at 75 in./sec. Rewind is accomplished at 250 in./sec.

Write protection, provided to prevent accidental erasure or writing over of previously recorded tape, is accomplished by a plastic ring that must be attached to the tape reel in order to write. The ring fits in a groove that pushes a microswitch.

During the write mode, data are read back and checked. This, referred to as a "read-after-write check," guarantees the validity of the recorded data.

The device controller, as in the other systems, controls data flow to and from the MIOP and controls tape motion by directing orders to the selected tape transport. The tape transports are selected by referring to their hexa-decimal unit address.

6. Buffered Line Printer

The buffered line printer (Model 7450) is basically made up of a line printer and a controller. Unlike the RAD controller, the 7450 controller is capable of controlling only one device. The line printer can print up to 128 columns, using a set of 64 alpha-numeric characters and symbols. Printing rates are: 225 lines/min, using all 64 characters; 300 lines/min, using the first 50 characters; and 450 lines/min, using the first 44 characters. The MIOP communicates with the printer by using the standard eight-bit data word, but the printer acknowledges only the six least significant bits (LSB's) of the word. A half-line buffer is fed data one bit at a time for either even or odd columns. The program terminates a line in the twice for each line of print, once for even and once for odd columns. The capacity of the buffer is 128 characters.

7. Character-oriented Communications (COC) Link

The COC link is primarily responsible for controlling communication between the computer and keyboard display units. The total system is comprised of the following units:

a. One COC Controller (Model 7611)
b. One Format-and-Timing Module (Model 7612)
c. Four Formatted Send Modules (Model 7615)
d. Four Formatted Receive Modules (Model 7616)
e. Four EIA* Interface Modules (Model 7621)

*Electronics Industries Association.

Data transmission between the computer and keyboard displays is asynchronous in the sense that the operating speed is not related to the frequencies of the systems to which the keyboard displays are connected. Therefore, operation is independent of realtime requirements.

The COC link is capable of three modes of operation. In the full duplex mode, simultaneous sending and receiving is possible. In the half duplex mode, both sending and receiving are possible, but not simultaneously. In the simplex mode, either sending or receiving is possible, but not both.

The system is basically arranged as shown in Fig. 9. The basic unit is the COC controller (Model 7611). It is the central source of control for the COC link and is connected to both the DIO interface and the MIOP. All input data are transmitted from the CPU, through the DIO interface, and to the COC. All output data are transmitted from the COC, to the MIOP, and then to the core. Data and control information both take the above paths.

Data to and from the keyboard displays are received by the send and receive modules (Models 7615 and 7616) via the EIA interface module (Model 7621). The send module accepts the output data from the controller one byte at a time, serializes it, and transmits it, along with start and stop bits, to the keyboard display. The receive module performs the opposite function of the send module As its name implies, the timing module (Model 7612) provides bit timing for all send and receive modules and the controller. One send module, one receive module, and one EIA interface are required for each keyboard display.

8. BEI Keyboard Display

The DAS contains four alpha-numeric keyboard displays (Model ALPHA-103), three of which are to be used in the reactor control room for reactor operations support, and one of which is to be used for operator/programmer support.

The keyboard displays are interfaced with the COC as shown in Fig. 1. They use a 53-character keyboard. The alpha-numeric characters are displayed on an 11-in. (diagonal) television screen capable of accommodating 20 lines of display at 40 characters/line. As with the COC, the BEI's are capable of full duplex, half duplex, and simplex modes of operation; the

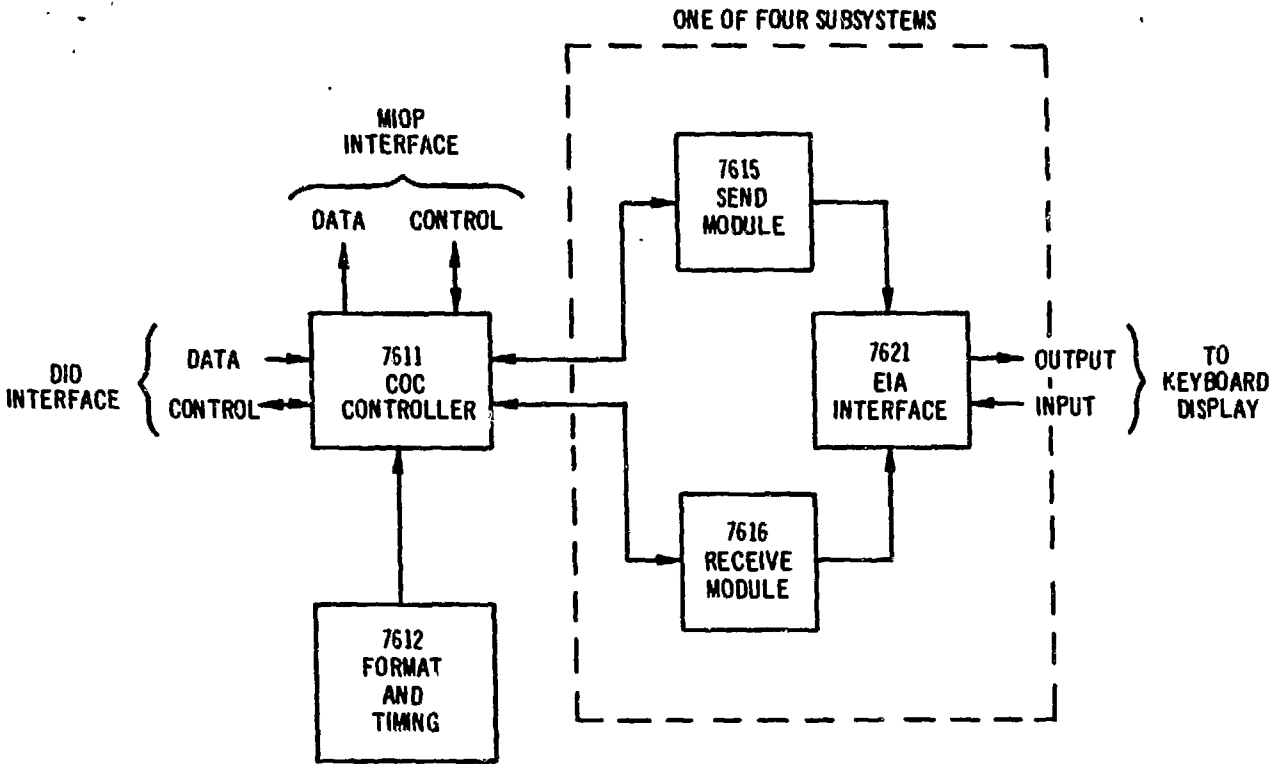

Fig. 9. Block Diagram of COC Link

standard mode is full duplex. Editing and erasing capabilities are provided.

9. Calcomp Plotter and Controller

A Calcomp plotter (Model 563) provides graphic display of data. A device controller (Model 7534) receives data from the MIOP, decodes it, and transmits it to the Calcomp plotter.

10. Graphics Display

The graphics display (Model 7580) allows dynamic display of data on a 21-in. cathode-ray-tube screen, in the form of points, lines, and vectors. Information can be fed back to the computer via an alpha-numeric keyboard consisting of 64 characters and a light gun that senses points of light on the tube screen. It should be noted that the 7580 does not interface with the MIOP as did all other I/O devices. The 7580 interfaces with the second bank of memory through a three-way access module (Model 8256).

The graphics display consists of a display console and primary controller (PC). The PC communicates directly with the memory for instruction, interprets the instruction, and generates codes for drawing the displays on the 21-in. cathode-ray-tube screen. Interrupts may be generated via four interrupt keys on the display console.

The light gun consists of a photomultiplier tube and associated control electronics that respond to light on the cathode-ray-tube screen within a small aiming circle of red light provided by the gun. The defined aiming ring allows the operator to feed back positional data to the CPU. Specific data may be identified by pointing the light gun.

Since the PC is directly connected to the memory, data stored in the memory automatically refreshes the display without CPU intervention.

The memory must not be operated in interleave during use of the graphics display.

REFERENCE

1. Data Acquisition System Technical Manual, XDS980380A, Xerox Data Systems (August 1970).