A Low-Power Wave Union TDC Implemented in FPGA

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ABSTRACT: A low-power time-to-digital convertor (TDC) for an application inside a vacuum has been implemented based on the Wave Union TDC scheme in a low-cost field-programmable gate array (FPGA) device. Bench top tests have shown that a time measurement resolution better than 30 ps (standard deviation of time differences between two channels) is achieved. Special firmware design practices are taken to reduce power consumption. The measurements indicate that with 32 channels fitting in the FPGA device, the power consumption on the FPGA core voltage is approximately 9.3 mW/channel and the total power consumption including both core and I/O banks is less than 27 mW/channel.

KEYWORDS: Time-to-Digital Convertor; Low-Power; Wave Union TDC.

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Contents

1. Introduction

Chain structure in existing FPGA families can be used for time-to-digital conversion (TDC) purposes [1-13]. The Mu2e experiment at Fermilab requires operating a large channel-count straw tube chamber system inside a vacuum demanding low-power consumption on all stages of readout electronics including the TDC device. The time difference of signals detected at both ends of a straw tube is measured to a precision better than 35 ps so that the location of the charged particle hit along the tube length can be determined. This required time resolution is much finer than that of typical straw tube TDC in which 1-2 ns is sufficient.

The Wave Union TDC [7] is a scheme developed in our previous work to improve the resolution of the TDC implemented in the FPGA beyond its cell delay. Multiple 0-1 and 1-0 transitions are generated in the delay chain in the Wave Union TDC and registered for encoding, which effectively provides multiple measurements with one set of delay chain and register array structure and thus improve time measurement resolution. (Note that regular TDCs make one measurement with a single 0-1 transition.) Intrinsically, the Wave Union TDC is a low-resource and low-power consumption scheme since less logic elements are used comparing to typical TDC schemes in order to achieve a finer resolution.

In addition, special digital design practices are taken to properly interface the fast clock (250 MHz) and the slow clock (62.5 MHz) domains so that in each channel, the fast clock is confined in the register array used to capture wave union transitions in the delay line, while most encoding and data handling blocks are put in the slow clock domain. Taking advantage that the required minimum double hits separation is relatively large, encoders and other

common functional blocks are shared among multiple channels to further reduce logic element usage and power consumption.

In this paper, the Wave Union TDC is first discussed in Section 2 followed with descriptions of the digital design practices utilized in the low-power edition of the 32 channels TDC in Section 3. Test results of the standard deviation of the time measurements and the power consumption are presented in Section 4. Future work and further improvements are discussed in Section 5.

2. The Wave Union TDC

2.1 Imperfectness of Delay Chains Inside FPGA

A special feature of the FPGA TDC is its large differential nonlinearity (DNL) as shown in Fig. 1(a) which is represented as apparent width of each TDC bin.

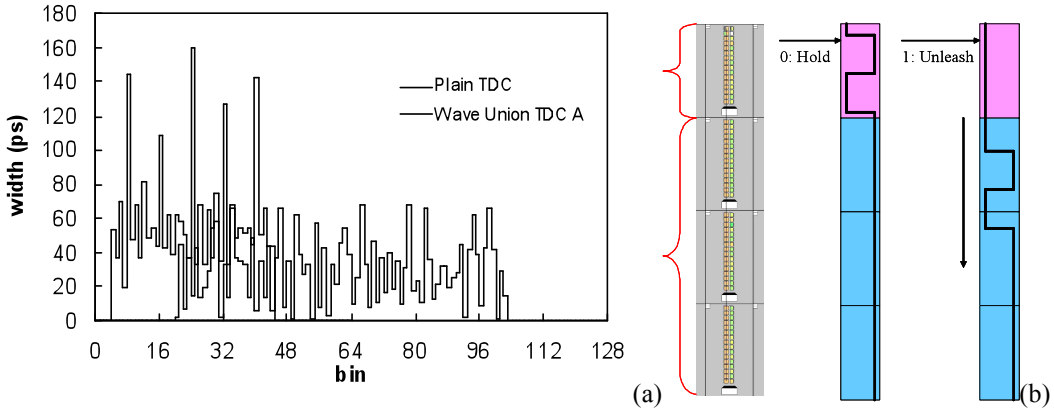


Fig. 1. The bin width plot (a) and a wave union launcher (b)

The most significant origin of DNL is the logic array block (LAB) structure. When the input signal in the carry chain passes across the LAB boundaries (and also the half-LAB boundaries in some FPGA families), extra delays added cause periodic "ultra-wide bins."

2.2 The Wave Union TDC Scheme

In our previous work [7], an approach called the "wave union TDC" was developed to sub-divide the ultra-wide bins and to improve measurement resolution. The key part in the wave union TDC is the "wave union launcher" as shown in Fig. 1(b). A wave union launcher creates a pulse train or "wave union" with several 0-to-1 or 1-to-0 logic transitions for each input hit and feed the wave union into the TDC delay chain/register structure, making multiple measurements. As shown in Fig. 1(a), effectively the "ultra-wide bins" are subdivided using the wave union TDC scheme.

3. Digital Design Practices for Low-Power Consumption

For operating in a vacuum, several digital design practices are taken so that the TDC consumes less power without degrading important performance requirements. The Wave Union TDC scheme itself is a power saving scheme. Additionally, in the FPGA environment, the clock frequency is a far more important factor than the data flipping ratio on power consumption

given the transistor usage in the internal clock distribution network. We have tried using a high frequency clock only in the necessary portion of firmware while keeping most other portions with a clock at lower frequency. Data flow sequence is carefully designed so that some functional blocks can be shared among multiple channels, which reduces silicon area usage and therefore power consumptions. These practices will be discussed in the following.

3.1 Wave Union TDC as a Power Saving Scheme

The TDC resolution can be improved by ganging several channels together, i.e., sending an input into multiple channels. When the bin widths of the delay chains are identical, ganging two channels together may make an improvement by factor of 2 on the time measurement resolution, when the relative delay between the two channels is exactly half of the bin width.

In the wave union TDC scheme, multiple measurements are made in a single set of the delay chain, register array, encoder and other logic functional blocks. Logic element usage and therefore, power consumption is clearly smaller than ganging channels together. In the wave union TDC, the resolution improvement is not as good as factor of 2 given uneven bin widths, but the primary gain is subdividing the "ultra-wide-bins".

3.2 Clock Domain Arrangement

The sampling registers are to be operated in a relatively high frequency so that the length of the delay chain is not too long. In our TDC firmware, the sampling registers are driven by a 250 MHz clock as shown in Fig. 2.

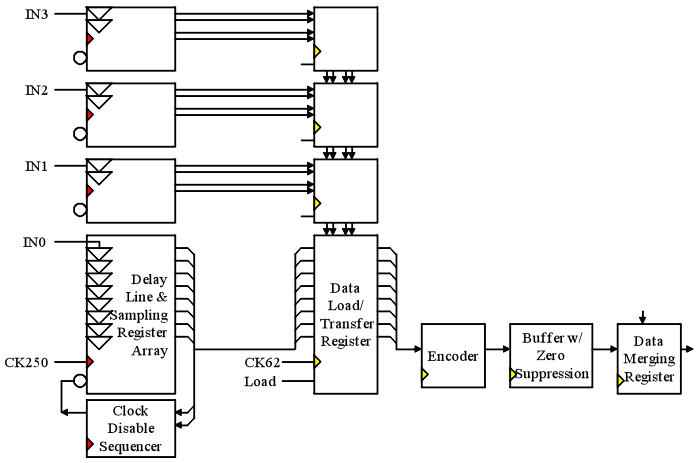


Fig. 2. Block diagram of a four-channel group.

On the other hand, encoders and other stages of the data processing do not need to operate at that high frequency given that the hit rates the TDC channels are not too high. In our firmware, encoders and other stages are clocked at 250/4 = 62.5 MHz to reduce power consumption. To interface the two clock domains, a clock disable sequencer disables the sampling registers for 15 clock cycles (at 250 MHz) after registering a valid hit, so that the outputs of the sampling registers become stable for exactly 64 ns. The data load/transfer registers are enabled to load data every 64 ns (4 clock cycles at 62.5 MHz) so that any valid hit can be loaded once and only once.

This scheme restricts the separation of double hits to be at least 64 ns, and this is acceptable in our application.

3.3 Silicon Resource Sharing

Note that if the data load/transfer registers were enabled to load every clock cycle, the double hit separation would be improved to 16 ns. The reason of choosing 64 ns is to permit further resource saving as discussed in this section. In every four clock cycles, the data load/transfer registers are enabled to load one clock cycle for the valid hit data while transferring data from other channels in the remaining three cycles. This will allow four channels to share one encoder and one zero suppression buffer as shown in Fig. 2. In the larger scale, the similar structure is also utilized as shown in Fig. 3.

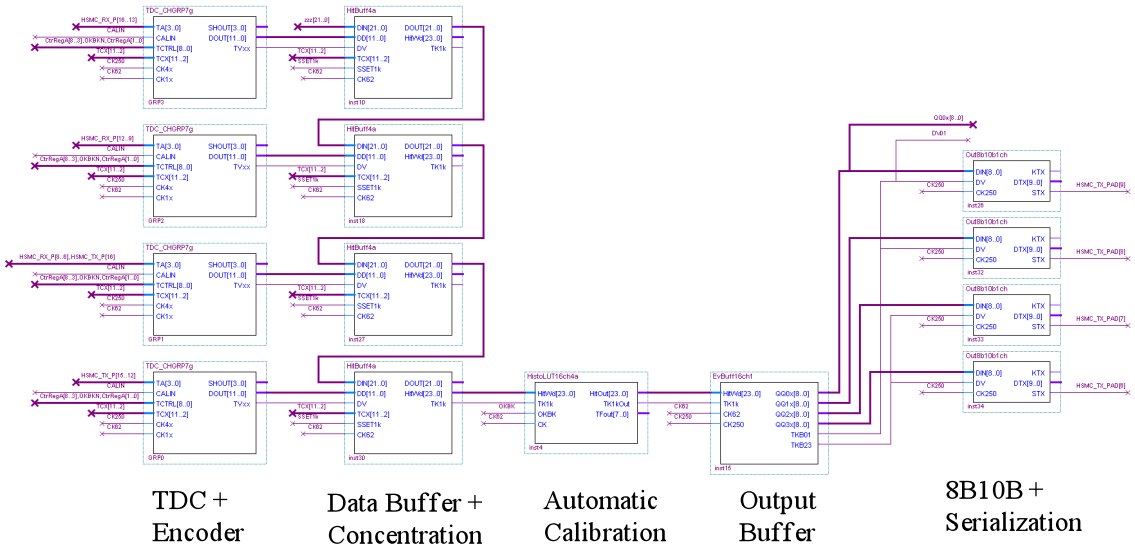


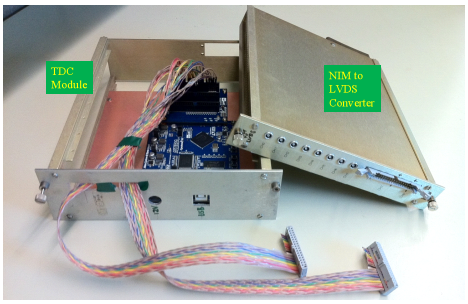
Fig. 3. Block diagram of a partial (16 channels) TDC firmware.

In Fig. 3, four sets of four-channel groups, 16 channels total, are connected in a daisy chain style. In each channel group, zero suppressed data are stored in the data buffer. Data are readout from the buffer and fed through the automatic calibration block. The calibrated data are sent into the output buffer. The data in the output buffer are distributed to four 8B/10B serialization blocks and sent out of the FPGA via 4 differential pairs at 250 M bits/s each.

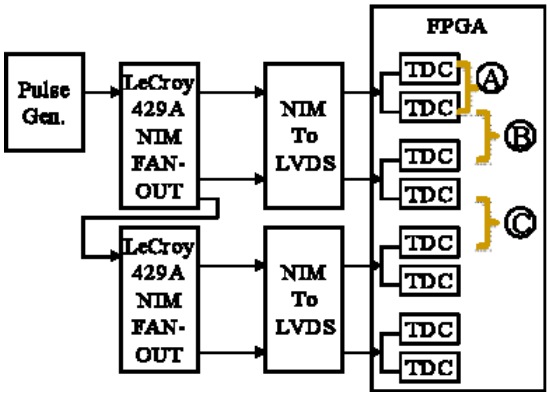
With careful resource saving design practices in various places, 32 TDC channels are fit into the FPGA, taking 56% of logic elements in the device.

4. Test Results

The low-power edition of the Wave Union TDC has been developed in a low-cost Altera Cyclone III FPGA device and tested in an evaluation board as shown in Fig. 4(a).



(a)

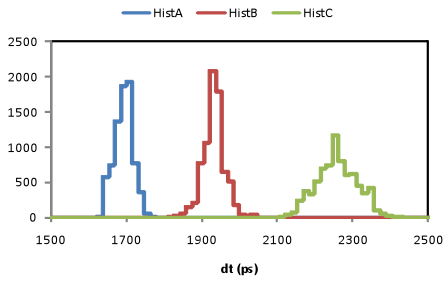


(b)

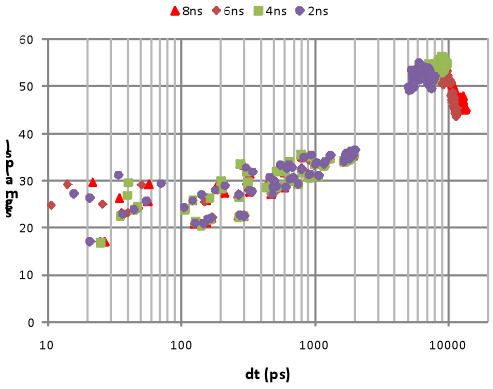
A NIM pulse is generated and fan-out units are used to create 8 copies of the pulse, 4 of which come from the first fan-out unit and another 4 from the second fan-out unit with the input delayed from the first unit by 2, 4, 6 and 8 ns. The NIM pulses are converted into LVDS signals and interfaced with the FPGA. Inside the FPGA, 16 channels TDCs are ganged into 8 groups, 2 channels each. There are three types of time differences as marked A, B and C in Fig. 4(b). They are time differences between (A) two ganged channels, (B) two channels from the same NIM fan-out unit and (C) different NIM fan-out units. The test results of these time differences are described in the following.

4.1 Time Measurement Resolution

Typical histograms of three types of time differences described above are shown in Fig. 5(a). The standard deviations of these time differences are plotted in Fig. 5(b).



(a)



(b)

Fig. 5. Typical time difference histograms (a) and standard deviations vs. time differences (b).

When the two channels are ganged together inside the FPGA (type A), the time differences are less than 100 ps and the standard deviations are mostly in the range of 20 to 30 ps. The type B time differences ranging from 100 ps to 2 ns are closest to regular in-system applications, which have standard deviations from 20 to 35 ps. The type C time differences actually show the additional jitters of the additional NIM fan-out unit and have total standard deviations around 50 ps.

It can be seen that even under conditions of using switching power supplies provided on the evaluation board and having single ended signal connections between the FPGA and other devices, a time measurement resolution of 30 ps is achieved.

4.2 Effects of Power Supply Noise

It is known that the power supply noise degrades TDC time measurement resolution severely. The power voltages needed for the FPGA, i.e., 1.2V for the core and 2.5V for the I/O banks are generated with a switching power converter on the evaluation board and the tests described above are performed under this condition. The power nets on the evaluation board can be disconnected and cleaner linear power supplies can be connected to achieve better time measurement resolutions. A comparison of the different power supplies is shown in Fig. 6.

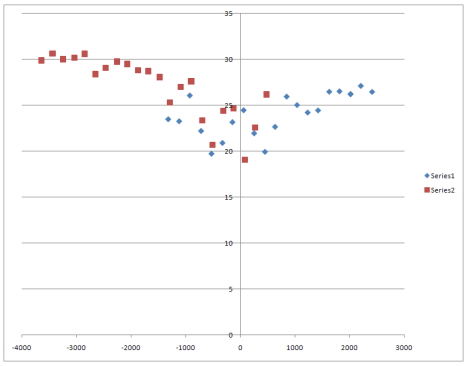


Fig. 6. The standard deviations vs. time differences for switching power supply (Series 2, left) and liner power supply (Series 1, right).

As expected, time measurement resolution indeed improves consistently when the FPGA is powered from voltages generated from a linear power supply.

4.3 Power Consumption

To evaluate power consumption, 32 TDC channels are fit into the FPGA and currents in power nets for both FPGA core and I/O bank are measured.

In normal operating conditions, the current in the 1.2V net supplying the FPGA core is 0.23 to 0.25 A that yields 276 to 300 mW for 32 channels i.e., 8.6 to 9.3 mW/channel. The 2.5V I/O bank power supply draws 0.17 to 0.22 A that consumes 425 to 550 mW for the entire chip. Therefore in this test, the total power consumption is around 22 to 27 mW/channel, including both FPGA core and I/O banks.

5. Discussions

For most applications requiring time measurement resolutions of 30 to 100 ps in nuclear physics, high energy physics and medical physics, FPGA TDCs become feasible due to their low-cost and flexibility. The power consumption can be reduced with various design practices. It can be seen that in our firmware, the core power consumption has already been reduced significantly lower than the one in the I/O banks with 2.5V I/O standards (LVDS, 2.5VCOMS etc.). Further reduction of total power can be anticipated when I/O standards at lower voltage are utilized.

Acknowledgments

This work was supported in part by Fermi Research Alliance, LLC under Contract No. DE-AC02-07CH11359 with the United States Department of Energy and the Student Inquiry and Research Program of the Illinois Mathematics and Science Academy.

References

[1] A. Amiri, A. Khouas & M. Boukadoum, "On the Timing Uncertainty in Delay-Line-based Time Measurement Applications Targeting FPGAs," in *Circuits and Systems, 2007, IEEE International Symposium on,* 7-10 27-30 May 2007 Page(s): 3772 - 3775.

[2] J. Song, Q. An & S. Liu, "A high-resolution time-to-digital converter implemented in field-programmable-gate-arrays," in 2005 *IEEE Transactions on Nuclear Science,* Pages 236 - 241, vol. 53.

[3] M. Lin, G. Tsai, C. Liu, S. Chu, "FPGA-Based High Area Efficient Time-To-Digital IP Design," in *TENCON 2006. 2006 IEEE Region 10 Conference,* Nov. 2006 Page(s):1 – 4.

[4] J. Wu, Z. Shi & I. Y. Wang, "Firmware-only implementation of time-to-digital converter (TDC) in field programmable gate array (FPGA)," in 2003 *IEEE Nuclear Science Symposium Conference Record,* 19-25 Oct. 2003 Page(s):177 - 181 Vol. 1.

[5] S. S. Junnarkar, et. al., "An FPGA-based, 12-channel TDC and digital signal processing module for the RatCAP scanner," in *2005 IEEE Nuclear Science Symposium Conference Record*, Volume 2, 23-29 Oct. 2005 Page(s):919 - 923.

[6] M. D. Fries & J. J. Williams, "High-precision TDC in an FPGA using a 192 MHz quadrature clock," in *2002 IEEE Nuclear Science Symposium Conference Record*, 10-16 Nov. 2002 Page(s):580 - 584 vol. 1.

[7] J. Wu & Z. Shi, "The 10-ps wave union TDC: Improving FPGA TDC resolution beyond its cell delay", in *2008 IEEE Nuclear Science Symposium Conference Record*, 19-25 Oct. 2008 Page(s):3440 - 3446.

[8] J. Wu, "On-Chip processing for the wave union TDC implemented in FPGA", in *2009 IEEE-NPSS Real Time Conference Record,* 10-15 May. 2009 Page(s):279 - 282.

[9] J. Wu, "An FPGA Wave Union TDC for Time-of-Flight Applications", in *2009 IEEE Nuclear Science Symposium Conference Record,* 25-31 Oct. 2009 Page(s): 299-304

[10] J. Wang, et. al., "A fully fledged TDC implemented in field-programmable-gate-arrays", in *2009 IEEE-NPSS Real Time Conference Record,* 10-15 May. 2009 Page(s):290 - 294.

[11] J. Wu, "Several Key Issues on Implementing Delay Line Based TDCs Using FPGAs," in 2010 *IEEE Transactions on Nuclear Science,* Pages 1543 - 1548, vol. 57.

[12] J. Qi, et. al., "A 20ps resolution wave union FPGA TDC with on-chip real time correction", in *2010 IEEE Nuclear Science Symposium Conference Record,* 30 Oct. - 6 Nov. 2010 Page(s):396 - 399.

[13] H. Sadrozinski & J. Wu, "Applications of Field-Programmable Gate Arrays in Scientific Research", Taylor & Francis, December 2010.

[14] Altera Corporation, "*Cyclone III Device Handbook*", (2010) available via: {http://www.altera.com/}