Vertically Integrated Pixel Readout Chip for High Energy Physics

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Abstract: *We report on the development of the vertex detector pixel readout chips based on multi-tier vertically integrated electronics for the International Linear Collider. Some testing results of the VIP2a prototype are presented. The chip is the second iteration of the silicon implementation of the prototype, data-pushed concept of the readout developed at Fermilab. The device was fabricated in the 3D MIT-LL 0.15 μm fully depleted SOI process. The prototype is a three-tier design, featuring 30×30 μm^2 pixels, laid out in an array of 48×48 pixels.*

Keywords: pixel detectors; 3D integration; through silicon via; data sparsification; particle tracking.

Introduction

Three-dimensional (3D) integration techniques bring solutions to pixel-segmented integrated system problems that have been unsolved for years. Scientific instruments are typically realized in small volumes but they re expensive developments, encompassing special needs, like large sizes of imaging fields and up to tens of millions of channels. Improving power distribution, allowing dead-zone-free large area pixel sensors, allowing in-hardware parallel, processing of signals and optimizing attachment of the readout integrated circuits (ROICs) to the sensors are the main areas where 3D techniques show clearly their advantages. 3D integrated circuits (3D-ICs), reported in this paper, are formed by bonding two or more IC wafers (tiers) and interconnecting them with a micron-diameter through silicon vias (TSV).

Fermilab submitted designs to two 3D Multi-Project-Wafer (MPW) runs organized by MIT-LL. Three 6" wafers, fabricated in a 0.18 μm (first) and 0.15 μm (second) fully depleted SOI (FDSOI) process, were stacked using the via last approach. The process features 3 routing metal layers on each tier, in addition to that, two upper tiers have back-metal patterned after thinning. The thickness of the whole structure is about 700 μm while the 3 active tiers are only about 22 μm in total. Each TSV occupies effectively about 5×5 μm^2. This includes metal pads establishing contact with vias on lower tiers of the stack and clearances between neighboring vias. Each TSV can be a buried via, or a fully stacked pillar [1].

Two versions of a 2.5×2.5 mm^2 prototype pixel readout chip, called VIP1 and VIP2, standing for Vertically Integrated Pixel, were submitted in 2006 and 2008, respectively. The VIP chips implement the functionality required by the vertex detector at the International Linear Collider (ILC) [2]. The VIP2 design branched off in two designs: the first one is VIP2a, realized in the MIT-LL process, delivered from the fab in August 2010 and described in this paper and VIP2b is the design that was migrated to the two-tier 0.13 μm Tezzaron/Chartered process. The latter is still in fabrication. The VIP1 and VIP2a prototypes feature a 64×64 array of 20×20 um^2 pixels and a 48×48 array of 30×30 μm^2 pixels, respectively.

The paper reviews the concept of the VIP design. Section II describes implemented functionality, section III reviews achievements of VIP1 and strategy for the design of VIP2a, section IV presents selected results of tests of VIP2a.

Implemented functionality

VIP2a is almost identical to its predecessor VIP1. The chip operates in the data sparsified (data-pushed) readout mode with the data sent off the chip between the bunch trains in synchronization with the accelerator cycle. The information provided by the chip includes digital word of x-y address of the pixel that was hit by a radiation event, digital and analog time stamping marking the incidence time and analog samples of signals taken at the opening of the integration window and after some delay added on purpose to let the signal reach full swing after exceeding the discrimination threshold. Samples of analog signals are used for obtaining more precise estimation of impact positions of particles by weighting amplitudes coming from neighboring pixels. The size of a square pixel between 20 and 30 μm is dictated by a few-micron position resolution that should be provided by the detector plane for the innermost layers of the ILC vertex detector. The functionalities, described above, translate into the transistor level architecture that is real-estate hungry. In order to fit the circuitry into the constrained space, 3D integration technology has no alternatives. The analog circuitry is on the closest to the detector tier (top), and the digital is on the farthest from the detector tier (bottom). The middle tier hosts the analog and digital time stamping blocks. Totaling from all tiers, there are about 200 transistors per pixel . The detailed description of the VIP architecture and the test results of the VIP1 prototype are given in [3].

Information if a given pixel was hit during the exposure time (acquisition phase) is latched in a pixel. During the readout (report phase), a token passing through all daisy

chained pixels finds those that were hit and the data, including their addresses, is send off the chip. The scheme of the token passing based readout is shown in Fig. 1.

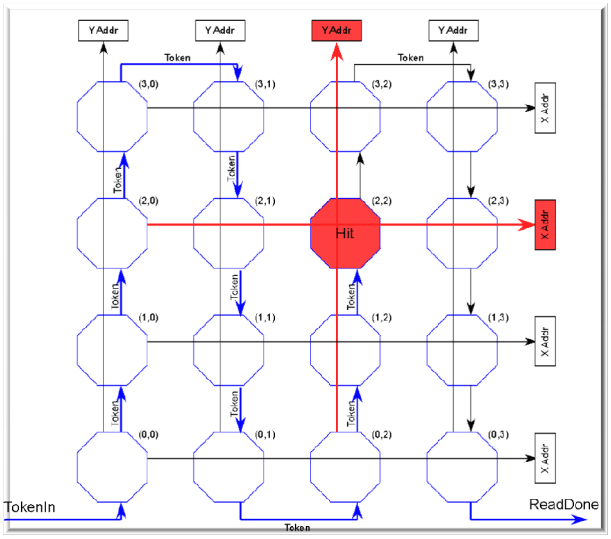

Figure 1 Token passing scheme for finding hit pixels in the detector.

The top tier contains a gated charge integrator, a single ended AC-coupled offset corrected discriminator with a capacitively injected threshold level, an analog memory for the reference sample, an analog memory for the signal sample after discriminator firing, a pulse generator for locking the code of the time stamping counter and for turning on the hit bit, one plate of the test-charge injection capacitance and a bonding pad to the detector. The intermediate tier contains) a 7-bit SRAM-like digital time stamping memory with output enable control to share the same lines on which time ticks in Gray code are distributed for readout of the latched codes and an analog memory cell for distributed voltage ramp, being an alternative time stamping. The bottom tier hosts the sparsification system: token propagation logic, wiredOR line access logic for X-line/Y-line of a hit pixel address generator, test-charge injection logic and a peripheral serialization and output driving part. Small prototypes of VIPs are extendable to sizes of megapixel arrays.

Review of VIP1 and strategy for VIP2A design

The tests of the VIP1 chip showed that the device functioned properly, but a very poor fabrication yield was discovered. The drop in yield was attributed in major part to the tradeoffs in performances of mixed-mode circuitry encountered in advanced, deep-submicron FDSOI processes. Various factors, like bipolar effects in transistors with floating or having resistive bulk connections (sample-and-hold circuits losing stored charges due to parasitic bipolar transistors that switch on under certain bias and driving conditions), oxides impeding heat flow, straining of transistors on the BOX, travel of ions through ubiquitous oxides (instabilities in characteristics of transistors), etc. are known as possible causes of the observed performance deficiencies. On the other hand, no signs of failures of TSVs were observed on the tested chips. However, some chips were found with failures of connections, i.e. shorts between power supply rails or lack of connections between any nodes. There were not more than 10% among the tested chips in which short and open circuits were detected. Since the functioning of the top tier does not depend on the connectivity provided by TSV, the described failures were attributed to the imperfections of the planar part of the processing of the wafers, excluding the 3D stacking from the causes. Other problems were unexpectedly high leakage currents in active devices and soft-shorts between the nodes that were not directly connected but were used within the same circuit blocks. ESD-protection diodes featured leakage currents many orders of magnitude higher than a few pA typically observed.

The architecture of the VIP1 chip was essentially preserved in VIP2a. However, great emphasis was placed on conservatism in the new design. A few modifications, correcting of obvious imperfections and resulting in more complete testability were introduced. The main architectural modifications include: increase number of bits in digital time stamping from 5 to 7, add clearing of the sparsification circuitry from spurious hits achieved simultaneously with arming of discriminators and reading a fixed analog voltage from the correlated double sampler in case of no hit in the pixel (for example in the test mode). The routing of the signal, used to arm discriminators, was done fully on the digital, bottom tier with vertical taps connecting directly to the switches in discriminators thanks to an additional TSV between the bottom and top tier in every pixel. This way of elimination of coupling of a digital signal to a highly sensitive analog amplifier is an example of an effective use of opportunities offered by 3D technologies. Another modification is abandonment of dynamic d-flip/flops for static devices. For improvement of yield, a set of self-imposed guidelines was adopted, targeting increase of yield and improved circuit operation. The original MIT-LL rules for trace routing were scaled by a factor of 1.2, resulting in wider paths and larger clearances to avoid shorts. The minimum transistor sizes, were increased (2×Wmin and 2÷3×Lmin). Thus, the actual process was brought to a 0.35 μm feature-size equivalent, hoping to decrease off-state leakages and to average out structural effects. Sizes of all capacitors in sample-and-hold circuits were increased at least 2 times. The selection between 3 pull-up strengths on wiredOR lines was added in the address generator of hit pixels. Source followers, outputting analog signals in VIP1, were replaced by regular buffers with OTAs. The power and ground routings were strengthened by linking them in an extensive mesh and by having strap connections between tiers in each pixel.

Results of tests of VIP2a

Test structures, featuring fully functional copies of the analog part of the pixel, were placed aside of the matrix of pixels on the top tier and they were characterized at the first step. Test charge could be injected through a 2.7 fF capacitor placed in series to the integrator input. An additional 20 fF capacitor could be added to increase the input load, mimicking connection to the detector. The analog current biases were 4.80 μA and 0.97 μA for the integrator and the discriminator, respectively. The gate-to-source voltages measured on biasing transistors did not differ from those obtained in SPICE simulation. Releasing of the *integrator reset* starts the integration phase and about 1 fC of parasitic charge is injected to the input of the integrator. Releasing of the *discriminator reset* arms the discriminator and automatically cancels offsets. Providing a voltage step across a capacitor connected to the input of the discriminator sets the threshold for triggering upon the integrating amplifier signal. The first analog sample is taken at the moment of arming of the discriminator. The second sample is taken after the discriminator fires waiting an internally set delay of about 500 ns in order to make sure that the signal has time to fully settle. The difference of these two samples corresponds to the integrated charge. Very good linearity of the integrator response was measured for input charges of up to 3 fC. A waveform of the response of the charge integrator to the injection of charge equal to about 1 fC is shown in Fig. 2 for C_{in} (input capacitance) equal to 0 fF and 20 fF. The charge-to-voltage gain is approximately 200 mV/fC at C_{in}=20 fF. The gain is higher for no capacitive load at the input due to finite open loop gain of the amplifier of only 32 dB, resulting from its very simple architecture. The rise-time of the integrator signal was measured 228 ns and 120 ns at C_{in}=20 fF for the *discriminator reset* kept active and released, respectively. The difference in the timing results from lower capacitance as upon activation of the discriminator one analog sample-and-hold cell is disconnected from the integrator. A threshold of 0.1 fC is injected internally when the discriminator reset is released due to parasitic charge injection. This initial value is sufficient to maintain the discriminator in the armed state until the injection of the actual threshold, which should occur immediately. A threshold pulse just adds to that initial level with either positive or negative sign. An intrinsic delay of the discriminator for triggering on large signals is about 200 ns. Noise of the analog front-end part was measured using injected charges and varying the delay after having the discriminator armed. This approach resulted in correlated double sampling processing with different time intervals. The results of the noise characterization are given in Fig. 3. The right axis gives noise values expressed in equivalent noise charge (e-) calculated using the 200 mV/fC charge-to-voltage conversion factor. The intermediate tier hosts a generator of the voltage ramp used in the analog time stamping. An input current is divided by 10 and integrated on a 5.5 pF capacitor. The resulting voltage is buffered by a voltage follower, built with a rail-to-rail class A-B operational amplifier. The ramp voltage is distributed to all pixels in the matrix. All biases and control signals for the ramp generator are routed from the top tier. Significant improvements of performance of current mirrors with respect to VIP1 were observed. The division ratio of 10:1 is maintained over 3 orders of magnitude of the input current and no excessive leakage currents were detected in VIP2a.

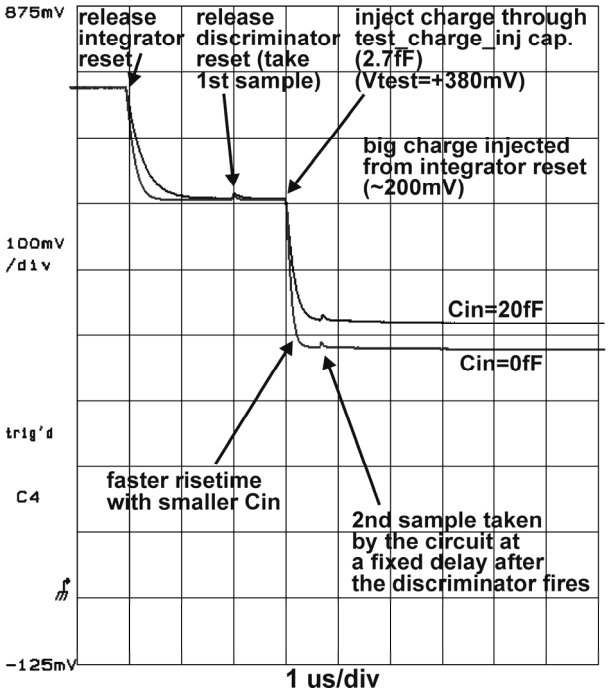

Figure 2 Integrator response for 0fF and 20fF of input capacitance, C_{in}.

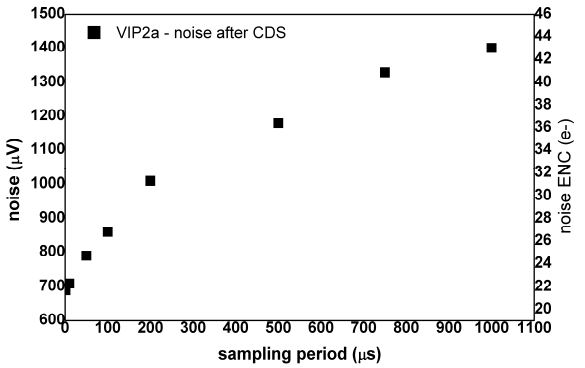

Figure 3 Noise as a function of sampling interval for C_{in}=20fF.

The ramp generator was characterized by measuring the time jitter of the ramp rise time and linearity of the ramp at constant ramp bias current. The ramp could be controlled thorough the whole range having practical importance for the functioning in the ILC environment, i.e. from 10 μs to 1 ms. The input voltage offset of the rail-to-rail operational amplifier did not exceed 10 mV. The time jitter and the linearity were measured to be better than 1% in the

designed 1.3 V range of the ramp, i.e. from 200 mV from the ground rail to 200 mV below the power supply rail.

At the beginning of the readout phase, the token is injected into the matrix of pixels and starts racing to find the first hit pixel. When the hit pixel is found, the first readout clock pulse releases the position and time stamp information for readout and the token can continue until it stops at the next hit pixel. The maximum readout clock frequency is determined by the token propagation delay. It must be slow enough that the readout cycle is longer than the time needed to find the next hit pixel or token exits the matrix. The tests of the token propagation were done by measuring the delay time of both edges of the square pulse injected to the token input to the matrix. The matrix was emptied beforehand from any hits by performing a full readout procedure until the matrix was transparent for the token. The token propagation delay calculated per pixel for 3 different chips is shown in figure 5 as a function of the digital power supply. The propagation delay time is almost 2 times longer than it was measured for the VIP1 chip. The increase of the token propagation time is due to the increase of sizes of transistors and consequent increase of the pixel size. However, the token propagation logic functions correctly within the whole range of power supply voltages on almost all tested chips.

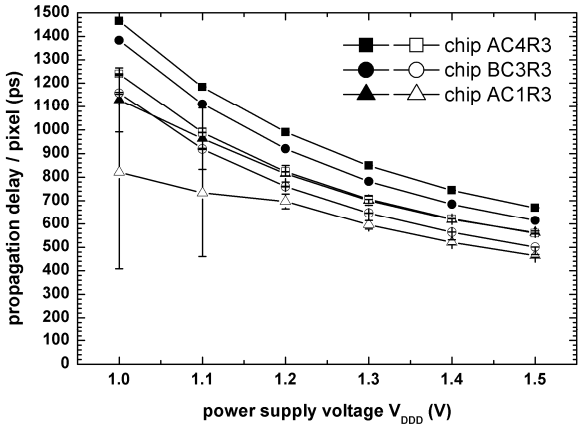

Figure 5 Token propagation delay per pixel for different chips at different power supply voltages.

The VIP2a chip was not bonded to the detector, although testing of the readout procedure was possible thanks to the implemented features allowing testability. Full sparsified readout was tested with test charges injected in individual pixels. Applying corresponding threshold allowed recording hits in pixels whose addresses were read out. Pixel-to-pixel threshold dispersions of discriminators were measured by scanning globally applied threshold levels and extracting number of triggered pixel for each point. Averaging of individual measurements over 10 measurements for each point in the scan led to the plot of the threshold dispersions presented in Fig. 6. The 1 sigma width of the distribution is 300 μV which is equivalent to about only 12 e^- of the input signal. The reset of the integrating amplifier is kept reset. The measured very low threshold dispersion results for an efficient auto-correction of offsets of the amplifier and of the discriminator. The offset voltage is sampled on the capacitance that is connected in series to the discriminator input.

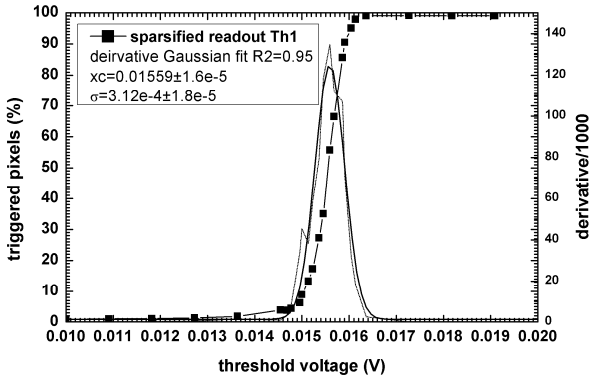

Figure 6 Pixel-to-pixel threshold dispersions of the discriminator σ=300 μV.

Conclusions

The VIP2a chip is the second realization of the pixel readout concept for the ILC in the 3D process at Fermilab. Based on the VIP1 experience, a set of conservative design rules was adopted, targeting improvement of yield. The use of these rules translated to the larger pixel size and slower operation of the device, however the yield seems to be improved. Without the 3D integration technology, enabling higher densities of electronic circuitry per unit area, implementation of the required functionality would not be possible. The size of the prototype is 2.5×2.5 mm^2, however the architecture of VIP2a allows an easy expansion to a megapixel scale. The tests of the VIP2a chip are underway. Some selected results were presented in the paper.

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