Evaluation of Emerging Parallel Optical Link Technology for High Energy Physics

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ABSTRACT: Modern particle detectors utilize optical fiber links to deliver event data to upstream trigger and data processing systems. Future detector systems can benefit from the development of dense arrangements of high speed optical links emerging from industry advancements in transceiver technology. Supporting data transfers of up to 120 Gbps in each direction, optical engines permit assembly of the optical transceivers in close proximity to ASICs and FPGAs. Test results of some of these parallel components will be presented including the development of pluggable FPGA Mezzanine Cards equipped with optical engines to provide to collaborators on the Versatile Link Common Project for the HI-LHC at CERN.

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1. Introduction

The Versatile Link common project is a joint project to specify and develop optical links for use in the HL-LHC upgrades at CERN [1], [2]. This project includes the development of custom radiation hard components for use on the front end (or on-detector end) of particle detectors with commercially available components employed as the back end (or off-detector end) optical transceivers. Commercially available components represent the most cost effective solutions for the back end applications and are not exposed to the intense radiation and magnetic fields that are present at the detector. The Versatile Link standard specifies a point-to-point architecture operating at a nominal data rate of 4.8 Gbps in each direction (uplink and downlink). Single mode and multimode fiber links are to be supported compliant with Versatile Link specifications [3]. The single channel format for the project adopts the Small Form Factor Pluggable Enhanced (or SFP+) format for back end optical transceivers [4]. Several vendors of this mature technology are also developing parallel optical components (transmitters, receivers, and transceivers) to operate at data rates up to 10 Gbps on each parallel channel.

The use of dense parallel optical modules in detector data readout of high energy physics experiments offers some advantages over single channel formats. By employing parallel channel technology, fibers can be managed more effectively with robust connectors and fiber ribbons. Several vendors of optical communications components are developing emerging parallel optical products including a class of devices known as optical engines. The emerging products are being developed in a variety of options including multichannel transmitters, receivers, and transceivers. Some of these devices allow designers to mount the electro-optical components in locations in the middle of a printed circuit board, reducing the space needed on the edge of rack-mounted cards and providing the designer with greater flexibility in layout and routing tasks. By allowing the optical transceivers to be located mid-board, the electromagnetic emissions and susceptibility can be reduced as the length of traces carrying high speed serial data can be minimized. Shorter traces will also reduce attenuation of high speed electrical signals between the optical engines and FPGAs or ASICs with which they are communicating.

The Versatile Link project team is evaluating the performance of several different devices being developed for parallel optical communications. These devices, driven by the need for high speed data transmission for telecommunications, storage area network, and high performance computing markets, are being evaluated using the same measurement techniques as those employed to characterize the SFP+ devices. Fermilab has partnered with a number of vendors to procure samples of emerging devices. Whenever possible, Fermilab has employed evaluation kits made available by the component vendors to quickly assess the performance of the components. However, in addition to the use of these evaluation kits, Fermilab is also developing custom Field Programmable Gate Array (FPGA) Mezzanine Cards (FMCs) to serve as hosts for several of these optical engines. These FMC platforms can be shared with Versatile Link collaborators to enable them to evaluate the optical engine offerings using FMC-equipped test platforms.

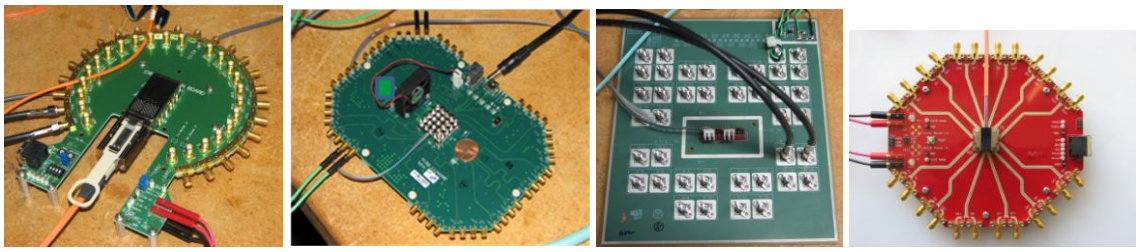
2. Examples of Parallel Optical Devices

Figure 1 illustrates four different parallel optical modules in a number of package options. Figure 1(a) illustrates a 12 channel transceiver (with 12 transmitters and 12 receivers utilizing a 24 fibre ribbon) which might be employed in a card edge application. Figure 1(b) shows a 12 channel optical engine also in a transceiver format. This option allows the device to be located

mid-board for lower electromagnetic emissions as trace lengths can be quite short. Figure 1(c) illustrates a 4 channel transceiver which employs a novel connector for ease of insertion and removal of the device. Figure 1(d) shows a 12 channel transmitter-only device. A complementary 12 channel receiver device is also part of this family of components.

The different physical formats that these devices represent indicate that these devices are emerging products and rigid common standards for package formats have not been defined. Some package formats may offer advantages over others in terms of thermal management, electromagnetic emissions and susceptibility, and robustness of connections. Some of these devices have fibre pigtails that are used to connect to standard fibre ribbon connections and would likely be terminated on a face plate in a rack with a transition to a standard ribbon connector (such as an MTP/MPO connector in 12 or 24 fibre formats).

A measure of the packaging efficiency can be computed with the ratio of the data rate to the board area consumed by a package. All of the devices shown are designed to operate at 10 Gbps on each of their multiple channels with a center wavelength of 850 nm on each channel. This rate density ranges from approximately 0.16 Gbps/mm^2 to 0.29 Gbps/mm^2.



(a) (b) (c) (d)

Figure 1: Four parallel optical communications options. In parts (a) and (b) of the figure are two different 12 channel transceivers. Part (c) of the figure illustrates a 4 channel transceiver while part (d) shows a 12 channel transmitter. All of the devices shown are mounted on vendor supplied evaluation boards which are designed for use with commercial test equipment or FPGA based signal integrity kits. Electrical inputs and outputs are located around the board and optical connections are established with fibre pigtails or directly to MTP/MPO connectors.

3. Test Results

Several of the devices have been tested for optical and electrical performance. Tests include the characterization of performance measures derived from the electrical and optical eye diagrams when the devices are excited with 5 Gbps pseudorandom bit stream (PRBS) data from an FPGA based signal integrity kit. Although the devices are all rated to at least 10 Gbps per channel, the use of 5 Gbps data streams reflects the expected data rate for Versatile Links. The use of signal integrity kits provides a low cost programmable test pattern generation and error checking capability. With these platforms, bit error rate tests can be performed with a variety of test pattern and encoding options. Optical sampling modules are used with digital sampling oscilloscopes for complete optical eye pattern analysis. Jitter performance is measured with the use of jitter decomposition software and a pattern synchronization module that allows the test equipment to repeat data collection on the individual transitions in the digital test pattern. The transmitter and receiver channels for each of the devices were characterized and compared to per channel specifications for Versatile Link compliant systems.

Transmitter tests include the measurement of the following characteristics:

1. Optical modulation amplitude
2. Extinction ratio
3. Eye opening
4. Rise time
5. Fall time
6. Transmitter deterministic jitter
7. Transmitter total jitter

Receiver tests include the measurement of the following characteristics:

1. Receiver sensitivity
2. Receiver deterministic jitter
3. Receiver total jitter

All measurements shown in the following figures were collected at room temperature (approximately 23 ^{o}C).

3.1 Transmitter Test Results

Figure 2 illustrates results for the measurement of optical modulation amplitude (OMA) for transmitter channels of the devices. Four 12 channel devices and two 4 channel devices were tested. These results are shown against OMA specifications designated as "calorimeter grade" and "tracker grade" specifications. The Versatile Link system specifications will include two versions reflecting the different OMA requirements for inner detector (tracker grade) and outer detector (calorimeter grade) applications. The reason for two different specifications for the tracker and calorimeter applications is due to the expected increased reduction in receiver sensitivity for tracker applications. This increase in receiver sensitivity is expected due to higher radiation levels in the tracker, requiring an increase in transmitter power to overcome this effect and meet overall link margins. From plots like these, it is possible not only to determine how the measurements compare with the specifications but also the degree to which the devices exhibit uniformity across the channels. While all three measured devices exceed their respective product specifications, only Dev 1_1 and Dev 1_2 meet the OMA requirements for Versatile Link tracker and calorimeter back end transmitters. Dev 3_1 and Dev 3_2 meet the OMA requirements for a Versatile Link calorimeter application.

While OMA is a measure of the optical signal strength delivered by a transmitter, other measurements reveal the timing quality of transmitter signals. Figure 3 illustrates the total jitter results for the transmitters tested. This is a measure of the deviation from ideal timing transitions in the data pattern. The results are expressed as a fraction of the unit interval (or UI which, for 5 Gbps data rates, is equal to 200 ps). Failure to meet the jitter tolerance specification increases the probability of bit errors degrading the link performance.

The total jitter includes contributions from random components (which are assumed to be Gaussian and independent of other contributions) as well as deterministic components (which are characterized by probability density functions which are bounded in that the peak to peak jitter observed in such contributions does not continue to grow with time). The relationship between these random and deterministic contributions and the total jitter is described by:

(1) $TJ(device) = DJ(device) + 14 \times RJ(device)$ *(for a bit error rate of 10^{-12})*

where

(2) $DJ(device) = | DJ(measured) - DJ(stimulus) |$

and

(3) $RJ(device)^2 = RJ(measured)^2 - RJ(stimulus)^2$

where TJ(device) is the total jitter of the transmitter to be determined. DJ(device) and RJ(device) are the deterministic and random contributions of the jitter due to the device. These formulas show how the uncorrelated (random) and correlated (deterministic) jitter components can be determined from the electrical stimulus contributions and the actual measured values impressed on the optical signal. The device values are extracted and plotted in Figure 3. The values of the jitter of the electrical stimulus (provided from an FPGA signal integrity kit used as a PRBS generator) were approximately 3 and 8-10 picoseconds for the random and deterministic jitter contributions respectively. The values plotted below are specifically the jitter contributions from the optical transmitters and receivers, after the contributions from the stimulus have been extracted from the measured values using the formulas (1-3) above.

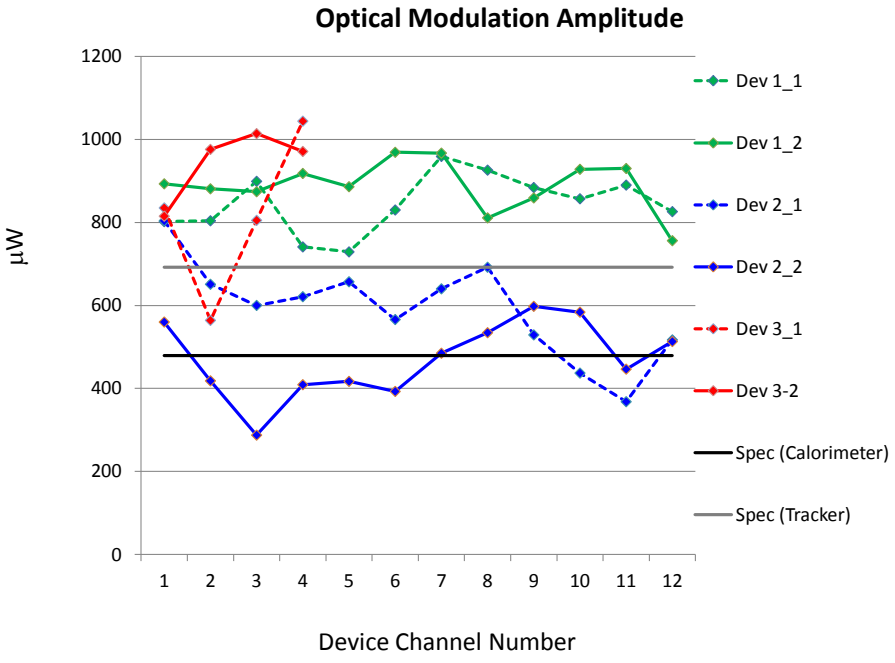


Figure 2: Optical modulation amplitude as a function of channel number for 3 different classes of devices. The specification thresholds for calorimeter grade (gray) and tracker grade (black) Versatile Link requirements are shown as horizontal lines. Data for four 12 channel transmitters and two 4 channel transmitters are shown.

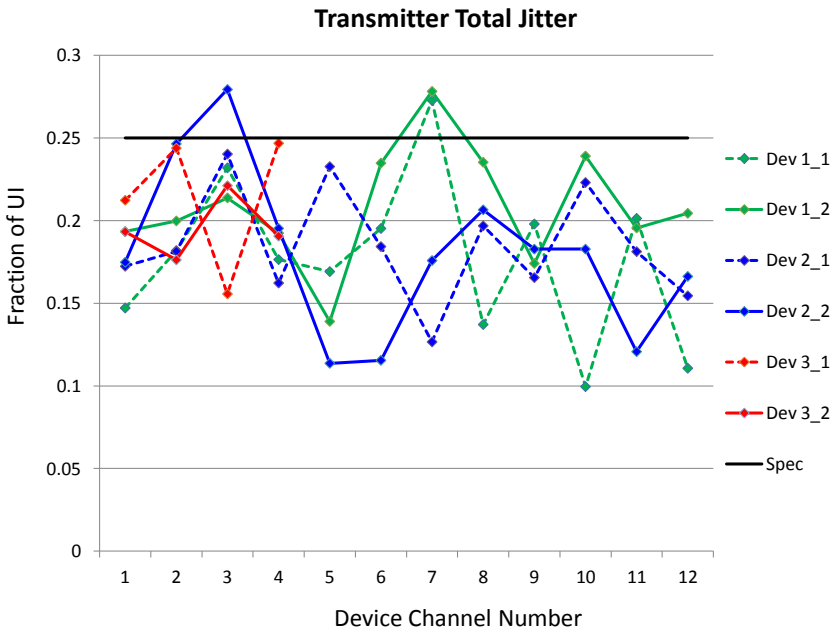


Figure 3: Transmitter total jitter (TJ(device)) measurements for the devices tested as a function of the channel number. Channels that exceed the specification threshold of .25 UI (where UI = 200 ps for 5 Gbps transmission) contain more jitter than would be acceptable for the Versatile Link jitter budget. Note that one class of device (Dev 1_1 and Dev 1_2) meets the requirements for all but a single channel located in the middle of the device. For the electrical stimulus, RJ(stimulus) ~ 3 ps and DJ(stimulus) ~ 8-10 ps.

3.2 Receiver Test Results

Receiver sensitivity is a measure of the minimum level of power needed to ensure that signals are received and interpreted with acceptable margin in a communication system. The sensitivity is measured by introducing attenuation into the optical path to the receiver in a controlled manner while observing the effect on bit error rates. Figure 4 illustrates the measured receiver sensitivity for the parallel devices tested. It should be noted that parallel devices also need to be characterized for their crosstalk. This measurement is to be made in a manner similar to receiver sensitivity except that channels which neighbor the channel under test will be controlled such that the transmitted power in the neighboring channels (also known as aggressor channels) will be a specified power level higher than that in the channel under test (also known as the victim channel). This measurement gives an indication of the effect that transmissions on one channel have on neighboring channels.

Jitter measurements are also important for receiver devices. Unlike transmitter jitter (which is measured in the optical domain), receiver jitter is a measurement of the quality of the timing

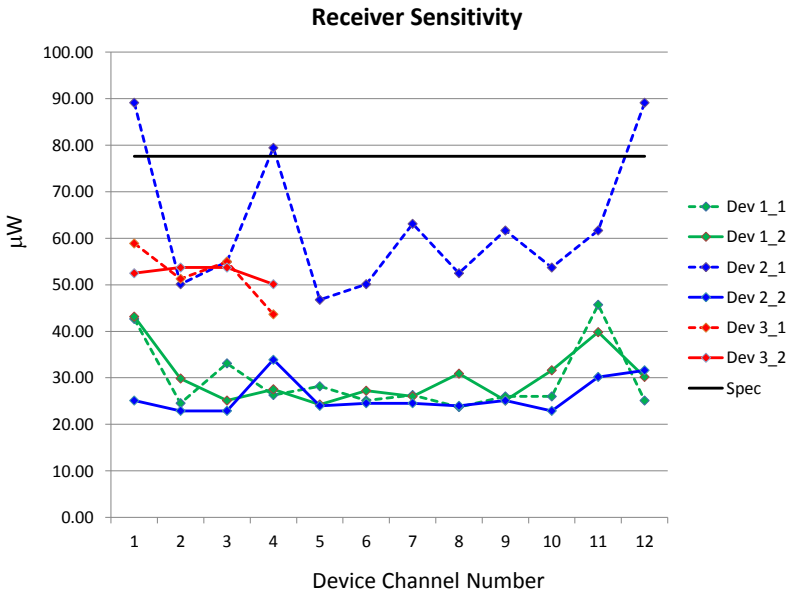


Figure 4: Receiver sensitivity by channel (defined for a bit error rate of 10^{-12}) for four 12 channel receivers and two 4 channel receivers. Measurements which lie above the per channel specification (solid black line) do not meet the requirements of the Versatile Link.

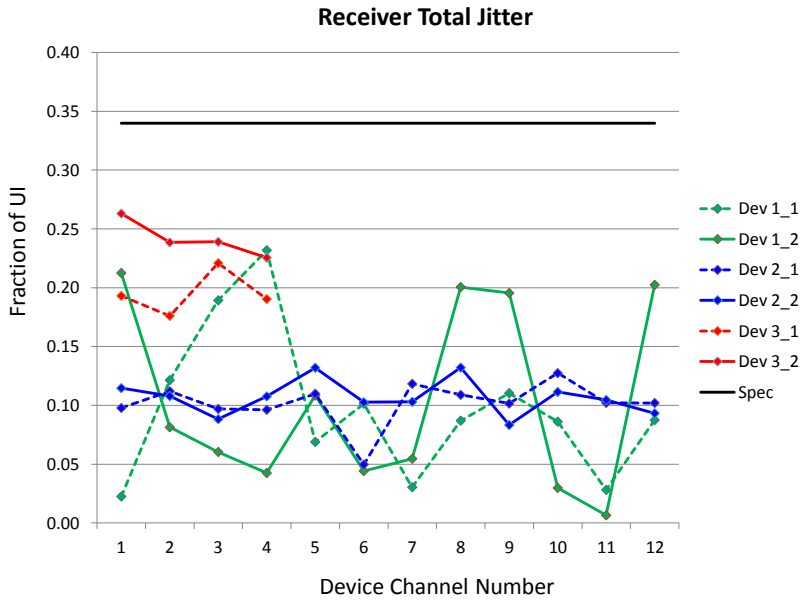


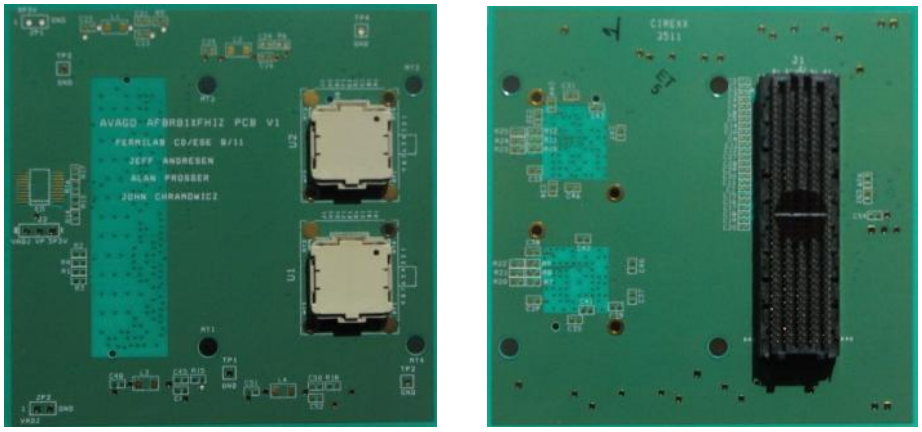
Figure 5: Receiver total jitter (RJ(device)) by channel for four 12 channel receivers and two 4 channel receivers. Results are shown as a fraction of the Unit Interval or UI (which is 200 ps for 5 Gbps transmission). For the optical stimulus, RJ(stimulus) ~ 3-4 ps and DJ(stimulus) ~ 14-20 ps.

of electrical signals output from the receiver and presented to the deserializers of an ASIC or FPGA which will transform the serial bit streams on each channel to parallel data. Figure 5 illustrates the total receiver jitter by channel for several devices.

4. Conclusions and Future Work

Several devices were tested at 5 Gbps for consideration as components for use compliant with the Versatile Link per channel specifications for parallel devices. The performance of these devices shows that there is potential for their use as back end components in Versatile Link implementation. Other devices are currently being tested and will be compared with the performance of those devices on which this report is based. It should be noted that no single device tested so far has met all of the performance targets of the Versatile Link per channel specification but some devices have shown performance that meets the requirements on all but a few channels. In particular, the 12 channel transmitters appear to be a solution to the problem of providing sufficient power to meet the requirements of multimode tracker grade Versatile Links. The requirements for the OMA (for tracker applications), eye opening, and transmitter total jitter were seen to be the most challenging requirements to satisfy as a result of this testing. Some of the devices tested were considered "alpha" or "beta" versions of the devices as opposed to more "market-ready" devices. The performance of these version reflected their somewhat less mature development and the data has been shared with the vendors to help with improvements that might meet the Versatile Link specifications. For example, devices Dev 2_1 and Dev 2_2 were specifically provided as "engineering samples" and still in a state of development. This status may well contribute to the generally lower performance of those devices compared to others tested.

While the evaluation boards that are illustrated in Figure 1 are convenient test platforms, they do not necessarily represent the most realistic designs on which the use of these parallel optical components may be based. To further pursue the performance of these devices under a more typical application, Fermilab has developed test hardware based on the use of FPGA Mezzanine Card (FMC) connectors. These mezzanine boards (see Figure 6) can be equipped with different optical engines and provided to Versatile Link collaborators for additional testing. For example, the optical engine mezzanine card shown below was specifically designed to be compatible with the Gigabit Link Interface Board design from CERN [5]. Fermilab will continue to develop mezzanine cards based on these optical engines and evaluate their performance and compare them to the ideal test platforms of the vendor provided evaluation boards.



(a) (b)

Figure 6: The top and bottom side views of an optical engine mezzanine card. The sockets for the optical engines (transmitters and receivers) are shown in (a) while the FMC connector which conveys the high speed electrical signals to and from the FPGA motherboard is shown in (b).

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