Small Area Array-Based LED Luminaire Design

Final Report

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ABSTRACT

This report contains a summary of technical achievements during a three-year project to demonstrate high efficiency LED luminaire designs based on small area array-based gallium nitride diodes. Novel GaN-based LED array designs are described, specifically addressing the thermal, optical, electrical and mechanical requirements for the incorporation of such arrays into viable solid-state LED luminaires. This work resulted in the demonstration of an integrated luminaire prototype of 1000 lumens cool white light output with reflector shaped beams and efficacy of 89.4 lm/W at CCT of 6000^{o}K and CRI of 73; and performance of 903 lumens warm white light output with reflector shaped beams and efficacy of 63.0 lm/W at CCT of 2800^{o}K and CRI of 82. In addition, up to 1275 lumens cool white light output at 114.2 lm/W and 1156 lumens warm white light output at 76.5 lm/W were achieved if the reflector was not used. The success to integrate small area array-based LED designs and address thermal, optical, electrical and mechanical requirements was clearly achieved in these luminaire prototypes with outstanding performance and high efficiency.

Table of Contents

EXECUTIVE SUMMARY

The objective of this three-year project is to develop GaN-based LED arrays, specifically addressing the thermal, optical, electrical and mechanical requirements for the incorporation of such array into viable solid-state luminaries. The scope of work encompassed individual small-area chip shaping and contact designs to improve LED efficiency and facilitate incorporation into arrays with associated electrical power handling and downconversion technologies to achieve target efficiency at the desired color point. The array elements then were matched to appropriately designed LED arrays including thermal management elements with minimal overall thermal resistance to ambient to ensure lowest possible LED operating temperatures. Finally, the resulting LED arrays were combined with a custom luminaire enclosure that has been designed to specifically address the thermal, optical, and electrical requirements of the LED luminaire prototype. At each development stage the trade-offs between performance and manufacturing feasibility/cost were addressed. The development efforts included materials, fabrication processes, and designs required to achieve the project goals. LED arrays and luminaire enclosure prototypes were fabricated to demonstrate the integrated luminaire performance and validate the proposed technology approaches. A summary of project milestones by Year and Task is shown in Table below.

SUMMARY TABLE OF PROJECT GOALS

Task	Attribute	End of Year 1	End of Year 2	End of Project
1	Chip Performance	60 lm/W	80 lm/W	100 lm/W
2	Array Design	Prototype #1	Prototype #2	Final Prototype
3	Thermal Resistance (junction-to-ambient)	20^{o}C	10^{o}C	5^{o}C
4	Downconversion/Color Temp. (CCT)	-	-	Achieve 2800-3500^{o}K

This report contains a summary of technical progress made during the three-year project. For the sake of clarity, the report is divided into four main parts according to the four main tasks in the statement of work. Each part contains challenges, results and discussions sections.

Section 1 describes the improvement of LED chip performance. It was determined that significant work would be necessary to improve the light emission efficiency from the LED chips in order to attain the goal of 1000 lumens output at 100 lm/Watt. Two approaches to achieve this were outlined as the first task in the project. However, at the end of first year, two unanticipated factors became apparent which have caused a re-assessment of the priority assigned to this task. Specifically, (1) it was noted that significant improvements in chip efficiency were being obtained through independent research at Cree, (work not directly connected to this project), and (2) issues related to the efficiency and reliability of the LED array design (described in Section 2) proved more challenging than anticipated. In particular, various array designs were developed during the first year showing strong improvements in emission efficiency, but subsequent accelerated reliability testing revealed a significant and unexpected degradation in light emission with time. Since the resulting LED luminaire prototype will require increased reliability and lifetime compared to current technology in order to offset the higher anticipated initial cost, the decision was made to increase work towards improving the robustness of the array design (Task 2), while de-emphasizing or postponing to a

later stage in the contract of improvements in chip efficiency (Task 1). By obtaining LED chips with improvements of light output efficiency from Cree at the final year, we demonstrated the performance of 1275 lumens cool white light output at 114.2 lm/W and 1156 lumens warm white light output at 76.5 lm/W in an integrated luminaire prototype without reflector attached.

Section 2 describes the works to develop GaN-based LED array designs addressing optical, thermal, electrical and mechanical requirements with optimized small area LED chip distributions. Two approaches to achieve this were undertaken: (1) Optimized distributed LED chip design addressing optical and thermal trade-offs; and (2) Electronic / power handling integration for distributed LED arrays and associated luminaire. The success to integrate electronic and power handling components for LED arrays and associated luminaire were demonstrated in the performance of an integrated luminaire prototype. This work resulted in the demonstration of integrated luminaire prototypes having performance of 1000 lumens cool white light output with reflector shaped beams and efficacy of 89.4 lm/W at CCT of 6000^{o}K and CRI of 73; and performance of 903 lumens warm white light output with reflector shaped beams and efficacy of 63.0 lm/W at CCT of 2800^{o}K and CRI of 82. The progress of reliability of LED arrays (including designs, materials and processes) was evaluated at stressed operating conditions of high temperature and humidity with prolonged time.

Section 3 describes the works to achieve effective luminaire design and thermal managements. Modeling and experimentation to determine the appropriate thermal design parameters for achieving the lowest possible thermal resistance from junction to ambient in the luminaire prototypes were undertaken. Issues such as the effects of luminaire orientation/attitude on convective thermal dissipation were considered and measured during development. Luminaire design was focused on utilizing existing commercial BR/PAR compatible track-mount luminaire enclosures for the LED lamp, with modifications implemented as necessitated by thermal and/or optical considerations. This work resulted in the demonstration of final LED luminaire prototype performance of 3.4 to 3.8^{o}C/W thermal resistance from LED chip to ambient, though these results were calculated through indirect measurement due to thermal crosstalk and luminaire configurations. Nevertheless, thermal resistance of 7.3^{o}C/W from LED chip to ambient and 4.1^{o}C/W from LED chip to board was measured directly in LED array prototypes.

Section 4 describes the works to identify and develop optimal method for achieving uniform white light generation at target color temperature of 2800-3500^{o}K. Two approaches to achieve this were undertaken: (1) identify alternative downconversion materials to achieve warm white emission; (2) investigate alternative methods for combining phosphor and LED in an array to improve efficiency and uniformity. Many phosphor materials with various properties were evaluated for light output at CCT of 2800-3500^{o}K as well as the application methods through this project period. Of an integrated warm white luminaire prototype, we demonstrated the performance of 1156 lumens white light output and efficacy of 76.5 lm/W at CCT of 2800^{o}K and CRI of 82 when reflector is not used.

SECTION 1
TASK 1 - SMALL LED CHIP EFFICIENCY AND COMPATIBILITY WITH ARRAY DESIGN

CHALLENGES

Small Area Bond Pad Reflectivity

As illustrated in Figure 1.1, the top electrical contact metallization for a small-area LED chip (right side of picture) occupies a significantly larger relative fraction of the top emitting surface than a similar size contact on a large-are LED chip (shown on the left). As a result, the optical performance and efficiency of small-area emitters is impacted more strongly by sub-optimal reflectivity at the top metal contact. Measurements in our lab have shown that the improvement in light extraction efficiency with decreasing chip size (illustrated in Figure 1.2) begins to saturate for chip sizes below 250 μm square, due primarily to absorption at the top contact pad. Improvement of the reflectivity of this layer is necessary to reduce the relative amount of light absorbed at the top contact, thereby improving LED emission efficiency.

To reduce absorption at this contact, a higher reflectivity metallization process will be developed using materials such as silver to improve the reflectivity with no associated increase in contact resistance (which would lead to higher operating voltage and reduced wall-plug efficiency for the device).

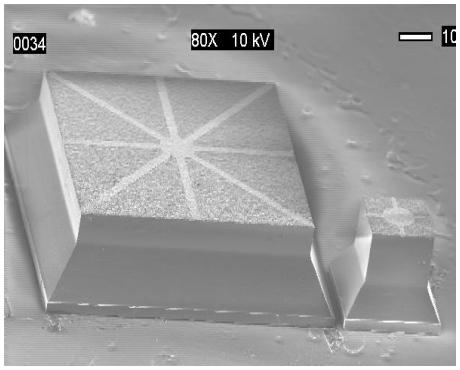


Figure 1.1. SEM image of large-area and small-area Cree LED chips.

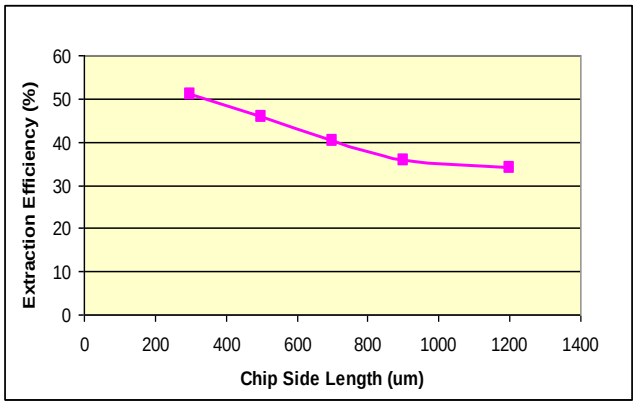


Figure 1.2. Calculated LED light extraction efficiency as a function of chip dimension showing increase in light extraction efficiency with decreasing chip size.

Small Area Chip Shaping

The introduction of facets to LED chips has been employed with great success to improve light extraction efficiency, or the proportion of light generated in the LED active layer that ultimately escapes the LED chip. The proposed effort seeks to optimize light extraction in small LED chips while introducing specific facets to facilitate the incorporation of small-area chips into distributed arrays necessary for the proposed luminaire. The facets of the chips will be customized to achieve desired light output profiles as a function of viewing angle to the extent possible through chip shaping. Novel, asymmetric facet schemes have the potential to provide narrowing of the emission beam from the chip, allowing for relaxed optical constraints on chip spacing and simplified optical design in the final luminaire. Asymmetric designs with

reduced top surface area may also facilitate the placement of wirebond or other methods of achieving electrical contact to the chip, as described below in Section 2.

Also to be addressed will be the issue of perimeter light leakage around the chip. Highly reflective coatings such as aluminum or silver layers, possibly in combination with transparent thin films such as SiO_2 or indium-tin oxide will be investigated to minimize the loss of light that is directed downward around the edges of the chip in present designs.

RESULTS AND DISCUSSIONS

It was determined that significant work would be necessary to improve the light emission efficiency from the LED chip in order to attain the goal of 1000 lumens light output at 100 lm/W. Two approaches were undertaken to improve the brightness and emission efficiency of LED chips: (1) improved reflectivity bond pad; and (2) improved chip shaping for compatibility with distributed design and beam shaping. However, at the end of first year, two unanticipated factors became apparent which have caused a re-assessment of the priority assigned to this task. Specifically, (1) it was noted that significant improvements in chip efficiency were being obtained through independent research at Cree, (work not directly connected to the project), and (2) issues related to the efficiency and reliability of the LED array design (described in Section 2) proved more challenging than anticipated. In particular, various array designs were developed during the first year showing strong improvements in emission efficiency, but subsequent accelerated reliability testing revealed a significant and unexpected degradation in emission with time. Since the resulting LED luminaire prototype will require increased reliability and lifetime compared to current technology in order to offset the higher anticipated initial cost, the decision was made to increase work towards improving the robustness of the array design (Task 2), while de-emphasizing or postponing to a later stage in the contract of improvements in chip efficiency (Task 1).

Year 1 Results

During the first year of project, the improvement of small-area LED chip efficiency through chip geometry encompasses a very wide variety of possible alternative designs. In order to minimize the number of experiments and focus on the approaches that show the most promise, a software model was developed in the form of a macro module for a commercially available optical modeling software suite. The developed module includes a flexible chip model, the geometry, design, and material properties of which may be modified simply through the definition of a set of parameters. Also included in the module are a number of standard packages to be used for characterizing the optical output (i.e., output intensity and color as a function of viewing angle). During the course of this project, the model was continually refined and developed, with the intent of using the model as a predictive tool to both improve understanding of the factors limiting small-area chip performance and to provide a guide to determining the optimum approaches for improving light output and color uniformity.

Also during the first year of project, a "blank" LED wafer segment was obtained which contains fabricated LED active layers and contact metals but has not yet been singulated into individual LED chips. It is intended that this wafer segment will be used in the fabrication of small-area LED chips to provide a quantitative determination of the light-enhancement approaches developed and identified through the optical modeling module.

As described in the challenge section, a key goal of this project is to improve LED chip efficiency and develop new chip geometries that increase compatibility with manufacturable array designs with uniform pre-defined light emission using simplified optics. Towards this

goal, a software modeling tool was developed to simulate various chip geometries and evaluate the resulting efficiency / emission characteristics to determine the most promising approaches for further investigation. During the first project year, the initial model was developed and compared to measured data, and the capability for modeling scattering / downconverting layers was added.

As model development progressed, a number of refinements were added to the model. A new user interface has been created which simplifies selection of various model parameters, reducing the time necessary to set up the model and enhancing the traceability of the various parameters (materials, simulation parameters, model components, chip geometries, etc.) as the model is modified and varied. Using this interface, a systematic series of simulations was conducted to investigate the effect of one of the critical optical parameters relating to quantum well emission layers inside the LED chip. This parameter, referred to hereafter as the "Emission Parameter", was found to have a significant effect on both the efficiency of light extraction (i.e., how many of the light rays generated inside the LED actually escape from the chip) and the resulting emission pattern from the LED as a function of viewing angle. By selecting an optimum value for this parameter, an improved fit was obtained between the simulated chip emission pattern and that measured for actual LED devices.

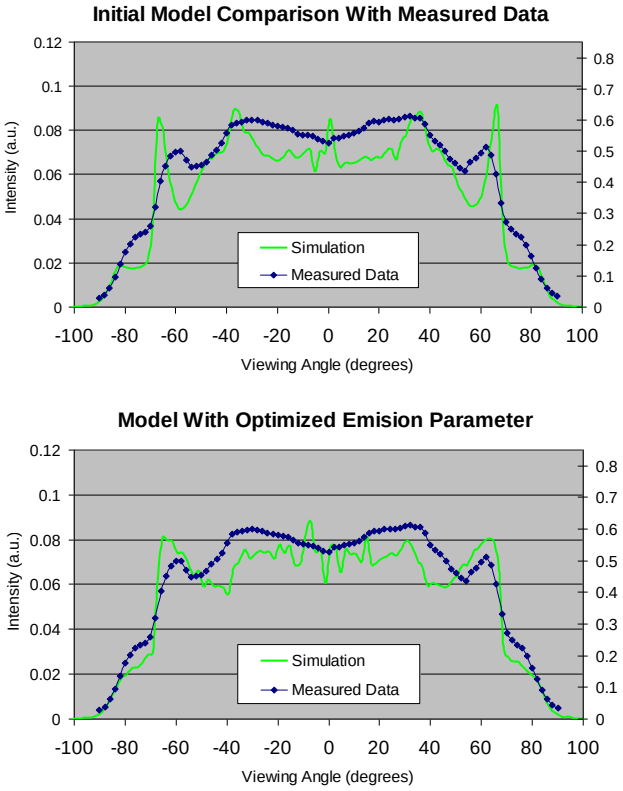


Figure 1.3. Improvement in model fit attained through optimization of the "Emission Parameter".

Figure 1.3 shows a comparison of the fit obtained with the new optimized Emission Parameter, compared to that described previously in the report. This improved fit should allow more accurate simulation of various chip geometries and a better prediction of how various chip geometries may be placed in an array to produce the desired beam profile characteristics with minimal optics. Figure 1.4 shows the simulated correlation between the Emission

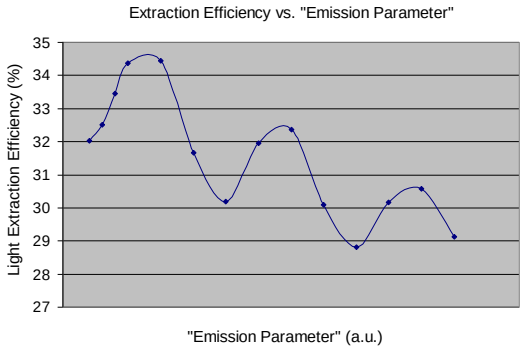


Figure 1.4. Simulated extraction efficiency vs. "Emission Parameter" describing periodic optimum extraction points.

Parameter and LED chip light extraction efficiency. This correlation gives insight into the relationship between the Emission Parameter (which may be controlled by varying specific LED device layers) and the chip geometry (which may be controlled by varying the shape of the resulting LED chip). This insight was used in optimizing both the light extraction efficiency from the chip (and hence the most efficient light output) and the angular distribution of the emitted light.

Year 2 Results

During the second project year, the computer model developed during the first project year was further refined, and additional capabilities were added to allow the modeling of downconverting / scattering materials distributed in the vicinity of the LED chip. The specific goal of the new model developments was to allow the simulation of a range of chip / downconverter combinations and geometries to provide insight into the fundamental mechanisms effecting uniformity and efficiency and identify promising new approaches to be subsequently fabricated and tested in actual LED arrays. It was intended that the refined approaches would be applicable to the fabrication of high-efficiency LED arrays with uniform white emission as a function of viewing angle – one of the primary requirements for a successful LED-based luminaire design.

At end of first year of project, the works were re-assigned to focus on Task 2. Therefore, the improvement of LED array performance will be assessed as LED chip performance since LED arrays will deliver the luminaire performance ultimately. During the second year of project, Cree has made progress on the chip efficiency through research outside this project. Cree has successfully produced a new LED chip family with the highest efficiency to date. The EZBright^{TM} product line contains both small and large chip products (see appendix). As indicated in the reports, we moved to this EZBright chip design to take advantage of the improved chip efficiency in the LED arrays. The other benefit with this design is that the efficiency scales from small chip to big chip, which was not the case in our previous chip design. With this benefit, we can take advantage of a high efficiency chip and optimize the size for the array design without reducing the chip efficiency. These EZBright LED chips combined with a cool white downconversion phosphor in our standard package can produce up to 95 lumens at 350mA.

Year 3 Results

During the final year of project, we obtained LED chips with improved light output efficiency from Cree and demonstrated the performance of 1275 lumens cool white light output at 114.2 lm/W at CCT of 6000^{o}K and CRI of 73; and 1156 lumens warm white light output at 76.5 lm/W at CCT of 2800^{o}K and CRI of 82 from an integrated luminaire prototype without reflector attached. Though the efficacy of 76.5 lm/W from warm white light luminaire prototype is short of our project goal, the efficacy of 114.2 lm/W from cool white light luminaire exceeds our project goal obviously. Still, this is an outstanding progress to exceed project goal of 100 lm/W light emission efficiency in cool white light luminaire prototype to date.

SECTION 2
TASK 2 – MONOLITHIC AND DISTRIBUTED LED ARRAY DESIGN

CHALLENGES

Intrinsic to the integrated LED luminaire design is the development of efficient, low cost arrays of multiple small-area LED chips. This challenge encompasses a range of interrelated issues including optical, thermal and electrical design considerations. The close interrelation between thermal and optical design constraints may be illustrated by considering a base prototype luminaire utilizing multiple LED chips and occupying a BR/PAR 30 –style footprint (Fig. 2.1 (a)). The BR/PAR 30 form factor specifies a 3.75" (95.25mm) output diameter. To meet the largest possible number of potential applications the resulting beam angle should allow a range from around 10 degrees (spot applications) to up to 40 degrees (flood illumination) without significant modification of the luminaire design. From a purely optical standpoint, the requirement for beam divergence as low as 10 degrees constrains the maximum effective size of the light emitting region – which in this case is comprised of an array of LED chips – to a diameter of just over 1 cm for a BR/PAR 30 lamp. Therefore, to achieve the narrowest desired beam profiles, it is necessary to place the LED chips a close together as possible.

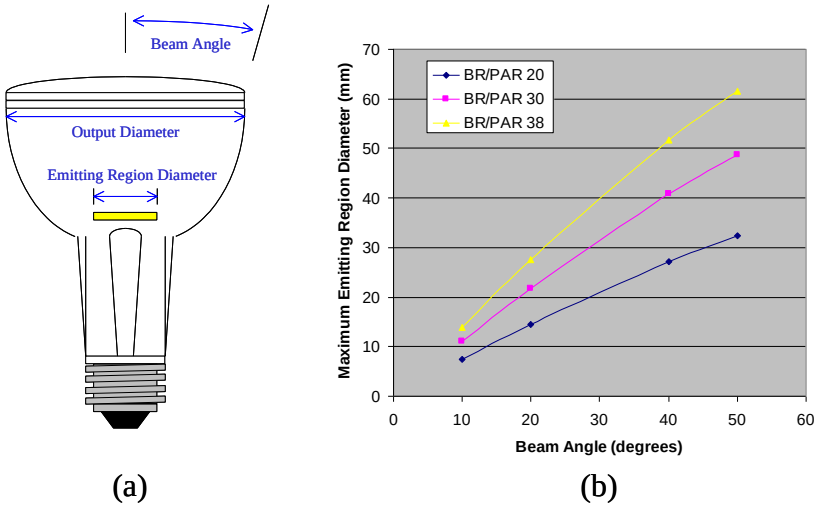


Figure 2.1. (a) schematic of a BR/PAR-style lamp (b) plot of the approximate maximum light emitting region diameter (assuming circular source) allowed as a function of required beam angle for various BR/PAR-style lamps.

In contrast, from a thermal design standpoint, close spacing of the multiple LED chips on a heat sink is generally undesirable in that closer spacing of heat sources results in increased thermal spreading resistance. Preliminary thermal modeling conducted at Cree SBTC has indicated that the penalty paid for closely spaced arrays can be significant. A summary of these simulations is shown in Figure 2.2. For this simulation, a distributed array in which 900 μm^2 LED chips are in close thermal contact with copper heat spreaders of varying thickness and diameter is compared to a monolithic chip distribution where the LED chips are closely grouped on a submount placed on a single heat spreader of varying diameter and thickness. As can be seen in Figure 2.2(b), the thickness of the heat spreader has little impact on the simulated thermal resistance, as does the presence or absence of the submount in the case of the monolithic array. However, over the full range of spreader diameters investigated, the distributed approach yielded significantly lower thermal resistance over the full range of heat spreader diameters. This difference in thermal resistance between the two approaches, which

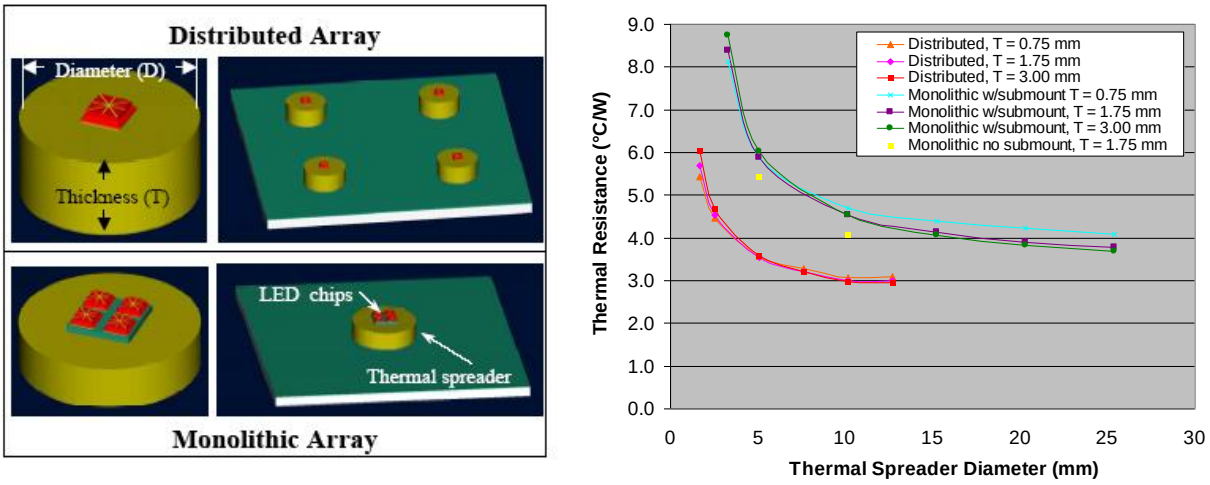


Figure 2.2. Thermal modeling simulation illustrating the reduction in thermal resistance possible using a distributed LED array approach compared to a monolithic array.

can be greater than a factor of two for smaller heat spreaders, is attributed primarily to thermal spreading resistance associated with closely spaced chips. Thus, fundamental trade-offs can and do exist between thermal and optical design considerations for LED-based luminaires. This is further complicated by design aspects addressing the manufacturability and cost of the final product. The project effort will seek to optimize these interrelated issues through a coordinated approach to design innovation that simultaneously considers thermal, optical, and cost factors.

LED array optical and thermal design development

The optical design constraints placed on the size of the LED array by the desired output beam profile, as described above, apply specifically to an array of individual LEDs with no specific additional optical elements. However, it is possible to circumvent the described trade-off between thermal and optical requirements by associating an optical focusing element with

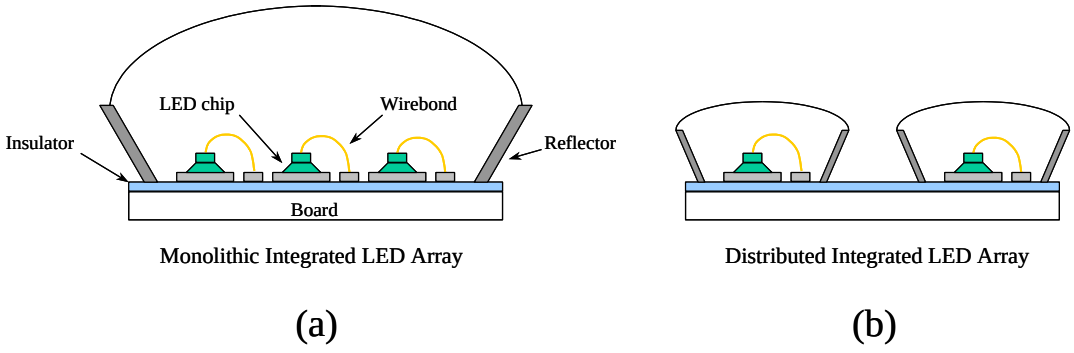


Figure 2.3. Schematic showing examples of (a) a monolithic LED array and (b) a distributed LED array.

each LED (or small groups of LEDs) in the array. Therefore, in the proposed effort, two separate LED array design approaches will be investigated (Fig. 2.3.). In the monolithic array approach, the individual LED die will share a common optic and thus be constrained by the

dimensional requirements imposed by the required beam divergence. In the distributed array approach, individual or small groups of LEDs will have their own associated optical element which will serve to form the emission profile to meet the desired beam profile, thereby allowing greater spacing between LED elements and facilitating thermal spreading and dissipation. When examined closely, luminaires utilizing the distributed array approach would appear to consist of multiple individual light sources within the luminaire. However, in the far field the resulting beam spread and pattern would be indistinguishable from that of the monolithic array-based luminaire. Critical factors in comparing the two approaches include the trade-off between thermal benefit and any additional associated cost of the optical elements. Designs will be considered which seek to minimize the potential cost of such elements, including approaches such as molding arrays of optical elements for the distributed array into a single piece.

LED array electrical and power handling design and development

Full development of novel, high efficiency LED power handling electronic elements is beyond the scope of this project. Rather, the proposed luminaire design will utilize commercially available power handling and conditioning elements where available. Specifically, the design will seek to minimize the complexity of the necessary power handling elements through consideration and design of parameters such as operating voltage / current. Such elements will be incorporated directly into the luminaire.

Separate from the issue of power handling for the luminaire is the electrical outlay of the LED array. Specifically, when dealing with a large array of LED chips, it is necessary to provide electrical contact to each element in the prescribed fashion as dictated by the requirements of operating voltage and current, number and operating voltage of the LED chips, manufacturing constraints, and luminaire lifetime (e.g., how the luminaire reacts to failure of a single chip in the array). To limit the necessary voltage of the luminaire to reasonable (e.g., line-level) voltages with minimum current requirements (to minimize cost of the power handling elements), it is necessary to arrange electrically the LEDs in a combination of series and parallel contact configurations.

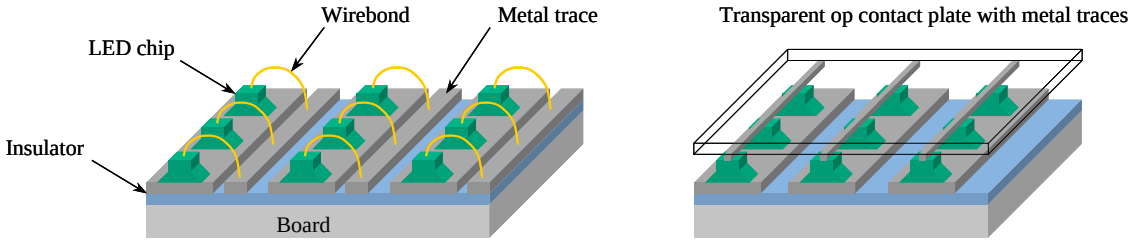


Figure 2.4. Simplified schematic showing (a) a monolithic LED array with conventional die attach and wirebond contacts (b) an alternative approach to providing electrical contact to arrays of LEDs utilizing a transparent top contact plate with metal traces.

Typical methods for providing electrical contact to LED chips include a combination of solder reflow processes and wire-bond contact. Purely reflowed (flip-chip) techniques have been employed in products utilizing "lateral chip" LEDs (both contacts on the same side of the chip). However, due to the associated reduction in thermal contact area (leading to increased thermal resistance) and increased complexity of such configurations, only "vertical chip"

(electrical contacts on opposing sides of the LED) approaches will be considered for the proposed luminaire array.

Solder reflow and wirebond methods have been well developed in the electronics industry, and hence multiple wirebond contacts to an array of LED chips is not viewed as a fundamental limiting factor in either array cost, manufacturability, or lifetime (robustness). However, alternative novel design approaches will also be considered to further reduce array (and hence overall luminaire) cost.

The efforts were focused to investigate various approaches for inexpensive, high-yield LED array fabrication. The more traditional approaches will focus on solder reflow combined with wirebond to achieve the desired configuration of parallel and series elements (Fig. 2.4.a). Alternative approaches will include investigation of an integrated top contact element (Fig. 2.4.b). In one embodiment of this approach an optically transparent 'contact plate' or fixture containing associated metal traces would be attached to the array using a solder reflow process, essentially providing top contacts to each chip all at one time in a single reflow step. The top plate could be fabricated at low cost from glass, with metal traces applied using standard, well-established lithographic processes. This approach, which is best suited for the monolithic array approach described above, could allow additional thermal and optical/converter advantages. For example, if the contact plate could be made with thermally conducting materials, significantly improved heat sinking would be achieved in that heat removal would be possible from both sides of the chip, thereby reducing junction temperature and increasing emission efficiency and chip lifetime. Such approaches are most promising for SiC-based LEDs such as those manufactured by Cree due to the high thermal conductivity of SiC. Additionally, the 'contact plate' could be pre-fabricated to incorporate phosphor conversion material, allowing improved emission uniformity and further simplifying the manufacturing process.

RESULTS AND DISCUSSIONS

Year 1 Results

The successful development of high-efficiency, robust small-area LED arrays is a prerequisite for the achievement of LED-based luminaires for commercial applications. As a first step towards this goal, a set of 2-inch square prototype arrays were designed, fabricated, and tested during the first year of project. As illustrated in Figure 2.5, each array consisted of a set of 20 LED elements arranged in a grid pattern, with associated electrical contacts, downconverter material (to produce white light), and rudimentary optics for each element (e.g., a distributed array design – in contrast to a monolithic array design in which all LED elements share a single optic). In order to compare the efficiencies at cool-white (~6000 Kelvin) and warm-white (~3000 Kelvin) color temperatures, some arrays were fabricated using standard Ce:YAG phosphor and some were fabricated using warm-white phosphor materials (investigated and reported on during previous contract periods). Large-area LED chips were

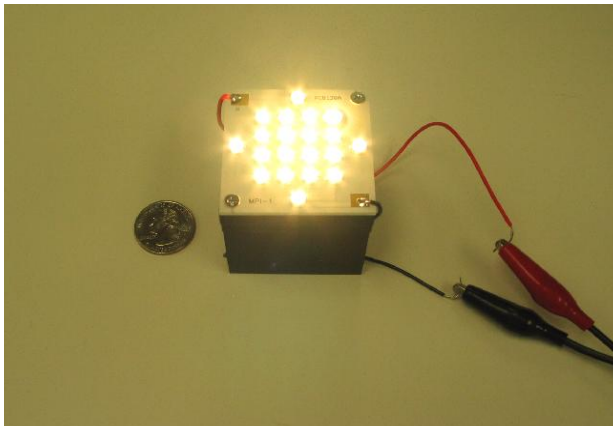


Figure 2.5. Example of a prototype LED array with 20 individual array elements.

used to minimize the number of array elements required for the initial high-output array prototyping development. As the array element design is further refined, a transition will be made to larger numbers of elements containing small-area LED emitters in order to achieve the highest possible output efficiency and thermal dissipation.

Fabrication of the arrays utilized standard manufacturing tools and processes. Following fabrication, the arrays were tested in an integrating sphere to determine the total luminous output, color point, etc. Table 2.1 summarizes the measured properties of the better-performing

Table 2.1. Measured performance for prototype arrays.

Table 2.1.	Current	Voltage	Chromaticity		Lumens	CCT	Efficacy	Color rendering
	(mA)	(V)	x	y	(Lum)	(K)	(Lum/W)	(CRI)
Cool White Array	350	64	0.328	0.350	730	5850	32.6	78.3
Warm White Array	350	64	0.439	0.403	418	2950	18.7	76.6

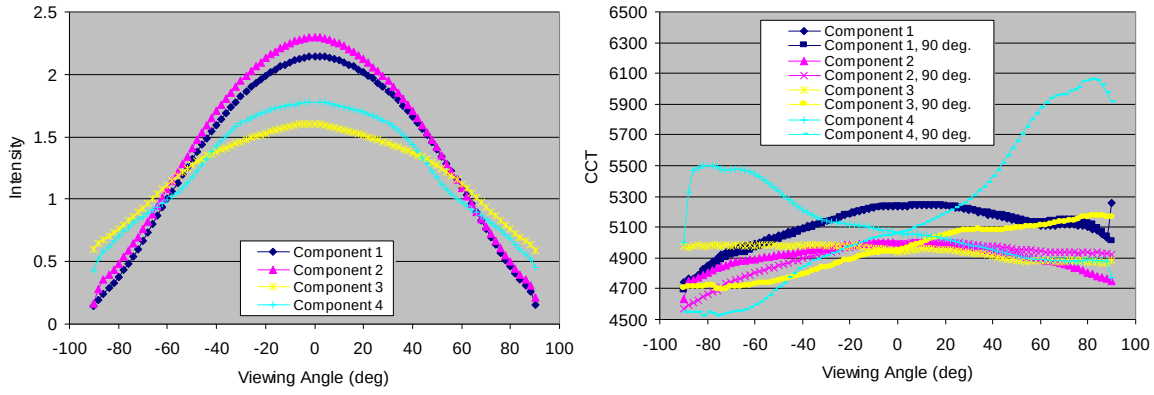
arrays operating at the ~6000K and ~3000K color points.

Operating at a current of 350 mA and a voltage of 64 V, the cool-white array yielded an optical output of 730 lumens, while the output for the warm-white array was significantly lower at 418. This difference is not unexpected due to the high Stokes shift (energy loss) inherent in converting blue light to lower energy red light, and relative immaturity of the phosphor technology currently used to produce the warmer color temperatures. However, based on the output flux specifications of the LED chips used to make the arrays, the resulting luminous output for both the cooler and warmer white arrays was significantly lower than expected. Subsequent testing and analysis of the parts and the processes used to fabricate the arrays resulted in the identification of a number of processing-related issues which resulted in the loss of light output from the individual array elements. Correction of these issues is currently underway in order to improve the overall array output efficiency.

Based on the output flux specifications of the LED chips used to make the initial prototype arrays, the observed output flux values were significantly lower than expected. During subsequent contract periods, the cause for the reduced power output was correlated to a specific processing step (one commonly used in electronic fabrication) that was having a detrimental effect on the output efficiency of the LED chip. Through the process of elimination, specific package materials and aspects of array element geometry were found to be incompatible with the process step and a possible physical mechanism for the observed light reduction was developed. Experimentation showed that this process step cannot be eliminated completely, and further work is underway to identify alternative processes or process parameters to minimize the observed reduction in light output.

The fabrication and testing of the prototype array also allowed an opportunity to identify a variety of design issues related to the efficiency, manufacturability, and reliability of the arrays for use in high-output luminaires. To address these issues, focus was placed on improving the individual array elements. Fifteen new element designs were developed and the associated piece-parts submitted for fabrication.

Figure 2.6 shows an example of the measured light emission characteristics for array elements fabricated using four different design approaches to one of the key array element

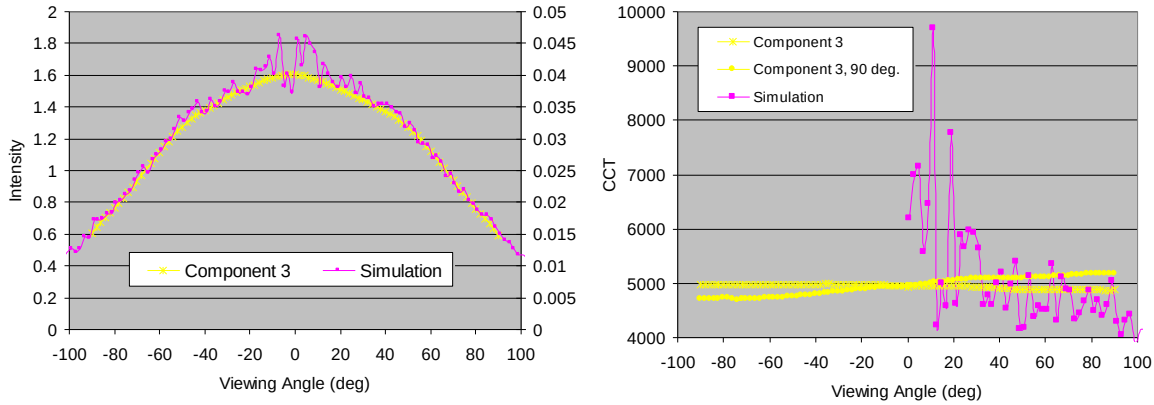


(a) (b)

Figure 2.6. Measured optical beam output profile for four different component array element designs.

components (designated Components 1,2,3 and 4 in the figure). As can be seen in Fig. 2.6 (a), each approach yields a significantly different angular dependent beam intensity profile. Differences in this profile will impact the design and efficiency of the optical elements to be used with the luminaire array. Figure 2.6(b) shows the corresponding color uniformity measured in terms of correlated color temperature (CCT) as a function of viewing angle. For each sample, two measurements were taken along perpendicular azimuths (90 degrees apart) to check for symmetry. As can be seen in the figure, significant differences were observed for both uniformity as a function of viewing angle and symmetry. However, in general, the uniformity was good for three of the four designs.

Figure 2.7 shows the optical modeling results for the case of Component 3. As can be seen in the figure, close agreement was achieved between simulated and measured optical beam



(a) (b)

Figure 2.7. Comparison of measured and optical modeling results, Component 3.

intensity profiles. However, further refinement is necessary to improve the agreement between the measured and observed color uniformity.

Initial characterization was conducted to compare the optical and thermal efficiency of each of the fifteen new array design approaches. However, this characterization was not used to eliminate specific approaches since past experience has shown that initial performance is not generally an adequate predictor of reliability or lifetime performance. That is, for the final commercial array product, the performance over time (degradation, etc.) is generally as important to the customer as initial performance. Our past experience in the development of LED-based lamp packages has shown that lumen maintenance over time is a critical issue for LED-based lighting approaches. Therefore emphasis was placed on reliability as well as initial performance.

To assess the reliability of each approach, sample sets were fabricated and divided into sub-groups for accelerated environmental testing. The tests that were chosen are as follows:

1) Wet high-temperature operating life (WHTOL)
2) High-temperature operating life (HTOL)
3) Wet high-temperature reverse-bias (WHTRB)
4) Thermal shock (TS)
5) Mechanical shock (MS)
6) Salt (SALT)
7) Variable vibration (VV)

These standard reliability tests were chosen to investigate the behavior of each approach under 'accelerated' environmental conditions.

Each of the array element approaches was found to yield different light output, thermal, optical, etc. advantages and drawbacks, and each approach had specific processing requirements which impact the overall cost of the element, and hence the array and the luminaire into which the array was to be placed. In addition to cost, manufacturability, and performance, the reliability of each approach under accelerated testing intended to simulate real-life operation over extended periods provided a critical criteria for selecting between the various approaches.

In general, it was found that each approach tested displayed, in general, a significant reduction in light output over time when subjected to WHTOL and HTOL testing. In contrast,

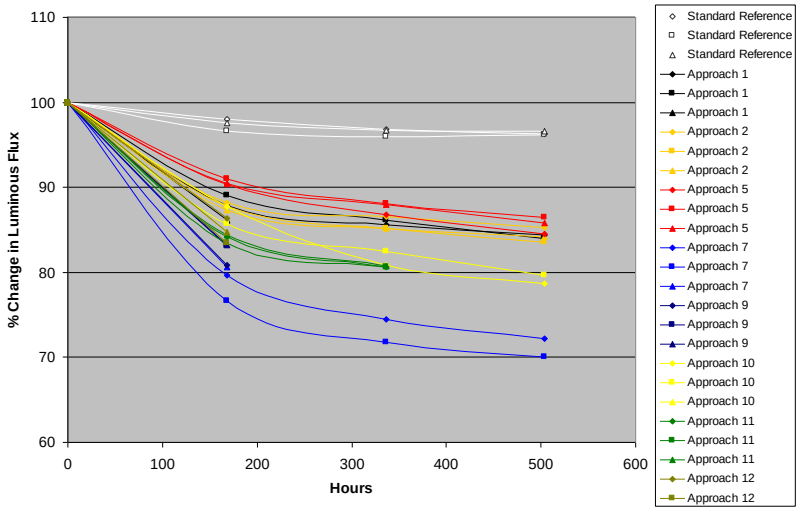


Figure 2.8. Percent change in luminous flux observed during WHTOL testing of various array element approaches.

samples exposed to WHTRB testing did not show a corresponding decrease in light output. Figure 2.8 shows the observed light output reduction for a number of approaches exposed to WHTOL testing conditions. Each curve in the plot corresponds to an average value obtained for up to 10 individual array elements, and up to three such sets were tested for each approach. Also included for reference are data from a "standard" sample having 5-20% reduced light output (compared to the various array element approaches) but a combination of materials and parts that are known to withstand extended testing at the product level. As can be seen in the plot, each of the approaches shown displays a significant reduction in light output over time. Failure analysis is currently underway to determine the origin of the light output decrease in order to begin correcting the various issues. A number of other failure mechanisms were discovered during TS testing of the array elements, resulting in 'open circuit' failures. These failures are also under investigation to determine the origin of the problem.

In addition to array element reliability testing, a second prototype full array was fabricated based on a similar element design incorporated in previous array demonstration. The intent of the array fabrication was to demonstrate an expected improvement in light output (prior to reliability testing) due to advances in the array fabrication process developed during previous months. However, this array resulted in an output of only 640 lumens, or 29 lumens per watt, at a correlated color temperature (CCT) of 5100 Kelvin. This compares with the previous 'best result' of 730 lumens at an efficacy of 33 lum/W at a CCT of 5850 Kelvin. It was discovered that the improved processing had, by mistake, not been implemented during the second array build. This error was corrected, allowing the fabrication of a third prototype array displaying a luminous efficacy of 54 lumens per watt, or a 65% increase over previous results (Table 2.2). The resulting array produced 1285 lumens at approximately 24 watts. For

Table 2.2. Measured performance for prototype array fabricated.

Table 2.2.	Current	Voltage	Chromaticity		Lumens	CCT	Efficacy	Color rendering
	(mA)	(V)	x	y	(Lum)	(K)	(Lum/W)	(CRI)
Cool White Array (2)	350	68	0.332	0.367	1285	5550	54.0	78.5

comparison, a typical standard 60W light bulb produces only 825 lumens with an efficacy of only ~14 lumens per watt!

It should be noted that, along with the process change mentioned above, the array fabricated during the present contract period incorporated a number of design changes that have been developed during recent months, which may have added to the increased performance. Also, the array performance has been tested using an integrating sphere that has been calibrated for small light sources (e.g., individual array elements). As a result, the absolute array efficacy reported herein may contain inaccuracies and we are currently investigating alternative measurement set-ups to verify absolute efficacy. However, relative improvements, such as those observed, should be accurate. It should also be noted that the arrays fabricated to date have utilized large-area (900 micron square) LED chips. As the contract progresses, a transition will be made to small-area LEDs with the goal of further improving array performance.

While these results are encouraging, a high-efficacy array is useful in a commercial luminaire only if the array can demonstrate sufficient lifetime and stability with respect to environmental degradation. The investigation of the reliability of different array element approaches as outlined in previous contract reports (some of which were utilized in the fabrication of the prototype array described above) has indicated that substantial challenges

remain regarding the operating lifetime of the individual elements comprising the array. Specifically, many of the material combinations and design features implemented in the fabrication of the prototype array have shown degradation when exposed to accelerated lifetime testing including thermal shock, wet high-temperature operating life (WHTOL) and high-temperature operating life (HTOL) testing.

Issues of array element stability and lifetime have been a primary focus of the recent contract effort and will remain so until suitable design solutions are obtained. Accordingly, accelerated lifetime testing continued on the 15 separate array element designs developed during recent months, along with detailed inspection and failure analysis. Based on the preliminary results of this analysis, a new design concept has been developed encompassing (at present) three primary variations. Piece-part designs have been submitted for fabrication, and upon receipt will be assembled into array elements and tested for luminous efficacy, angle-dependent emission properties, and reliability.

Year 2 Results

At the end of first year of prject, LED array prototypes were fabricated utilizing standard manufacturing tools and processes. Table 2.3 summarizes the measured properties of the LED arrays operating at the ~6000K and ~3000K coordinated color temperature (CCT). Operating at a current of 350 mA, the cool-white LED array prototype displayed a luminous efficacy of 54 lm/W and produced 1285 lumens at approximately 24W. The warm-white array prototype resulted in a luminous efficacy of 25 lm/W and yielded 558 lumens at approximately 22W. This difference in the luminous efficacy and luminous flux between the two color temperatures is not unexpected due to the high Stokes shift (energy loss) inherent in converting blue light to lower energy red light, and relative immaturity of the phosphor technology currently used to produce the warmer color temperatures.

Table 2.3. Measured performance for prototype arrays.

Year 1	Current	Voltage	Chromaticity		Lumens	CCT	Efficacy	Color rendering
	(mA)	(V)	x	y	(Lum)	(K)	(Lum/W)	(CRI)
Cool White Array	350	68	0.332	0.367	1285	5550	54.0	78.5
Warm White Array	350	64	0.407	0.385	558	3375	25.0	76.6

During the second year of project, the goal was to improve the array efficiency to 80lm/W. The first step was to use more efficient chips. As mentioned in Task 1, we incorporated our new EZBright power LED chip into the LED array elements. The EZBright LED features a proprietary optical design that delivers an optimal Lambertian radiation pattern, reducing emission losses and significantly increasing efficiency. Due to the configuration of EZBright LED chip, we had to adjust our assembly process to fit this chip into our new LED array element design. Specifically, we focused on the following steps of assembly process – pick and place, die attach and wire bonding.

Our previous experience in the development of LED-based lamp packages has shown that lumen maintenance over time is a critical issue for LED-based lighting approaches. We have seen that initial performance is not generally an adequate predictor of reliability or lifetime performance. In brief, we found that improper selection of materials in close proximity to the LED chip would lead to degradation during reliability testing and negatively impact the final performance of the array. Therefore emphasis was placed on reliability as well as initial performance during Year 2. We continued our evaluation of alternative materials for placement in close proximity to the LED chip in this second year to ensure that they would not degrade and reduce the light output after reliability testing.

Figure 2.9. Percent change in luminous flux observed during WHTOL testing of various alternative materials in the array elements.

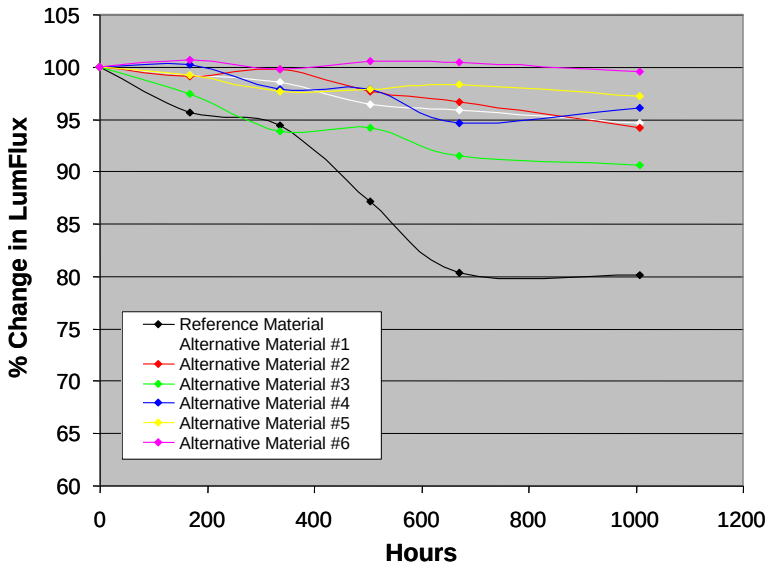


Figure 2.9 shows the observed light output reduction for the various alternative materials exposed to WHTOL testing conditions (high temperature and humidity conditions). Each curve in the plot corresponds to an average value obtained for up to 10 individual array elements. Also, included for reference are data from a "standard material" having 5-20% reduced light output, but a combination of materials and parts that are know to withstand extended testing at the product level. As it can be seen in the plot, the most of the alternative materials exhibit a significant reduction in the light output over time. This was the status in the early part of the second year. As the year progressed we have been able to identify materials that exhibited less than a 5% light output reduction from the LEDs under stressed conditions (WHTOL) up to 1000 hours.

An LED array prototype was fabricated incorporating the new alternative materials with improved lifetime as well as a number of array design changes. Table 2.4 summarizes the array performance. The cool white LED array prototype yielded a luminous efficacy of 78.6 lm/W at

Table 2.4. Measured performance for prototype arrays.

Year 2	Current	Voltage	Chromaticity		Lumens	CCT	Efficacy	Color rendering
	(mA)	(V)	x	y	(Lum)	(K)	(Lum/W)	(CRI)
Cool White Array	350	22	0.326	0.358	601	5850	78.6	80.1
Warm White Array	350	22	0.401	0.347	424	3225	55.4	65.2

350 mA and a correlated color temperature of 5850K, representing a 45% improvement over previous array results. The resulting array prototype produced 601 lumens at approximately

8W. The warm-white array prototype resulted in a luminous efficacy of 55.4 lm/W and yielded 424 lumens at approximately 8W. These arrays utilized large-area LED chips (~ 1000 μm^2). Large-area LED chips were used in this array prototype to minimize the number of array elements required for the initial high-output array prototyping development. As the array element design is further refined, a transition in Year 3 will be made to the optimum chip in order to achieve the highest possible output efficiency and thermal dissipation.

Year 3 Results

During the final year of project, we successfully fabricated a new cool white LED array prototype that yielded a luminous efficacy of 95.3 lumens/watt at 350 mA and a correlated color temperature of 5850°K – representing a 21% improvement over previous array results. The resulting array prototype produces 800 lumens at approximately 8 watts. Based on the same design, we fabricated a new warm white LED array prototype that yield a luminous efficacy of 67.3 lumens/watt at 350 mA and a correlated color temperature of 2825°K. The resulting array prototype produces 529 lumens at approximately 7.7 watts. Table 2.5 summarizes the array performance below. It should be noted that the array fabricated during the final year of project incorporated a number of design changes that have been developed through the entire project period.

Table 2.5. Measured performance for prototype arrays.

Year 3	Current	Voltage	Chromaticity		Lumens	CCT	Efficacy	Color rendering
	(mA)	(V)	x	y	(Lum)	(K)	(Lum/W)	(CRI)
Cool White Array	350	24	0.325	0.354	800	5850	95.3	79.3
Warm White Array	350	22	0.449	0.406	529	2825	67.3	80.5

The progress of array performance through the entire project period is summarized in the Figure 2.10. As shown in Fig. 2.10, the progress of array performance of cool white light output from small area arrays follows the task goals of this project very closely, while the output for the warm-white array was significantly lower. This difference in the luminous efficacy and luminous flux between the two color temperatures is not unexpected due to the high Stokes shift (energy loss) inherent in converting blue light to lower energy red light, and relative immaturity

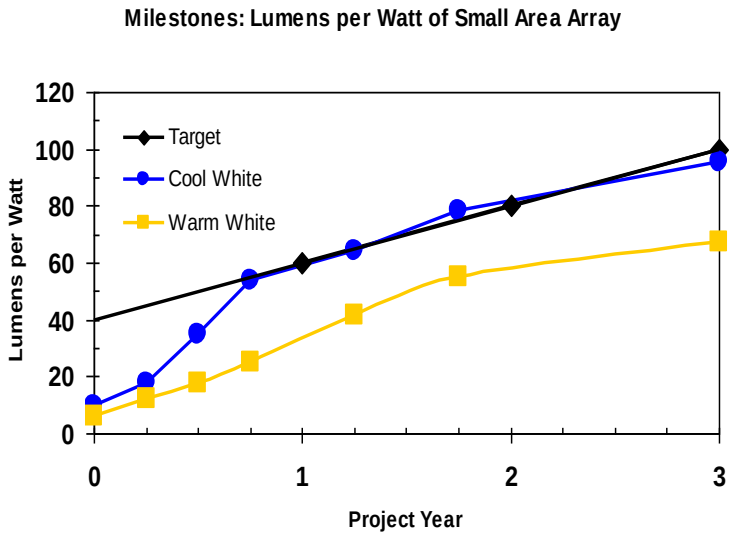
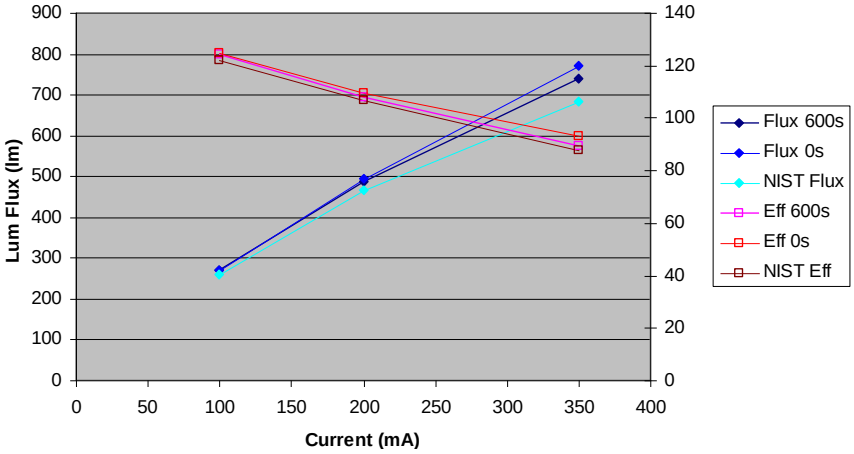


Figure 2.10. Lumens per Watt as a function of project years.

of the phosphor technology currently used to produce the warmer color temperatures.

Figure 2. 11. Comparison of luminous flux and efficacy as a function of drive current for the array prototype measured at Cree (quasi-steady state and steady-state) and an NIST (steady state).



During the final year of project, a cool white LED array prototype was mounted to a heat sink for verification testing with NIST. The array prototype was measured at three different currents – 100, 200 and 350mA – at NIST and also at Cree at steady state. The three different current levels help explain the different heating effects seen in the

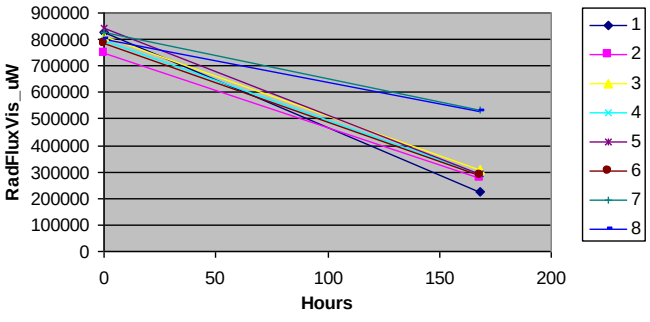
Table 2.5. Measured performance for the prototype array mounted on a heat sink measured at steady state (10-minute hold) at Cree and at NIST.

Table 1.	Current	Voltage	Chromaticity		Lumens	CCT	Efficacy	Color Rendering
	(mA)	(V)	x	y	(Lum)	(^{o}K)	(Lum/W)	(CRI)
Array at Cree	350	23.6	0.322	0.353	738	5950	89.3	80.2
Array at NIST	350		0.321	0.351	684	5995	87.9	76.9

sphere measurements between Cree and NIST. Figure 2.11 shows a plot of the luminous flux and efficacy of the array measured at Cree and at NIST as a function of current. As expected from the testing configurations of the Cree and NIST spheres, there are more heating effects present in the NIST measurement, which is seen by the increasing divergence of the luminous flux at higher current levels. At low currents of 100 mA there is good agreement between the measurements. The lower flux at higher currents in the NIST sphere is attributed to the heating effects. As the current increases to 350, the heating effecting in the NIST sphere is greater due to the sample mounting configuration and results in a lower flux than at Cree. Table 2.5 shows the results for the steady state measurement for the array prototype at Cree and at NIST. For the steady state testing condition with a 10 minute hold, the array on a heat sink yielded a luminous flux of 738 lumens and efficacy of 89.3 lumens/watt at 350 mA and a correlated color temperature of 5950^{o}K when measured at Cree. The same array measures a luminous flux of 684 lumens and efficacy of 87.9 lumens/watt at 350 mA and a correlated color temperature of 5995^{o}K when measured at NIST. The discrepancy in flux is 7%, of which 4% is attributed to the heating effect in the NIST sphere compared to Cree's configuration. The efficacy is 1.5% lower in the NIST measurement at all currents compared to the Cree measurement (10-minute hold). The difference in efficacy is a smaller percentage than luminous flux, which is likely due the voltage dropping slightly with the heating of the array. Since NIST did not certify the voltage performance this cannot be confirmed but is a logical conclusion.

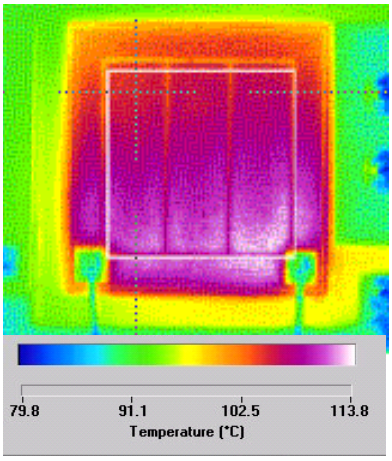
Also, we continued our investigation of the reliability performance of the array prototypes through the final year of project, since a high-efficacy array is only useful in a commercial luminaire if the array prototype can demonstrate sufficient lifetime and stability with respect to environmental degradation. For example, several alternative materials around the proximity of the LED chip were evaluated under cycles up to 1000 hours and stressed conditions (high temperature and humidity). We found that the chips were turning dark after 168 hours of testing under stressed conditions. This "charring" of the chip results in serious deterioration of the light output. Figure 2.12 shows the observed light output reduction for the parts exposed to WHTOL testing conditions, with each curve in the plot corresponding to an individual array element. This result shows that charring is a killer for light output with less than 40% lumen maintenance after only 168 hours for most array elements. This is far below the target lumen maintenance of greater than 90% over 1000 hours under stressed conditions.

Figure 2.12. (a) Change in luminous flux observed during WHTOL testing of the array elements due to charring of the LED chip. (b) Optical micrograph of the dark LED chip after 168 hours of WHTOL testing.



We have linked this darkening in the chip to overheating of the chip and the possibility of contaminants incorporated during processing. More thermal imaging of the array elements was performed to assess the whether or not the chip was overheating. Figure 2.13 shows a typical thermal image of an LED chip in operation. Under bias, the chip is heating to over 105°C when the heatsink was kept at a constant temperature of 25°C . Temperatures at this high in the array element can lead to deterioration of some of the materials and thus cause darkening.

Figure 2.13. Thermal imaging of an LED chip under bias.



We have also identified a thermal choke in the array element, which is causing the chip to overheat. Figure 2.14 shows scanning acoustical microscope (SAM) images of the LED chip in the array element. From this technique we can access the quality of our chip

attach to the board. The dark areas indicate a good bond, whereas the light areas are voids. These voids that are seen in the SAM images are a thermal choke since they do not allow good heat dissipation to the board which causes the chip to overheat. At these higher temperatures, we are damaging one of our materials in the array elements leading to the charring. Therefore, we modified our processing conditions to eliminate the voids that act as a thermal choke. While the overheating of the chip remains the likely candidate, it does not exclude the contribution of contaminants to the charring problem. Contaminants or impurities can get trapped in these voids during processing and lead to the deterioration of the materials in the array element during WHTOL testing. In parallel to the development of the aforementioned new improved chip attach process, we developed a second process to combat the charring of LED chips. This second approach has a varied chip attach process and a different alternative material around the proximity of the LED chip. The performance of this second process and material combination was investigated under stressed conditions (high temperature and humidity) and cycles up to 1000 hours. After 1000 hours, no charring was evident on the chips. Although this chip darkening has been a significant set back in our progress, we indeed identified new alternative materials around the proximity of the LED chip with controlled process steps of chip atach to yield an acceptable condition of our new array prototype designs at the end of our project. In Figure 2.15, it is shown that the luminous flux stayed constant during 1000 hours of testing under stressed operation conditions (high temperature and humidity).

Figure 214.. Scanning acoustical microscope images of the LED chip in an array element.

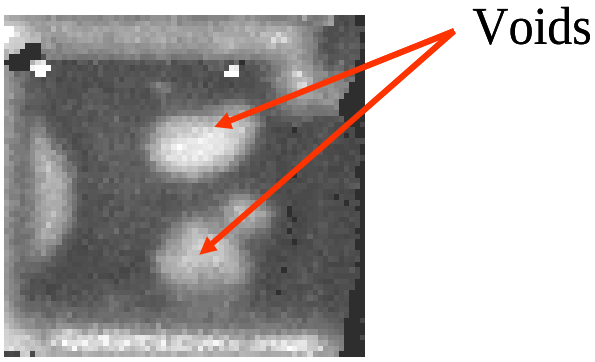
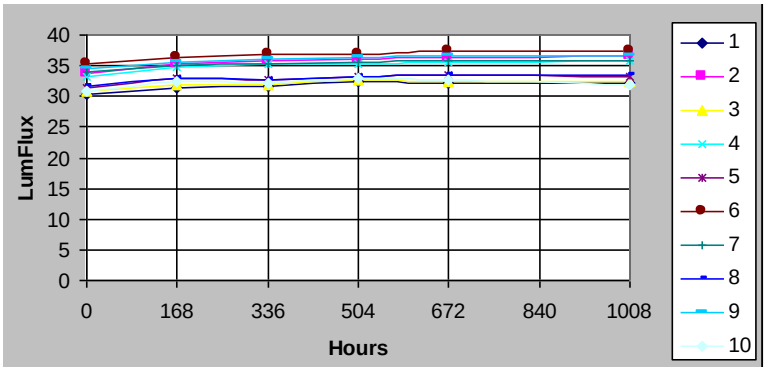


Figure 2.15. Percent change in luminous flux observed during WHTOL testing of various alternative materials in the array elements.



SECTION 3
TASK 3 – EFFECTIVE LED MODULE DESIGN AND THERMAL MANAGEMENT

CHALLENGES

Achieving the current target luminaire output of >1000 lm at an efficacy of 100 lm/W would require an input power of ~10 W. Assuming a (system) wall plug efficiency of 30%, this would require the effective dissipation of ~7W of generated heat to the surrounding

environment. Removing this excess heat is one of the critical issues associated with improving performance and viability of LED-based lighting, since heat build-up leads to increased LED junction temperature and a corresponding decrease in LED efficiency as well as phosphor conversion efficiency. Further, heat flow out of the system should be independent of luminaire orientation, and allow efficient operation in ambient temperatures as high as 85C for recessed ceiling mounted fixtures.

Figure 3.1 shows the measured relative flux for a blue (470 nm) Cree XB900 (900 μm square) LED chip as a function of junction temperature. From the figure it is seen that the output performance of the chip decreases by 20% as the temperature is raised from 25C to 120C. Further, for the case of white LEDs incorporating phosphor downconversion materials, the properties and lifetime of the downconverter can also degrade with increasing temperature. For example, it has also been found[1] that Ce:YAG, a commonly used phosphor for white LED applications, undergoes a color shift and a decrease in quantum efficiency on the order of 80% upon heating from room temperature to 120C. Therefore in the case of solid-state lamps based on white LED technology, it is desirable to keep the temperature of the chip and its surroundings as close to room temperature as possible. However, maximizing the heat dissipation from the chip can result in very large, bulky heat sinks and/or expensive fabrication processes using current technology. Taking the balance of performance and cost into account, an initial target of 5 degrees C/watt (with 7W dissipation) from junction to ambient has been selected for the proposed luminaire. This value would allow chip/junction operation at a reasonable 60C in a room temperature ambient for the proposed luminaire.

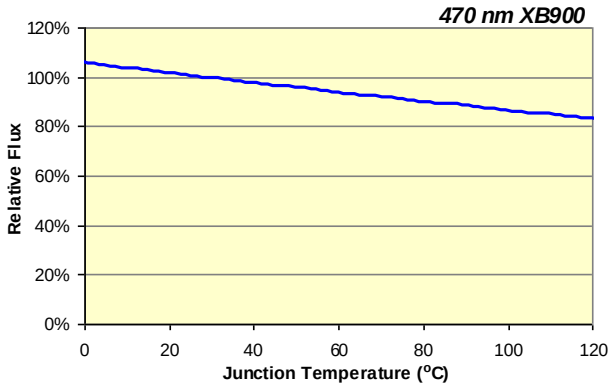


Figure 3.1. Relative flux as a function of LED junction temperature measured for a 900 μm square chip.

In typical state-of-the-art configurations, waste heat must pass through a number of interfaces before reaching the ambient. In general, these stages may be divided into the following parameters: (1) Resistance from junction to package; (2) Resistance from package to heat sink; (3) Resistance from heat sink to air.

Traditionally in proposing generalized LED-based solid-state lighting, the (technologically) favorable configuration with an 'infinite' heat sink is assumed- essentially a very large heat dissipater with active (e.g., electric fan) cooling. In reality, however, additional active cooling using fans, thermoelectric cooling, etc. are not feasible due to the overall loss in system (luminaire) efficiency associated with the power requirements of these methods. Further, from an end-user viewpoint, a noisy, failure-prone fan or 'infinite' (i.e., very large) heat sink are likely to be quite undesirable, leading to limited customer acceptance. Such issues have typically been neglected by LED power package designers by focusing primarily on chip-to-package thermal resistance and leaving package-to-heat sink and heat-sink-to-air to lighting system designers. Lighting system designers, however, typically have little experience in the heat dissipation requirements of LED lamps, as they differ significantly from more traditional fluorescent and filament-based lighting. Not surprisingly, this gap between LED power

packages and current luminaire design has seldom been bridged successfully. It is our belief that, initially, this gap must be addressed, at least initially, by LED power package manufacturers, who have detailed knowledge and experience with the thermal dissipation requirements of LED-based lighting. For this reason, we propose the development of the full luminaire package which includes LEDs sources, phosphor conversion media, appropriate optical output characteristics (beam form and color temperature), and thermal dissipation from chip through ambient. This approach allows an optimized, integrated design which makes the best use of materials and technology, with the goal of achieving a form factor which meets both technical and end-user requirements.

Chip-to-board thermal management

Commercial packages incorporating LEDs typically use either a die-attach (e.g., solder or conductive epoxy) plus wirebond approach or a flip-chip / solder bump approach to attach the die to the package and provide electrical and thermal contact. The flip-chip approach generally significantly reduces the thermal contact area, and the die-attach approach with conductive epoxy typically introduces a thermal barrier between chip and package due to the comparatively low thermal conductivity of conductive epoxies. Therefore the proposed effort will exclusively focus on the use of solder reflow to attach the chip to the luminaire body. Various approaches will be investigated to optimize the thermal resistance of the solder junction between chip and board, including:

- develop lead-free, void free junction between chip and spreader.
- investigate dual sided heat sink approach (heat removal from top and bottom of chip)
- investigate alternative paths for heat removal such as the use of transparent thermal conducting encapsulants around the chip.
- optimize thermal spreading resistance and minimize thermal choke at insulator layer using novel materials such as graphite, carbon nanotubes, thermally conducting insulating layers.

Board-to-heat sink

The proposed luminaire incorporates a LED array in which the LED chips are mounted on an appropriate carrier or board (providing the necessary electrical contact and isolation for each LED chip) which subsequently must be attached with good thermal contact to the body of the LED lamp (which incorporates the main heat sink or heat dissipative elements). Optimization of the junction between the board and heat sink will focus on the nature (smoothness, etc.) of the interface surfaces and the nature (material, process conditions, etc.) of the bonding material. A unified approach will be considered in which the board and heat-sink (lamp body) are fabricated from a single piece (thereby eliminating the junction altogether). To accomplish this, an integral electrical isolation layer is required such that the chips are not all in direct electrical contact. Approaches for achieving this through the use of techniques such as anodization will be investigated, and weighed in terms of performance benefits vs. additional cost of manufacture.

Heat sink-to-ambient

Achieving adequate thermal convection between the LED lamp body, luminaire, and surrounding environment provides one of the greatest challenges in the design of the proposed

luminaire. The thermal resistance between the heat-sink portion of the body and the ambient can be complicated by factors such as orientation, dust accumulation, and the presence of the luminaire enclosure. Optimizing the lamp body design and the luminaire enclosure design must occur together. Preliminary screening of designs will be conducted via thermal modeling that includes convective air flow where possible. Scale models of select approaches will be fabricated and tested to provide iterative feedback.

RESULTS AND DISCUSSION

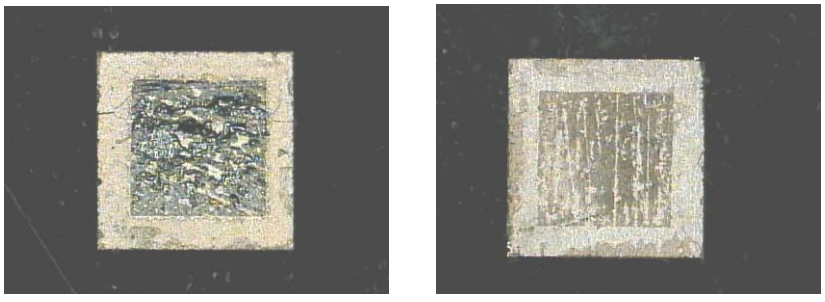
Year 2 Results

Removing the excess heat is one of the critical issues associated with improving performance and viability of LED-based lighting, since heat build-up leads to increased LED junction temperature and a corresponding decrease in LED efficiency and phosphor conversion efficiency. Further, heat flow out of the system should be independent of luminaire orientation, and allow efficient operation in ambient temperatures as high as 85^{o}C for recessed ceiling mounted fixtures. In typical state-of-the-art configurations, waste heat must pass through a number of interfaces before reaching the ambient. In general, these stages may be divided into the following: junction to board and board to ambient.

During the first year of project, the LED array prototype had a measured thermal resistance of 40^{o}C/W from junction to ambient. This was much higher than the targeted value of 20^{o}C/W for Year 1. Due to the requirements for LED chip attachment, electrical and thermal performance, the options of surface finishing of this substrate are limited. A good surface finishing on the substrate is required for a good soldering interface. Of course, a good soldering interface between LED chip and substrate offers an effective heat dissipation to achieve low thermal junction temperature. A poor soldering interface between LED chip and substrate was identified to be the root cause of the unexpected high thermal junction temperature in the first LED array prototype. This interface was a focus of the effort in the second year. We focused our efforts to optimize the soldering process for LED chip attachment by adjusting our soldering equipment for LED chip attachment in the laboratory to monitor process parameters effectively.

By examining the soldering interface and bonding strength of LED chip attachment, we completed a set of experiments to determine the optimum conditions and process parameters for soldering LED chip to substrate. Two types of soldering interface of LED chip attachment after push-off testing are shown in Figure 3.2 below. In Figure 3.2a, a good soldering interface between LED chip and substrate is shown at the

Figure 3.2. The solder attachment of the backside of LED chips after push-off test. (a) The solder coverage is shown in dark color at the center and ~90% area are covered by solder and bonded to substrate during attachment. (b) The solder coverage is shown in light color at the center and ~30% area is covered by solder.



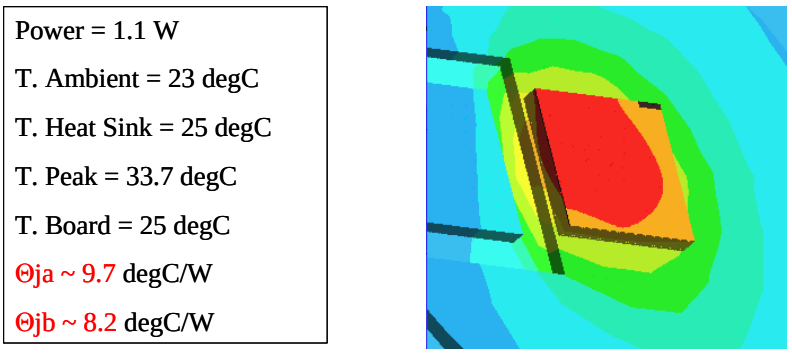
(a) (b)

backside of LED chip after push-off testing. The solder coverage is shown in dark color at the center. Approximately 90% of the area is covered by solder and it is bonded to substrate. In contrast, a poor soldering interface is shown in Figure 3.2b. The solder coverage is shown in light grey color at the center. There is approximately 30% of the area covered by solder therefore the bonding strength between LED chip and substrate is very low. Now that we have realized a good soldering interface (>90% solder coverage) of LED chip attachment to substrate in our process we should see an improvement of the thermal resistance.

The circuit layout was adjusted in the new LED array prototype, which allowed us to achieve uniform and effective heat spreading around each LED chip through thermal modeling. We targeted a junction temperature of ~10°C/W from LED chip to the ambient to meet the goal of this task for Year 2.

Figure 3.3 shows the temperature gradient contour of an array element in the new array prototype. We achieved the junction temperature of 10.1°C/Watt from LED chip to ambient at a constant ambient and board temperature of 25°C through thermal modeling. Specifically, the temperature distributions that are shown in color are very uniform (round shape) around each LED chip. The results from the modeling were compared and validated with the measured thermal performance of the array prototype after fabrication. Using a test unit of new LED array prototype (simplified array with a reduced number of LED chips), we measured a junction temperature of 10.2°C/Watt from LED chip to ambient in the lab. This result indicates that the thermal modeling is consistent with the measured thermal resistance. The new LED array prototype design is a step in the right direction to achieve the final project goal of 5°C/W.

Figure 3.3. Temperature gradient contour of an array element in the new array prototype.



After modification of the circuit layout in the new LED array prototype, we re-examined the thermal model to improve the effectiveness of heat spreading around each LED chip in the new LED array prototype. At a constant ambient and board temperature of 25°C, the modeling predicted a junction temperature of 8.1°C/W from LED chip to ambient with a new circuit layout. This is an important improvement comparing to our previous design of LED array prototype. Using a test unit of the new LED array prototype, we measured the junction temperature of 10.1°C/W from LED chip to ambient in the lab. This result was a little surprising since the previous design yielded a junction temperature of 10.2°C/W from LED chip to ambient. When we looked at the various components of this measurement, the discrepancy in the outcome can be explained. The resulting junction temperature of the LED chip to ambient (Rja) consists of the junction temperature of the LED chip to the board (Rjb) and the junction temperature of the board to ambient (Rba). Rja consists of Rjb + Rba. From our measurements listed in Table 3.1, we saw an improvement of Rjb of ~2°C with the new circuit

board layout but this did not translate into the equivalent improvement of Rja. This leads us to the fact that Rba was not the same between the previous two circuit boards designs. We then investigated this difference between the Rba values for the two designs. Improving Rba was a focus in the third year to reach the thermal resistance goal of 5°C/W.

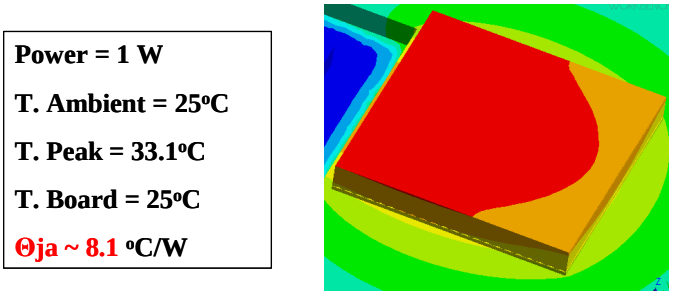
Table 3.1. Junction temperature measurements comparing the new and previous circuit board design.

Array prototype Design	Rja (°C/Watt)	Rjb (°C/Watt)
Circuit board design #1	10.2	8.1
Circuit board design #2	10.1	5.9

Year 3 Results

During the final project year, we redesigned our circuit layout to accommodate smaller size LED chips than the 1mm x 1mm chip we were previously using. In order to achieve our end of the project goal of a 1000 lumen array with 100 lumen/Watt efficacy, we needed to move to smaller chips. This layout maintained approximately the same array footprint as before, though the new design have ~ 3 times the number of small chips compared to the larger power chips. This modification allowed more uniform and effective heat spreading around each LED chip through thermal modeling. After modification of the circuit layout in the new LED array prototype, we re-examined the thermal model to improve the effectiveness of heat spreading around each LED chip in the new LED array prototype. Figure 3.4 shows the temperature gradient contour of an array element in the new array prototype. We achieved the junction temperature of 8.1°C/Watt from LED chip to ambient at a constant ambient and board temperature of 25°C through thermal modeling. Specifically, the temperature distributions that are shown in color are very uniform (round shape) around each LED chip.

Figure 3.4. Temperature gradient contour of an array element in the new array prototype.



Also, we identified a new material set to improve the thermal properties of our circuit board and thereby achieving a lower junction temperature from the LED chip to ambient during the final year of project. A new LED element design was started using this new material to achieve low junction temperature from the LED chip to ambient. We then worked on completing a new thermal model for the circuit board design using this new material. At a constant ambient and board temperature of 25°C, the modeling predicted a junction temperature of 7.3°C/W from LED chip to ambient and 4.1°C/W from LED chip to board with a new circuit layout. Of this new design, we fabricated array prototype and mounted it on to heat sink of LED luminaire with reflector for final evaluation. Table 3.2 shows the results of thermal

resistance of our final luminaire prototypes. Due to thermal crosstalk and luminaire configurations, we measured the thermal resistance of Rhs-a (between heat sink and ambient) and Rb-hs (between board and heatsink) instead. The thermal resistance between LED and board was estimated from our previous measurement of individual LED arrays. Though thermal crosstalk can occur between the arrays in the luminaire prototype, the thermal resistance between LED and ambient is considered to be 3.4 to 3.8°C/W in this case. This is a great achievement in our project, though these results were calculated through measurement partially.

Table 3.2. Junction temperature measurements comparing the array and luminaire design.

Prototype	Rj-b (°C/Watt)	Rb-hs (°C/Watt)	Rhs-a (°C/Watt)	Rj-a (°C/Watt)
Array	**4.1**	**2**	**-**	**7.3**
Luminaire	**0.2**	**0.2**	**3**	**3.4**

SECTION 4
TASK 4 – UNIFORM AND REPRODUCIBLE CONVERTER PROCESS

CHALLENGES

To achieve the desired goal of rapid market penetration into the target commercial reflector lamp market, a warm (2800-3000K color temperature) light with a high degree of color rendering is desired. However, the development of highly efficient phosphor converters to enable high color rendering index and efficient output at 3000K color temperature presents a formidable task which is beyond the scope of the proposed effort. The project effort will therefore employ two basic approaches to achieving the target specifications; utilization of emerging phosphor downconverters and phosphor blends as they become commercially available, and investigation and development of novel approaches for achieving warm white with high color rendering through the combination of multi-color LEDs with phosphors within the LED array.

Commercial phosphor blends developed specifically for combination with blue LEDs are becoming increasingly available as phosphor companies become aware of the emerging SSL markets. Reliance on the availability of commercial phosphor blends has the advantage of adding no additional cost to the proposed efforts above the cost required to procure the materials. However, achievement of the target specifications becomes contingent upon the developments in the phosphor industry. As an alternate course, Cree SBTC will also investigate the potential for combining chips of different colors – readily accomplished in the proposed array fabrication schemes – along with phosphor conversion media to produce the desired hue of light. For example, the combination of blue LEDs with red-emitting LEDs and yellow emitting phosphor provides a potentially very efficient means for attaining warm white illumination with high color rendering index. Very efficient red LEDs are inexpensive and commercially available, and their use in the production of warm white light has intrinsic advantages over approaches that use downconversion to produce red light from the emitted blue LED radiation. This benefit arises since the red light is produced at high efficiency without the

Stokes loss associated with phosphor conversion from short to long wavelengths. Attendant to the potential benefits of this approach also comes a number of challenges associated with the combination of different LED materials systems having differing characteristics as a function of temperature, voltage and operating lifetime. The project effort will include an analysis of the various trade-offs associated with both approaches, with a best-effort goal of achieving color temperatures in the range of 2800-3000K with high color rendering, stability, and efficiency.

RESULTS AND DISCUSSIONS

Year 1 Results

The achievement of a successful commercial LED-based luminaire will require a source which has the proper hue or color temperature of white light and projects that light in a uniform fashion. Further, the materials and processes developed towards this goal must be manufacturable (readily fabricated and uniform from part-to-part) and stable over time (e.g., successfully pass a variety of accelerated environmental tests to simulate operation over a suitable lifetime in a "typical" operating environment). During the first year of project, experiments have been conducted in both the application process and materials (including both encapsulants and phosphor materials) to begin the development effort to achieve uniform stable, reproducible white emission from small-area LED arrays. Specifically, LED test lamps were fabricated and characterized using a variety of encapsulant materials and two recently available commercial phosphor materials.

To take advantage of the emerging opportunity presented by the recent availability of alternative phosphor materials with high conversion efficiency in a broad range of color temperatures, sample quantities of a variety of phosphor compositional variations were obtained and tested using a standard LED lamp testbed. The primary focus of the testing was to determine the workability, efficiency, color temperature, and stability of the phosphor materials.

Each compositional variation tested belonged to the same general phosphor chemical family, with slight variations. White LED-based lamp sample lots were fabricated using each composition, and (after some process adjustments to obtain the desired color point) tested in an integrating sphere apparatus to determine the efficiency, color temperature, color rendering index, temperature dependence, etc.

Figure 4.1 shows the resulting chromaticity points measured from a sample set of LED-based lamps incorporating two new phosphor materials. The combination of the emitted blue LED light and the downconverted light generated by the phosphor layers results in a measured color temperature of ~3000 Kelvin. This represents a "warm" or more yellowish-red white hue which is not generally achievable using conventional Ce:YAG phosphors (which can only produce a "colder" or more bluish white). The chromaticity points achieved using the new phosphor materials are also located close to the black-body (Plankian) locus yielding a desirable emission for many lighting applications. Color rendering index values of ~80 have been measured. A range of promising luminous efficacy values have been measured which are, however, generally lower than those possible using Ce:YAG. This is due, in part, to the incorporation of lower efficacy red light (necessary to achieve the desired color point).

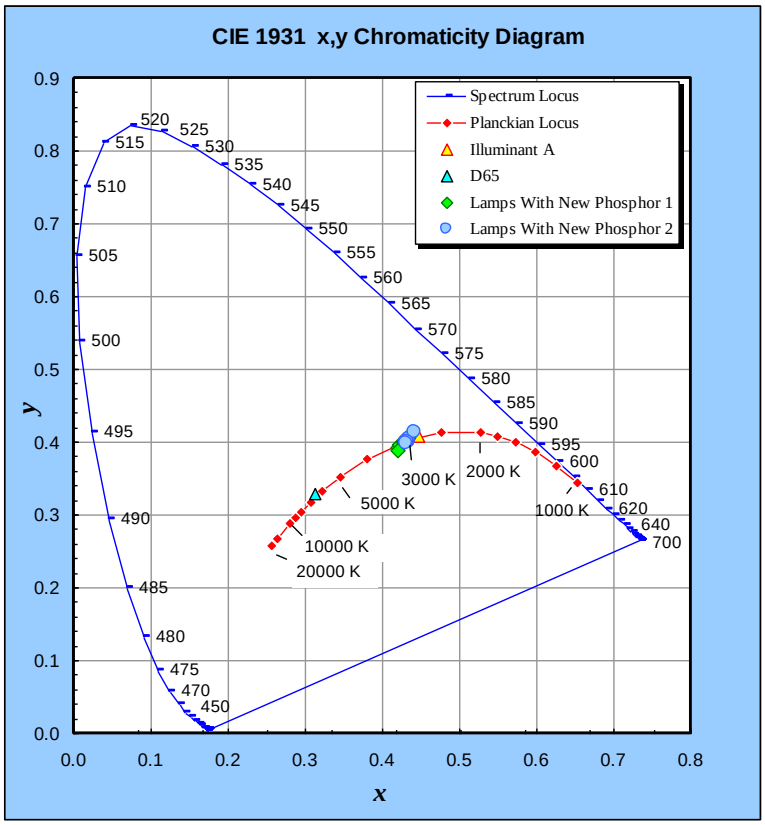


Figure 4.1. Chromaticity points measured for LED-based warm white (~3000 Kelvin color temperature) lamps incorporating two new phosphor materials.

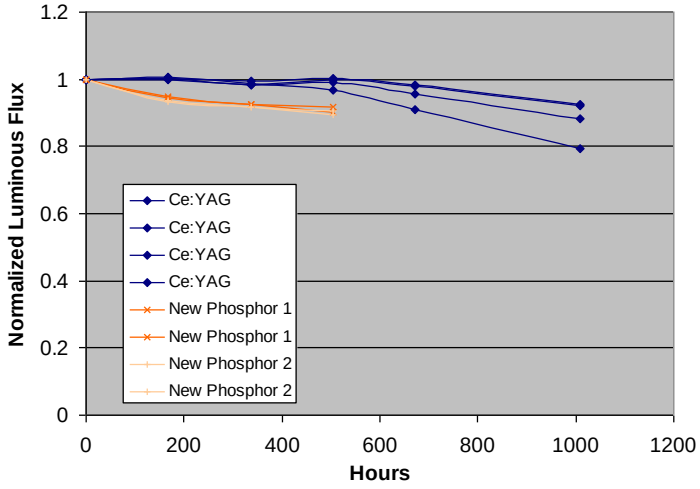
While chromaticity and efficacy are important factors in the commercialization of LED-based solid-state white lighting, it is also critical that the phosphor materials used to generate the white light withstand operating conditions without degrading or changing color point significantly. To determine the reliability of the new phosphor materials, sample lamps containing the materials were subjected to accelerated operating condition tests such as "wet high temperature operating life" or WHTOL (85C, 85% relative humidity operating conditions) and then monitored as a function of time.

Figure 4.2 shows the observed variation in the luminous flux output for lamps fabricated using the two new phosphor materials "New Phosphor 1" and "New Phosphor 2". The new materials show a greater initial decrease than observed for lamps containing Ce:YAG phosphor (also shown). However, the light output appears to be stabilizing with continued operation. Similar reliability testing has been and will continue to be performed on additional new phosphor materials to ensure compatibility with the project goal of a reasonable operating lifetime for the target luminaire.

The achievement of a successful commercial LED-based luminaire will require a source which has the proper hue or color temperature of white light and projects that light in a uniform fashion. Further, the materials and processes developed towards this goal must be

manufacturable (readily fabricated and uniform from part-to-part) and stable over time (e.g., successfully pass a variety of accelerated environmental tests to simulate operation over a suitable lifetime in a "typical" operating environment). During the second year of project, we have evaluated new phosphor materials with high conversion efficiency in a broad range of color temperatures as they became commercially available. Several different phosphors were obtained and tested using a standard LED lamp testbed. The primary focus of the testing was to determine the workability, efficiency, color temperature, and stability of the phosphor materials. White LED-based lamp sample lots were fabricated using each phosphor and tested in an integrating sphere apparatus to determine the efficiency, color temperature, color rendering index, temperature dependence, etc.

Figure 4.2. Change in normalized light output as a function of time for new phosphor materials compared to Ce:YAG when subjected to 85C, 85% relative humidity, constant operation.



The first phosphor material was evaluated for light output at the correlated color temperature of ~ 3000K; however the color rendering index values of ~50 was measured for this new phosphor material. This is not satisfactory for our project and applications. The second phosphor material was evaluated for light output at the correlated color temperature of ~ 3200K after standard and stressed storage conditions. Table 4.1 shows the chromaticity points and luminous flux of a set of LED-based lamps incorporating this new phosphor material measured after standard and stressed storage conditions (high temperature and humidity) for 288 hours. The standard storage condition of LED-based lamps was set at room temperature (25°C) and humidity (~50% relative humidity) and high temperature and humidity was set at 85°C and 85% relative humidity. In Table 4.1, the changes of chromaticity point, correlated color temperature and luminous flux are observed in these LED-based warm white lamps incorporating this new phosphor material measured between standard and stressed storage conditions (high temperature and humidity). There is ~300K shift of correlated color temperature and ~7% reduction of light

Table 4.1. Chromaticity point and luminous flux of LED-based warm white (~3200K correlated color temperature) lamps incorporating a new phosphor material measured after stressed storage conditions (high temperature and humidity) for 288 hours.

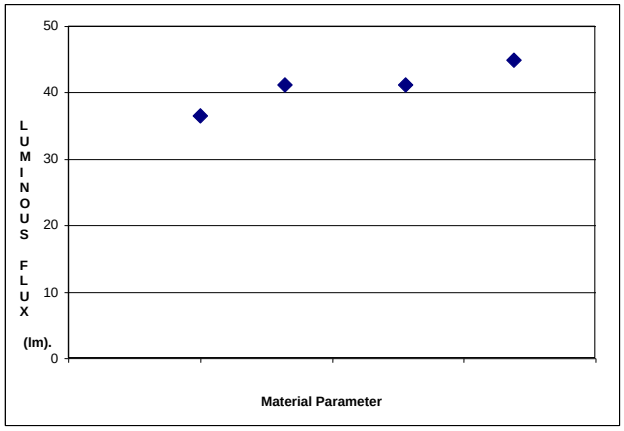
Storage Conditions (288 hours)	Current	Voltage	Chromaticity		CCT	Luminous Flux
	(mA)	(V)	X	Y	(°K)	(Lumens)
Standard Conditions (at room)	350	3.1	0.4212	0.3935	3196	40.84
High Temperature	350	3.1	0.4137	0.3871	3291	36.96
High Temperature and Humidity	350	3.1	0.4028	0.3864	3522	38.15

output between standard and stressed storage conditions after 288 hours. Therefore, this is not a satisfactory phosphor material for warm white color temperature downconversion of our project and applications. These two warm white phosphors were not promising for our purposes and we will continue to evaluate more phosphor materials as they become available.

Year 2 Results

During the second year of project, we also obtained phosphor materials with various properties from a commercial vendor. Using a standard LED lamp testbed, we evaluated these phosphor materials for light output at a CCT of ~ 5850K. Figure 4.3 shows the resulting light luminous flux of each phosphor and its corresponding material property characterized by a "material parameter". Based on this evaluation, it is clear that the selected material property has an influence on the light emission from the phosphor when a standard LED material and piece-parts combination is considered. This is an important step for us to select phosphor materials and its material property to be used for the LED array elements in the future.

Figure 4.3. Resulting luminous flux of the phosphor material with various properties as characterized by a "material parameter".



We also investigated various methods for applying a phosphor material to an array element for cool white color temperature downconversion using a phosphor obtained from a commercial vendor. Using a standard LED lamp testbed and LED chips with nearly equivalent radian flux emission, we evaluated this phosphor material for light output at the correlated color temperature of ~ 6000K with various application methods at a constant composition. Table 4.2 shows luminous flux of a set of LED-based lamps incorporating the phosphor material measured after various application methods. It is clear that various phosphor application methods have yielded different luminous fluxes, though we used LED chips with equivalent

Table 4.2. Luminous flux of LED-based cool white (~6000K correlated color temperature) lamps incorporating the phosphor material at a constant composition with various application methods.

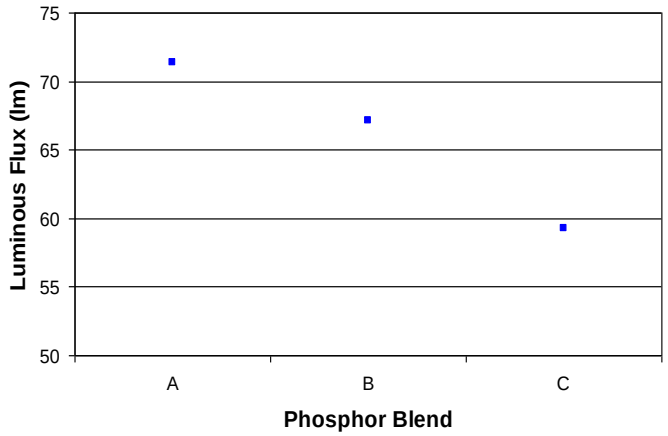
Phosphor Application Method	Current (mA)	Voltage (V)	CCT (^{o}K)	Luminous Flux (Lumens)
Method A	350	3.1	5683	47.4
Method B	350	3.1	6165	50.2
Method C	350	3.1	6000	53.4

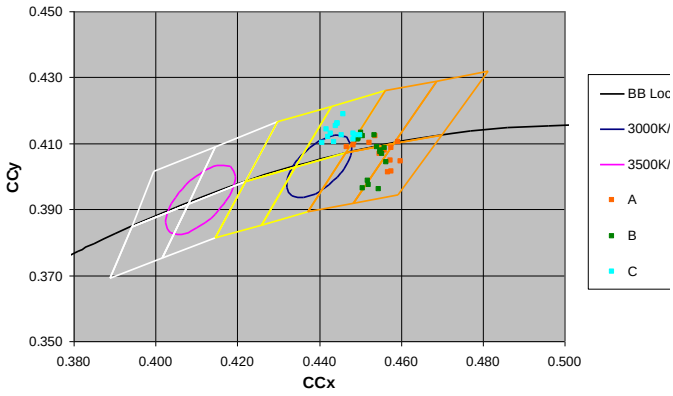
radiant flux of light and the same batch of phosphor material at a constant composition. Specifically, the Method C has shown the highest luminous flux and it is ~12% higher than that of Method A. Therefore, it is important for us to consider the application methods of phosphor materials when we design new array element to achieve the optimum light output in the future.

Year 3 Results

During the final year of project, a number of commercial phosphor materials were evaluated. Specifically, we focused on warm white phosphors at CCT of 2800 to 3500K. Using a standard LED lamp testbed, we evaluated these phosphor materials for light output at a CCT of ~ 3000K. As we reported previously, various application methods of a cool white phosphor yielded different luminous fluxes, though we used LED chips with equivalent radiant flux of light. Of warm white phosphor materials, the same results were identified in the final year of project. Figure 4.4 shows the resulting light luminous flux at CCT of ~3000K and its corresponding application method characterized by a "phosphor blend". Though we used LED chips with equivalent radiant flux of light, the Phosphor Blend A has the highest luminous flux and it is ~10% higher than that of Phosphor Blend C. It should be noted that these warm white phosphor materials were not completely evaluated through stressed conditions (high temperature and humidity). It is our best interest to achieve color temperatures in the range of 2800-3000K with high color rendering, stability, and efficiency in our luminaire prototypes.

Figure 4.4. (a) Resulting luminous flux of the phosphor material with various application methods as characterized by a "Phosphor Blend". (b) Chromaticity point of various application methods.





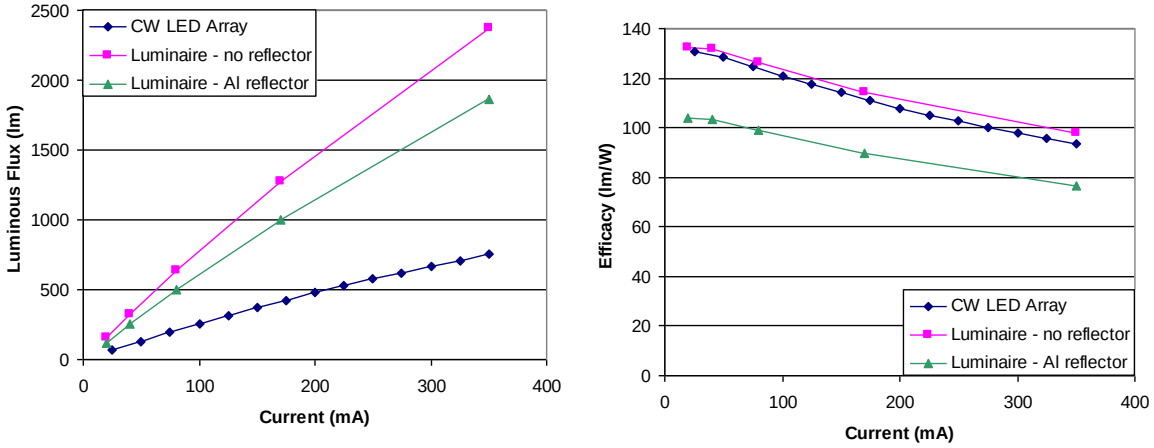
LUMINAIRE RESULTS

As stated in the goals of this project, the resulting LED arrays will be combined with a custom luminaire enclosure that has been designed to specially address the thermal, optical, and electrical requirements of the LED luminaire prototypes. Based on the above development efforts, we assembled several integrated LED luminaire prototypes and demonstrate the performances as follows.

Cool White Luminaire Prototype

Figure 5.1. An integrated cool white LED luminaire prototype with metal reflector.

The performance of 1000 lumens cool white light output with reflector shaped beam and efficacy of 89.4 lm/W at CCT of 6000K and CRI of 73 was achieved in an integrated LED luminaire prototype. If the reflector is not used, the performance of 1275 lumens and efficacy of 114.2 lm/W was measured. The custom DC driver provided ~170mA constant current with ~11.2 Watt total input power. Since the custom AC converter was attached as a separated control unit, the driver loss was measured of ~2-3%. It should be noted that all luminous flux and DC measurement was done in an integrated sphere after ~30 seconds of power on before measurement. Figure 5.1 shows an integrated cool white LED luminaire prototype with metal reflector. Figure 5.2(a) shows the comparison of measured luminous flux of integrated luminaire with and without reflector at various DC current input. Figure 5.2(b) shows the changes of efficacy of integrated luminaire with and



(a) (b)

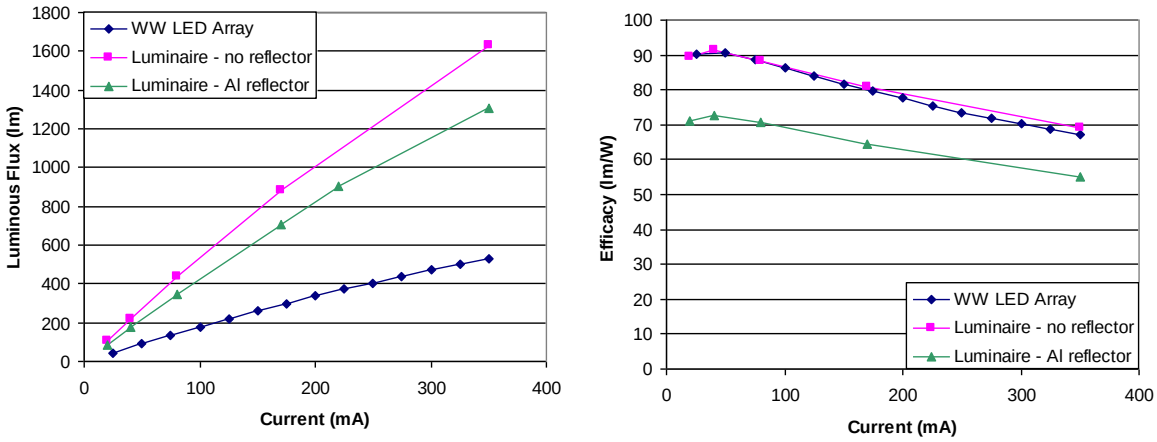
Figure 5.3. The variations of (a) luminous flux and (b) efficacy vs. DC current of LED array, no reflector and with reflector in an integrated luminaire prototype.

without reflector at various DC current. In both figures, the performance of LED array was included for comparison as well. Comparing to no reflector attached to the integrated LED luminaire prototype, the loss of luminous flux and reduction of efficacy is obvious in these figures. The actual luminous flux loss of was then calculated of ~21%. This is a very significant reduction of light output if the reflector is used.

Warm White Luminaire Prototype

Figure 5.3. An integrated warm white LED luminaire prototype with metal reflector.

The performance of 903 lumens warm white light output with reflector shaped beam and efficacy of 63.0 lm/W at CCT of 2800K and CRI of 82 was achieved in an integrated LED luminaire prototype. If the reflector is not used, the performance of 1156 lumens and efficacy of 76.5 lm/W was measured. The custom DC driver provided ~220mA constant current with ~15.2 Watt total input power. A compatible driver loss of 2-3% in the AC converter was measured as well. It should be noted that all luminous flux and DC measurement was done in an integrated sphere after ~30 seconds of power on before measurement. Figure 5.3 shows an integrated warm white LED luminaire prototype with metal reflector. Figure 5.4(a) shows the comparison of measured luminous flux of integrated luminaire with and without reflector at various DC current input. Figure 5.4(b) shows the changes of efficacy of integrated luminaire with and without reflector at various DC current. In both figures, the performance of LED array was included for comparison as well. Comparing to no reflector attached to the integrated LED luminaire prototype, the loss of luminous flux and reduction of efficacy is obvious in these figures too.



(a) (b)

Figure 5.4. The variations of (a) luminous flux and (b) efficacy vs. DC current of LED array, no reflector and with reflector in an integrated luminaire prototype.

SUMMARY

In summary, significant technical progress has been accomplished during three years of this project. Using improved blue LED chips obtained from Cree, the performance of an integrated luminaire prototype with reflector achieved 1000 lumens cool white light output at efficacy of 89.4 lm/W with CCT of 6000K and CRI of 73; and 903 lumens warm white light output at efficacy of 63.0 lm/W with CCT of 2800°K and CRI of 82. In addition, up to 1275 lumens cool white light output at 114.2 lm/W and 1156 lumens warm white light output at 76.5 lm/W were achieved if the reflector was not used. The success to integrate small area array-based LED designs and address thermal, optical, electrical and mechanical requirements was clearly demonstrated in these integrated luminaire prototypes with outstanding performance and high efficiency. The performances of small area LED arrays in an integrated luminaire prototype has demonstrated an outstanding progress in light output of 100% (comparing to the start of project) with high efficiency. The summary of achievement to project goals is listed below.

Milestones	Target	Achieved (Year 3)	
Task 1: Chip Performance	100 lm/W	95 - 100 lm/W (350 mA)	
Task 2: Array Design	100 lm/W	95.3 lm/W (350 mA)	
Luminaire Prototype Source: DC measurement System: AC converter (Note: source and system have ~ same input power)	1000 lumens, 100 lm/W (source) 90 lm/W (system) 2800-3500K CCT, 80 CRI, 5°C/W	1000 lumens 95.3 lm/W 89.4 lm/W 6000K, 73-80 CRI 3.4°C/W 11.2 W input	903 lumens 67.3 lm/W 63.0 lm/W 2800K, 82 CRI 3.4°C/W 15.5 W input
Task 3: Thermal Resistance (T_{ja})	5°C/W	3.4°C/W	
Task 4: Down Conversion (CCT)	2800-3500K	2800K CCT	

REFERENCES

[1] "Characteristics of Phosphors Excited by Long-UV Light" presented by T. Hase, et al., International Symposium on the Light for the 21st Century, March 2002, Tokyo.

APPENDIX

Copy of Cree Press Release 8/31/06

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Cree Launches EZBright™ LED Power Chip for Lighting Applications

DURHAM, NC, August 31, 2006 — Cree, Inc. (Nasdaq: CREE), a leader in LED solid state lighting components, today announced the release of its new EZBright™ LED power chip. The new EZBright1000™ LEDs are twice the brightness of Cree's current power chips. The EZBright1000 power chip is designed for general lighting applications, such as home and office lighting, auto headlamps, streetlights, and garage and warehouse low bay lighting, as well as consumer applications including flashlights, camera flash and projection displays.

"This is an important milestone for power LEDs. For the first time, these chips should enable solid-state lamp makers to challenge the efficacy of not only incandescent, but also fluorescent lamps," said Chuck Swoboda, Cree chairman and CEO. "The EZBright1000 LED power chip is one of several advancements we are working on to help drive LEDs into more mainstream lighting applications."

"The blue EZBright1000 power chip, measured as a bare die, exhibits power output up to 370mW at 350mA of drive current and 800mW at 1A of drive current," stated Scott Schwab, Cree vice president and general manager of optoelectronics. "This product should enable our customers to reach new levels of power output and efficiency from a single chip and redefine what is possible with power LEDs."

The EZBright1000 power chip is the third product released based on the Cree EZBright platform, which features a proprietary optical design that delivers an optimal Lambertian radiation pattern, with low emission losses and high efficiency. This product incorporates technology that was in part developed with support provided by the U.S. Department of Energy, National Energy Technology Laboratory, and the U.S. Department of Commerce, National Institute of Standards and Technology, Advanced Technology Program.

EZBright1000 LEDs are now available in commercial quantities. Additional EZBright products are targeted for release over the next several months. For additional information on Cree EZBright LEDs, please call (800) 533-2583 or visit www.cree.com.

About Cree, Inc.
Cree is a market-leading innovator and manufacturer of semiconductors and devices that enhance the value of solid-state lighting, power and communications products by significantly increasing their energy performance and efficiency. Key to Cree's market advantage is its world-class materials expertise in silicon carbide (SiC) and gallium nitride (GaN) for chips and packaged devices that can handle more power in a smaller space while producing less heat than other available technologies, materials and products.

Cree drives its increased performance technology into multiple applications, including exciting alternatives in brighter and more tunable light for general illumination, backlighting for more vivid displays, optimized power management for high-current switch-mode power supplies and

variable-speed motors, and more-effective wireless infrastructure for data and voice communications. Cree customers range from innovative lighting-fixture makers to defense related federal agencies.

Cree's product families include blue and green LED chips, lighting LEDs, LED backlighting solutions, power-switching devices and radio-frequency/wireless devices. For additional product specifications please refer to www.cree.com.

This press release contains forward-looking statements involving risks and uncertainties, both known and unknown, that may cause actual results to differ materially from those indicated. Actual results may differ materially due to a number of factors, such as the risk we may encounter delays or other difficulties in ramping up production of our new products; the risk we may be unable to manufacture products with sufficiently low cost to offer them at competitive prices or with acceptable margins, the rapid development of new technology and competing products that may impair demand or render our products obsolete; the potential lack of customer acceptance for the products; variations in demand for Cree's products and its customers' products; the risk we may encounter delays or other difficulties in developing and commercially releasing additional new products for mainstream lighting applications; and other factors discussed in Cree's filings with the Securities and Exchange Commission, including its report on Form 10-K for the year ended June 25, 2006, and subsequent filings.

# # #

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Copy of Cree Press Release 10/9/06

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Cree Delivers the First 160-Lumen White Power LED

— XLamp LEDs now as efficient as fluorescent sources —

DURHAM, NC, October 9, 2006 — Cree, Inc. (Nasdaq: CREE), a leader in LED solid state lighting components, today announced new benchmarks for power LED brightness and efficacy with the release of the newest white Cree XLamp® 7090 power LED. This new XLamp LED, available in volume quantities, produces luminous flux of up to 95 lumens or 85 lumens per watt at 350 mA, and up to 160 lumens at 700 mA.

Typical luminous flux for the new Cree XLamp 7090 LED is 80 lumens at 350 mA, yielding 70 lumens per watt. The new XLamp LED was designed to enable general lighting applications, such as street lighting, retail high bay lighting and parking garage low bay lighting, as well as to vastly improve the light quality in consumer applications such as flashlights. LED technology has been sufficiently bright for many general illumination applications for some time. The new XLamp 7090 LED, however, offers the efficiency and reliability needed to make LEDs cost-effective for more of these applications. The new XLamp 7090 LED is the first power LED based on the company's EZBright™1000 LED chip, which provides the industry's highest efficacy at 350 mA.

"Cree LEDs are achieving efficacy levels formerly delivered only by the most efficient traditional lighting sources, including fluorescent bulbs. We have established a new class of LED performance," notes Mike Dunn, Cree general manager and vice president, lighting and backlighting LEDs. "Our goal at Cree remains to aggressively increase the brightness and efficacy of our LEDs to ensure that LEDs become a cost-effective, energy-saving alternative for all lighting applications."
"The Department of Energy is pleased to have been a contributing partner in the Cree research and development efforts that have achieved a new level of performance for power LEDs," notes Alexander Karsner, Department of Energy Assistant Secretary for Energy Efficiency and Renewable Energy. "Now, more than ever, our nation needs energy-saving technology that is top-quality and cost-effective. The Department will continue to work with Cree and other lighting-industry partners to turn advanced energy-saving technology into commercially available and successful products that save energy for consumers."

The Cree LED research and development efforts were enabled in part through funding from the Department of Energy's Building Technologies Program, within the Office of Energy Efficiency and Renewable Energy, and also in part through funding from the Department of Commerce's National Institute of Standards and Technology's Advanced Technology Program. Cree is also a charter member of the Department of Energy's Solid-State Lighting Partnership with the Next Generation Lighting Industry Alliance, an organization of lighting manufacturers that provides input to enhance the manufacturing and commercialization focus of the Department's solid-state lighting portfolio.

For additional information on Cree XLamp 7090 power LEDs and Cree EZBright LED chips, please call (800) 533-2583 or visit www.cree.com.

About Cree, Inc.
Cree is a market-leading innovator and manufacturer of semiconductors and devices that enhance the value of solid-state lighting, power and communications products by significantly increasing their energy performance and efficiency. Key to Cree's market advantage is its world-class materials expertise in silicon carbide (SiC) and gallium nitride (GaN) for chips and packaged devices that can handle more power in a smaller space while producing less heat than other available technologies, materials and products.

Cree drives its increased performance technology into multiple applications, including exciting alternatives in brighter and more-tunable light for general illumination, backlighting for more-vivid displays, optimized power management for high-current, switch-mode power supplies and variable-speed motors, and more-effective wireless infrastructure for data and voice communications. Cree customers range from innovative lighting-fixture makers to defense-related federal agencies.

Cree's product families include blue and green LED chips, lighting LEDs, LED backlighting solutions, power-switching devices and radio-frequency/wireless devices. For additional product specifications please refer to www.cree.com.

This press release contains forward-looking statements involving risks and uncertainties, both known and unknown, that may cause actual results to differ materially from those indicated. Actual results may differ materially due to a number of factors, such as the risk we may encounter delays or other difficulties in ramping up production of our new products; the risk we may be unable to manufacture products with sufficiently low cost to offer them at competitive prices or with acceptable margins, the rapid development of new technology and competing products that may impair demand or render our products obsolete; the potential lack of customer acceptance for the products; variations in demand for Cree's products and its customers' products; and other factors discussed in Cree's filings with the Securities and Exchange Commission, including its report on Form 10-K for the year ended June 25, 2006, and subsequent filings.

About the Department of Energy
The Department of Energy's Office of Energy Efficiency and Renewable Energy invests in a diverse portfolio of energy technologies to provide American consumers with a greater choice of energy-efficient products and enhance quality of life. The Building Technologies Program works with a wide array of industry, state, and university partners to accelerate the development and use of advanced building technologies such as solid-state lighting (SSL). SSL has the potential to more than double the efficiency of general lighting systems, saving energy costs for consumers and reducing overall U.S. energy consumption.

The unique attributes of SSL drive the need for a coordinated Federal approach that encompasses research, development, and commercialization support. In partnership with industry, the Department has developed a comprehensive R&D plan to ensure that DOE funds appropriate research topics that will improve efficiency and move SSL from the laboratory to the marketplace. To ensure that DOE R&D investments result in technology commercialization, the Department also implements commercialization-support strategies including lighting design competitions and the development of ENERGY STAR® criteria for SSL products. The Department works closely with the Next Generation Lighting Industry Alliance, utilizing the expertise of this organization of manufacturers to enhance the manufacturing and commercialization focus of the SSL portfolio.

For more information on the DOE solid-state lighting portfolio, visit www.netl.doe.gov/ssl.

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