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Extremely High Frequency RF Effects on Electronics

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Abstract

The objective of this work was to understand the fundamental physics of extremely high frequency RF effects on electronics. To accomplish this objective, we produced models, conducted simulations, and performed measurements to identify the mechanisms of effects as frequency increases into the millimeter-wave regime. Our purpose was to answer the questions, "What are the tradeoffs between coupling, transmission losses, and device responses as frequency increases?", and, "How high in frequency do effects on electronic systems continue to occur?" Using full wave electromagnetics codes and a transmission-line/circuit code, we investigated how extremely high-frequency RF propagates on wires and printed circuit board traces. We investigated both field-to-wire coupling and direct illumination of printed circuit boards to determine the significant mechanisms for inducing currents at device terminals. We measured coupling to wires and attenuation along wires for comparison to the simulations, looking at plane-wave coupling as it launches modes onto single and multiconductor structures. We simulated the response of discrete and integrated circuit semiconductor devices to those high-frequency currents and voltages, using SGFramework, the open-source General-purpose Semiconductor Simulator (gss), and Sandia's Charon semiconductor device physics codes. This report documents our findings.

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INTRODUCTION

The Problem

A great diversity of electronic devices and systems provides critical capabilities to military and civilian operations. An unknown aspect of our reliance on these systems is the potential for their disruption using mm-wave Directed Energy. This potential remains largely unknown, while high-power mm-wave sources are rapidly becoming available commercially. The deployment of active denial systems, for example, raises important questions as to the effects on electronics that might be in use in a zone protected by this high-power mm-wave source.

Testing by our group and others has demonstrated that RF effects on electronic systems can be observed at frequencies up to nearly 100 GHz. Extremely high frequencies (EHF, 30-300GHz) are advantagous from the point of view of antenna size for a given gain, but the optimum frequency for a given scenario depends on many factors besides achievable antenna gain. In their discussion of radio communications, David and Voge (1969) wrote, "… the radiocommunication frequency range extends over such a large interval that phenomena which are important at one extremity are negligible at the other, and vice versa." This comment applies to RF Directed Energy as well. Coupling and electronic response issues that are important at 1 GHz may be negligible at 100 GHz, and vice versa. Part of our purpose here is to identify and quantify which phenomena are important in the mm-wave frequency range.

This report describes our theoretical, numerical, and experimental effort to understand the potential of extremely high frequency RF energy to disrupt electronic systems for communications, computing, or other critical functions. The specific purpose of this work was to understand the fundamental physics of extremely high frequency RF effects on electronic systems. The primary goal was to understand the fundamental mechanisms of effect and their scaling with frequency. Accomplishing this goal will provide information needed to determine if an adversary could design and build a mm-wave system to disrupt our critical electronic systems.

Technical Approach

Understanding high-power microwave (HPM) effects on electronics at any frequency requires an understanding of the physics of four basic areas:

1. Coupling – how does the energy get into the target?
2. Energy Distribution – how much energy makes it to a critical component (usually a semiconductor device) through wires, cables, or printed circuit traces?
3. Device Interaction – how does the energy affect the component (bias shift, rectification, frequency pulling)?
4. System Impact – how is the electronic system affected by this interaction?

These areas affect each other. For example, device interaction can change an impedance that changes the energy distribution. Part of understanding the physics includes knowing when these

stages can be taken serially, ignoring their mutual interactions, and when the interactions among them must be included.

Understanding the RF coupling, energy distribution, and device interaction effects and their sensitivities to the details of the physical geometry and materials is greatly aided by the computational tools that are now available. To accomplish our objective, we produced models of the interactions, conducted simulations, and performed measurements to identify the mechanisms of effects as frequency increased. Our purpose was to answer the questions, "What are the tradeoffs between coupling, transmission losses, and device response?", and, "How high in frequency do effects continue to occur?" Using full wave electromagnetics codes (Eiger, HFSS, Feko, and COMSOL) and a transmission-line/circuit code (LineCAP), we investigated how extremely high-frequency RF propagates on wires and printed circuit board traces. We investigated both field-to-wire coupling and direct illumination of printed circuit boards to determine the significant mechanisms for inducing currents at device terminals. We measured coupling to wires and attenuation along wires for comparison to the simulations, looking at plane-wave coupling as it launches modes onto single and multiconductor structures. We simulated the response of discrete and integrated circuit (IC) semiconductor devices to those high-frequency currents and voltages, using COMSOL, SGFramework, the open-source General-purpose Semiconductor Simulator (gss), and Sandia's Charon circuit/semiconductor device physics codes.

Previous Work in this Area

Adams et al. (1987) examined electromagnetic field coupling onto terminated wires at SHF (3-30 GHz) and EHF (30-300 GHz). They found that the equivalent impedance of these single and multiconductor transmission lines, treated as receiving antennas, rapidly spirals in to relatively small circles in the complex impedance plane as the lines become longer electrically. This means that the maximum and minimum equivalent impedances quickly approach bounds as the frequency increases. In addition, the maximum open circuit voltage induced on the "antenna" changes slowly with frequency. Thus, although the specific value of induced signal becomes more and more difficult to compute as the electrical size of the problem stretches our computational resources, *bounding* this signal does not require simulating the complete, electrically large problem, and can be relatively simple.

This spiraling impedance behavior is, in fact, normal for a dipole, as shown by impedance calculations as a function of frequency (Straw, 2011, Chapter 2), and it may be normal antenna behavior in general. A rule-of-thumb in estimating HPM coupling to cables is that "it is the last wavelength that matters," and that "the coupling cross-section is 'X' dB below isotropic," with X depending on other shielding factors.

These SHF/EHF results were incorporated into IEMCAP, an intrasystem electromagnetic compatibility estimating tool developed at Rome Air Development Center in the 1970's (Brock et al., 1989; McMahon et al, 1989). Leviatan and Adams (1982) considered analytically the effect of higher-order modes on coupling to two-wire transmission lines as the electrical separation between the wires becomes large, as it does in the mm-wave frequency regime.

More recently, Andrieu et al., 2008 and Andrieu et al., 2009, investigated techniques for simplifying full wave, three-dimensional coupling to bundles of wires at high frequencies by combining the wires into an equivalent, simplified cable bundle. Although intended for the microwave range, the techniques may have applicability in the mm-wave regime as well. Our group is developing a technique of incorporating the linear coupling problem into a non-linear circuit solver to account for the interaction between these parts of the total process that is applicable to this wavelength regime.

COUPLING AND ENERGY DISTRIBUTION

General Coupling Issues at Millimeter Wavelengths

In the millimeter wavelength regime, even individual electronic components can be several wavelengths in size. For example, consider the 8-pin, dual-inline package (DIP) ua741 integrated circuit operational amplifier (opamp) shown in the xray view of Figure 1. Next to the IC header is a scaled photograph of AM radio station KKOB's transmitting tower, which, at 645 feet in height, is a half-wavelength long at KKOB's 770 kHz frequency. KKOB's tower and the IC package (considered to be illuminated by 100 GHz) are shown on the same *wavelength* scale. Thus, the IC bondwires from the leadframe to the square in the center (the actual chip) would radiate as well at 100 GHz as KKOB's antenna does at 770 kHz. The IC pin connecting the package to the traces on the printed circuit board, and the portion of the pin internal to the package in the leadframe are also about one-half wavelength long. Clearly, circuit parasitic or even transmission line concepts are invalid for such an electrically large distributed system.

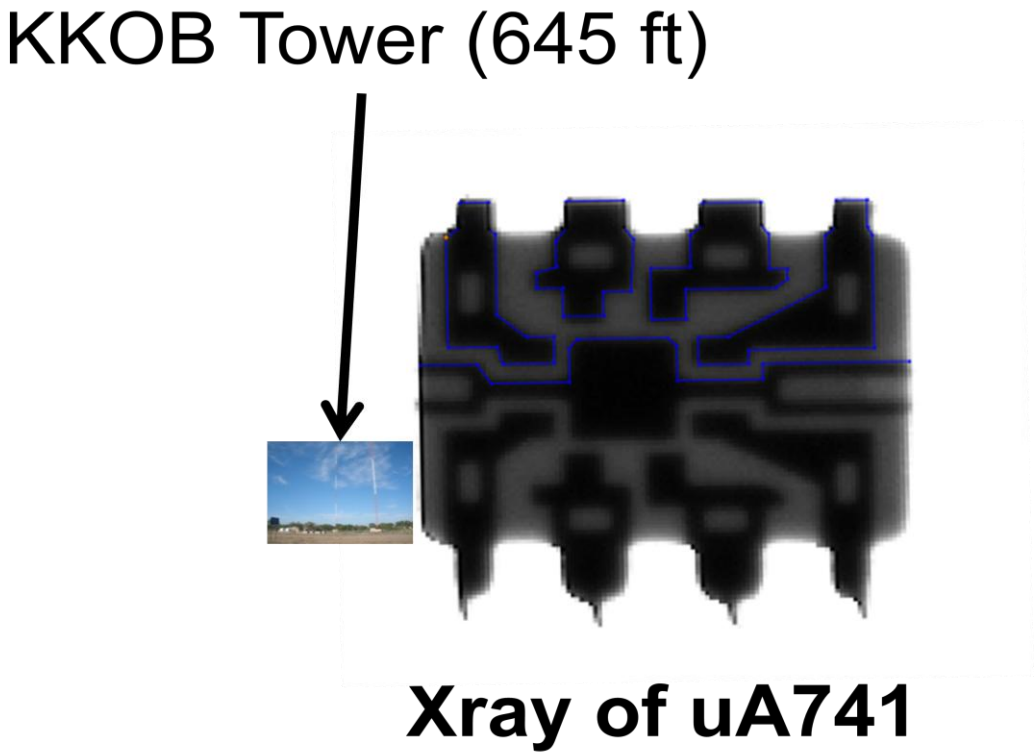


Figure 1. Perspective on Size in Wavelengths. Tower is one half wavelength at 770 kHz; Bondwires are one half wavelength at 100 GHz.

Suppose a strong 100 GHz signal is coupled to the vertical rise of the IC pin from the circuit board to the bend where it enters the IC package. This signal would likely be re-radiated by the length of the pin in the leadframe and by the bondwire from the leadframe to the chip, so that little energy is left to affect the semiconductor device on the chip. Conversely, an adjacent bondwire can receive this energy and couple it strongly to a different device on the chip. This "energy shedding" leads to the rule-of-thumb mentioned above, that it is the last wavelength that

matters in coupling. Thus, although Maxwell's equations remain the same for conventional RF directed energy and for the mm-wave regime, the physical length scales of devices and systems cause the general features of the geometry that are important for coupling and energy distribution to change. For example, at VHF and UHF, external cables dominate the coupling problem. At mm-waves, they are far less important. This point will occur again in the discussion of frequency dependent circuit response below.

Circuit Trace Coupling

In the mm-wave band, exposed circuit board traces and connectors can act as electrically large antennas. An example of this behavior is shown in the simulation illustrated in Figure 2 and Figure 3 below. As shown in Figure 2, a 2in by 2in circuit board with a single 8mil wide trace running its full length terminates in a 2.4mm edge connector. The dielectric is standard 62mil thick G10 circuit board material. A 50Ω semirigid coax with a simple model of a 2.4mm connector is attached to the edge connector on the board. Internally, the 50 Ω coax is terminated in a matched load. Externally, the outer conductor continues either 5cm or 10cm until it ends in an open circuit. A 10 to 20GHz plane wave is incident on the board/cable combination at an angle of incidence θ. It is polarized in the x-z plane.

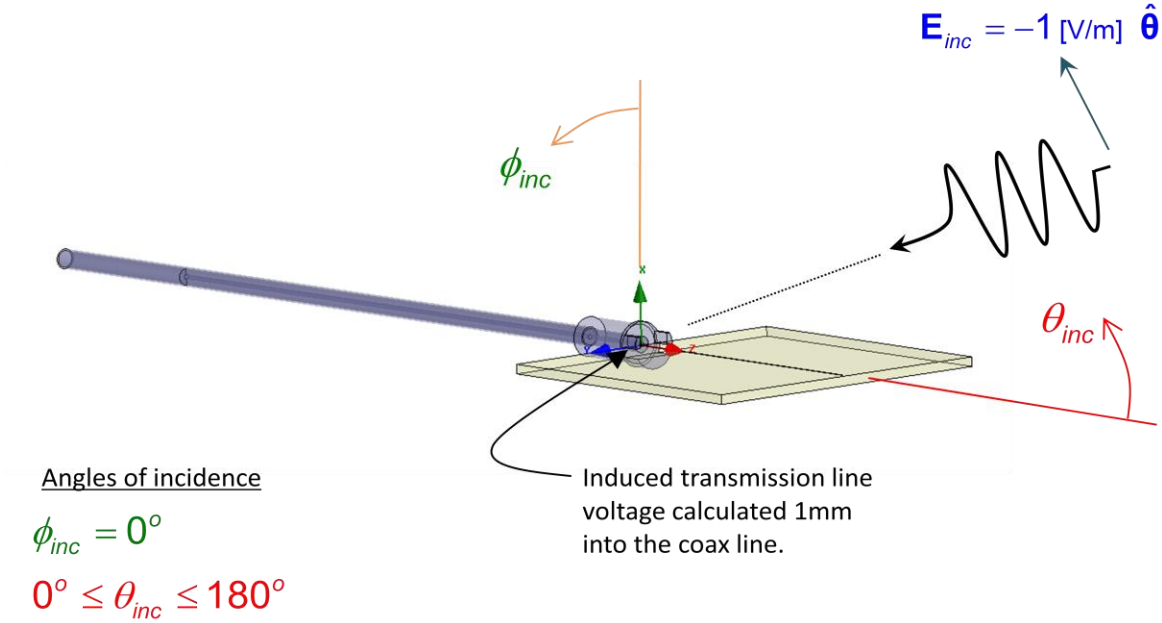


Figure 2. Circuit Trace Modeling Setup.

This geometry was simulated using Ansoft's HFSS, a finite element full wave electromagnetic simulator. The voltage induced by the incident field was measured in the coaxial transmission line at a depth of 1mm into the line. Figure 3 shows plots of the induced voltage as a function of frequency and of angle of incidence. The plot on the left is a linear plot of voltage versus frequency for the two cable lengths of 5 and 10 cm. Notice that the variations in the response for the 10cm long cable occur twice as rapidly as frequency changes as those for the 5cm long cable. The reflection from the end of the cable clearly affects the response, even though the cables are between 1.5 and 6.67 wavelengths long. This is related to the results of Adams et al. (1987) mentioned above. Notice also that although the lengths of the cables in the two cases differ by a

factor of two, the maxima and minima appear to follow the same smoothly decreasing curve as frequency increases.

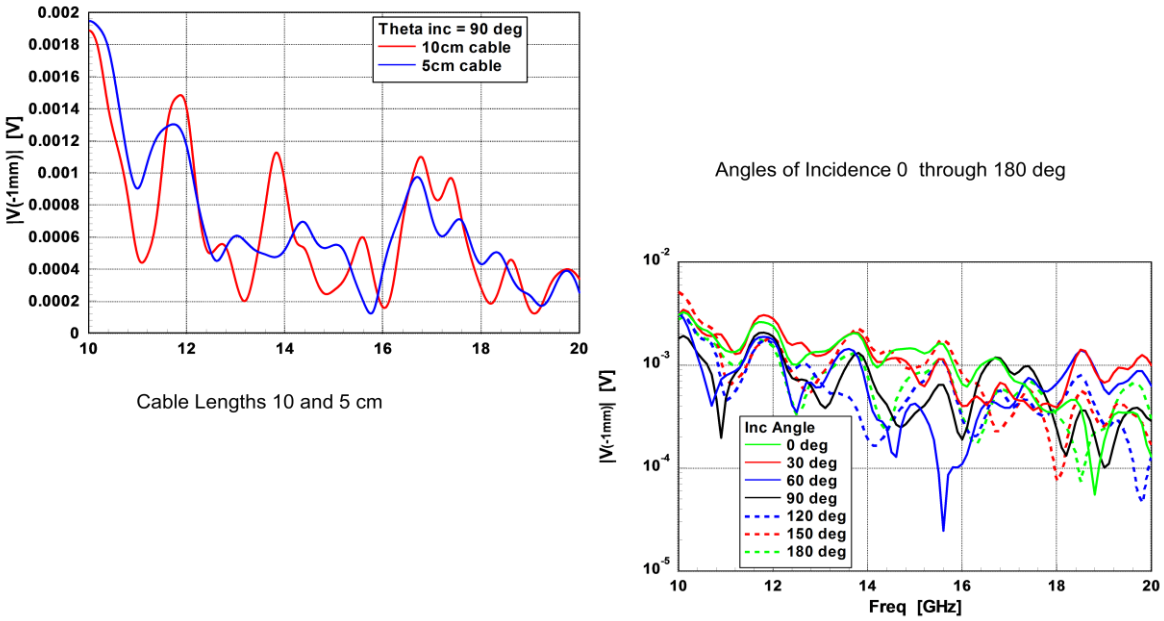


Figure 3. Induced Voltage vs Frequency and Angle.

The right hand curve illustrates the effect of the angle of incidence over the same frequency range. Curves of the same color but of different line styles are for angles of incidence that are symmetric with respect to the normal to the board. We expect these related curves to be similar but not the same, since the geometry is not symmetric. Both graphs manifest a decreasing response with increasing frequency. One qualitative way of explaining this is that if it is the last wavelength of structure that contributes most to the response, due to energy re-radiation, then the power collected should scale as $\lambda^2 \sim 1/f^2$. An additional contributing factor is that losses in the dielectric increase with frequency.

The capability that EM simulations provide to visualize fields and their interactions with structures is very useful in providing insight into this problem. For example, Figure 4 shows the total electric field in a vertical plane centered on the circuit board trace and coax cable for an incident plane wave at 20 GHz and angle of incidence $\theta = 30°$. The wave fronts and their interaction with the structure are apparent in the figure, including scattering by the edge of the board and reflections at the top of the coax. Figure 5 shows a closeup of the connector region. At this 1.5 cm wavelength, the connector structure itself affects the coupling into the coaxial line. The weaker signal coupled into the line, with its shorter spatial wavelength due to the slower velocity in the dielectric, can be seen in this figure. It is the variations in this signal that are shown in Figure 3 above. We have created animations of the waves moving across the structure that provide very useful insight into the interactions.

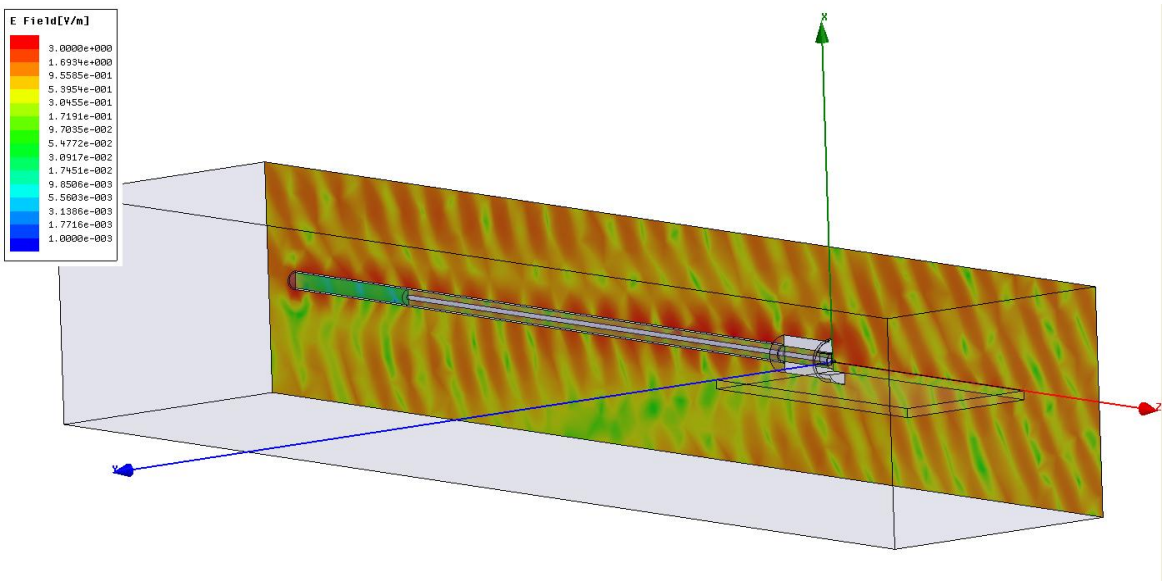


Figure 4. Total Electric Field at 20 GHz, Wave incident from θ=30°.

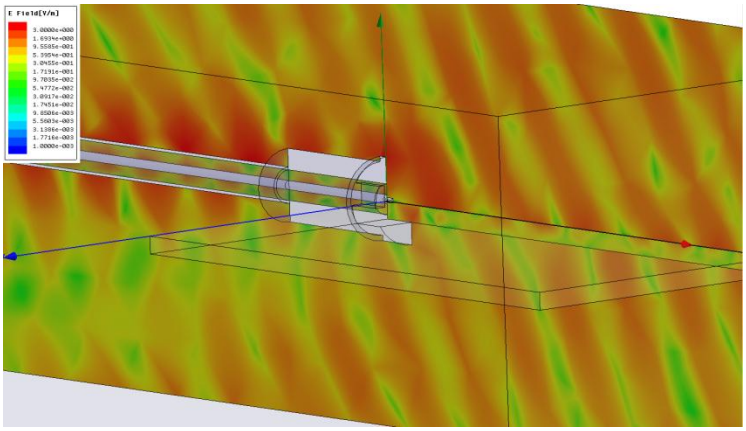


Figure 5. Closeup of connector region.

FEKO Model of Circuit Board Coupling

To investigate some of these effects further, a model of a small printed circuit board (PCB) with the ua741 integrated circuit amplifier on it was constructed using FEKO. FEKO is a commercial electromagnetic simulation software package. This software package allows the user to build complex models with various media and simulate that model in a variety of ways. The features of FEKO used to complete the modeling and simulation of the PCB board are the CAD, simulator, and post processing packages. FEKO implements a method of moments (MoM) algorithm to solve Maxwell's equations and determine the field quantities.

Method of Moments

The method of moments is a computational approximation that can be applied to electromagnetics (Harrington, FCBMM). This method can be preferable in some geometries to other methods, such as the finite element method or the finite difference method, because it

calculates boundary values instead of values thoughout the volume. It is very efficient for problems with a small surface area to volume ratio. In order to implement the method, the surface of the objects in the problem is meshed. Once the mesh is created the unknowns are expanded using basis functions. These basis functions are then combined with a testing or weighting function in the operator equation describing the electromagnetics. The result is a system of equations that can be written in matrix form. The currents and fields can be calculated by solving this linear set of equations. One drawback to the MoM is that each matrix is completely full, so sparse matrix solution techniques cannot be applied. As the size of the problem grows, the time and memory requirements grow by the square of the size of the problem.

Constructing the Model

The model of the PCB board was constructed and then simulated in several steps. The general process for constructing the model consisted of creating the leaded package frame of the part, constructing the PCB board, generating the ground plane, and adding the traces and vias. The package frame was originally constructed in SolidWorks. A parasolid file in the format of a *.x_t file was generated from the SolidWorks software package and imported into FEKO. The circuit board was modeled as a 2-layer FR4 board, with the backside of the board being a ground plane. The traces were generated by importing the *.dxf file used to manufacture the board into the Advanced Design System (ADS) software package and utilizing the board layout feature of ADS to make measurements of the traces. An attempt was made to import the *.dxf file directly into FEKO. Unfortunately, the import feature for a *.dxf file does not contain any layer information, and since the board is a multilayer board the geometries imported by the *.dxf file could not be implemented. Figure 6 shows a picture of the model.

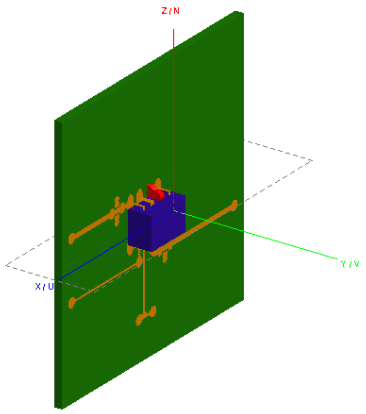


Figure 6. FEKO model of the PCB Board.

Simulating the Model

In order to simulate the model there needs to be some sort of electromagnetic excitation. For this particular case, an edge port was constructed on pin 2 of the part. Pin 2 is the inverting input pin of the ua741 opamp. A voltage of 1 V is applied to this edge port. The next step is to create the simulation mesh for the model. The frequency for the simulation was set at 24 GHz with a typical simulation mesh edge length of $\lambda/10$. A picture of the generated mesh is shown in Figure

7. Initial simulations were done using MoM. As the level of fidelity of the model grew, so did the number of unknowns the FEKO simulator had to solve. Eventually, the simulation time and PC memory requirements became excessive, and another, more efficient method to simulate the model needed to be explored.

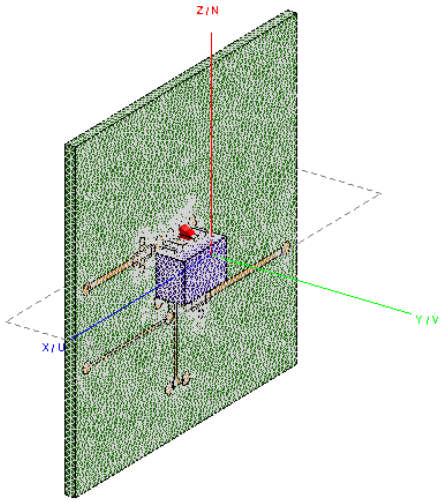
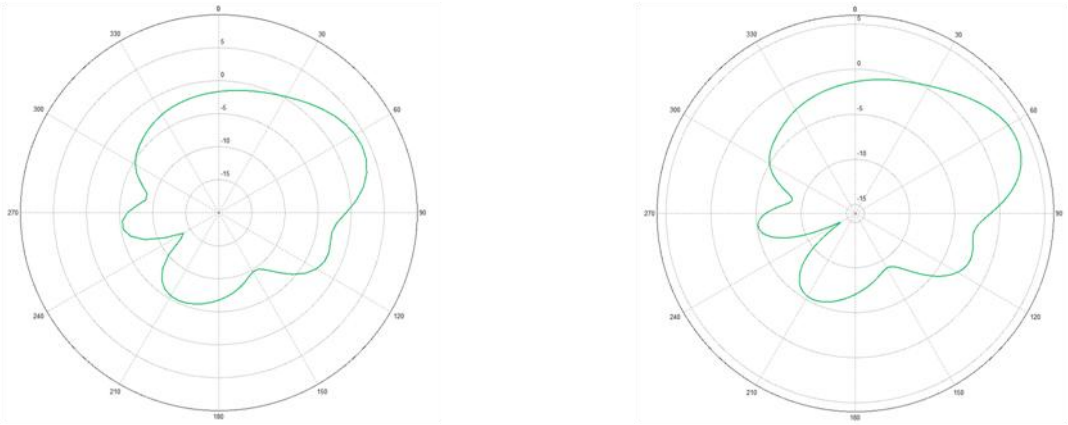


Figure 7. Simulation Mesh. Triangle edges typically λ/10 long.

The FEKO simulator has an alternative simulation option to the MoM. That option is called Multilevel Fast Multipole Method (MLFMM). MLFMM is a useful option when the structure is electrically large in wavelengths. MLFMM is similar to MoM, in that the impedance matrix models the interaction between all the basis functions. Where MLFMM differs from MoM is that MLFMM groups the basis functions and computes the interaction between groups of basis functions, whereas MoM considers interactions between every pair of basis functions. The grouping of basis functions significantly reduces the number of unknowns resulting in faster run times and a decrease in the overall memory requirements. Another benefit of implementing MLFMM is that the simulation mesh generated for the MoM does not need to be changed for the MLFMM simulation. Figure 8 illustrates the difference between a full MoM and an MLFMM simulation. This particular simulation was done with a smaller PCB board and without traces or the plastic packaging in order to keep the number unknowns within the PC capabilities. The results, although not identical, are very similar, and the ability of MLFMM to simulate larger problems outweighs the inaccuracy incurred.

Simulation Results

FEKO outputs the results of each simulation to a *.out file. The *.out file contains all of the simulation parameters, errors or warnings, currents, and the fields. Along with the *.out file, FEKO has post-processing capabilities to allow the user to view the results of the simulation graphically. A 3-D plot of the far fields generated from the 1 V excitation of the printed circuit board are shown in Figure 9.



MoM Simulation

MLFMM Simulation

Figure 8. MoM and MLFMM Simulation Comparison.

Below, we will compare slices of this 3-D pattern to measurements. The measured data are actually plots of the baseband offset voltage induced by rectification of the RF by the IC.

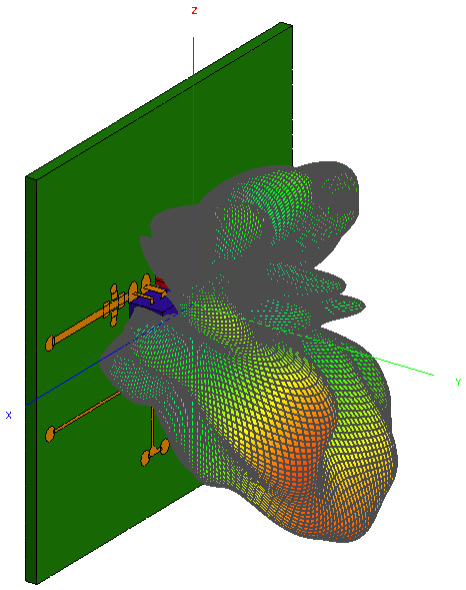


Figure 9. 3D Far Field Pattern at IC pin 2.

Figure 10 shows the far field radiated pattern of the PCB at φ = 0° and φ = 90°. By reciprocity, the receiving and transmitting pattern of the PCB are the same.

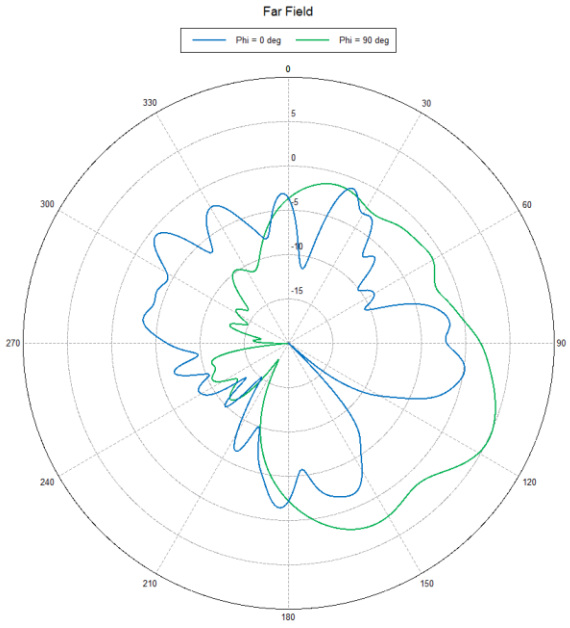


Figure 10. Far Field Radiated Pattern.

To compare the model with experimental results, the simulation results were taken at θ = 90° with the "horizontal" and "vertical" polarizations in the Eφ and Eθ directions respectively, due to the model being constructed in a different Cartesian coordinate system than the measurement coordinate system. Figure 11 and Figure 12 illustrate the electric field taken at θ = 90° for the horizontal and vertical polarizations compared with the measured data.

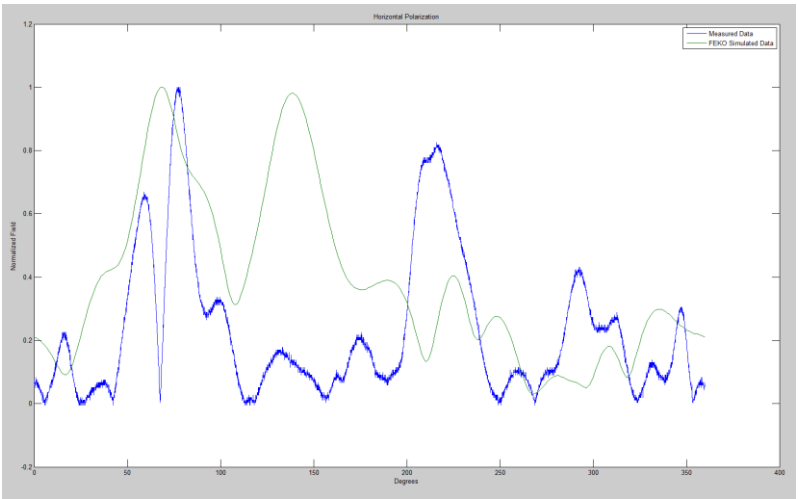


Figure 11. Horizontal Polarization. Green: Calculation; Blue: Measurement.

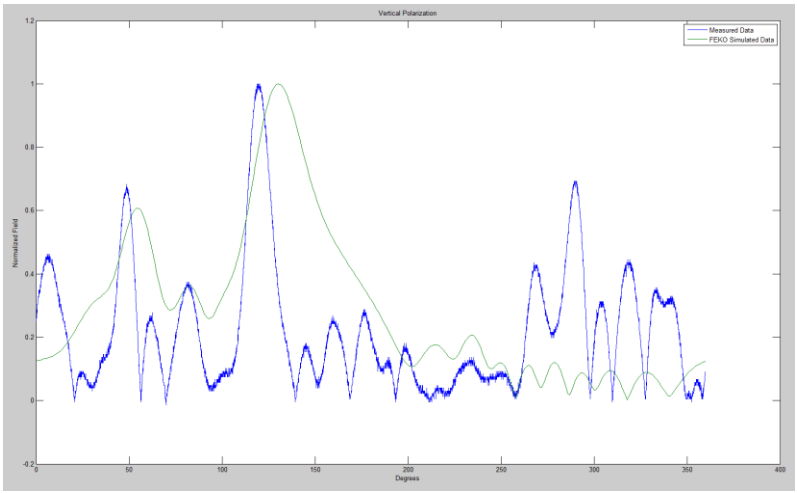


Figure 12. Vertical Polarization. Green: Calculation; Blue: Measurement.

Improvements to Model

As one can see, the FEKO simulation results do not closely match the experimental results. The measured data shows a significant response on the back side of the PCB board. The FEKO simulation shows little response on the back side of the board. This is likely due to wires and other structures that were present in the measurements but not modeled in the simulation. Another observation is that the width of the peaks on the FEKO simulation seem too wide. This indicates that the coupling features that are significant in the measurement are electrically longer than in the simulation, causing the phase to change more quickly with angle – again consistent with coupling to the physical wires that are not present in the model. As the fidelity of the FEKO model improved as we added further details of the board geometry, the qualitative characteristics of the simulation came closer to those of the measured data. Some features that are still missing from the model are the SMA connectors on the coplanar waveguide, the resistors and the leads for those resistors, and the wires connected to the board during testing. Adding the SMA connectors and the wires should allow for some coupling to the back side of the board and would decrease the angular width of the peaks. It is expected that as the fidelity of the model is increased, the simulation will continue to become more like the experimental results.

PC Board Attenuation

Once an RF signal has been coupled onto a circuit board, it must propagate along traces to reach the active electronics. Two issues are important here: first, the mode of propagation along the trace, and second, the losses incurred by that mode through both re-radiation and resistive losses in the trace and dielectric. We investigated these issues through measurement and modeling of the attenuation of a simple PC board trace configuration – the microstrip transmission line. This corresponds to the case where a trace on one side of the board is over a ground plane on the other side. The modeling results will be discussed in conjunction with the measurement results below.

Measuring propagation losses accurately at millimeter wavelengths is challenging due to the difficulty of converting the transmission line mode of the test instrument (coax or waveguide) to or from the transmission line mode of the microstrip over a broad frequency range without large reflection losses. Three approaches to implement a broadband launcher that would work up to 100 GHz were tried: a microstrip probe antenna coupled to WR-10 waveguide, a commercial coax to microstrip "spark-plug" edge launcher, and a dielectric wedge transition from WR-10 waveguide to the microstrip line on the board. Figure 13 illustrates the first approach.

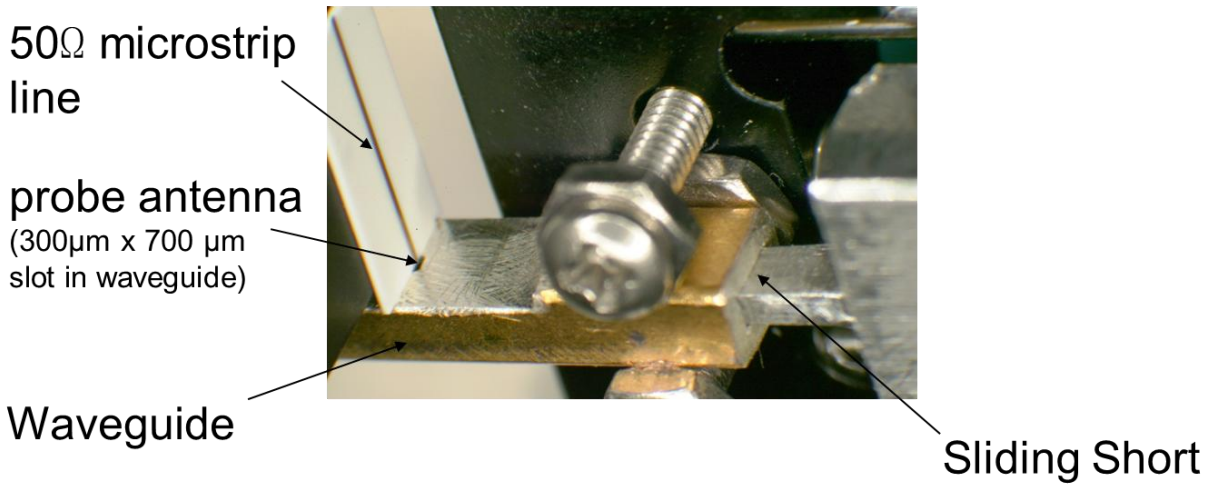


Figure 13. WR10 - Microstrip Antenna Transition.

The WR-10 waveguide runs horizontally along the bottom of the figure. A sliding short that acts as a tuner for the transition is shown on the right. The top wall of the waveguide has been thinned on the left side, and a 300μm x 700μm slot has been cut in the center. A broadband probe antenna attached to a 50Ω microstrip line on an alumina substrate extends into the waveguide through this slot and couples to the electric field in the waveguide. Our HP 8510C vector network analyzer uses WR-10 waveguide as its input and output ports in W-band (75 – 110GHz). To test the throughput of this transition method, two transitions were connected back-to-back by connecting their 10 mm long microstrip sections together. Port 1 of the 8510 fed the first waveguide, and Port 2 was fed by the second waveguide. S21 represents the loss of the two transitions as a function of frequency. The measurement setup is shown in Figure 14, and the results are shown in Figure 15.

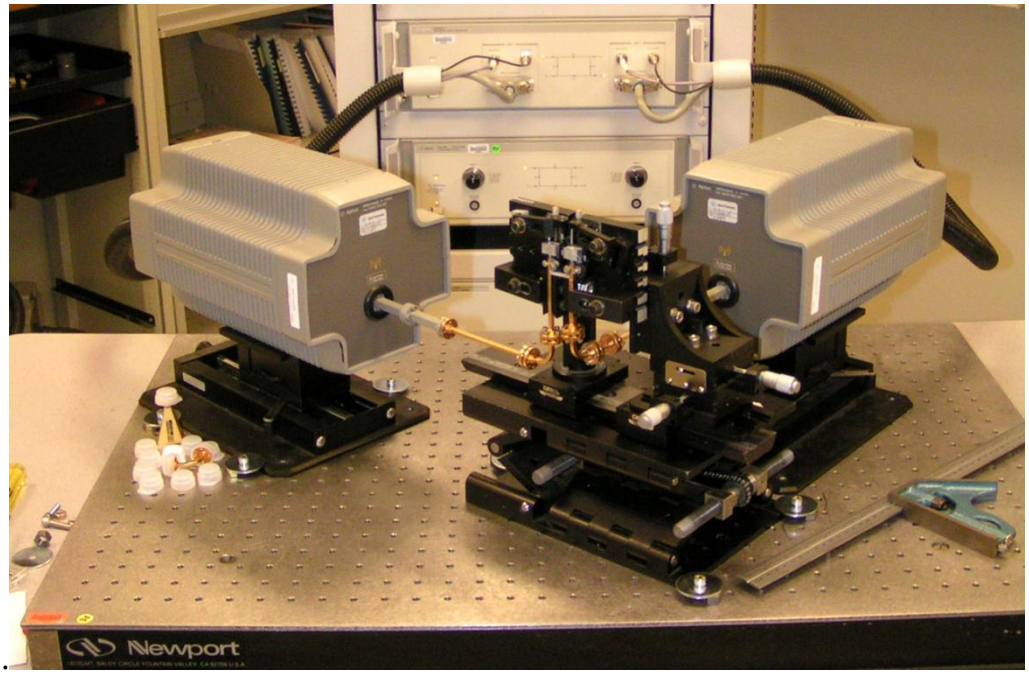


Figure 14. WG-Antenna-Microstrip Transitions Attached to W-band VNA Testsets.

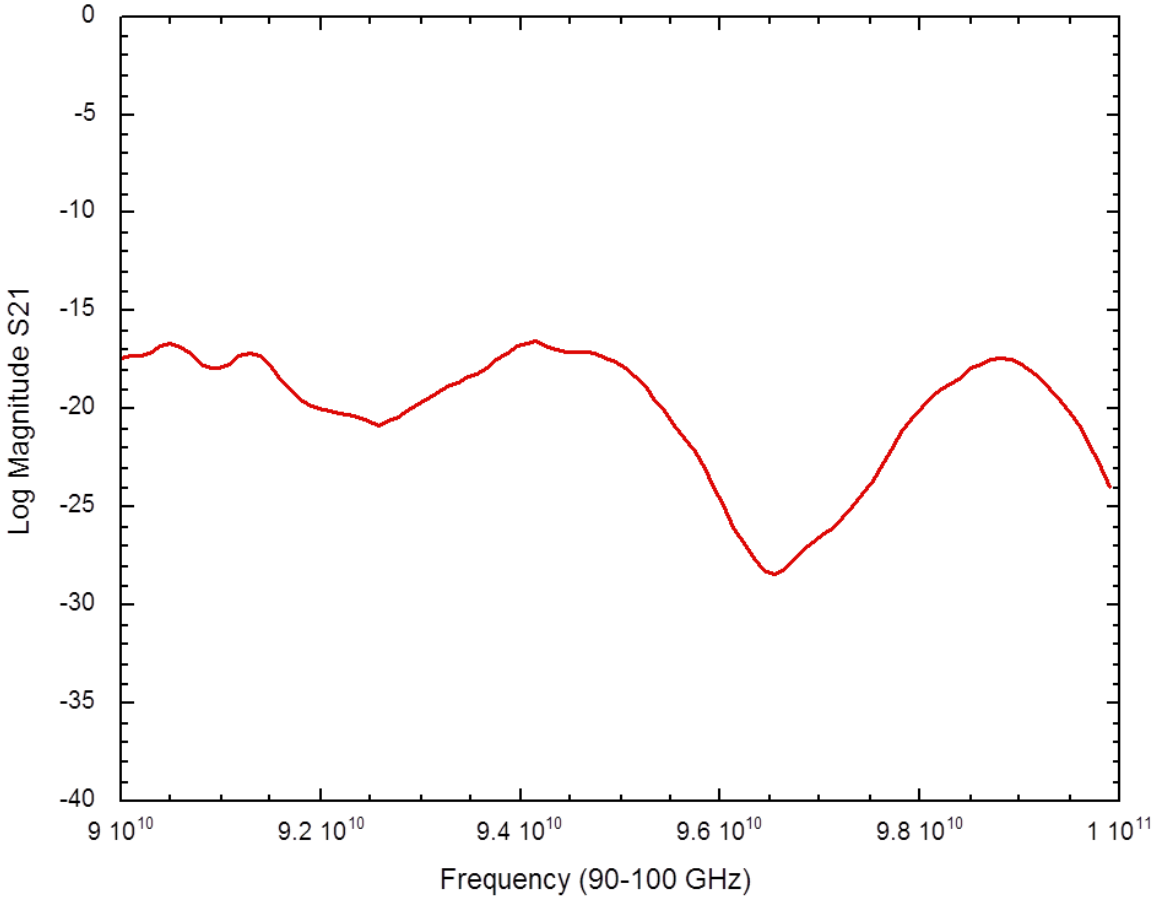


Figure 15. Thruput (S21) through waveguide transitions.

The loss is 18dB at 95GHz and is sensitive to the tuning of the sliding short. We considered this loss (60X) to be excessive.

The second approach was to use a commercial Anritsu W1-105F coax-stripline "sparkplug" launcher, shown in outline in Figure 16.

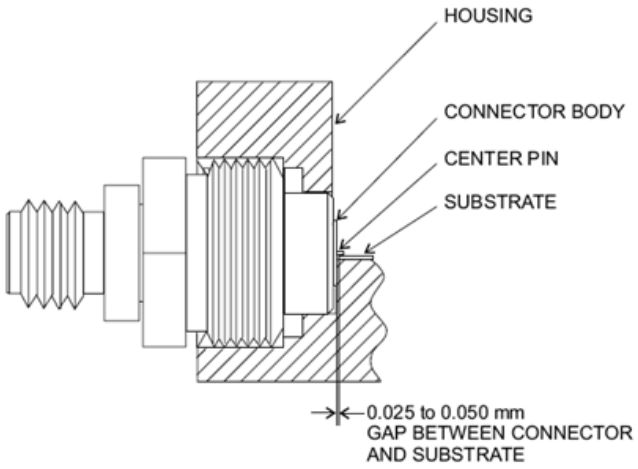


Figure 16. Anritsu "Spark-plug" Coaxial Launcher.

This launcher converts from coax to microstrip, launching into the microstrip from the edge of the board. A photograph of two of these launchers connecting to and from a microstrip line in a test fixture is shown in Figure 17.

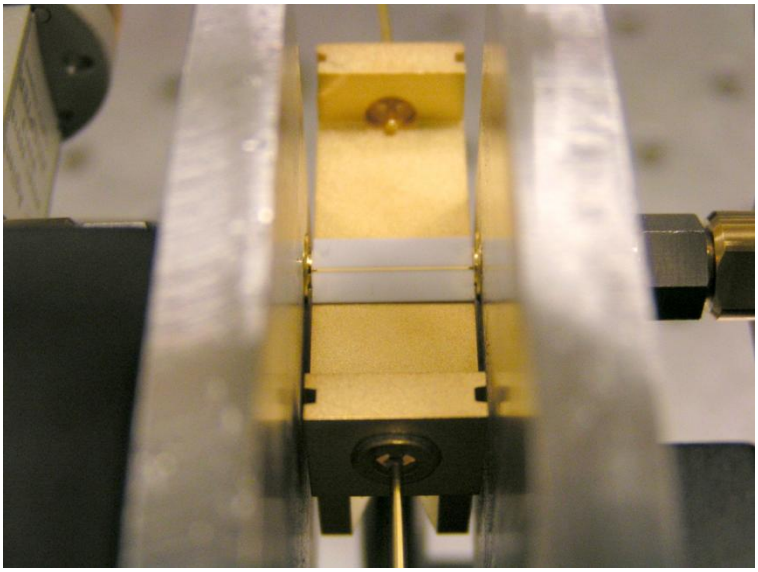


Figure 17. Coax - microstrip transitions using the Anritsu launchers.

Since the launchers convert from coax to microstrip, the 8510 ports were converted from WR-10 to coax using HP W281D waveguide-coax adapters. The test setup is shown in Figure 18.

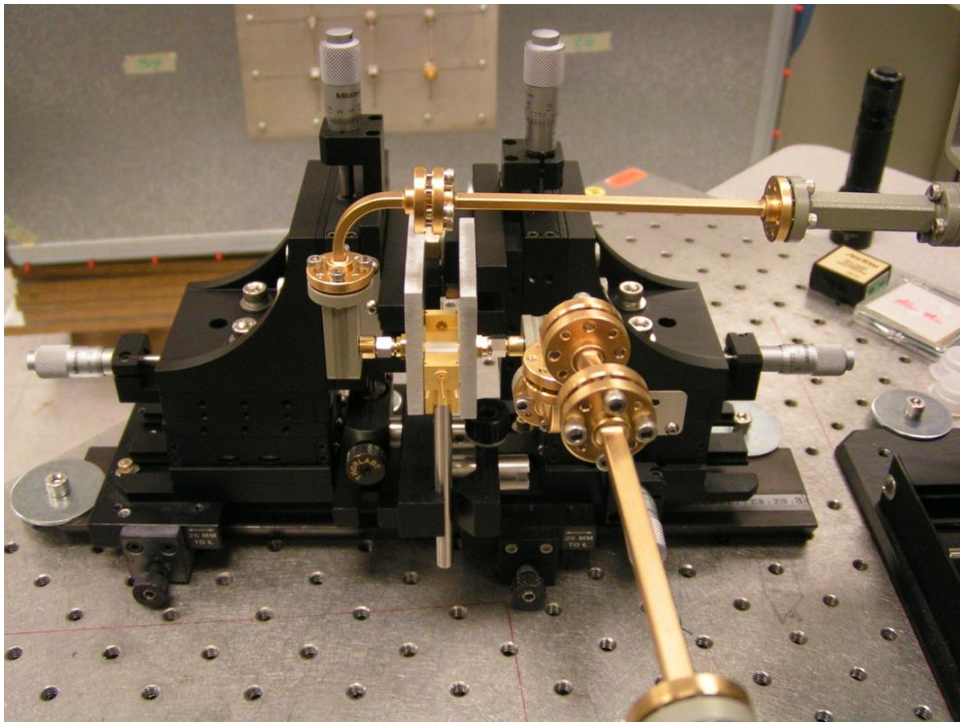


Figure 18. Waveguide-Coax-Microstrip Transitions Attached to W-band VNA Testsets.

Measured results for S21 are shown in Figure 19.

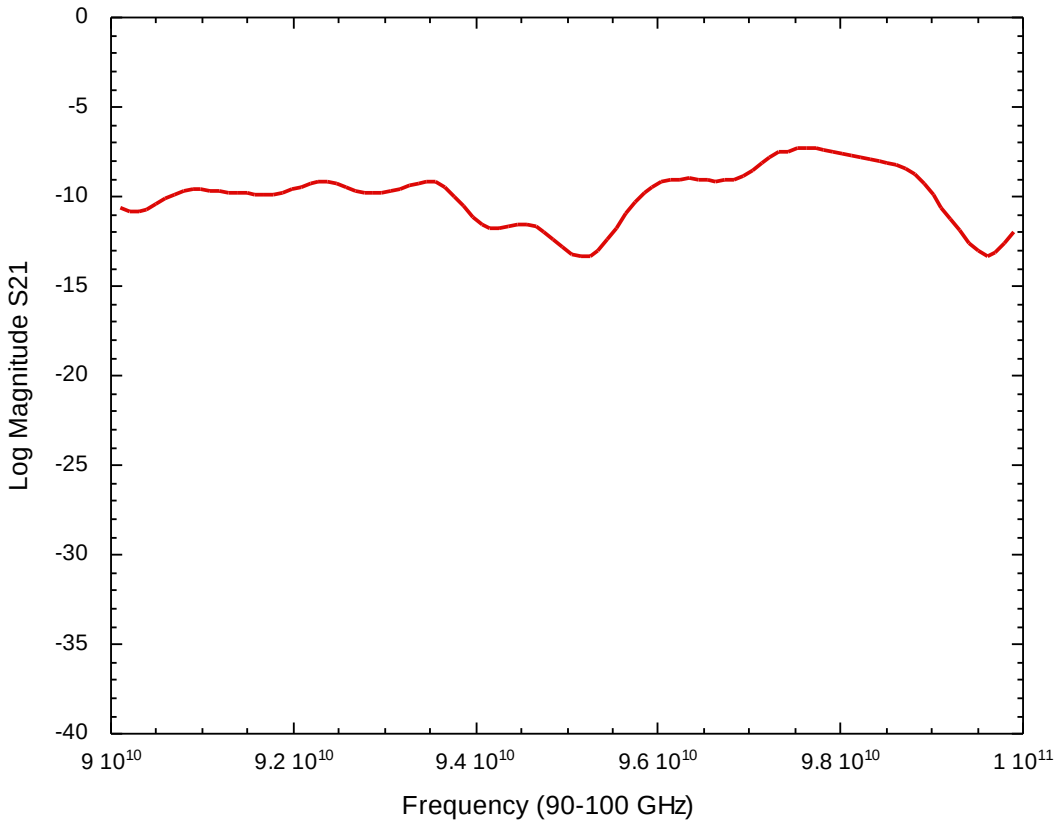


Figure 19. Measured Thruput for waveguide-coax-microstrip adapters.

The loss is 13 db at 95 GHz. This loss includes the loss of one 10 mm section of alumina microstrip line.

Measurements of various lengths of microstrip line indicated that the losses were dominated by the transisitions, making measurement of the propagation losses by themselves very difficult. This led to a third approach: a dielectric wedge transition from the interior of the waveguide to the region underneath the microstrip. This approach gradually transitions the TE_{10} mode in the waveguide to the TEM microstrip mode. A photo of the test setup is shown in Figure 20.

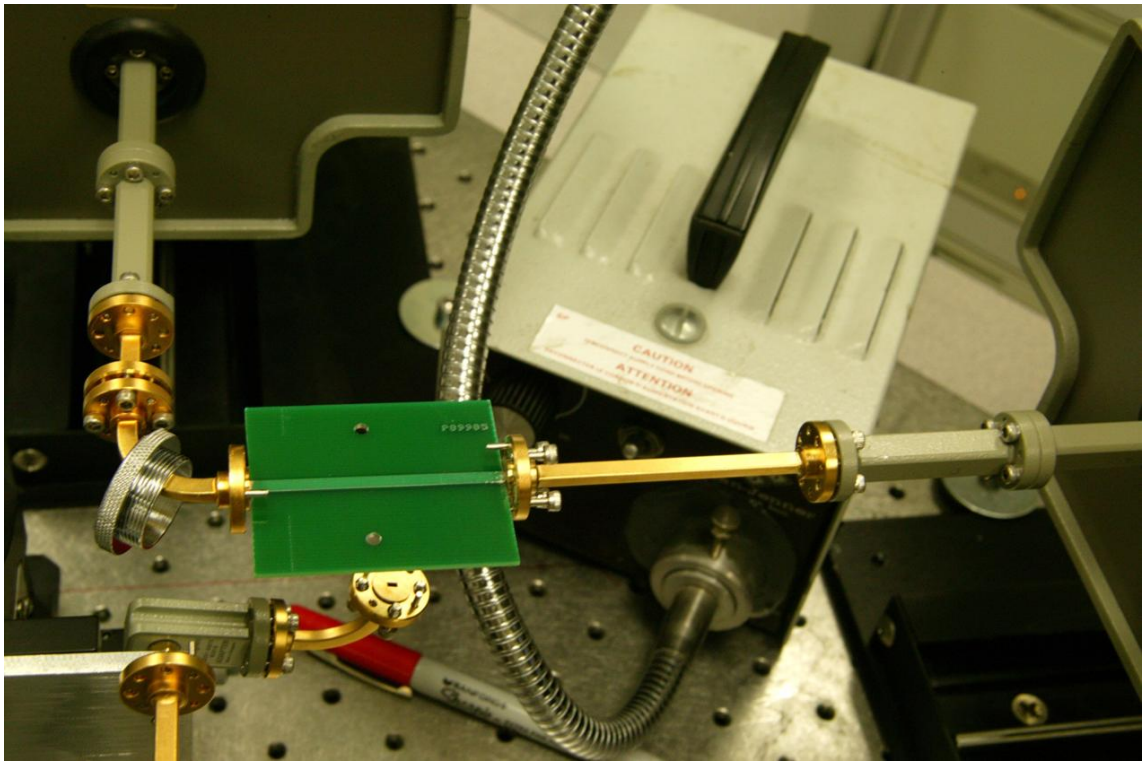


Figure 20. Dielectric wedge transitions from WR-10 to microstrip and back.

Figure 21 shows a close-up of the wedge, which is made from the fiberglass circuit board dielectric material. This relatively simple transition was surprisingly effective.

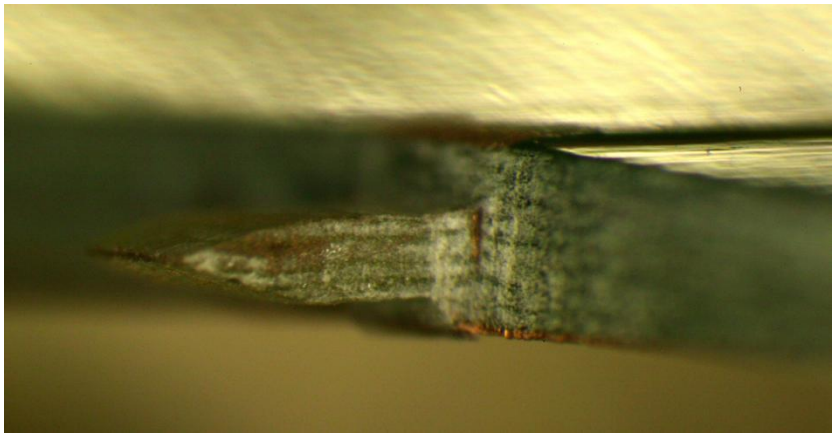


Figure 21. Greatly Enlarged Photo of Dielectric Wedge.

Figure 22 shows an HFSS model of such a microstrip transmission line.

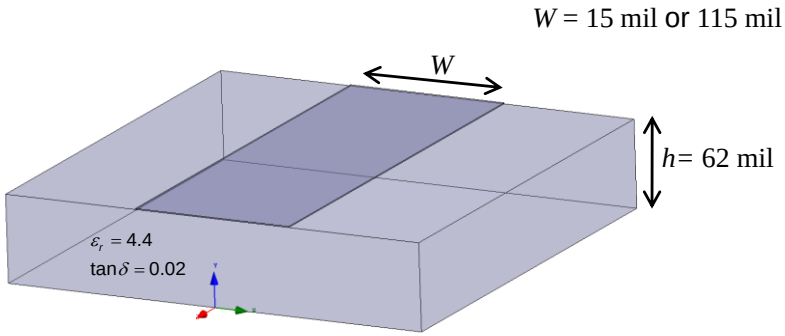


Figure 22. HFSS model of a microstrip transmission line.

The dielectric modeled for the microstrip line is FR-4, a fire-resistant fiberglass often used in low-frequency printed circuit boards. The electrical parameters for FR-4 are assumed to be as shown in the figure. To approximate the effect of the surface roughness of rolled copper, the conductivity of the trace is assumed to be $3x10^8$ S/m. Figure 23 shows a parametric study of the microstrip loss in dB per mm of line for two line widths and four values of the loss tangent. The full-wave HFSS calculations are superposed on the measured loss. The spikes in the measured data are artifacts caused by the inaccuracy of taking the difference of two large attenuation numbers at those frequencies. Note the very sensitive dB/mm scale.

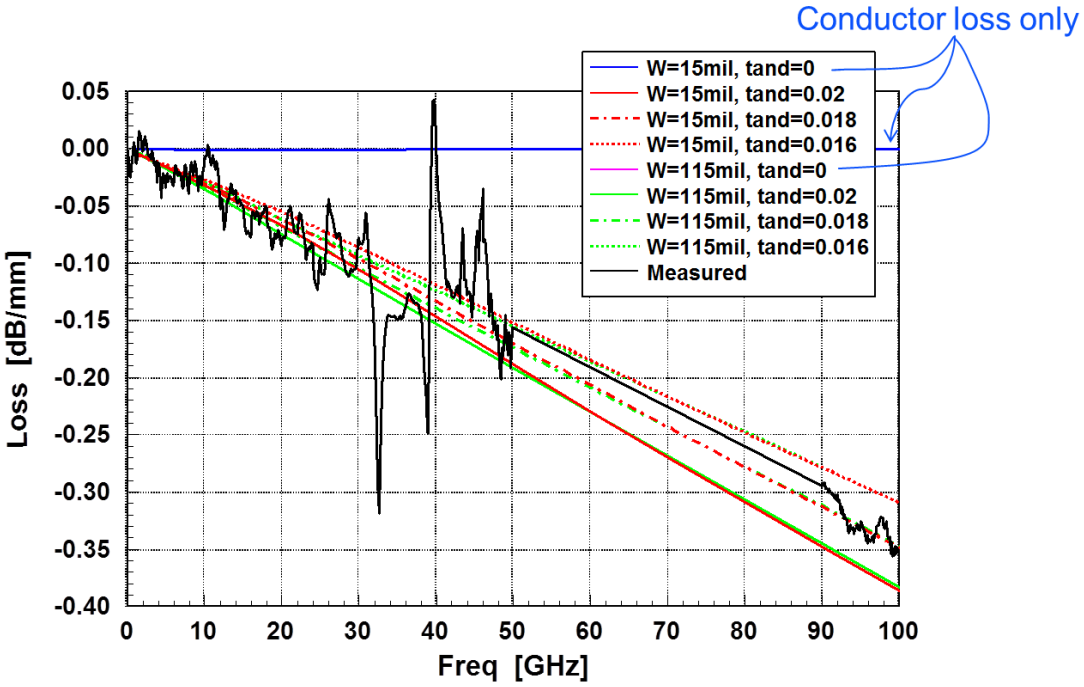


Figure 23. Parametric Study of Microstrip Loss, with Measured Data.

These results clearly show that the loss on a microstrip line fabricated on a 62 mil thick FR-4 substrate is dominated by dielectric loss for frequencies above 2 to 3 GHz. As such, the loss in the dominant microstrip mode is nearly independent of the strip width. The dielectric loss for a perfect TEM mode *is* independent of the transmission line geometry.

DEVICE INTERACTION

A natural first question to ask is, "Are RF effects on semiconductor devices not already well understood?" For this problem, where the response of a circuit to energy that is outside of its designed operating band, the answer is no. Normal circuit simulators treat both active and passive devices as circuit elements, with dimensions that are insignificant when compared to wavelength. RF design codes account for the high-frequency response of components, but the systems of interest to this project are not intentionally-designed millimeter wave RF circuits with well-controlled transmission lines and parasitic inductances and capacitances. The simulation of these circuits and components is pushed to far above their usual design frequencies in this wavelength regime. Package parasitic inductances and capacitances, when they can even be defined meaningfully, are important and may dominate the response. The nonlinear behavior of semiconductor devices interacting with these parasitic inductances and capacitances can lead to the generation of subharmonics as well as of harmonics of the threat waveforms. The subharmonics can be within the operating bandwidth of the system. As the disturbing amplitude increases, circuit disruption may occur and then disappear as competing mechanisms within the system come into operation.

Ideally, we would quantify the package RF parasitics for a device, model the device physics using the coupled partial differential equations that describe the carrier densities and fields in the device, and then compare the results to measurements. This has not been practicable, even in a very simple case, due to the fact that the detailed construction – doping levels and detailed geometries – for commercial parts are simply not available. A program to produce custom parts and characterize them is possible, and is being pursued in the broader RFDE community, but it is expensive and time consuming. For this program, we have attempted to correlate RF effects simulations and measurements of junction diodes and bipolar junction transistors in a qualitative way.

Diodes

As our first example, a very simple system consisting of a junction diode mounted in a 50Ω-microstrip line was measured and simulated. The diode is the simplest semiconductor device, and the microstrip line provides a well-controlled RF environment from which to drive the semiconductor and to measure its response. Originally, we chose the common 1N914 switching diode as our example. It turns out that this diode's behavior is significantly more complex than a simple pn junction diode, because it is doped with gold to increase its switching speed. Gold doping reduces the minority carrier lifetime, increasing the switching speed, but it also introduces a relaxation behavior, its trapping centers behaving like the radiation induced traps described in (McPherson, 2002). This is the reason for the relatively poor agreement seen in this project's first year between the measured harmonic generation and the harmonic generation predicted by the Spice diode model, even though the Spice model used *measured* diode parameters and parasitics. The Spice models, even the one provided by the manufacturer, simply do not include this relaxation physics.

To clarify this and to validate our semiconductor device physics model, we measured and simulated a more standard pn-junction device without the gold doping. We first compare

simulation results to an analytic diode example from (Hodges and Jackson, 1988). This device is four microns thick, with the junction located at two microns. Both the analytic and our numerical model assume one-dimensional behavior, as indicated in Figure 24. In the plots below, the lightly doped p-region is on the left, and the heavily doped n-region is on the right. Figure 25 shows the doping profile for this example. Figure 26 shows the numerical calculation of the uncovered charge in the depletion region for 0 V applied to the diode, the equilibrium state. This is a logarithmic plot of the number of charged ions per cubic centimeter versus distance x into the diode.

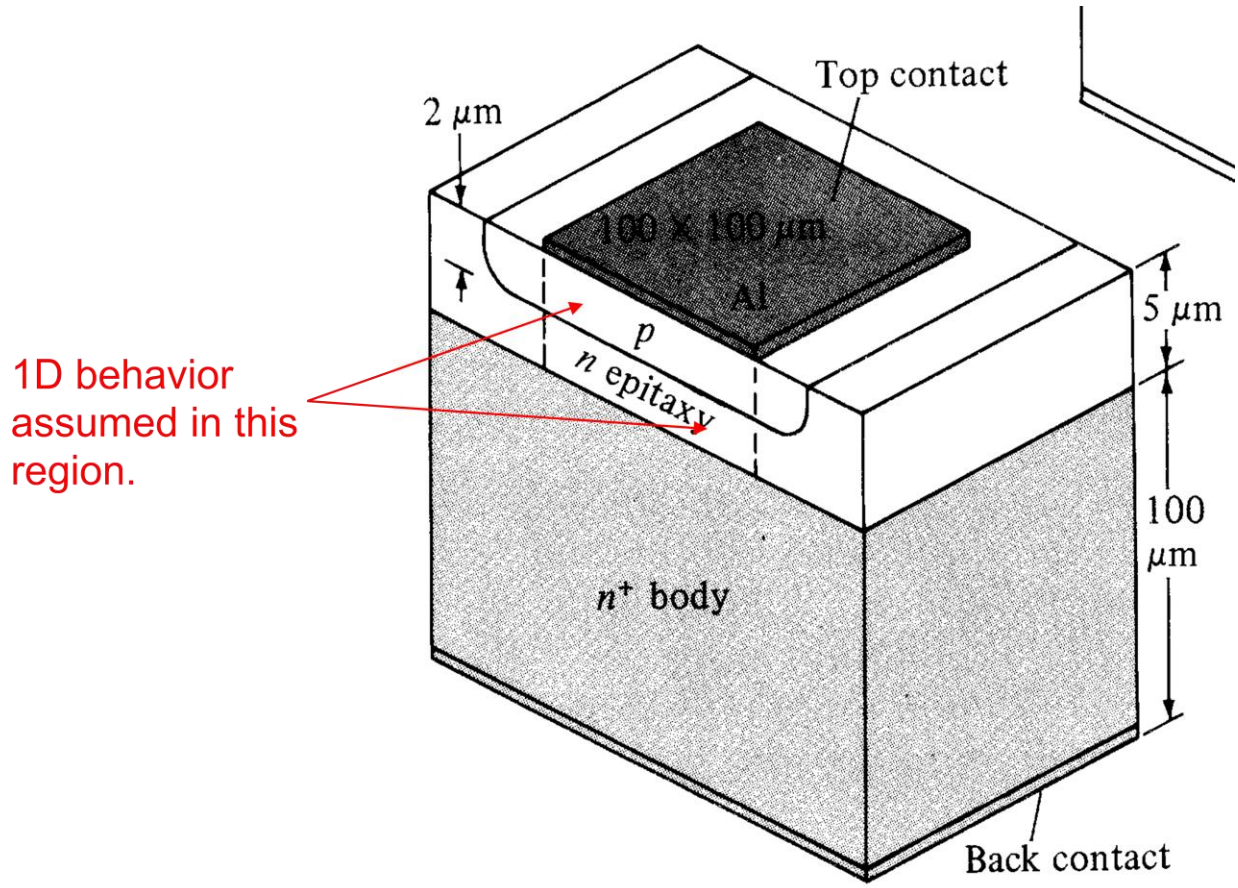


Figure 24. One dimensional diode model derived from 3D device. From Hodges and Jackson, 1988, p. 114.

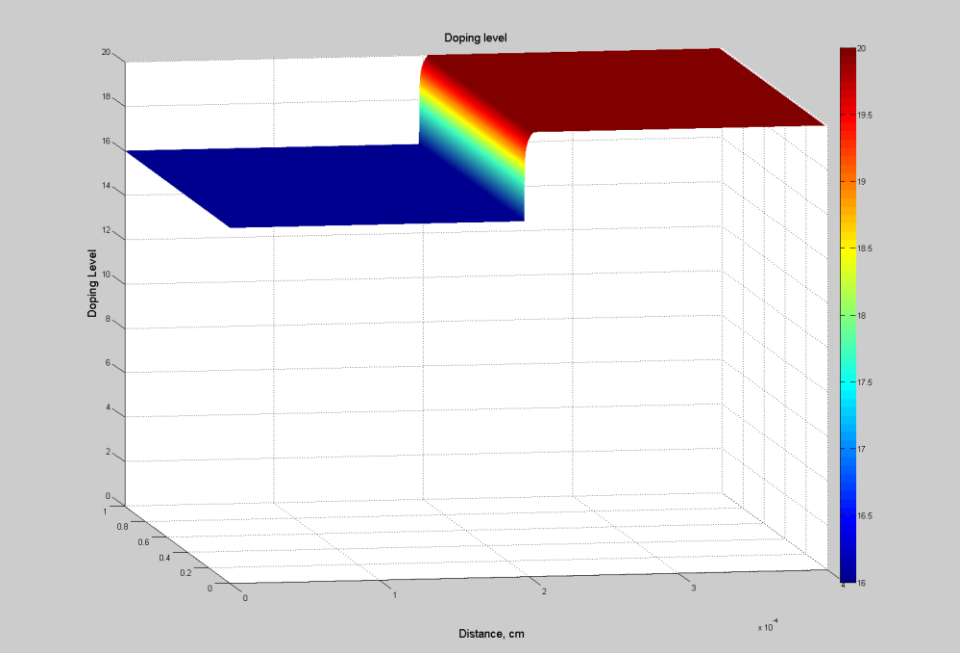


Figure 25. Example Doping Profile.

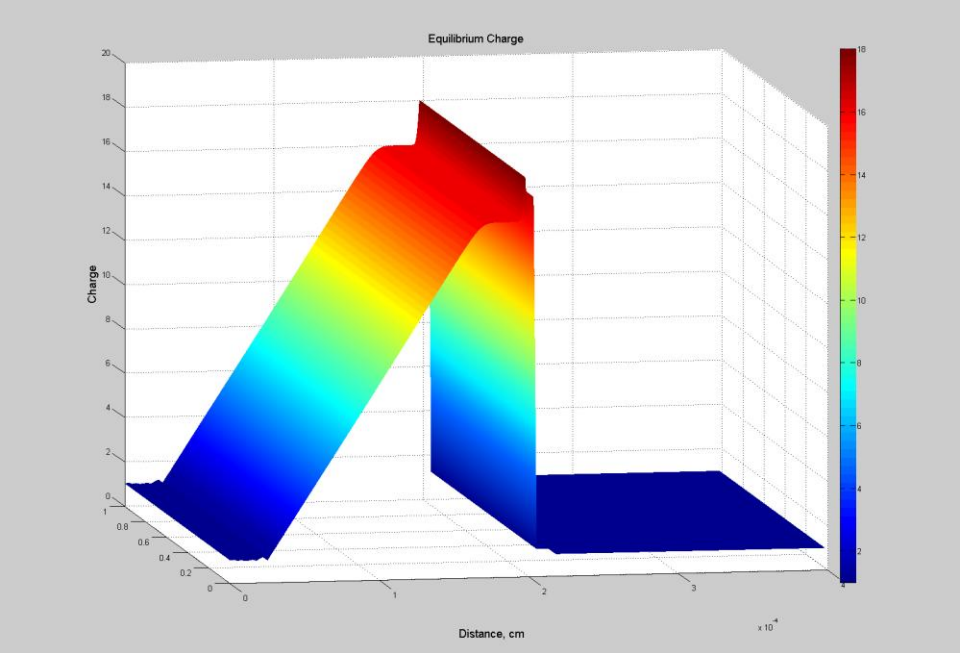


Figure 26. Uncovered Charge Density at Equilibrium.

x=0 corresponds to the positive anode contact, x=2 microns (2e-4 cm) is the junction, and x=4 microns is the negative cathode contact. The gradient of the carrier densities caused by the abrupt change in doping level causes diffusion currents, with holes moving to the right and electrons moving to the left. These currents ionize the dopant atoms on each side of the junction, leaving exposed negative charge on the left and positive charge on the right. The junction region has its mobile charge carriers depleted, forming the depletion region, which extends primarily into the more lightly doped side. The process of exposing more and more fixed charge in the depletion

region continues until the electric field created by these fixed charges creates a drift current in the opposite direction that just balances the diffusion current. The width of this depletion region depends on the voltage applied to the diode. A reverse bias increases its width; forward bias decreases it. Looking at Figure 26, the flat region at a height of 16, corresponding to the logarithm of 1e16 per cubic cm, is the depletion region. The doping level N_A in the p region is 1e16 per cubic cm. To the left in the figure, the charge density falls off linearly on a log plot. That is an exponential dependence on distance, as simple analytic theory predicts. It falls off much faster on the right because the n region is much more heavily doped; N_D is 1e20 per cubic cm. The spike in the depletion region is caused by the injection of electrons from the n region due to the very high concentration gradient. This is not present in the simple analytic theory. The assumptions of the analytic theory would show charge density only in the depletion region, with a vertical drop in density on both sides. Figure 27 below shows a similar plot for the voltage applied to the diode of -5 V, that is, reverse bias. Note that the depletion width has extended further to the left, as it should for reverse bias.

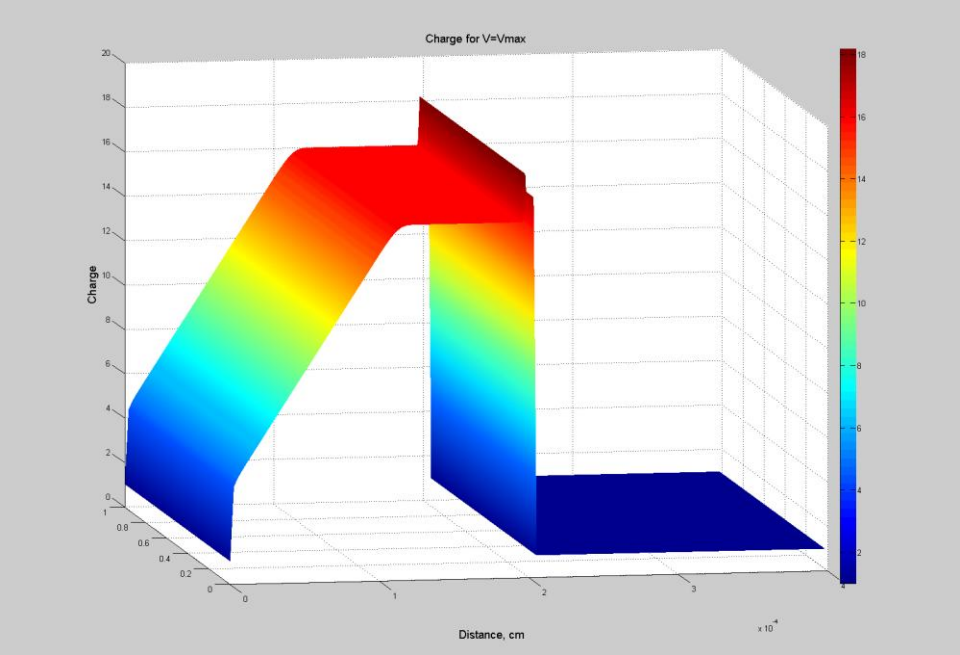


Figure 27. Uncovered Charge Density for 5V reverse bias.

We can compare the numerical calculation with the analytic results presented in Example 4.1 of (Hodges and Jackson, 1988). In Figure 28 below, the total stored charge in the diode is plotted as a function of the applied voltage, using both the numerical and analytical results. The numerical results do not include the electrons injected into the depletion region (the spike in the previous figures), since this is neglected in the analytical approximations. The two curves agree quite well, with the numerical result at a slight offset above the analytical approximation. The numerical result may actually be more accurate due to the simplifying assumptions of the analytical method.

The absolute value of the slope of this curve as voltage increases is the junction capacitance C_j. The numerical and analytical values for C_j are shown in Figure 29. Again, the agreement is very

good, except for small applied diode voltages where the difference in stored charge is a larger fraction of the total than at larger voltages.

Being able to predict the voltage dependent capacitance is the first step in predicting the response of semiconductor devices to applied RF voltages.

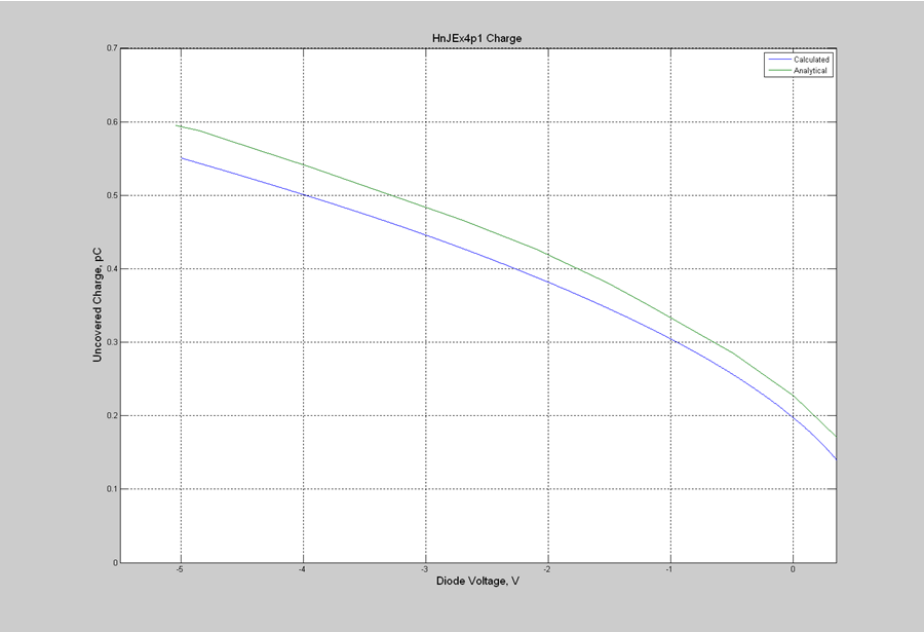


Figure 28. Total Stored Charge versus Applied Voltage.

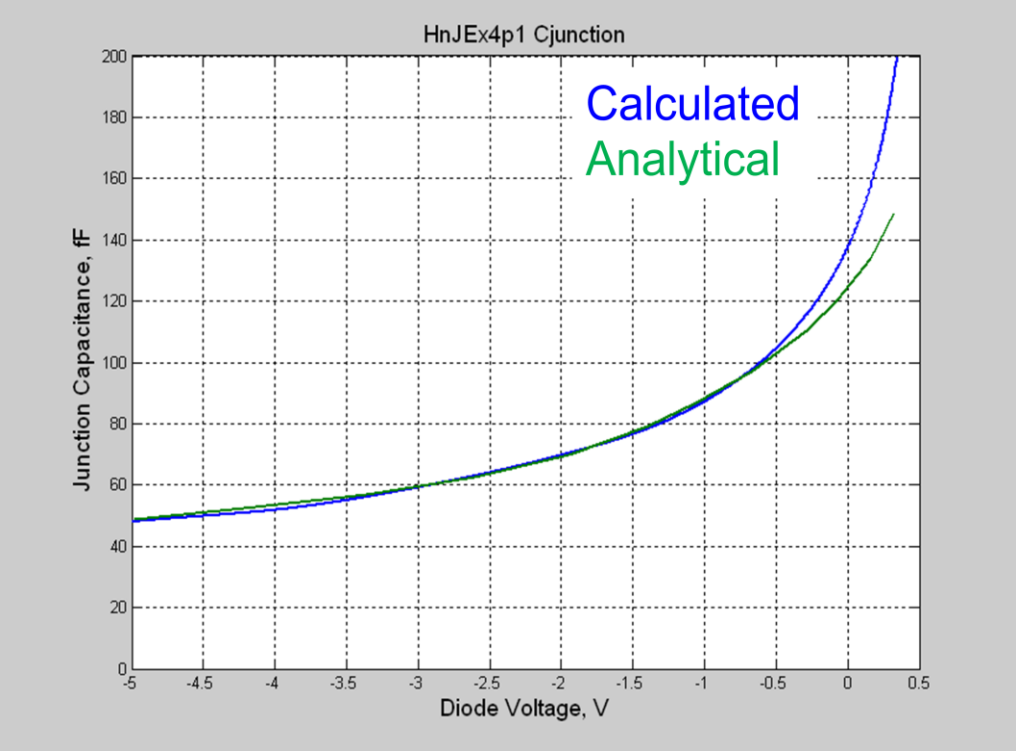


Figure 29. Nonlinear Capacitance.

Diode Experimental Characterization and Spice Modeling

The Spice diode modeling consists of using a standard Spice diode model to represent the semiconductor and passive elements to model the external package parasitic elements. Figure 30 shows a generic layout of both the Spice diode model and external passive elements. Lead inductance and stray capacitance can be modeled with parameters CA0, CCO, and LSA. These parasitic parameters, although not related to the semiconductor physics, are not totally separable from the semiconductor, because they are all in the same package. In a first order approximation, however, these elements can be thought of as independent from the semiconductor. The diode's semiconductor parameters can be modeled by the Spice model parameters Is , Rs, N, Tt, Cjo, VJ, M, and FC.

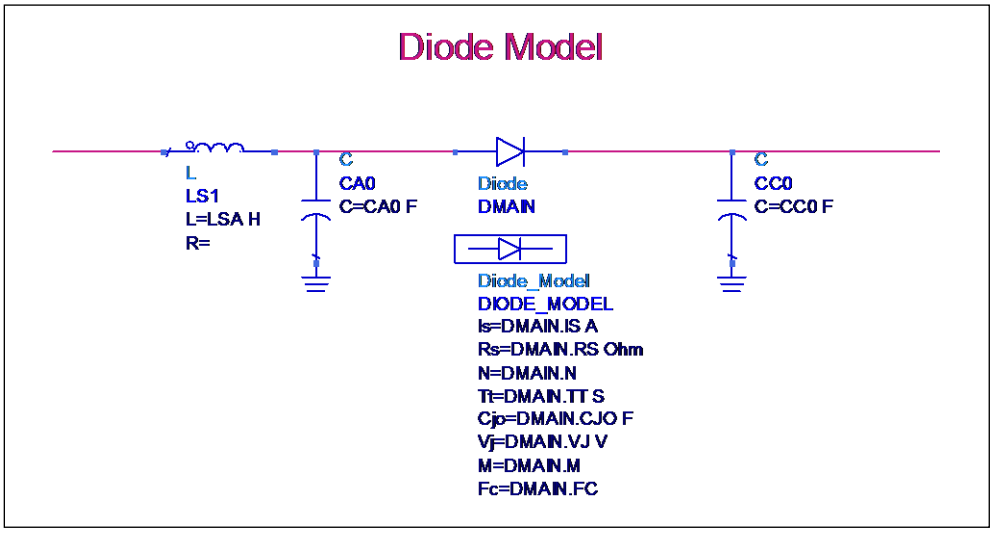


Figure 30. Generic Spice Diode Mode with parasitic elements

Spice Diode Model Parameters and equations

The Spice diode model consist of both DC and AC models. The DC model is independent of the AC model. The AC model, however, relies on the DC parameters to properly determine the diffusion capacitance.

Spice Diode DC Model

The Spice diode DC model simply models the non-linear interaction between the DC current and voltage through the diode. The DC current can be expressed with the following equation:

$$Id = Is \cdot \left(e^{\frac{Vd}{N*vt}} - 1 \right) \quad \textbf{(1)}$$

where Vd is the diode voltage, N is the ideality factor, and vt is the thermal voltage.

The current Id is only part of the story, because at high currents there is a voltage drop in the neutral regions of the diode. This drop causes only a limited amount of the voltage applied to the diode to appear across the pn junction. This limits the amount of DC current through the diode. Therefore, the expression for the actual voltage across the pn junction is:

$$Vd' = Vd - Rs \cdot Id \quad \textbf{(1a)}$$

where Vd' is the voltage dropped across the pn junction and Vd is the voltage applied to the leads of the diode. To correctly model the diode Vd' needs to replace Vd in Equation **(1)**.

Spice Diode AC Model

The Spice diode AC model is centered on the non-linear charge storage (capacitance) seen across the diode. The model separates the capacitance into two distinct regions of interest, which are reverse and forward bias. The definition of these two regions is summarized by

$$Vd < FC \cdot Vj \quad \textbf{(2)}$$

or

$$Vd > FC \cdot Vj \quad \textbf{(3)}$$

Where FC is a fitting coefficient and Vj is the junction potential. The value for FC is normally around 0.5, thus the dividing line between the two regions typically becomes half of Vj. The capacitance in the reverse region, called the junction capacitance, is caused by N and P type donors, which are separated by the distance associated with the space charge region. As negative voltage is applied to the diode, the space charge region expands, as discussed above, and the N and P type donors become further apart, lowering the capacitance. This is similar to a normal capacitor where:

$$C = \frac{\varepsilon \cdot A}{d} \quad \textbf{(4)}$$

If $\varepsilon \cdot A$ is constant and the distance, d, increases, the capacitance decreases. Unlike an ideal capacitor, the diode's behavior is a non-linear function of capacitance with respect to voltage. This behavior is captured by the Spice model in the following equation:

$$Cj = \frac{CJO}{\left(1 - \frac{Vd}{Vj}\right)^{M}} \quad \textbf{(5)}$$

The junction capacitance is similar to the ideal capacitor, but the capacitance changes as function of the diode voltage, which moves charges non-linearly with respect the grading coefficient, M. The constant CJ0 is the zero-bias Junction capacitance and is defined as the capacitance when Vd is equal to zero. The junction capacitance is only valid in the region where $Vd < FC \cdot Vj$.

For the region where $Vd > FC \cdot Vj$, the junction capacitance contribution becomes negligible and major contributor is diffusion capacitance. Diffusion capacitance is caused by minority carrier charges, either holes in the N-doped region or electrons in the P-doped region, which were injected across the space charge region. Since it takes a finite time for the injected minority carriers to recombine, there is a finite time where minority carries exist in the oppositely doped region, causing charge separated by distance and, thus, capacitance. The Spice definition for this capacitance is:

$$Cd = Tt \cdot \frac{Id}{vt \cdot N} \quad \textbf{(6)}$$

where Tt is the transit time. The mechanism for the diffusion capacitance charge storage is highly non-linear, which can be seen in the equation **(6),** because it is a function of the diode current, Id. Also, the charge storage has a significant effect on how fast the diode can turn off, since the device is limited by how long it take the majority carriers to recombine.

Measurement Approach

Diode characterization consisted of using various instruments and software packages for measurement and model fitting. The two software packages used for this characterization were Agilent's IC-Capture (IC-CAP) and Agilent's Advance Design System (ADS). IC-Cap is a measurement collection and model fitting program, where all of the measurement gathering, with the exception of the harmonic data, was done. The measurements included DC currents and voltage, capacitance, and S-parameter data. This data was then fit in IC-CAP to a Spice model. The harmonic data was also fit in IC-CAP, although it was not directly measured in IC-CAP, and had to be manually collected and then manipulated with the help of ADS. ADS software was not only used for the harmonic data, but was also used to determine the proper topology for the parasitic elements of the diode, such as lead inductance and stray capacitance. ADS was also used by IC-CAP to perform harmonic balance simulations not native to IC-CAP or Spice. IC-CAP would send the Spice model to the ADS engine, which would run the harmonic balance simulation and feed the data back to IC-CAP for model fitting.

DC IV Measurements

The DC current and voltage measurements were done in IC-CAP using an external current/voltage source, the HP4142. Forward and reverse current measurements were taken over regions specific to the diode. In general, the reverse current measurements are taken from 0 Volts to the part's break down voltage. For the forward current case the voltage starts at 0 Volts and continues until high-level injection, where the current starts to roll off with voltage due to the presence of an electric field in the neutral region. From these two measurements the ohmic resistance (Rs), the saturation current (Is), and the emission coefficient (N) can all be extracted. In IC-CAP the extraction is done by graphically comparing the measured data to the Spice model while varying the dc parameters Rs, Is, and N for best fit.

Non-linear Capacitance

The non-linear capacitance measurement in IC-CAP only measures the junction capacitance and not the diffusion capacitance, which is treated later during S-parameter measurements. The junction capacitance was measured using a HP4275A LCR meter, and the measurement returned the capacitance vs. voltage from reverse to zero bias. From this information the zero bias junction capacitance (CJO), the grading coefficient (M), and the junction potential (Vj) were extracted. It should also be noted that the junction capacitance is an exponential function of voltage as stated above, which is highly dependent on the grading coefficient. This coefficient describes how the junctions are transition from the P-N regions at the metallurgical junction, but also brings some practical understanding of how the junction capacitance works.

Consider equation (5). If M were equal to zero, then the junction capacitance would be CJO regardless of voltage. For most cases, however, M is between zero and one half depending on the grading of the junction.

S-parameter measurement

S-parameter measurements are used by IC-CAP to determine parasitic elements of the diode, such as lead inductance and stray capacitance along with the diode semiconductor physics parameter transit time (Tt). The HP8510 network analyzer was used by IC-CAP to get the S-parameters in conjunction with the HP4142 to step the bias. The S-parameter measurements were broken up into two regimes, where the diode is reversed biased or forward biased. In the reverse bias region CA0 and CC0 can be extracted and in the forward bias region the transit time (Tt) and Ls are obtained. In the reverse bias region there is no significant current flow and the diode model reduces to the junction capacitance and the stray parasitic capacitance as can be seen in Figure 31. The S-parameters are then fit to the diode model and CAO and CCO are extracted. In the

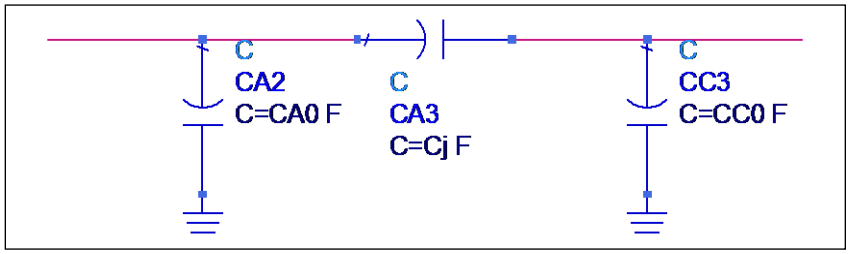


Figure 31. Equivalent circuit of diode model in reverse bias

forward bias region, current flows through the diode and through the parasitic inductor Ls. With forward bias, a build-up of minority carriers trying to recombine creates capacitance across the diode. As was stated earlier, this diffusion capacitance (Cd) is associated with the time it takes for carriers to recombine and evacuate the neutral regions. This time is the transit time (Tt) and is related to the diffusion capacitance by Equation 6 $Cd = Tt \cdot \frac{Id}{vt \cdot N}$ **(6)**. The measured forward bias S-parameters are then compared with the Spice diode model and optimized for the best possible match of Tt and Ls.

1N914/1N4148 Characterization

The 1N914 and 1N4148 are gold doped diodes, which are fast switching diodes, typically used for high voltage suppression or other fast switching applications. Since the 1N914 and 1N4148 diodes are interchangeable in almost every application, 1N914 will be used to describe the function of both diodes. In the 1N914, gold doping is used in the neutral regions. This adds recombination centers, lowering the amount of time it takes for recombination and enhancing the switching speed of the diode. This gold doping also affects the device physics of the diode making it less suited for the generic Spice diode model, and harder to fit. The areas of concern and the characterization of the 1N914 will be shown below.

1N914 DC Characterization

The DC characterization of the 1N914 is fairly straight forward. The diode current is measured as function of the voltage and parameters Rs, Is, and N are extracted. Figure 32 shows the measured vs. modeled fit for the forward and reverse bias regions.

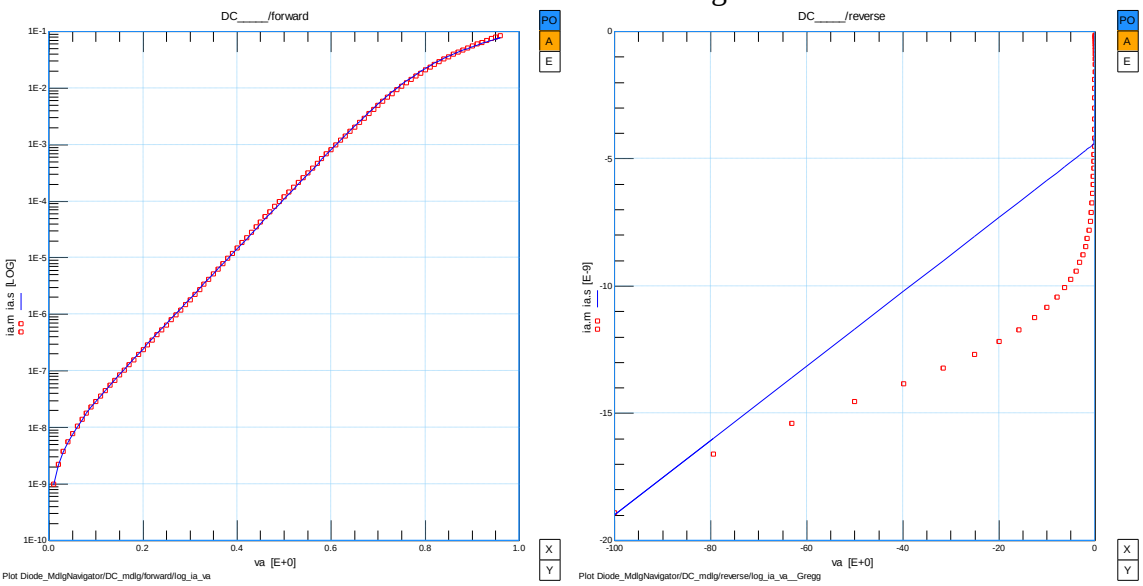


Figure 32. Forward and Reverse Current vs. Voltage (Red Square-meas.; Blue line-sim.)

$$Id = Is \cdot \left(e^{\frac{Vd}{N*vt}} - 1 \right)$$

Since the reverse current does not asymptotically approach zero as equation (1) would suggest, another parameter, Rrev, must be added between the anode and cathode to force the reverse leakage current to more closely model the 1N914's operation. However, since the leakage current is exponential, the linear resistor only approximates the physics of the device. The leakage current is small (~nOhm), and therefore the value of Rrev becomes quite large (~GOhm in this case). This large value of resistor helps to model the leakage current, but since it is so large is often not useful for Spice simulations because it is considered an open circuit.

1N914 Non-linear Capacitance

The 1N914's capacitance parameters are much harder to pin down than the DC parameters. The diode capacitance in the reverse bias region is a function of CJ0, Vd, VJ, and M, but as it transitions to forward bias it becomes more of a function of Id, FC and Tt. In addition to modeling the capacitance in the reverse bias, forward bias and transition region, there is the effect of the gold doped neutral regions which is not accounted for in the Spice model. The measurements were taken using IC-CAP and a HP4275A LCR meter at 1 MHz with a 10mV peak to peak ac voltage and while stepping the DC bias.

As seen in Figure 33, the model fits the diode measurements well in the reverse bias region and poorly in the forward bias region. In reverse bias, CJO is easy to extract, as it is just the value of capacitance when the diode voltage is zero volts. However, it is hard to determine M and VJ, because not only do they determine the slope of the capacitance in reverse bias, but VJ along with FC determines when the model switches from junction capacitance (Cj) to diffusion capacitance (Cd), as described above.

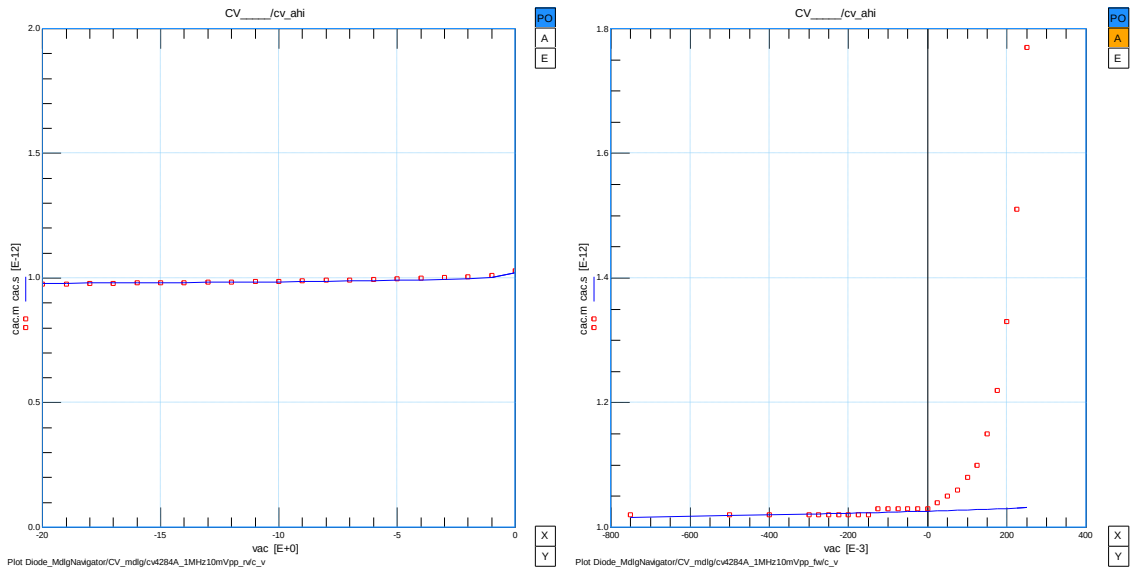


Figure 33. Diode capacitance--reverse bias (left) and forward bias (right) (Red Square-meas.; Blue line-sim.)

The forward current can be forced to fit the exponential slope seen in the figure, by manipulating Vj, M, Fc, and TT, but this is not advisable, since it causes a non-realistic fit of S-parameters and spectrum data.

1N914 S-parameter data

S-parameter data was collected from the 1N914 using IC-CAP and both an HP8510 network analyzer and an HP4142 current source. Bias was stepped from the reverse to forward conduction while S-parameters from 0.4 to 20.4GHz were taken at each bias. The goal of these measurements was to determine the 1N914 package parasitics and the transit time (Tt).

Up to this point, all of the measurements have either been DC or 1 MHz measurements where the parasitic elements of the test fixture have been negligible. With S-parameter measurements extending to 20 GHz, this is no longer true. In order to remove the unwanted package parasitics of the test fixture, a TRL calibration technique was used to de-embed the fixture's parasitic elements, leaving only the response of the 1N914 semiconductor properties and its own package parasitic elements.

TRL Calibration

Thru-Reflect-Line (TRL) calibration is procedure for removing fixture parasitic elements from measurements by mimicking the parasitic elements in the calibration that exist in the measurement fixture. Since the calibration contains a copy of the parasitic elements in the measurement fixture, after calibration the fixture parasitic elements are accounted for and removed from the measurement. The reference plane of the test fixture can then be calibrated to remove all of the test fixture and only leave the response of the device under test. The reference plane for 1N914 and the TRL test fixture can be seen in Figure 34.

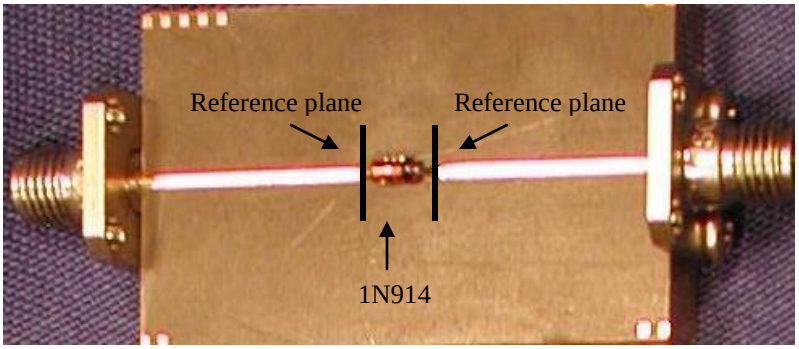


Figure 34. TRL Calibration 1N914 test fixture

A thru connection, a reflecting connection, and three different-length lines were needed for this calibration in order to cover the frequency range of 0.4 to 20.4 GHz.

1N914 Package Parasitic Elements.
The 1N914's package parasitic elements were determined in a two step process. First IC-CAP, an HP8510 and an HP4121 were used to measure the S-parameters, and then ADS was used to optimize the 1N914 along with its parasitic elements. The 1N914 model obtained from the DC and capacitance measurements was optimized in ADS to determine

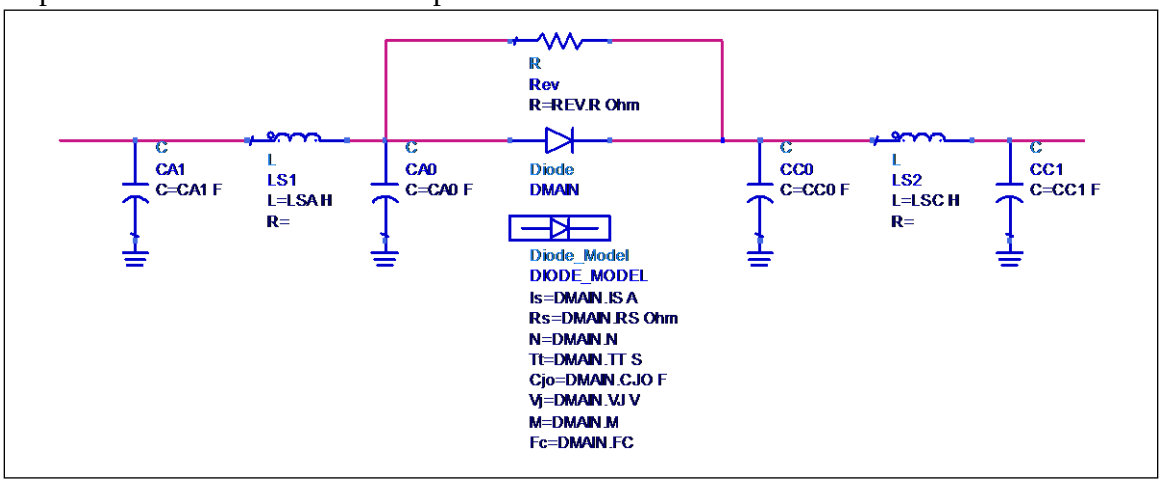


Figure 35. Spice model including package parasitic elements of the 1N914 diode

the approximate value of the package parasitic elements along with the proper geometry of the elements. This was done by placing the diode in hard reverse bias
(-10V) and optimizing parasitic elements for best match. The hard reverse bias technique allowed the 1N914 to be easily characterized, because the diode simply looks like CJO, and could have been optimized without the Spice model. The diode model can be seen in Figure 35 with the package parasitic elements CA1, LSA, CAO, CCO, LSC, and CC1.

The geometry and circuit elements were then ported back to IC-CAP and optimized for best fit. The results of the reverse bias measured vs. modeled fit can be seen in Figure 36, with the S-parameters fitting nicely from 0.4 to 20.4 GHz.

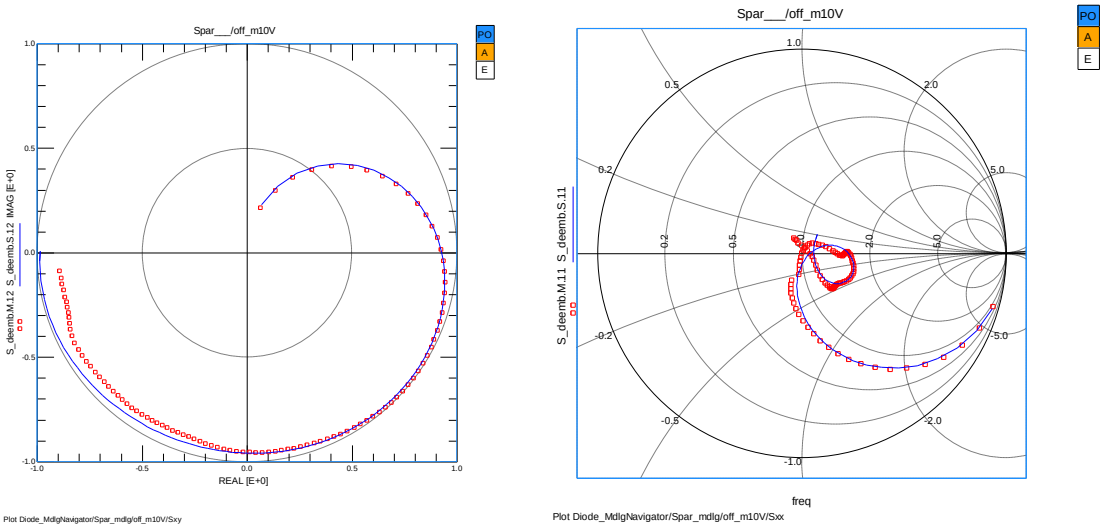


Figure 36. S-parameter data of 1N914-- S12 (right) and S11 (left) (Red Square-meas.; Blue line-sim.)

1N914 Forward Bias

S-parameter measurements and model fits for the forward bias region are shown in Figure 37.

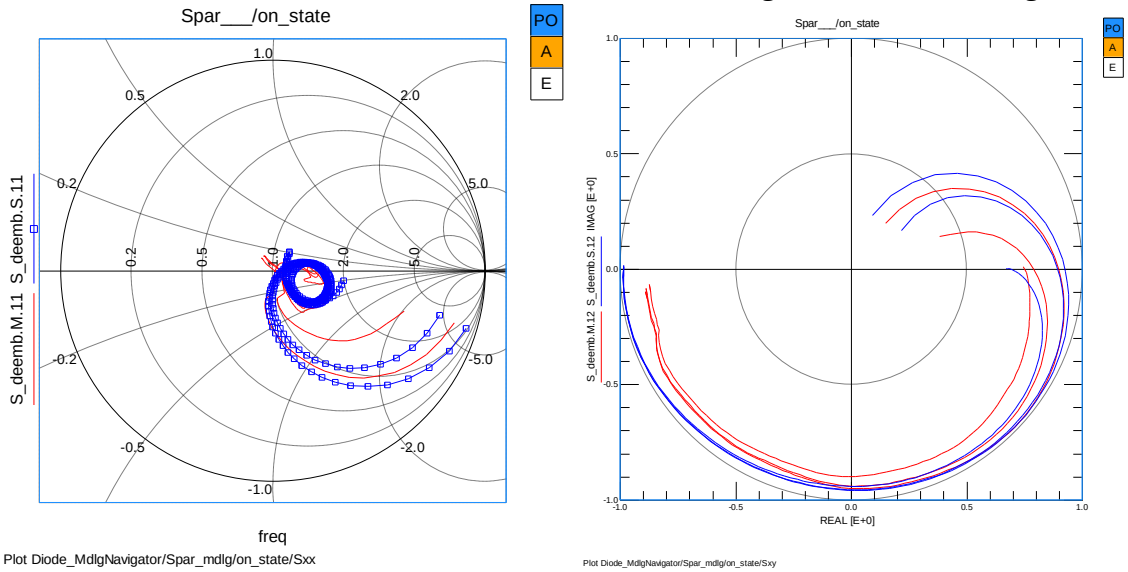
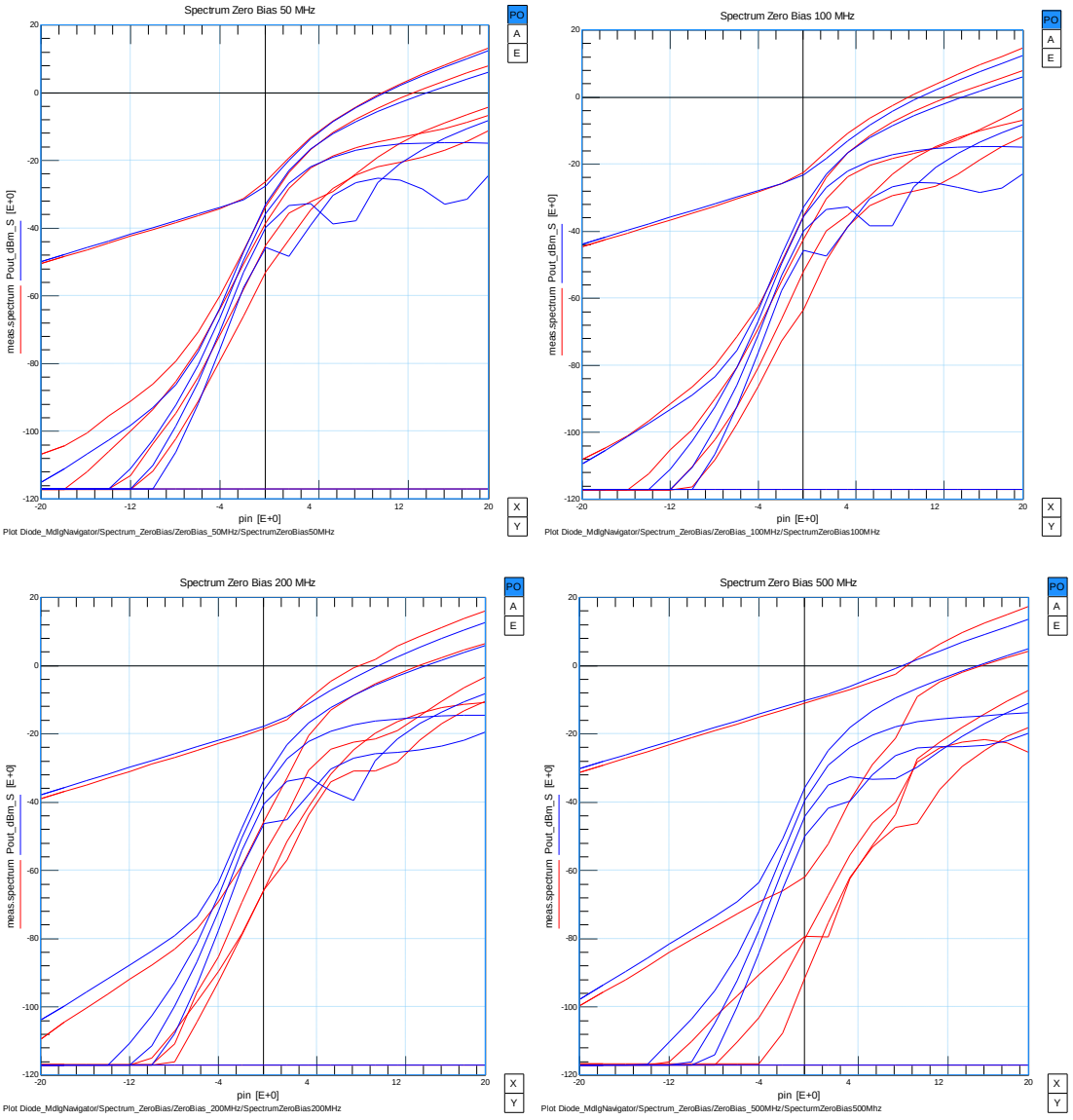
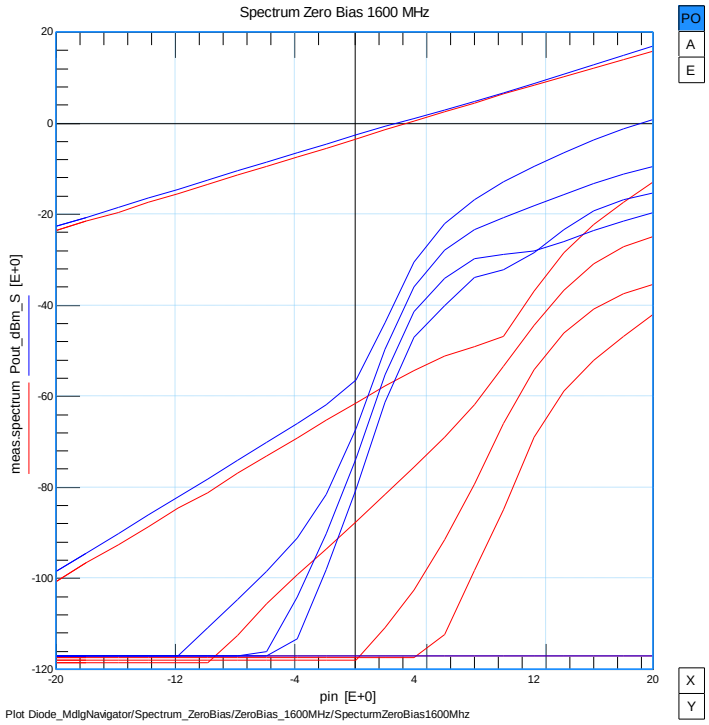


Figure 37. S-parameters for Forward Bias

Spectrum Data

The final stage in accurate modeling of diodes in Spice consists in measuring spectra as drive power is increased. For the 1N914, the measured spectra matches the simulated only approximately. The fundamental matches 50 MHz to 1.6 GHz, but the rest of the harmonics get progressively worse with increasing frequency. As mentioned above, this is most likely due to the fact that the gold doping does not allow equations (5) and (6) to properly predict the capacitance vs. voltage behavior.

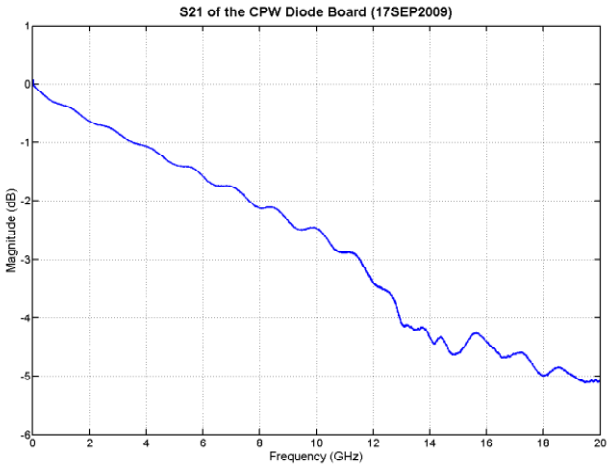




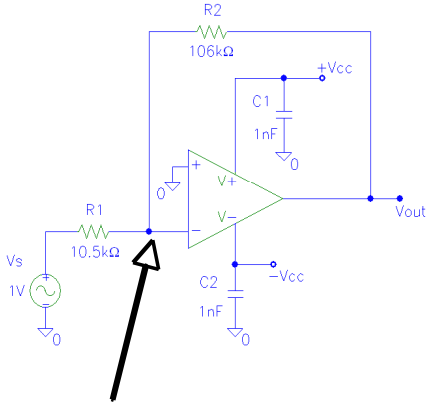
Analog IC Characterization and Modeling

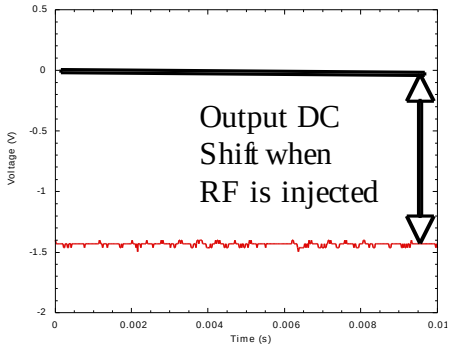
The 741 type op-amp is one of the oldest and most popular general purpose amplifier devices, and remains in production today, more than 40 years after its introduction. The 741 and its very similar more modern incarnations are so ubiquitous that it is an appropriate choice as an important component to include in our study of RF effects.

Our 741 op-amp circuit is the most basic, designed to operate with a gain of 10 and bandwidth of 100 KHz. The circuit is laid out on a FR10 PCB with provisions for surface mount TVS devices on the input and 1nF surface-mount power supply bypass capacitors. 50Ω coplanar waveguide (CPW) transmission lines are laid out to the input pins of the 741 IC for direct-drive RF signal injection. Because the E-fields of CPW transmission line are largely in air, it has lower dielectric loss compared to microstrip, and therefore better microwave performance even in lossy material such as the FR10. This has been verified using network analyzer measurements, and we verify that we incur only ~2.5dB propagation loss at 20GHz for 1" of line on our 741 op-amp PCB.



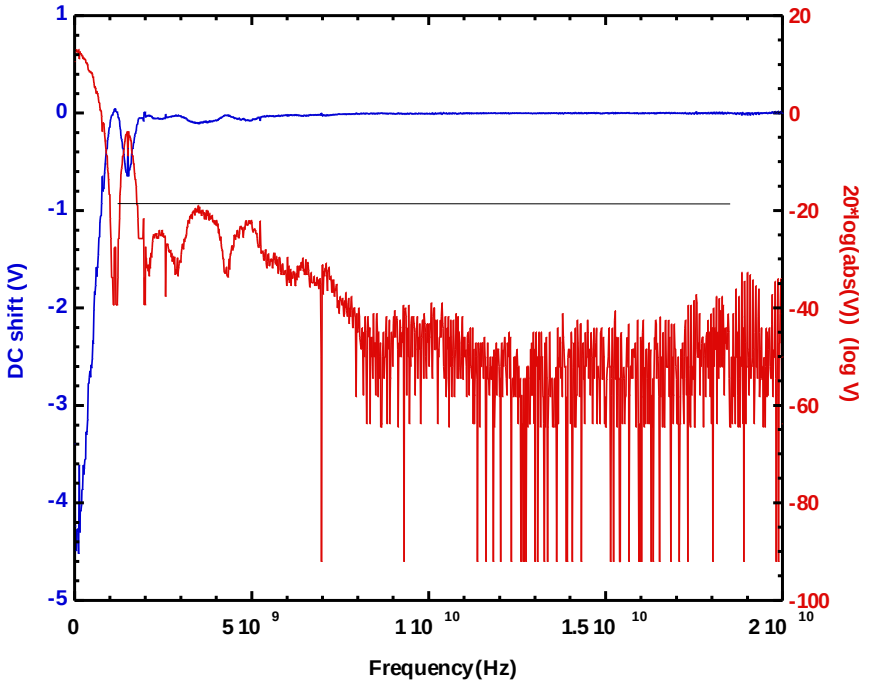
741 op-amp circuit schematic:





RF signal injection point

When RF is injected directly to pin 2 (inverting input) of the 741, we observe DC shifts in the amplifier output. Depending on the amplitude and frequency of the injected RF, these shifts can be quite large (several volts), even driving the amplifier to its supply rail voltages. We have characterized the frequency dependence of this DC shift behavior to 20 GHz. The measurement hits a noise floor above 7GHz, due to the decreasing response of the amplifier to the RF, the impedance mismatch to the 50Ω RF source, the increasing loss in the CPW line on the PCB, and the noise limit of the oscilloscope used to record the DC shift. Between 0 - 7GHz, the response falls off by more than 60dB.



Much of the decrease in response with frequency may be due to impedance mismatch of the op-amp circuit (audio frequency baseband) to the 50Ω RF source and feed. We characterized this using an RF vector analyzer and Thru-Reflect-Line (TRL) calibration to determine S11 at the input pin 2 at the IC where the RF direct drive is applied. A calibration fixture that uses a metal blocking plate short substituted for the 741 IC was fabricated so that the calibration has its physical reference plane exactly where pin 2 attaches to the PCB.

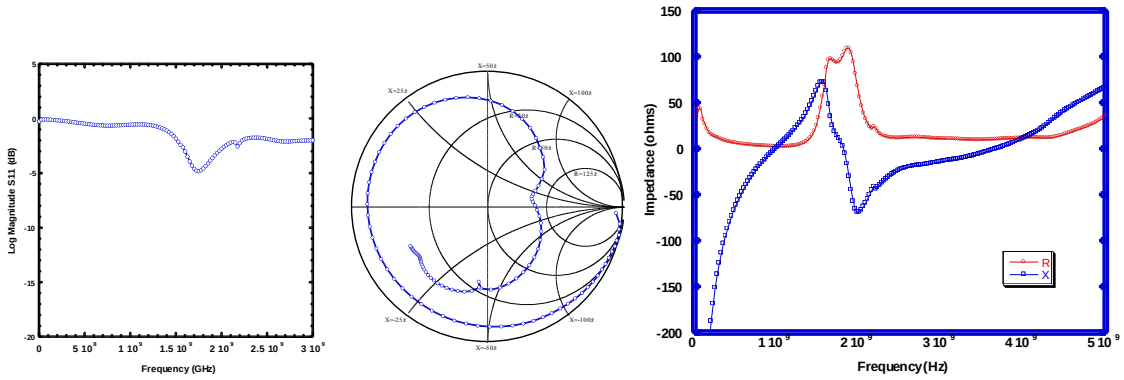


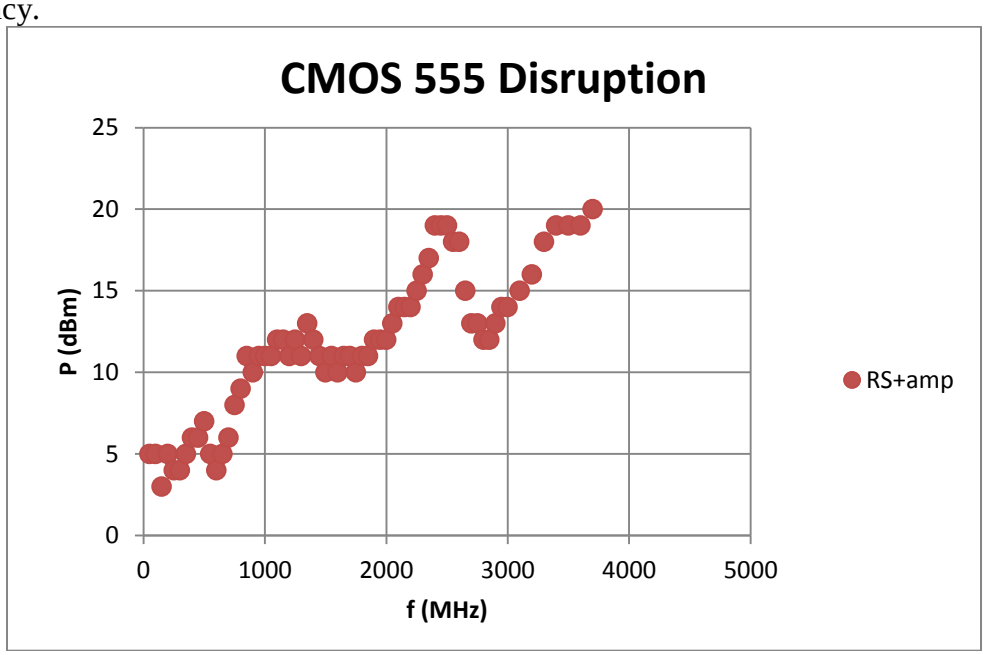
Figure 38. Reflection Coefficient Magnitude (left) Smith Chart (center), and Real and Imaginary Impedances.

The measurement of S11 reveals a resonance at 1.6GHz corresponding to an enhancement of the DC shift response at a similar frequency. This DC shift was used in the section on PC board modeling above as a diagnostic for the response to millimeter wave excitation.

Digital CMOS Flip-Flop

This section considers direct injection of RF into a CMOS 555 chip wired in a flip-flop configuration. 1 kHz pulse trains are applied to the trigger and reset pins of the 555. This results in a pulse train on the output pin. The output goes high when trigger goes low, and output goes low when reset goes low. The duty factor of this output train is adjustable be changing the relative "phasing" of the trigger and reset pulse trains.

RF power is injected onto the trigger pin of the 555. With sufficient power, this results in the output latching high. The plot below shows the required input power for latch up as a function of frequency.



A closer looks at the output of the flip flop shows that as power levels approach latch up levels, the duty factor begins to increase just before the output latches high.
We have looked at using this increase in duty factor as a measure of the injected RF effect. We consider the case where the injected power is below that needed for latch up, but high enough to result in some change to the duty factor. At this fixed injected power level, we then look for the induced effects as a function of frequency. The larger the change in duty factor the larger the RF effect.

The output waveform can be represented with a Fourier series:

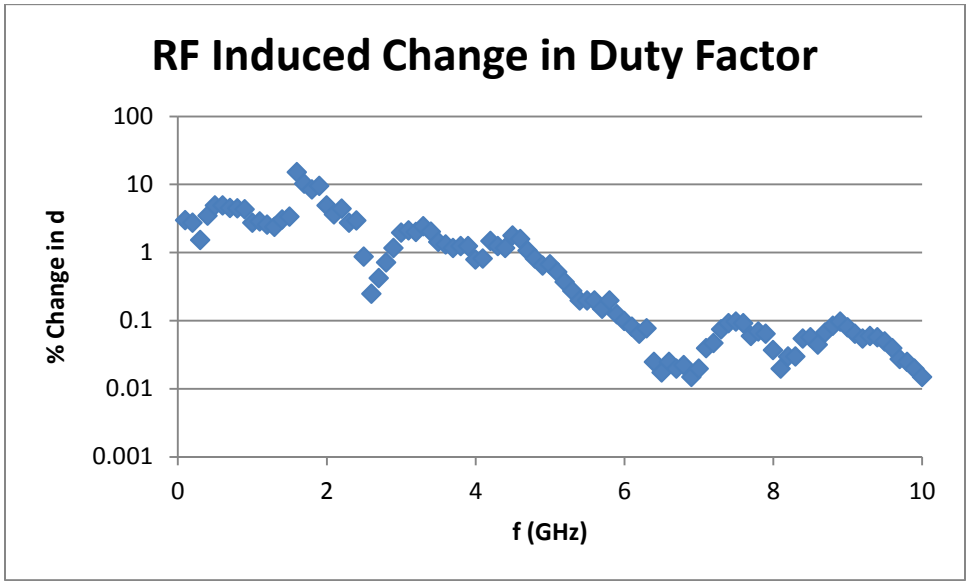
$$V_{out} = A * \sum_{n=0}^{\infty} \frac{\sin(n\pi d)}{n\pi} \cos(n\omega t)$$

$$V_{out} = Ad + \frac{A}{\pi} \sin(\pi d) * \cos(\omega t) + \frac{A}{2\pi} \sin(2\pi d) * \cos(2\omega t) + \cdots$$

Where d is the duty factor. For small d we have:

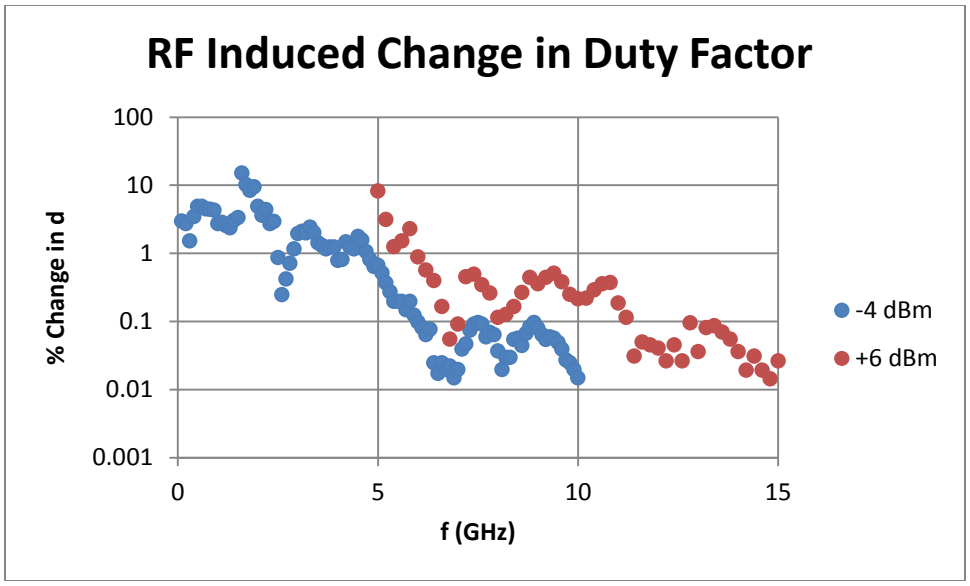
$$V_{out} \approx Ad + Ad * \cos(\omega t) + Ad * \cos(2\omega t) + \cdots$$

So that for small duty factors, the magnitude of the component at ω scales as d.
Use of a Lock In Amplifier (LIA) allows one to accurately measure the magnitude this component at ω. We use the sync out from the signal generator feeding the 1 kHz pulse train to the trigger pin as the reference for the LIA. The output line of the 555 is used as the input to the LIA. Application of the appropriate low pass filter results in the output of the LIA being proportional to d.
The plot below shows the result of such an analysis out to 10 GHz. The pulse train frequency set to 10 KHz, and the injected RF power to the trigger pin was -4 dBm.



At 10 GHz the effect is down to 0.01% change in duty factor. This corresponds to +/- 5 μV variations and represents the noise floor for the current configuration.

In order to measure effects out to higher frequencies, the RF power was increased. A new scan was performed at a +6 dBm level. Operating at the higher injected level resulted in latch up a many of the lower frequencies. Hence the high power scan starts at 5 GHz. The plot below shows the observed effects at the two power levels.



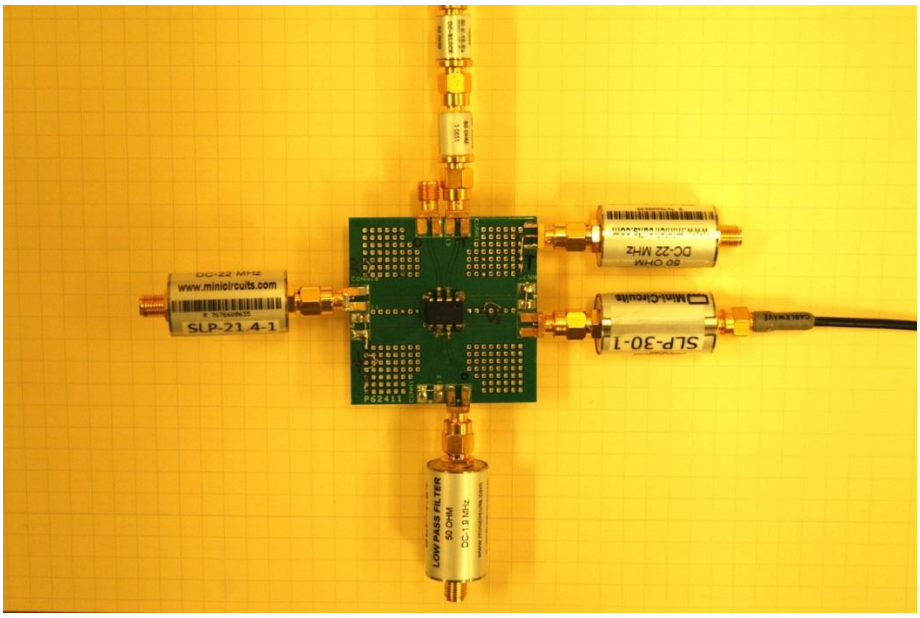
The +6dBm scan demonstrates RF effects are present out to at least 15 GHz.

It is desirable to measure RF effects at higher frequencies. Increasing the injected power has been shown to be one method to achieve this. Due to the signal generator's limited output power, this would require the use of high frequency amplifiers in order to boost the power levels beyond the +6 dBm already used.

A second approach would be to reduce the noise floor of the measurement. Currently it is unclear what is setting this noise level. However if the noise drops with frequency, it may be beneficial to run the flip flop at higher frequencies, i.e. 100 kHz. Use of the LIA at this higher reference frequency may then allow better filtering of the noise.

CMOS 555 Input Impedance Measurements

The photo below shows the latest board configuration:



Initially, various signals in and out of the board (trigger, reset, output, bias) were simply made using clip leads to appropriate test points. It was found that the position of the lead wires had an excessive influence on the measurements. To overcome these variations, these signals were routed to SMA connectors at the board's edge. Coax lines were then used to bring the signals in and out.

A second change was the addition of low pass filters to all the input and output ports. Initial measurements of S11 were made with all the SMA connectors open (except for the trigger injection line). This gave a clean measurement, but not the correct one. It was found that hanging coax cables off the SMA connectors greatly affected the S11 measurement. The lines act as either inductive or capacitive components coupled into the circuit. This greatly changed the measurement especially on the trigger and reset ports.

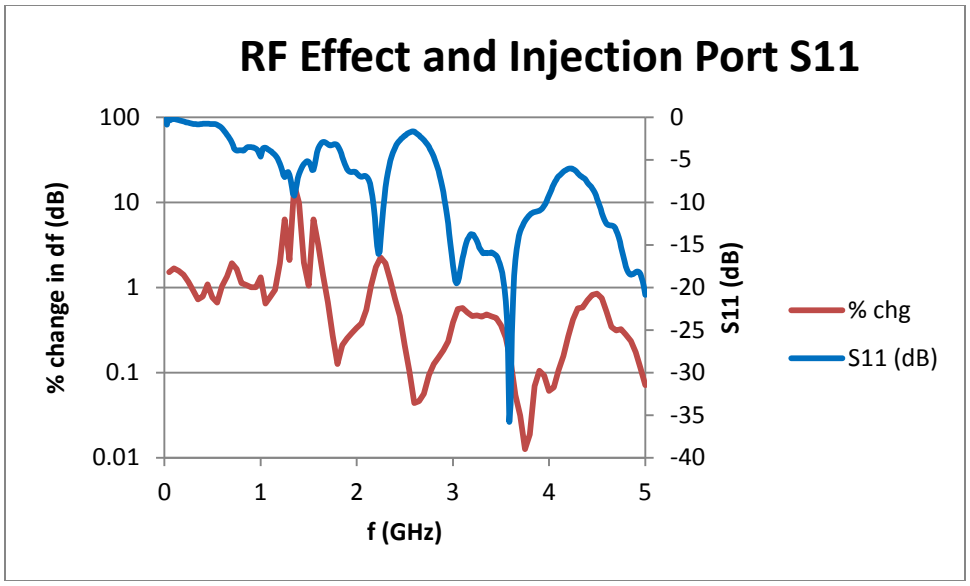
To address this issue, low pass filters were added to all the ports. This effectively isolated all the external cabling from influencing the RF response of the board.

As previously noted, the RF effect on the performance of the flip flop was to latch the output high. In addition, as the injected RF amplitude was increased from zero, it was observed that just before latchup, the duty factor of the flip flop operation was increased. This increase in duty factor is used to quantify the RF's effect on the circuit. A Lock In Amplifier (LIA) is used to measure the increase in duty factor (see earlier write up).

It is desired to find the input impedance at the 555's trigger pin. This measurement was made by measuring the S11 on the injection line.

The calibration used was a 1 port, SOL (short, open, load) cal. An unstuffed PCB was modified so that a short, open and load were placed at the 555 pin locations. The short consisted of a wire shorting the center trace to ground on both sides. The open was simply leaving the center trace open ended. The load consisted of two surface mount 100 ohm resistors in parallel. (I have concerns about the quality of the open and especially the load at the higher frequencies.)

The chart below displays the measured change in duty factor along with the S11 at the trigger port.



Measurement conditions:

- 10 kHz, 5% nominal duty factor.
- -10 dBm RF injected to trigger pin.

The effects observed appear to be well coordinated with dips in S11 up to 3.5 GHz. Dips in S11 correspond to frequencies at which most of the injected RF is absorbed in the "load". One would expect increased effects at these optimally coupled frequencies.
The lack up correlation above 3.5 GHZ may be due to inadequacies in the calibration "standards" at high frequencies.

Performing a TRL cal may provide better calibrations at the higher frequencies. Measurements should be repeated using this cal approach.

CONCLUSIONS

This report has discussed our work to understand the basic physical mechanisms of extremely high frequency RF effects on electronics. In our measurements and modeling, we have attempted to connect our understanding of lower frequency microwave effects with the interactions that are observed at millimeter wave frequencies, noting where in frequency the important coupling and response aspects appear to change. Although we have made progress, this problem's challenges are as extreme as the frequency designation "extremely high frequency" indicates.

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