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Three Wafer Stacking for 3D Integration

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Abstract

Vertical wafer stacking will enable a wide variety of new system architectures by enabling the integration of dissimilar technologies in one small form factor package. With this LDRD, we explored the combination of processes and integration techniques required to achieve stacking of three or more layers. The specific topics that we investigated include design and layout of a reticle set for use as a process development vehicle, through silicon via formation, bonding media, wafer thinning, dielectric deposition for via isolation on the wafer backside, and pad formation.

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FIGURES

Introduction

Considerable technical advantage is obtained by combining separate analog, digital, and other technology functions in a single low-volume solution utilizing vertical die stacking. In a previous LDRD (08-0600) we explored and developed technologies to achieve vertical die and wafer stacking, also known as 3D Integration, with particular success in the area of stacking two layers. However, stacking three or more layers introduces additional complexities that need to be investigated. With this LDRD, we propose to explore the combination of process and integration techniques required to achieve stacking of three or more layers.

Stacking three or more die or wafers requires some means to establish electrical continuity between the layers. Through silicon vias (TSVs) are a powerful and elegant solution to achieving these interconnects. In our LDRD (08-0600) demonstrated a robust TSV integration scheme in which TSVs that are established on the front side of a wafer penetrate deep into the wafer, and we have a simplistic process flow that describes how we might establish electrical contact through the back side, but the process and integration details remain to be sorted out so we can demonstrate and fully realize the benefits of vertical wafer stacking with three or more layers.

Broadly speaking, vertical wafer stacking will enable a wide variety of new system architectures by enabling the integration of dissimilar technologies in one small form factor package. Analog and digital Si-based integrated circuits, compound semiconductors, and microelectromechanical systems (MEMS) are all primed to be integrated by vertical stacking, thus enabling compelling system-on-a-chip (SOC) solutions. Defining the process and integration details as proposed with this effort is critical to fully realizing vertical wafer stacking of three or more layers.

TSV Integration Process Flow

We have previously reported how to form TSVs (SAND 2010-8585), and with this effort we seek to develop techniques for completing the integration. A high level overview of our notional process flow, with some embedded details, is summarized in text form below. We identify specific unit operations and integration points that need attention. The process flow is shown schematically in Figure 1.

Fabricate wafers with TSVs as described in SAND 2010-8585.

Once front side fabrication is complete, thin the wafers so that the terminus of the TSVs is within 5 μm of the back side surface of the wafers. In the past we have relied on an external vendor to thin our wafers but we are developing our own capability. For our needs, excellent thinning uniformity is required. Note that our TSV interconnect material is W, which is very hard. Our external thinning vendor objects to thinning wafers with W exposed, so we have evolved an integration scheme that complies with that constraint. However, as our own thinning capability develops, we may be able to modify our integration scheme to benefit our technologies rather than accommodate process limitations. Bringing wafer thinning "in-house" is an important and challenging goal for this effort.

If the device wafer is not already submounted to a suitable carrier prior to thinning, execute a submount after thinning to provide the mechanical robustness required to do the remaining processing. We have not identified and demonstrated a suitable temporary bonding media and bonding methodology.

Use a selective, uniform etch process to etch silicon until the TSVs are exposed by perhaps 2 μm. We expect to explore reactive ion etching (RIE) using SF6 in a capacitively coupled reactor in addition to a XeF2 etch process. We will also explore wet chemical processes.

Deposit PECVD SiO2 over the surface of the exposed plugs and thinned silicon. Deposited SiO2 films have inherent residual stresses which can induce wafer bow. We need to develop PECVD processes with less residual stress, or investigate other technologies like spin-on glass.

Using CMP, remove the SiO2 over the plugs to expose the W TSV. We perceive this to be a weak point in our approach. If the submounted thinned wafer is not flat or if the CMP processes are sufficiently non-uniform, this activity will be very difficult to do successfully, with the success metric being exposure of W TSVs with full integrity of the oxide film of over the surface of the thinned Si to ensure dielectric isolation of TSVs, all with good planarity. We perceive flexibility in doing a temporary submount with a reversible temporary bonding media in Step 3, but it may prove to be that a temporary bonding media imparts enough non-planarity that a permanent submount to a rigid, planar handle is necessary to conquer the difficulties associated with this step. This activity will be a key focus of our overall effort.

Form pads over the TSVs. This will most likely be done by lift-off but developments in the previous activities may steer us in other directions.

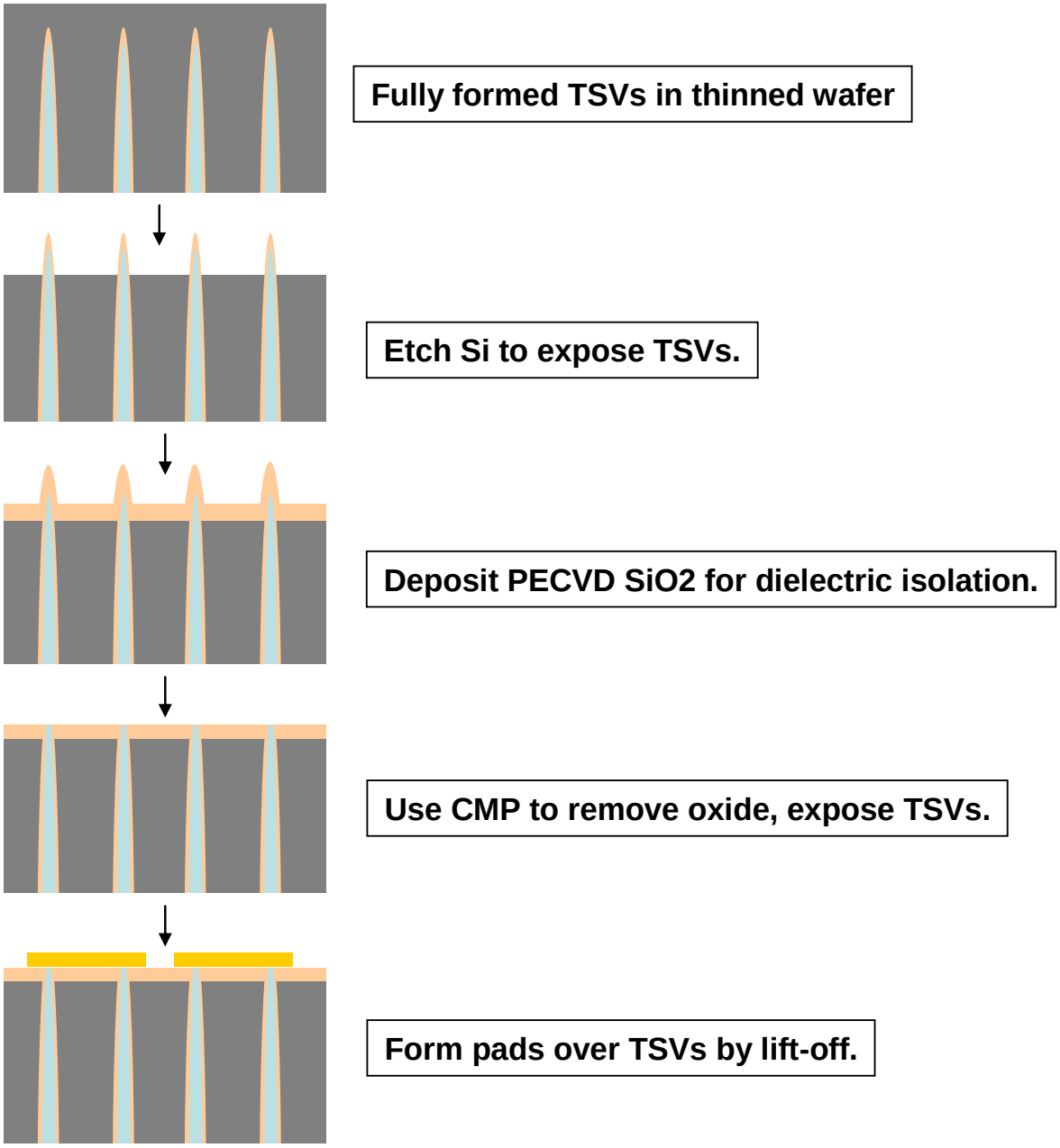

Figure 1: Schematic of notional process flow for integrating TSVs.

Design, Layout, and Reticle Set

To form TSV-based structures that result in testable devices, we need to design and procure a reticle set. For testable structures, we converged on via chains since a large number of structures can be instantiated in a small area, and the chains can be interrogated from both sides of any given wafer. Our design includes vias on both 25 µm and 50 µm pitch in X such that each die contains two distinct sets of chains. Furthermore, we made provisions for forming vias that are 2, 4, 6, and 10 µm in diameter. On each die, only one size of vias is possible, but from die-to-die and wafer-to-wafer, different size vias are possible. Note that we report the diamter of our vias, but our vias are actually octagons, which are easier to design into a mask than true circles (arcs are difficult for CAD tools and photomask makers).

We constrained the total die size to about 10 mm, which allows us to incorporate multiple fields on a single piece of glass using the Nikon stepper. In this manner, we included all of the photolithography data needed to establish the vias of different sizes on a single piece of glass. With the die size at approximately 10 mm on each edge, we found that we could form chains with 57000 vias at 25 µm pitch and 28500 vias at 50 µm pitch. The pitch is in the X direction only. In the Y direction, the pitch is 25 µm for both sets of chains. Also, we added taps so that we could test chains of intermediate length as such an arrangement allows us to uncouple random fails from systematic fails. The shortest chains that we can interrogate are 300 vias long at 25 µm pitch and 150 vias long at 50 µm pitch.

As for layers, our mask set contains an alignment mark layer (layer 1), via layers with 2 µm, 4 µm, 6 µm, and 10 µm diameter vias (layers 2-5, respectively), a front side metal mask (layer 6), and a backside metal mask (layer 7). The first six layers are 4X stepper masks, while the last layer is a 1X contact mask. Since we expect to form the backside metal using lift-off techniques, that processing will occur in the µfab portion of the MESAFab and as such a contact mask is the best option.

The next several figures show screen captures of the mask features. Figure 2 shows a screen capture of the whole wafer layout. After including all design features and compulsory lithography information, each die is 10.6 mm x 10.6 mm. 116 die fit on a single wafer.

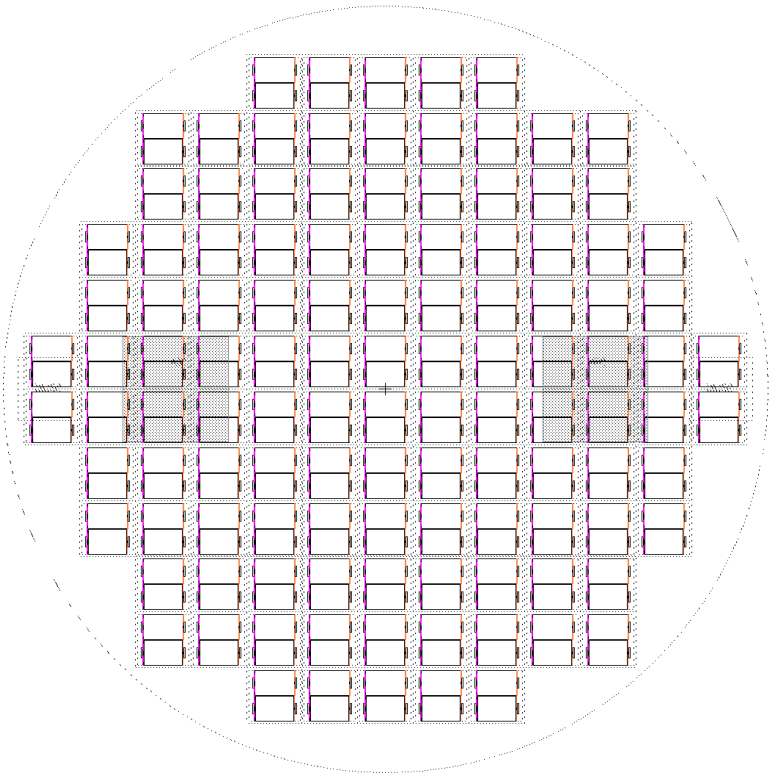

Figure 2: Screen capture of the full wafer layout.

Figure 3 shows a screen capture of a die layout. This image is misleading because much of the design information does not resolve at this resolution. However, the pads and some of the marks required to enable and characterize the photolithography are visible. The pad layout is in a 2x10 configuration, which is convenient for our autoprobers. Figures 4 and 5 show higher magnification screen captures where the more meaningful design data becomes visible. This screen captures show the pads in addition to the chain structure. The numbers adjacent to the pads show the notional via count at a particular pad. In fact, we miscalculated and are short by a factor of two.

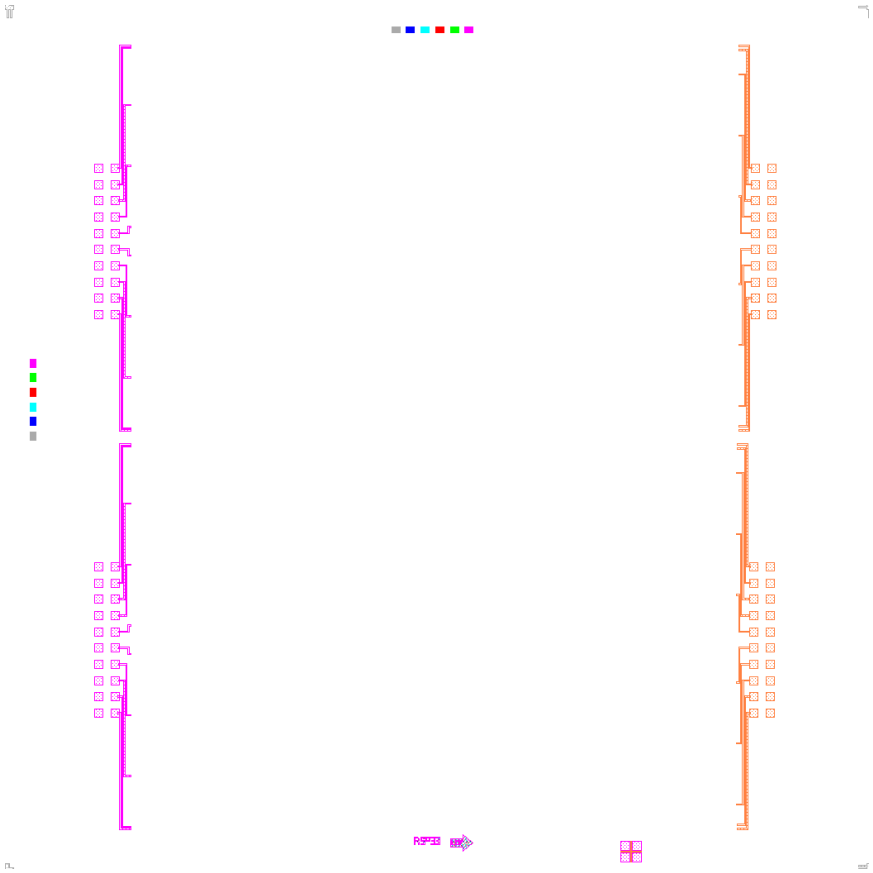

Figure 3: Whole die layout. The chain data is not evident at this magnification, but this view illustrates the pad layout.

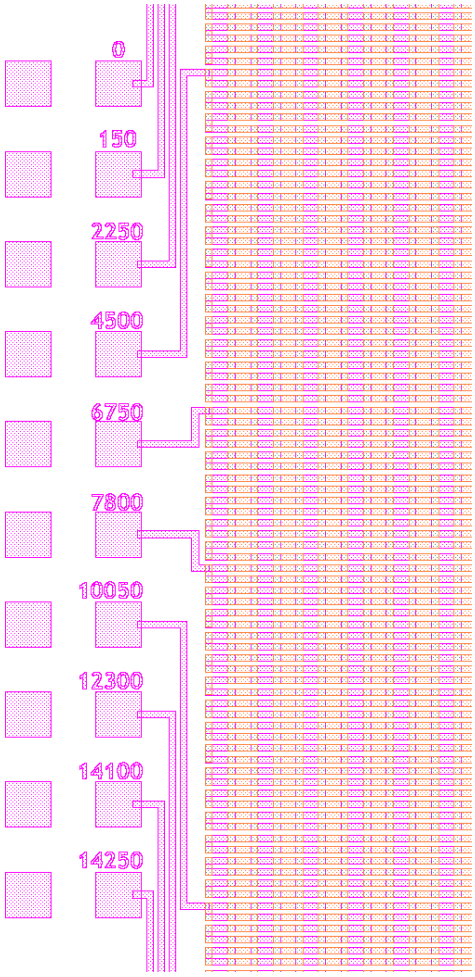

Figure 4: Screen capture of the pad layout from the layer 6 mask.

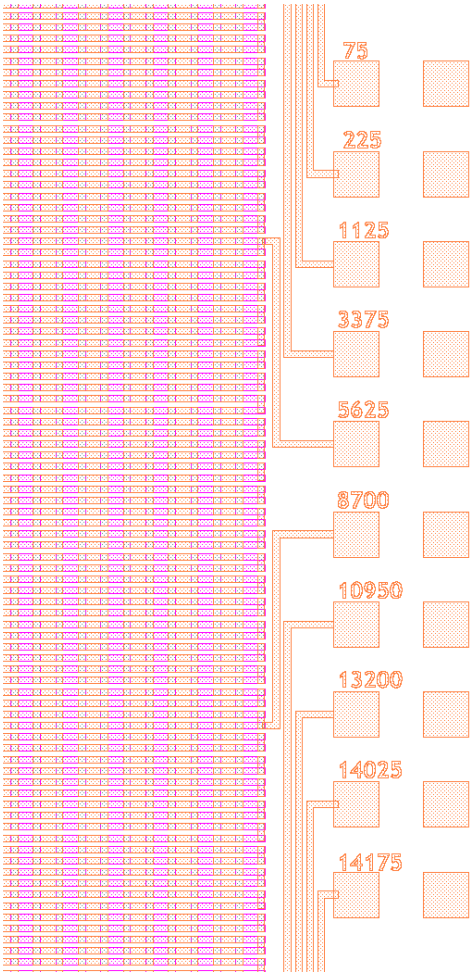

Figure 5: Screen capture of the pad layout from the layer 7 mask.

Figures 6 and 7 show the layout detail of a few links of the chain. Figure 6 shows the chains with vias on 25 µm pitch and Figure 7 shows chains with vias on 50 µm pitch. The vias of different sizes are evident with the concentric hexagons, as are the links of the chain on the front side (pink in color) and back side (orange in color) of the wafer.

Figure 8 shows a screen capture of some of the necessary photolithography information to characterize the layer information and the critical dimensions as patterned. The reticle set number is shown (933) as are the layer and revision for layers 1-7. The linewidth control feature includes structures for measuring the as-patterned features at each layer.

Figure 9 shows a screen capture of the alignment mark that enables front-to-back alignment of the front side metal and back side metal layers. This mark assumes that the wafers are thick enough to do a front-to-back alignment without a submount, or that the

submount is optically transparent. If the submount is opaque, we envision doing a same side feature-to-feature alignment. This arrrangment may not be optimal and we are considering other alignment marks that use TSVs penetrating the wafer to do same-side alignment.

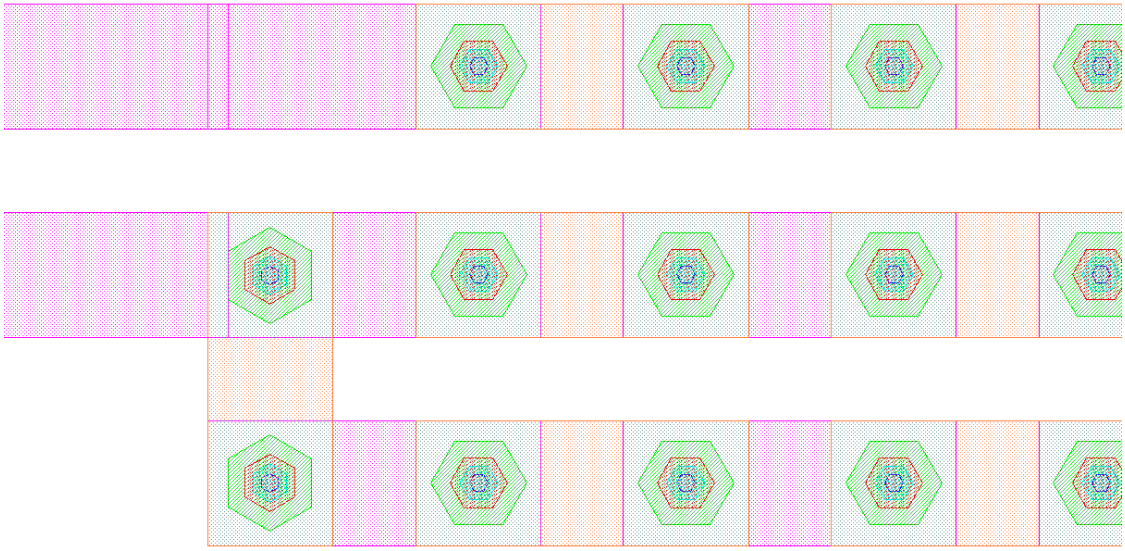

Figure 6: Screen capture of chains with vias on 25 µm pitch.

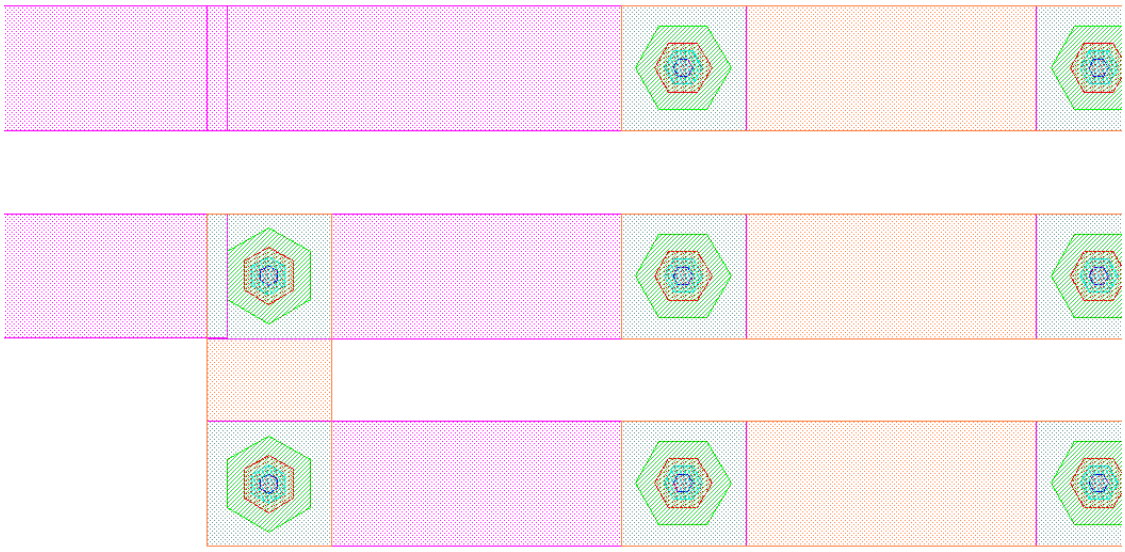

Figure 7: Screen capture of chains with vias on 50 µm pitch.

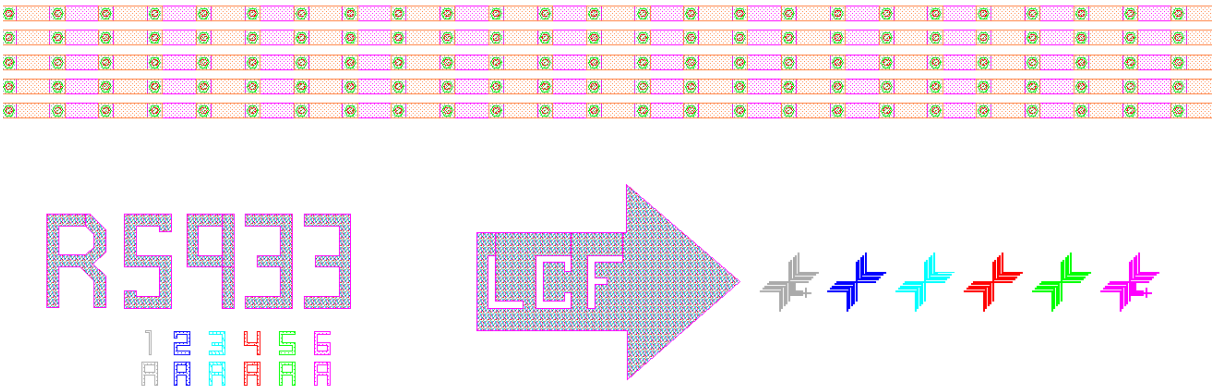

Figure 8: Screen capture of reticle set number (933), reticle layer and revision, and linewidth control feature (LCF).

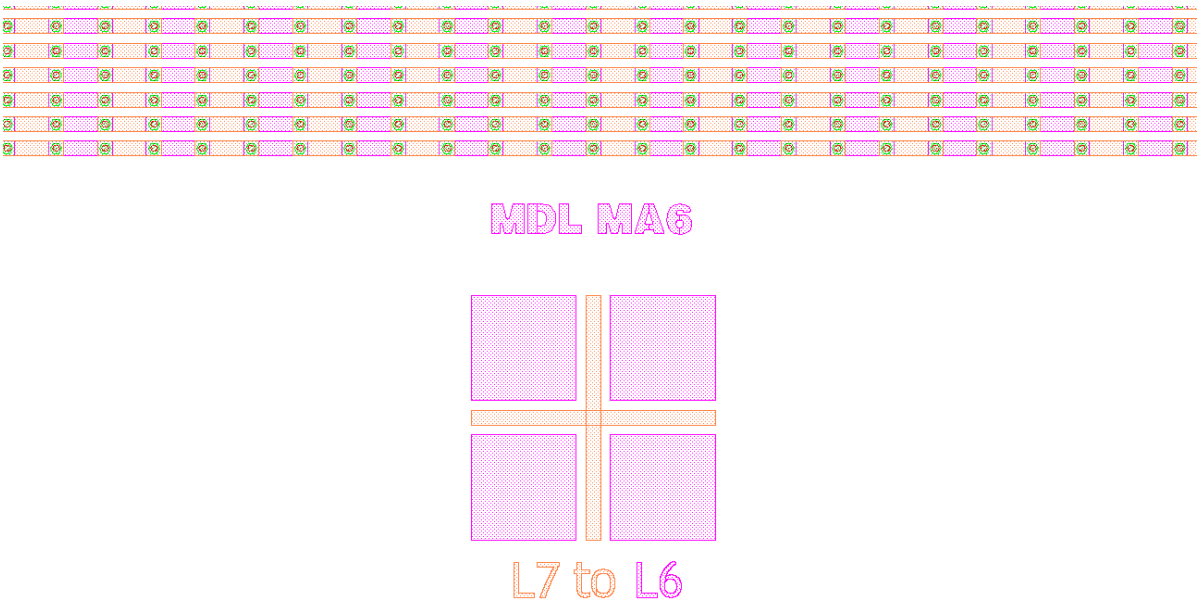

Figure 9: Screen capture of alignment mark that enables optical alignment of front side structures (L6) to the backside metal layer (L7).

Si Fab Fabrication

Broadly speaking, we compartmentalize the processing according to where it occurs. All of the front side patterning occurs in the Si Fab. Once front side patterning is complete, the wafers are thinned from the back side followed by additional processing. From wafer thinning on, the processing occurs in the µfab. Regarding front side processing, after obtaining the mask set, we initiated two silicon wafer lots to develop and exercise the unit operations and process integration for this 3D integration activity. Broadly speaking, the front side process flow is defined by these processes: alignment mark definition, via definition, dielectric isolation inside the via, via fill, metal definition, passivation deposition. The process plan is shown in Figure 10 and the lot specification file is shown in Figure 11. The total process is sufficiently complicated that the process flow requires two pages. The following text describes some of the non-obvious details of the processing.

We require alignment marks definition because TSVs are not always given to defining a first layer. TSVs are defined by Bosch etch, which in this case is an aggressive etch process of about 1 hour duration. The feature definition from a Bosch etch is not as crisp as one from a short process and the quality of the result can vary as the etch depth target varies. Defining a first level alignment mark independent of the TSVs is risk mitigation as it ensures that we will be able to do a high fidelity alignment to the first layer.

Prior to etching the vias, we form a 2 µm oxide hard mask to provide more mask material for executing the etch. In general, deeper vias are preferred and using more mask material allows us to etch deeper. We use oxide because it is easily removed with wet oxide etch processes after the Bosch etch. After depositing the oxide and patterning the vias using photoresist, we do a mask open etch to expose the silicon under the oxide. Without removing the resist, we begin the silicon etch. We consume about 0.4 µm of the PR mask doing the mask open etch. The remaining 2.6 µm photoresist and 2 µm oxide is dedicated to masking the Bosch etch. Reporting the details of the Bosch etch is outside the scope of this report, but we find that with our feature sizes we become diffusion limited before we exhaust our mask material. After etch, we strip the remaining photoresist and subject the wafers to aggressive cleans to remove any etch polymers. One special feature of the post etch cleans is the IPA dry, which helps prevents water from being entrained in the deep, high aspect ratio vias. After forming the via holes, we use wet processes to remove any remaining hard mask. Then we execute a thermal oxidation to effectively line the via walls with a dielectric material so that adjacent vias are not shorted. In this case, we are executing a 0.63 µm oxidation. This thickness is far in excess of what is required for electrical isolation, but that oxide will also serve as a polish stop for a subsequent tungsten chemical-mechanical polishing (CMP) operation.

After forming the liner, we fill with metal. Tungsten is an obvious choice because it is easily deposited using thermal chemical vapor deposition (CVD) and the fill is conformal, which is crucial to filling high aspect ratio structures. CVD-W is a highly tensile film, and at thicknesses greater than 1.2 μm, it is vulnerable to peeling owing to the residual stresses. Thus, we limit a single deposition thickness to 1.2 μm. However, in the case of our larger hole sizes, we cannot completely fill the hole with a single deposition. Thus we do multiple depositions. Note that after a single deposition, there is a layer of W in the via hole as well as on the planar surface of the wafer. We use W-CMP to remove the W from the planar surface and stop on oxide, leaving W lining the hole. We are then primed for an additional W-CVD step, after which we do an additional planarization and so on, until the hole is filled. The process plan and spec file in Figures 10 and 11, respectively, are for a 4 μm diameter via and thus use to cycles of W-CVD and W-CMP.

After filling the hole with W and removing W from the field so that primarily oxide is exposed, we deposit the metal stack. In the Si Fab we use a laminate stack that include, from top to bottom, TiN, AlCu (mixture, not alloy), TiN, Ti. After depositing the metal stack, we use photolithography to pattern the metal and then we use plasma processes to etch away the exposed metal. Following metal patterning, we deposit and planarize an oxide layer to promote bonding to a submount. That concludes front side processing in the Si Fab.

SubPlan	Step	Step Description
StartLot	LOT0000	allocate wafers
	LOT0001	Start lot
	LOT0002	EDC for more wafers
	LOT9150	check wafer type
LUMScribe	LOT9250	bare silicon scribe
	LOT1220	SC-1 megasonic clean
	LOT0918	spin rinse dry
MARKS_PHT	PHT5033	SPR850 3um PR COAT + DEV
	PHT5305	NIK I EXP | Nikon I-line Expose
	PHT8700	MEMS PR Dev. Check, cursory inspection
3DZEROET	DRY4698	special | nitride etch
	DRY4224	ASP 250C
	WET1023	10:1 Sulfuric:Nitric 150C
	WET0910	spin rinse dry
S5SacOx1	DIF1055	5:1 piranha (general)
	DIF0912	spin rinse dry
	DIF2392	TEOS w/850C anneal, 2uM
	DIF8057	TEOS w/850C anneal, 2uM thickness meas
	DIF8657	TEOS w/850C anneal, 2uM particle meas
3UM_NS_EXP_1	PHT5033	SPR850 3um PR COAT + DEV
	PHT5399	special | Exposure
	PHT8111	MEMS PR CD | EDC not linked to subplan
	PHT8700	MEMS PR Dev. Check, cursory inspection

Ox_Etch_Only	DRY4699	special | oxide etch
TS_VIA_ET	DRY4797	special | deep trench etch
	DRY4224	ASP 250C
	WET1570	post back etch strip, 15 mins
	WET0941	IPA dry, recipe 1
	WET1023	10:1 Sulfuric:Nitric 150C
	WET0940	IPA dry, recipe 1
NS_3D_ANNEAL	DIF1055	5:1 piranha (general)
	DIF0912	spin rinse dry
	DIF7099	special | oxide
	DIF8199	special | thickness meas
	DIF8899	special | particle or pepper meas
TSVFILL_1	MTL1516	PRS1000 clean/rinse, pre-metal
	MTL6873	100 SE 250 TiN
	MTL2052	12K tungsten for MEMS, 450C
WCMP_1	CMP1952	12kA WCMP w/EP & W2000
	CMP1840	W scrub
	CMP1870	CMP decontamination, 100:1 HF, 15 secs
	CMP0900	spin rinse dry
	CMP8740	post CMP inspection
RMV_WFR1	COM9899	remove wafer
TSVFILL_2	MTL1516	PRS1000 clean/rinse, pre-metal
	MTL6873	100 SE 250 TiN
	MTL2052	12K tungsten for MEMS, 450C

WCMP_2	CMP1952	12kA WCMP w/EP & W2000
	CMP1840	W scrub
	CMP1870	CMP decontamination, 100:1 HF, 15 secs
	CMP0900	spin rinse dry
	CMP8740	post CMP inspection
ADD_WFR	COM9898	add wafers
MET_STACK	MTL6850	SE/200Ti/500TN/12kAL/500TN
METET_3UM_PR	PHT5033	SPR850 3um PR COAT + DEV
	PHT5305	NIK I EXP | Nikon I-line Expose
	PHT8111	MEMS PR CD | EDC not linked to subplan
	PHT8700	MEMS PR Dev. Check, cursory inspection
SP_MET_ET4	DRY4999	special | metal etch
	DRY1660	30:1 HNO3, 1:30 mins
	WET0910	spin rinse dry
	DRY1530	CMOS7 post metal etch strip
HDP_PASS	CVD1519	PRS1000 clean/rinse
	CVD2175	6.0 DSR IMD 500A linr 2.4uM 1-step
	CVD8175	6.0 DSR IMD 2.4uM 1-step thickness meas
	CVD8275	6.0 DSR IMD 500A lnr 2.4uM 1-step particles
PLANAR_OX	CMP1900	test wafer polish
	CMP1979	C7 ox CMP, new reticle
	CMP1860	post ox scrub clean, prog20
	CMP9881	match wafer # to slot #
	CMP8399	special | ELIP3/4 (UV12x0) meas

	CMP1870	CMP decontamination, 100:1 HF, 15 secs
	CMP0900	spin rinse dry
EndLot	COM9930	Box Transfer
	COM0050	take ownership
	COM0010	End Lot

Figure 10: Process plan to define TSVs in the Si Fab.

Lot Number	TV093301A
Plan	3DI_TSV_BS_INT
Responsible Engineer	Todd Bauer 845-0086 283-1076
Alternate Contact	Doug Greth 284-4982 283-1856
Purpose	Testable TSVs
Initial Wafer Count	12
Reticle Set	RS933

Reticle Information

SubPlan	Layer	Rev	Comments
MARKS_PHT	1	A	
3UM_NS_EXP_1	3	A	
METET_3UM_PR	6	A	

Split Instructions

SubPlan	Child Lot	Child Plan	Child Qty	Note

Merge Instructions

SubPlan	Parent Lot	Note

Process Instructions

SubPlan	Step	Note
StartLot	LOT0001	PN 2046-02, 400 µm thick, DSP.
3DZEROET	DRY4698	Process in tool P5K-C using sequence 4662. Set the etch time to 25 sec.
3UM_NS_EXP_1	PHT5399	PHT5305 – normal exposure. Holes will be 4 um diameter hexagons.
Ox_Etch_Only	DRY4699	Process in tool P5K-C using sequence 4420.
TS_VIA_ET	DRY4797	Etch deep vias in tool EPCNT1-D according to Rob's instructions. Note to Rob: substrate I 400 um thick bulk silicon, features are 4 µm diameter hexagons, open area is less than 1%, mask is 2.5 µm I-line PR plus 2 µm annealed TEOS. Deeper vias are better, but stop short of burning through the mask and etching the underlying silicon. Instructions: Please etch in EPCNT1-D using recipe/sequence DT-TFO-1E for 540 cycles. The etch should take about 58 minutes per wafer. Afterwards hold wafers for inspection and remaining oxide measurement. Follow wafer run with 2 blank Si SEAS dry clean wafers.
NS_3D_ANNEAL	DIF7099 DIF8199 DIF8899	Grow 6300 A thermal ox, as in DIF7120.
RMV_WFR1	COM9899	Ignore – dispatch through witout removing wafers.
ADD_WFR	COM9898	Ignore – dispatch through without adding wafers.
SP_MET_ET4	DRY4999	Etch metalstack like C7 M4,,landing on oxide, but with 3 um I-line PR.
PLANAR_OX	CMP1900 CMP8399	Metal stack thickness is about 1.4 um, oxide film over metal is 2.4 um HDP ox. Target 9000 A oxide after polish. +/-2000 A rnge is fine, as long as we're close to planar when done.

Figure 11: Lot specification file for a TSV lot.

TSV Imaging

Figures 12 and 13 show cross-sectional scanning electron microscope (SEM) images of 4 µm diameter TSVs. Figure 12 is from a sample from the wafer edge, while Figure 13 is from a sample from the wafer center. The via depth is superimposed on each sample. At wafer edge it is 80.15 µm and at wafer center it is 79.62 µm. This is a difference of about 0.67 percent, which we consider to be an excellent result as we are relying on good process uniformity to facilitate wafer thinning. The oxide liner is clearly present. The W plugs are present in some of the vias in Figure 13. Presumably the plugs broke off during the cleave for the vias where plugs are not present. We note the high quality of the etch overall: no undercut of the mask, straight sidewalls, rounded profile at the bottom. 80 µm etch depth in a 4 µm diameter via peg the aspect ratio at 20.

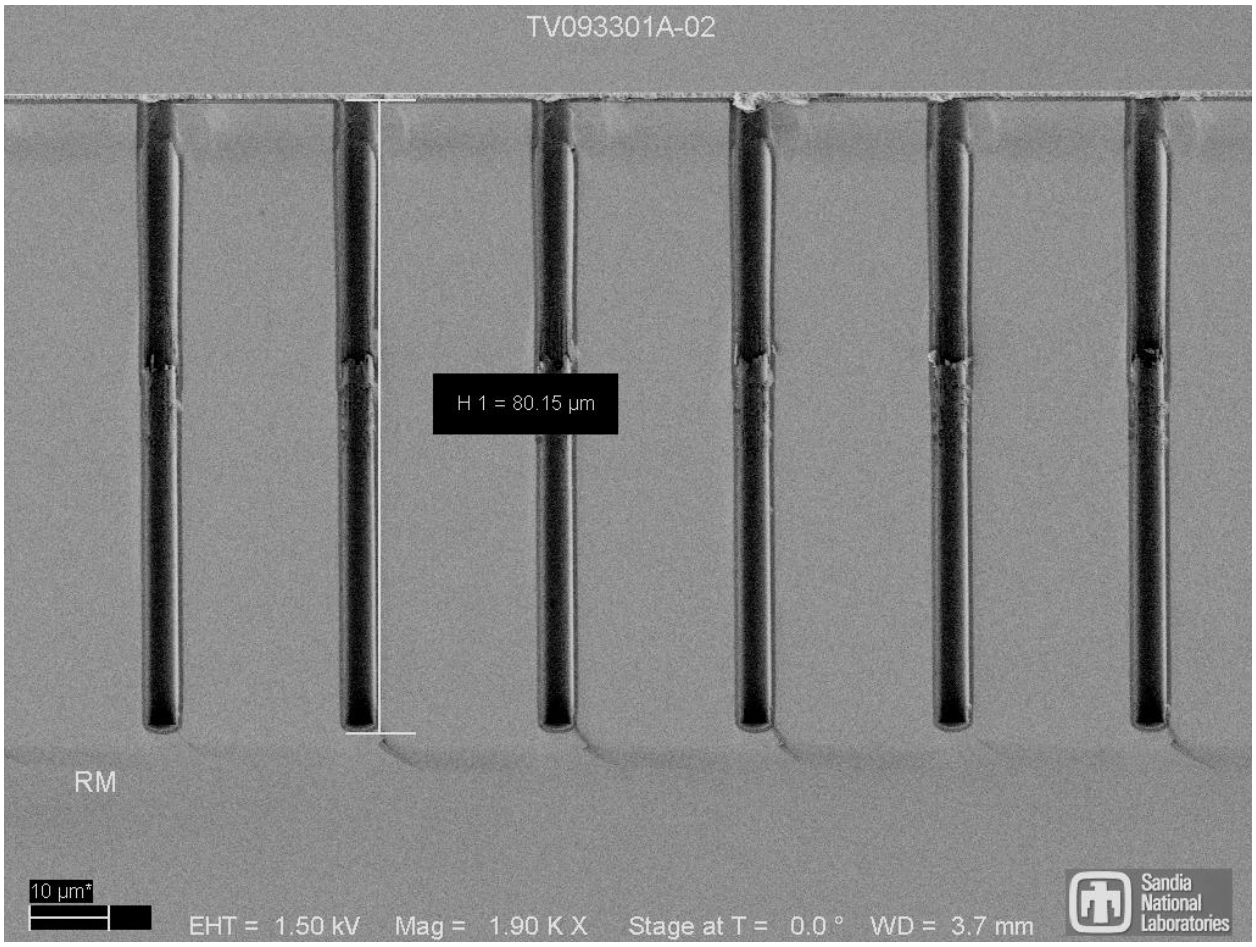

Figure 12: Cross sectional SEM image of 4 µm diameter vias. Sample is from wafer edge.

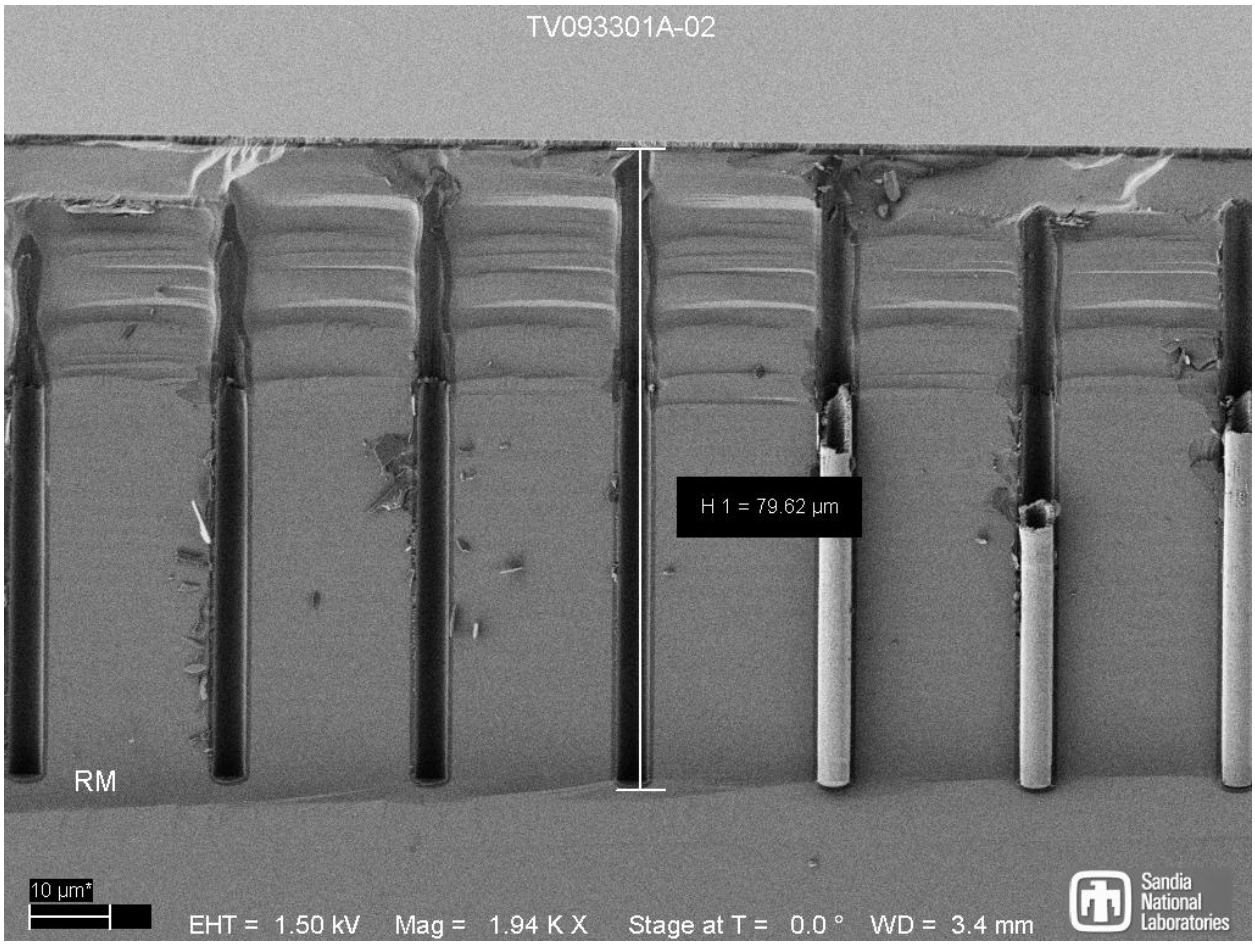

Figure 13: Cross sectional SEM image of 4 µm diameter vias. Sample is from wafer center.

Si Fab Process Complexities

For our first two lots we opted to use 400 µm thick wafers as our starting substrate. In retrospect this was a bad decision as it created unnecessary process complexity. We typically use 685 µm thick wafers, but we expected that by starting with thin wafers we would reduce the burden on wafer thinning. In fact, using thin wafers created problems for the Si Fab processing. At the photolithography steps we prefer to use automated, in-line SEM imaging to characterize the critical dimensions of the patterned features. But, the wafers that we used are sufficiently thin that they exceed the depth of field of the SEM so only relatively crude manual SEM images were possible. Also, the wafer carriers in CMP are optimized for 685 µm thick wafers. At 400 µm thick, our wafers were shallower than the minimum depth on the carrier and a carrier had to be modified to process our wafers, and even then some wafers were mishandled and had to be scrapped. Finally, residual stress in deposited films has a greater impact on thinner wafers (stiffness of the wafer goes as the cube of the thickness) so deposited films induced greater wafer bow and in some cases rendered a tool incapable of handled the bowed wafers.

As a consequence of our problems handling thinner-than-normal wafers, we opted to use normal thickness wafers on lots started after the first two lots.

Bonding Media

Thinning wafers with TSVs results in a wafer that is at least as thin as the deepest TSV. If the TSVs are 20 µm deep, then the wafer must be thinned to at most 20 µm to expose them. A 20 µm thick wafer is practically impossibly thin to handle, which necessitates the use of a submount to add mechanical integrity. For this effort, we used primarily photoresist as a medium to temporarily bond the TSV wafer to a submount. Somewhat surprisingly, photoresist was sufficient to bond the TSV wafer to the submount. We did not quantify the bonding other than to note that it was "good enough" to hold our wafers. As such, we did not commit our limited resources to exploring alternatives. In our proposal we focused on temporary bonds, but now we recognize that, in the long term, a permanent bond offers important advantages and that is guiding our thinking regarding future integration and applications. Specifically, we recognize that a permanent bond that is executed well offers perfectly planar interfaces between wafers. This is important when it comes to using CMP to expose W plugs as well as bonding a thinned wafer to another wafer. We also recognize that a permanent bond is likely to tolerate higher temperatures, as can be required to deposit a dielectric film or cure a spin on film, as well as tolerate higher shear forces associated with CMP. We have worked through the mental exercise of how an active device wafer with TSVs could be permanently submounted, thinned, prepped for bonding, and bonded to another active wafer. Furthermore, we envision that a suitably clever design and fabrication methodology could be extended so that each additional active wafer has TSVs and can be bonded to the growing stack.

Wafer Thinning

In our proposal we identified wafer thinning as one of the key technical risks to this project. It is also a technology enabler. To develop a thinning capability in house, we used a 3300-Series Acid Spray Tool by Solid State Equipment Corporation. Our process uses a HNO_3:HF:H_3PO_4 chemistry. Silicon etch rate is about 6 um/min. We optimized recipe settings for chemical tank pressure, chuck spin speed, arm sweep speed and amplitude in an effort to get the best possible etch rate uniformity across a full 150 mm diameter wafer. There is a short, dilute HF etch and rinse step before the Si etch. The HF etch step ensures that no oxide is present since oxide is a good etch stop for our etch chemistry.

Using this process, we demonstrated that we can thin wafers to about 20 µm. We also demonstrated that we can use our thinning process to reliably, cleanly expose TSVs. In our proposal and in the notional process flow, we identified thinning and TSV exposure processing as distinct (steps 3 and 4), but in fact we have demonstrated that we can combine that processing. Figure 14 shows a macroscopic image of a wafer thinned so that the vias are exposed. Good optical images are a challenge due to the reflectivity of the wafer, but the squares that are visible are attributable to light scattering off of the exposed plugs.

The image in Figure 15 is from a tilt objective microscope. It shows corners of the squares evident in Figure 14. Each of these corners represents a corner of a large square that is a sea of vias. Figures 16 and 17 are higher magnification views of the exposed vias. Figure 18 is a top down microscope view of the same wafer. The scale bar shows the vias to be about 2 µm in diameter, on 20 µm pitch.

We are concerned with the uniformity of the "height" of the exposed vias above the planar silicon surface. We expect that a uniform height will result in easier-to-manage CMP processes to make the backside planar prior to pad formation. Figure 19 shows a profilometer trace obtained over exposed vias. This trace shows that the vias at wafer center are exposed about 2.55-2.6 µm above the surface of the silicon. We have a comparable profilometer measurement from the wafer edge that shows the via height to be the same, thus demonstrating that we have good uniformity for the height of our exposed plugs.

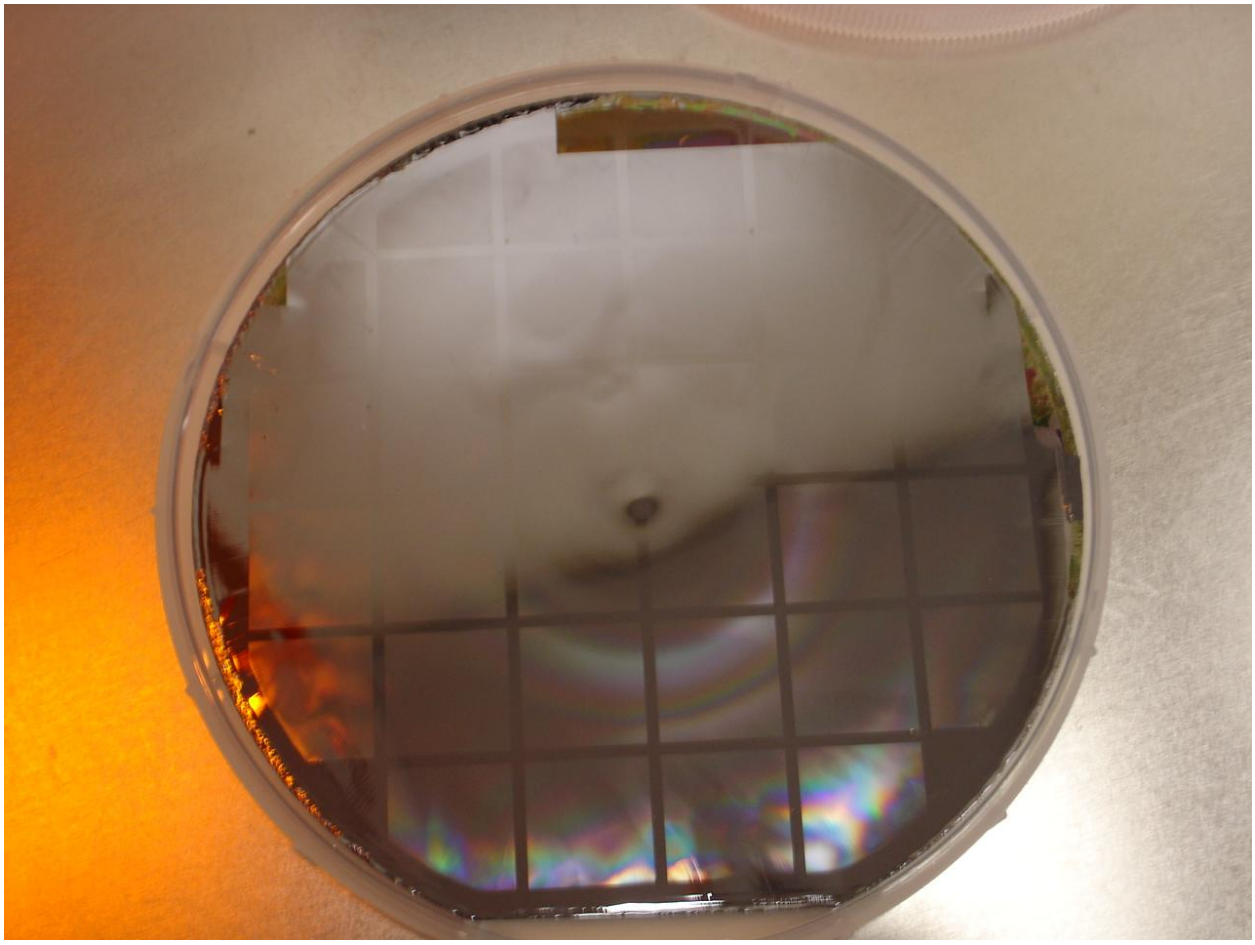

Figure 14: Macroscopic optical image of a thinned wafer. The squares are attributable to exposed vias.

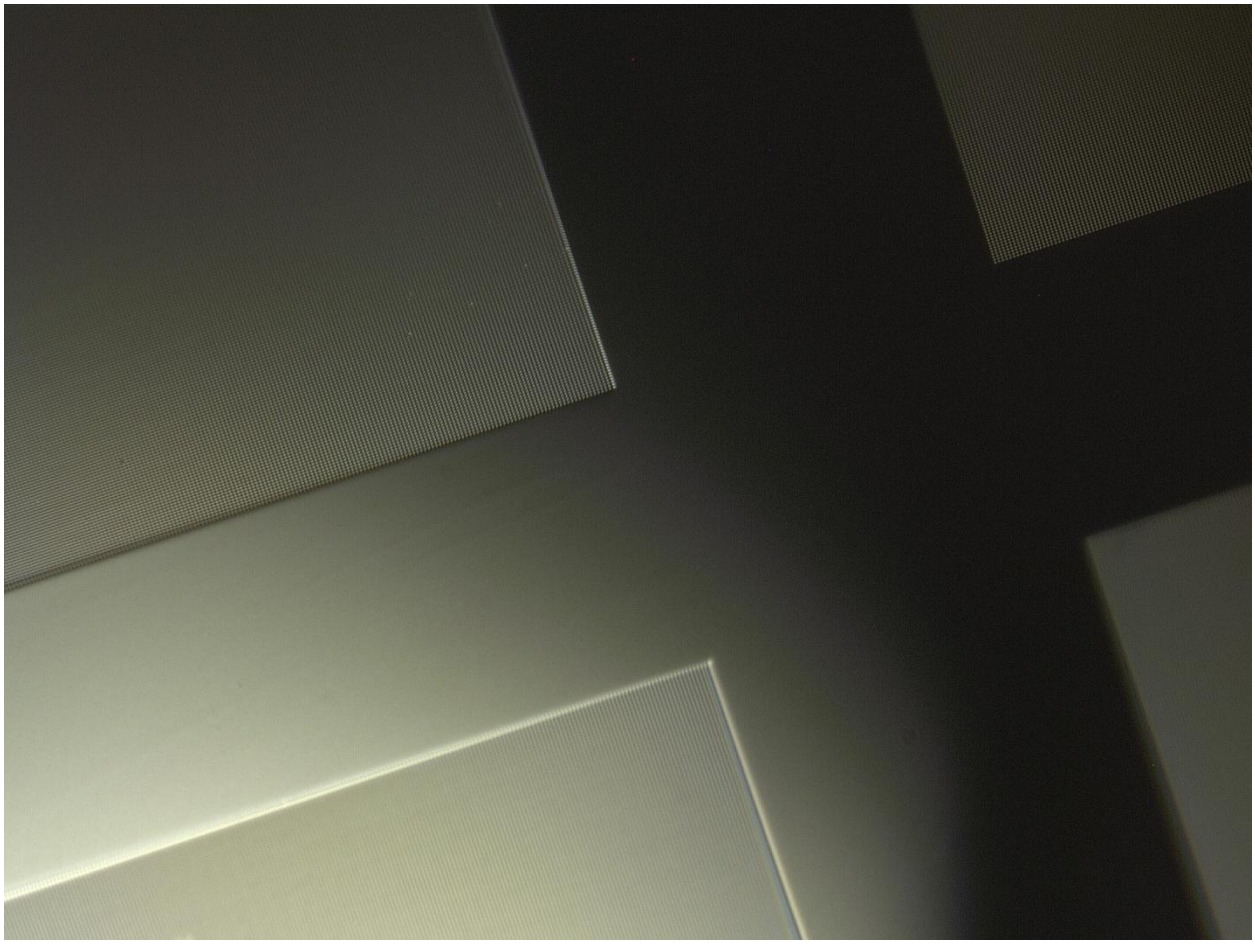

Figure 15: Optical image from a tilt objective microscope of a thinned wafer with exposed TSVs.

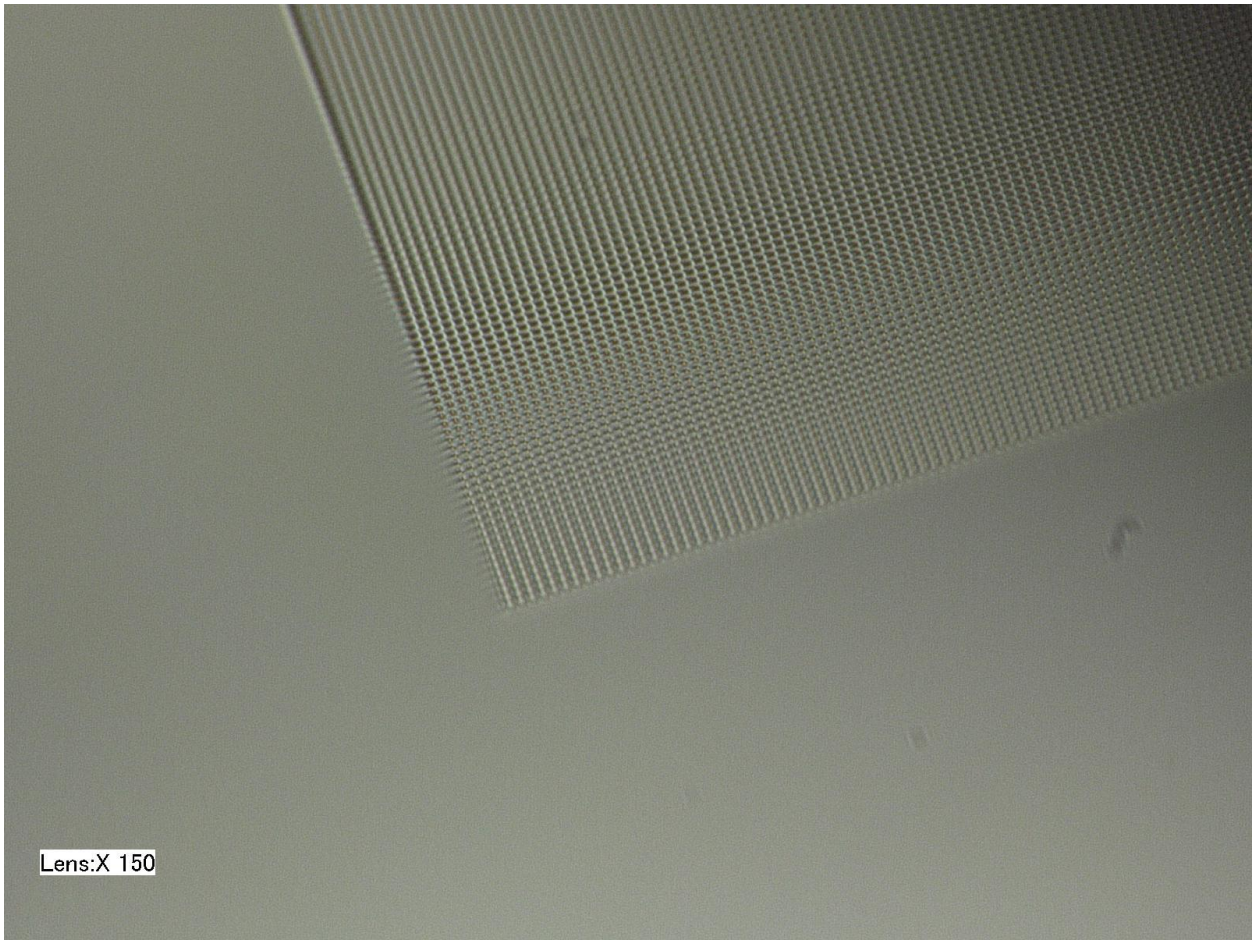

Figure 16: Optical image from a tilt objective microscope of a thinned wafer with exposed TSVs.

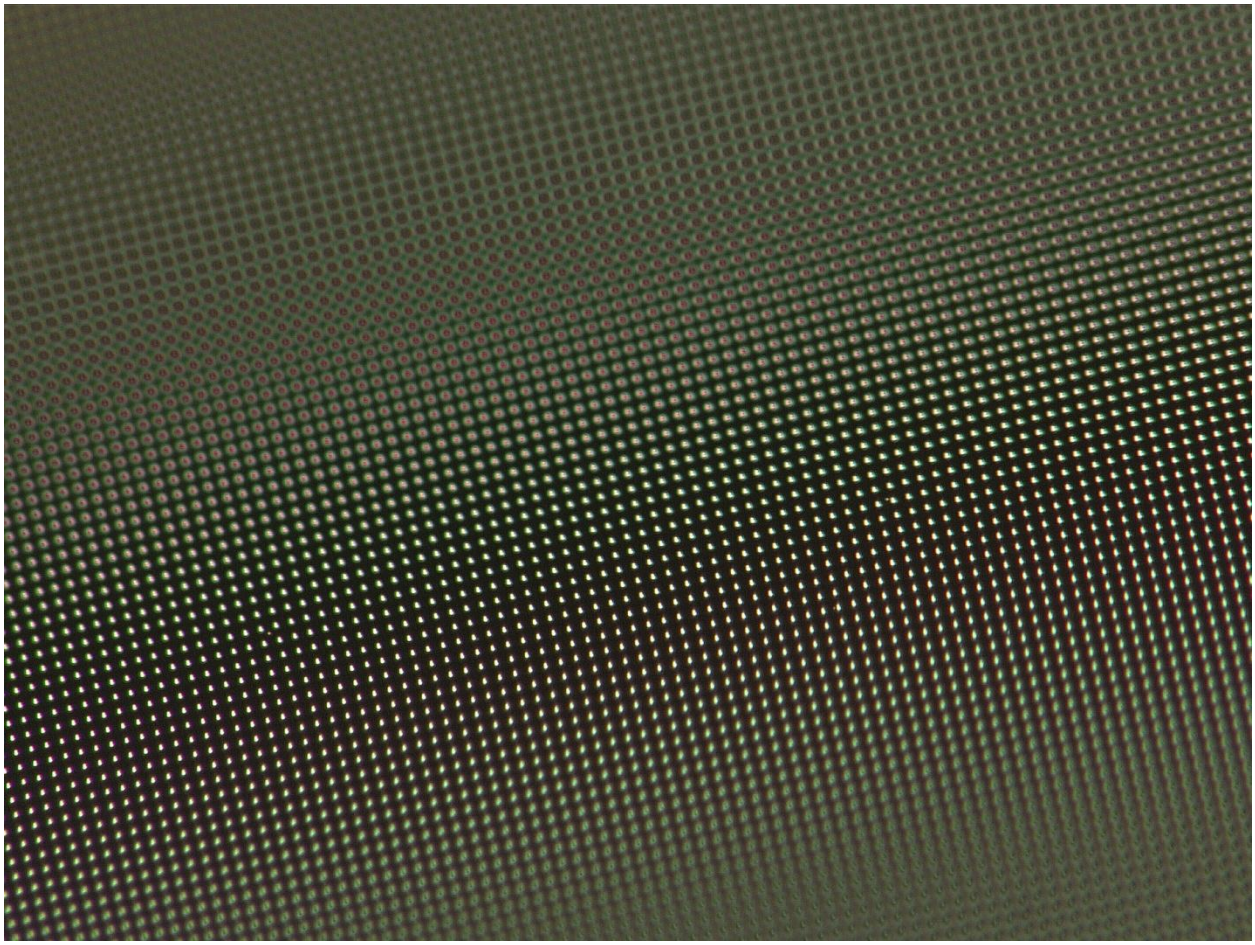

Figure 17: Optical image from a tilt objective microscope of a thinned wafer with exposed TSVs.

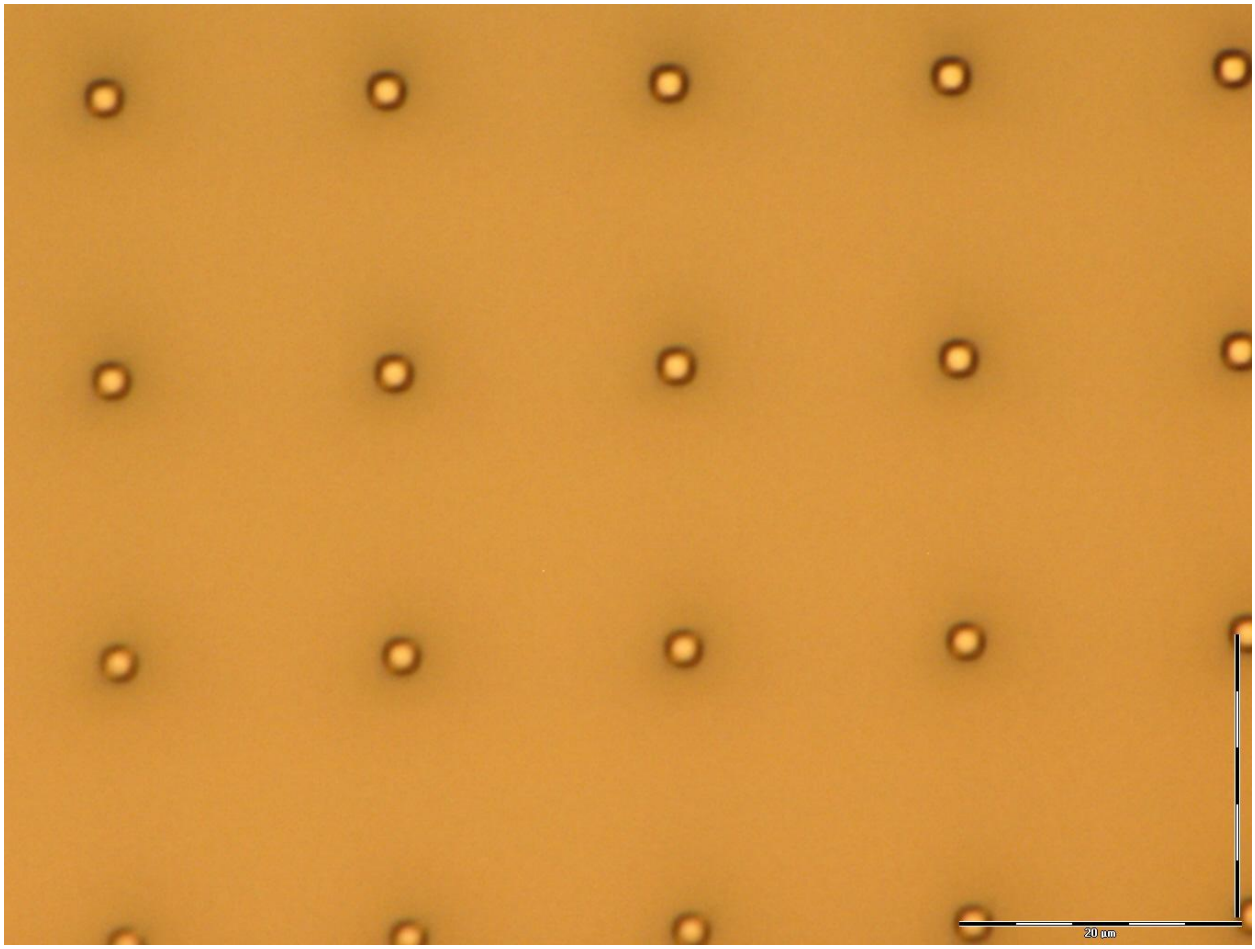

Figure 18: Top down optical microscope image of a thinned wafer with exposed TSVs.

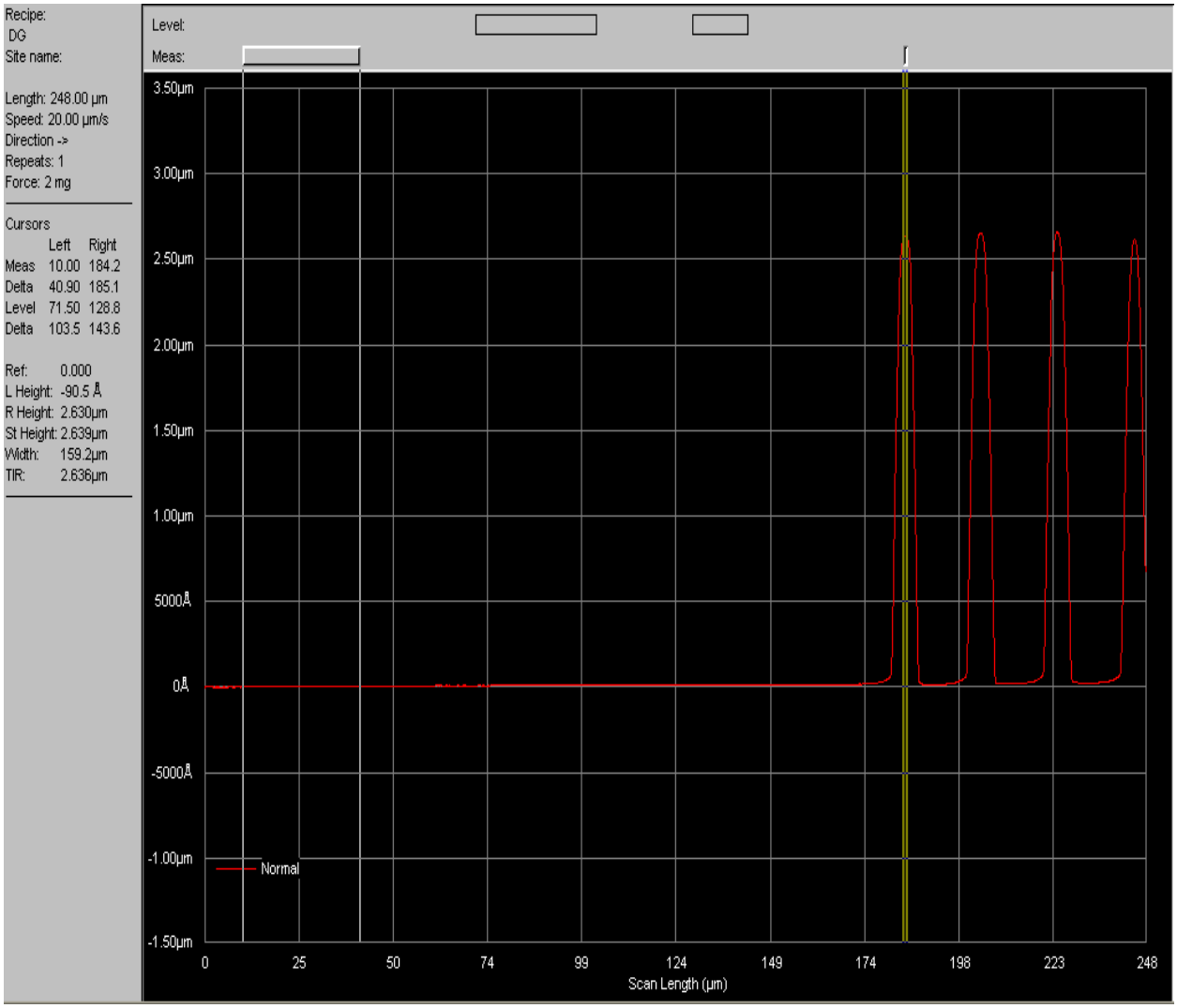

Figure 19: Profilometer measurement of exposed vias.

Dielectric Isolation on Wafer Back Side

For dielectric isolation of TSVs exposed from the backside, we demonstrated plasma enhanced chemical vapor deposition (PECVD) of silicon oxide. We demonstrated processes as low in temperature as 90C, which is compatible with many temporary bonding materials and integration schemes. Demonstrating these processes closes the loop on the third step in the notional process flow in Figure 1. , or spin-on glass. Figure 20 shows a representative SEM image. In this case, we deposited on a high aspect ratio structure to demonstrate the directionality of the deposition. We envision advantage in this directionality because we want oxide on the planar silicon surface but not on the sidewalls of the W plug.

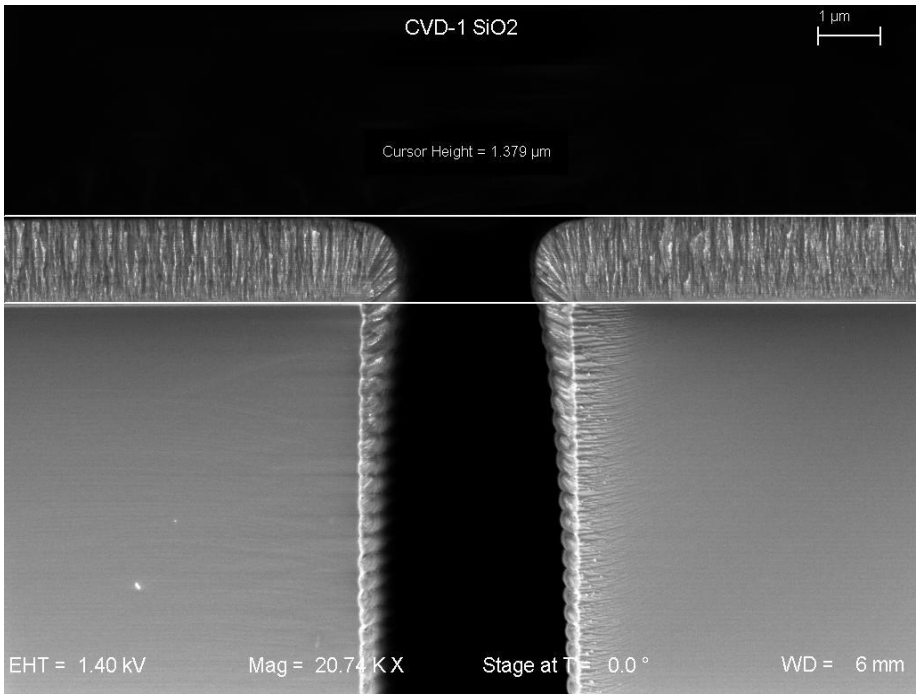

Figure 20: SEM image of PECVD oxide deposited over a high aspect ratio trench.

Pad Formation

Pad formation by lift-off is now a well-characterized process for us. We use a bi-layer resist scheme with AZ5214 as the photo-definable layer and LOR as the lift-off layer. AZ5214 offers as a benefit that it can be forced to perform as either a negative or positive resist. With the bi-layer resist scheme, we can use either developer or solvent to lift the field metal. Also, we can tune the LOR thickness to our metal stack to provide a clean lift over a wide range of metal stack thicknesses. This integration scheme is amenable to a variety of metal stacks. Figure 21 shows a SEM image of metal deposited on a bi-layer resist stack and substrate.

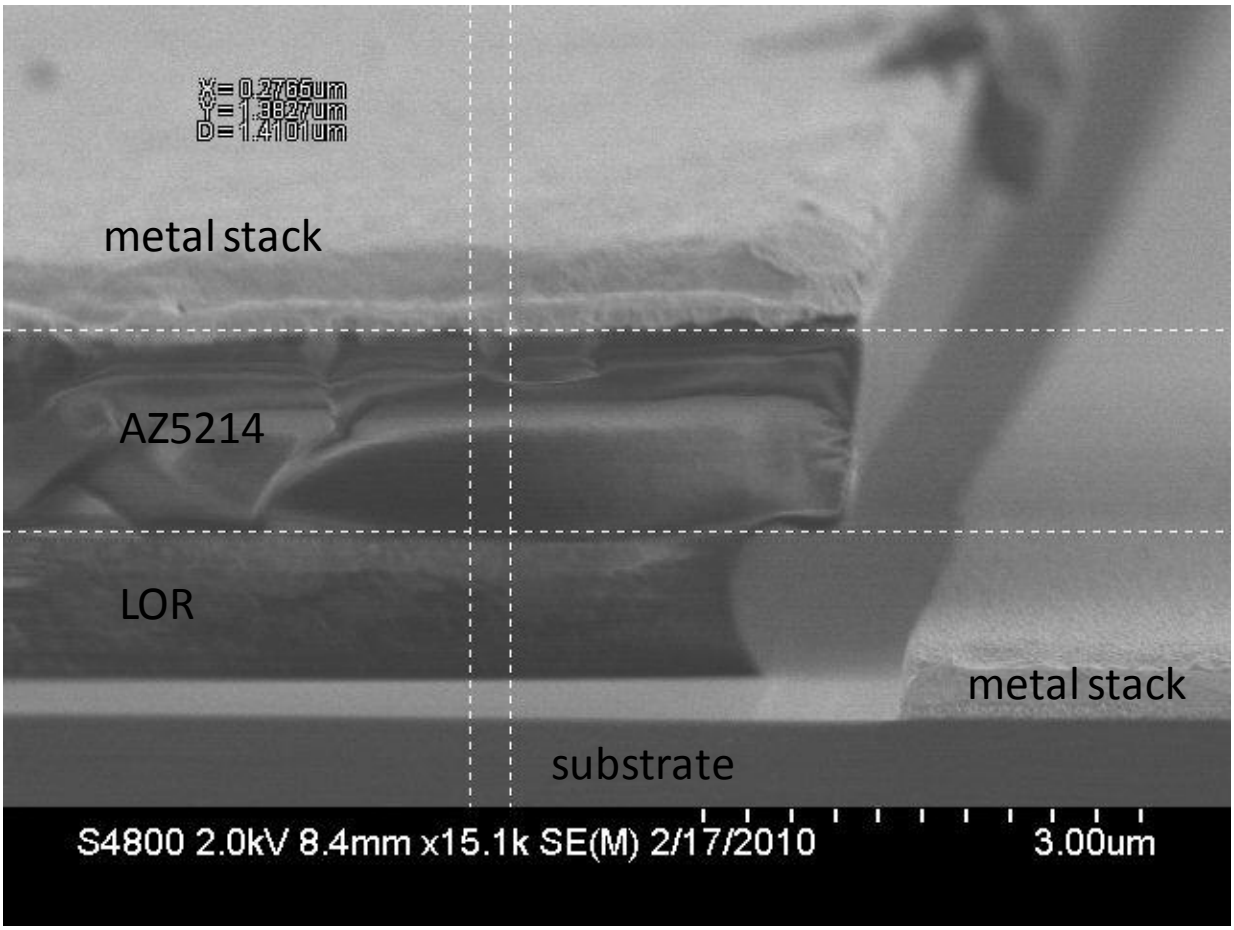

Figure 21: SEM image of metal deposited over a bi-layer resist stack.

CMP to Expose Plugs

One of the key technical risks that we did not have resources to address is the use of CMP to expose the TSVs. This step is illustrated in the fourth step in Figure 1. Once wafer thinning exposes the plugs, the W is still encased in thermal SiO_2. To thin the wafers we choose processes that are intentionally selective to SiO2 so that we do not expose the plug to silicon etchant, and we envision depositing an oxide over the entire wafer back side and following it with CMP to expose the plugs. Following that CMP step, we envision that the W plug will be exposed and planar with the oxide that insulates the Si surface. With that structure, we would be able to form metal pads by liftoff, where the metal contacts the W plugs but the oxide provides dielectric isolation so that the metal pad does not contact silicon (contacting the silicon could potentially short the plugs).

Summary and Conclusions

In our proposal, we identified as milestones:
Design and procure the masks necessary to demonstrate a testable TSV technology characterization vehicle.
Identify, develop, and demonstrate suitable wafer thinning techniques.
Identify, develop, and demonstrate suitable temporary and permanent wafer bonding techniques.
Develop and demonstrate techniques to reveal our TSVs.
Demonstrate a low temperature, low stress SiO2 deposition process.
Develop and demonstrate the CMP processes that remove the oxide over the TSV, so that we can make Ohmic contact to the TSVs.
Demonstrate a pad formation process.
Deliver final report.

We identified the key technical risks as follows:

"The key technical risk of this proposal is that we've carved out a lot to do with a modest amount of funding. We feel that "Key R&D Goals" 1), 4), 5), and 7) are readily achievable. Goal 3) may prove to be very difficult using a temporary bonding media, but we are confident that we can find success with a permanent bond. Goals 2) and 6) are the most challenging, and may prove to be too much for the scope of this effort."

In fact, we made good progress toward all of our milestones with the exception of 6), which we identified as a most challenging milestone, and likely out of scope given the resources. The high point of this effort is our excellent progress toward wafer thinning. Overall, our success through this modest LDRD effort puts us closer to being able to execute 3D integration for vertical wafer stacking, which positively impacts much higher value National Security activities.

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