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sLine: a High Voltage Switcher ASIC for LCLS Detectors with Rolling Shutter

P. Caragiulo*, A. Dragone, R. Herbst, G. Haller

***Abstract*–sLine is a fast-frame 128 dual-channel high-voltage switcher ASIC for 2D SLAC LINAC Coherent Light Source (LCLS) detectors with rolling shutter. The ASIC allows each row of pixels in a sensor to be addressed according to a time-division multiplexing scheme, so that the pixels in the selected row are read out and reset in parallel by a multi-channel front-end ASIC. Optimized for the X-ray Charge Pump Sensor, each channel of the ASIC can operate independently, with two control lines replicating low-voltage control patterns at high voltages. The two high-voltage outputs per channel can be arbitrarily set between ±16 V and are able to switch a 1 nF load within about 300 ns. The active outputs are selected by inserting a token into a bidirectional shift register. Control input level for the ASIC are LVDS. In this paper, the ASIC architecture and performance of the final release are presented.**

I. Introduction

The unique characteristics of X-Ray Free-Electron Laser (X-Ray FEL) sources, in terms of brilliance and narrow pulse duration, have increased the need for new large area detectors with fast read out and specifications that, depending on the experiment, can range from ultra-low noise requirements to extremely large full-scale and dynamic ranges.

Two different column-parallel readout detectors with rolling shutter are under development: one based on the X-ray Active Matrix Pixel Sensor (XAMPS) [1, 4] in collaboration with Brookhaven National Laboratory and one based on the X-ray Charge Pump Sensor (XCPS) [2-3]. Targeted for different kinds of experiments, both systems feature sensors with pixels that can gate the charge transfer by means of dedicated control lines common to the pixels in a single row. Pixels in the same row are read out in parallel using one front-end channel per column. Because of the processes used to fabricate sensors, high voltages are typically required to switch the gating lines [3]. sLine (Fig. 1) is a high voltage switcher Application Specific Integrated Circuit (ASIC) that complements the eLine class [4-6] of multichannel time-variant integrating front-end ASICs that SLAC has developed for the readout of high capacitance 2D sensors with rolling shutter, and for 1D strip sensors. The class is composed of two front-end ASICs, one designed for high-dynamic range applications (eLine10k [4-5]) and one designed for ultra-low noise applications (eLine100 [6]).

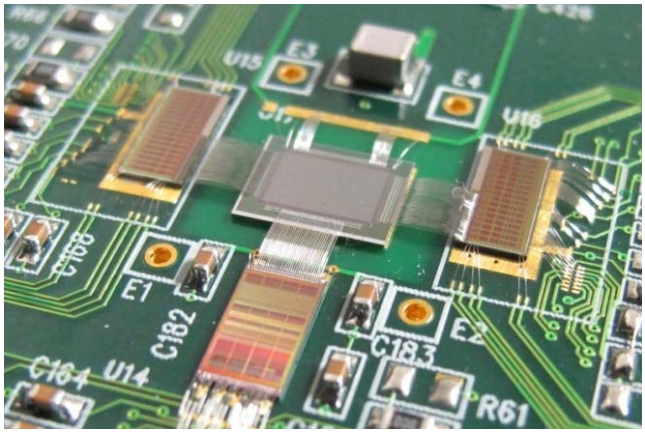

Fig. 1: eLine10k (bottom) bonded to a XCPS (center) operated by two sLine ASICs (left, right).

Optimized for the XCPS, each channel of the ASIC can independently operate two control lines replicating low voltage control patterns at high voltages. The two high voltage outputs per channel can be arbitrarily set between ±16 V and are able to switch a maximum load of 1 nF in about 300 ns. The actual version of the ASIC was fabricated in TSMC 0.18 µm HV LDD-MOS technology. It has 128 dual-channels, a size of 3.4×6.9 mm^2 and a power dissipation of 1 mW/channel at a frame rate of 120 Hz with maximum load. In this paper, after a brief description of the detector system, the ASIC architecture and performance of the final release are presented. In Section II and III the ASIC architecture and some consideration concerning circuit design in high voltage processes are discussed. Sections IV and V are focused on the level shifting cell design. The ASIC layout is described in Section VI. The ASIC characterization and the experimental results are reported in Section VII.

II. Column-Parallel Readout Detector Systems

During the first years of operation at LCLS the need for several new large area detectors arranged in different form factors and shapes, and covering a wide spectrum of experiments has been apparent. Modular, scalable designs are a must. To simplify integration and reduce development time detectors have been designed around common platforms so that dedicated sensing heads could be incorporated in a common detector system. eLine is the first example of a class of ASICs for LCLS sharing a common back-end section and interface to the rest of the system. The class is designed for

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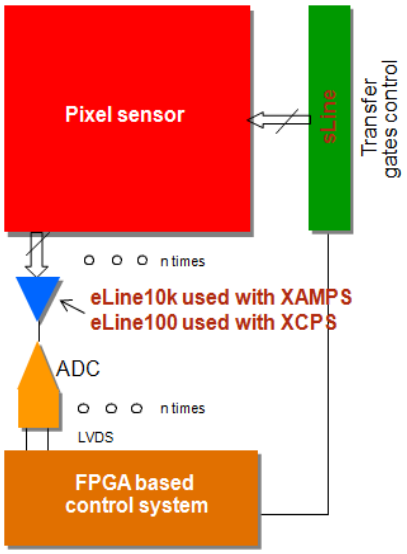

Fig. 2: Column-parallel readout system based on eLine.

column-parallel readout sensors, although it can also be used for the readout of 1D strip sensors.

A typical block diagram of these kinds of systems is shown in Fig. 2. Pixels in the sensor are arranged in a matrix fashion. The collecting nodes of the pixels are isolated by means of a "switch". In applications like XCPS, the collecting nodes are isolated from the collection area by means of controllable potential barriers. In other cases, the switch could be a FET (XAMPS [1, 4]). The "switches" associated with the pixels in a column are connected to the same readout line, while the gates (named transfer gates) of those associated with the pixels in a row are activated simultaneously. Columns of the sensor are read out in parallel by the front-end ASIC. This scheme allows a parallel readout of all the pixels in the same row. The full frame can be read out by cycling through the rows. Each column of the sensor is read out by a dedicated electronic channel.

External commercial ADCs are used to convert the output analog signals. The acquisition is controlled by an FPGA that maintains synchronization between the LCLS beam and the selection of the rows to be read out. Typical array sizes (frame sizes) are in the range of 1024x1024 pixels. In XCPS tiles of 256x384 pixels are considered. Given the repetition rate of the LCLS beam (120Hz) a frame has to be read out in 8 ms which, because of the parallel row readout, turns into a readout time slot of 32 µs per row (i.e., per pixel on a specific readout channel).

III. ASIC Architecture

Fig. 3 shows a simplified block diagram of the sLine ASIC. The ASIC architecture can be divided in two sections: the balcony and the channels.

The channels section has a total of 128 dual-channels. The two outputs (*A* and *B*) per channel can be operated in parallel to control sensors requiring two control lines per row (XCPS) or sequentially to control sensors requiring a single control line per row (XAMPS). When the dual outputs are operated sequentially, a single ASIC can control sensors with 256 rows.

To minimize digital crosstalk around the sensor, non-static digital lines are implemented in LVDS logic. The ASIC has three LVDS inputs: two for the input patterns *A* and *B* and one for the clock called Slot Control (*SC*). The *SC* signal is the only signal required to control the readout protocol in the eLine class of ASIC; its period defines the read out time reserved for each single row of the sensor. In sLine, the *SC* clock controls the movement of tokens in two shift registers used to address sequentially the 128 channels. When a channel is addressed, arbitrary patterns on the *A* and *B* inputs are replicated at high voltage on the respective outputs.

The balcony includes the bias voltage generators, the LVDS receivers, and the control logic. Two additional input lines (*PA* and *PB*) are used to define the default state for the channel outputs. The two shift registers used to address the channels are bidirectional, allowing the ASIC to control the direction in which rows are read out. This feature adds versatility to the architecture, since in many sensors rows can be controlled from both sides as shown in Fig. 1. In that case, the token needs to be moved in the same direction on both controllers. The direction of the token in the shift register is controlled by a dedicated input line (*DIR*). The two bidirectional token

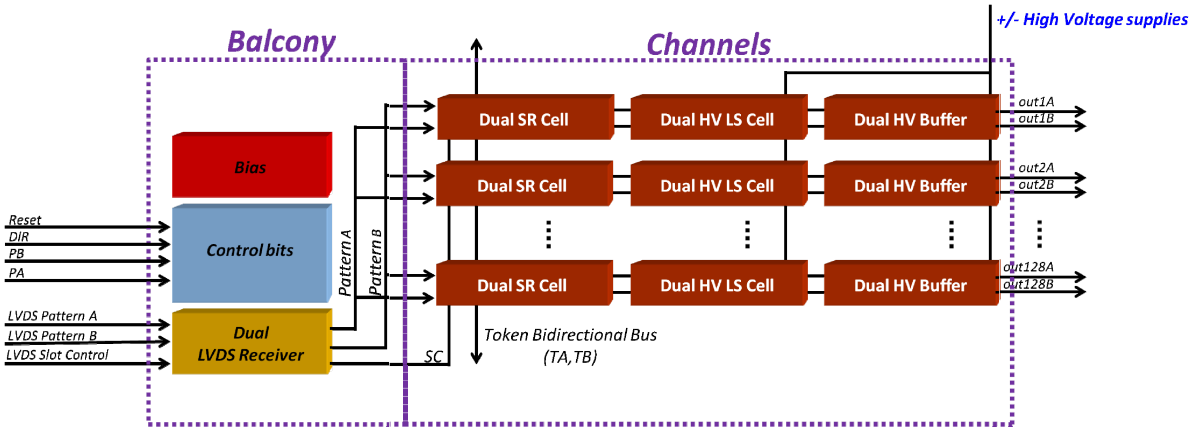

Fig. 3: Simplified block diagram of the 128-channel sLine ASIC.

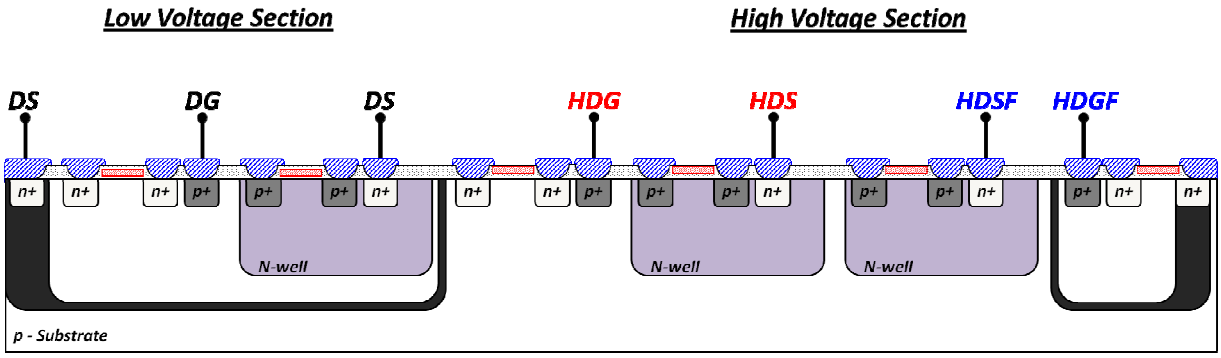

Fig. 4. Simplified cross-section of a typical 0.18µm high voltage process.

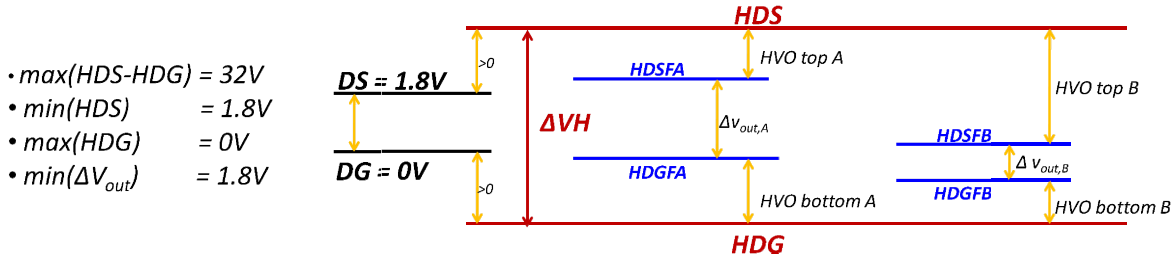

Fig. 5: Supply voltages constraints in sLine.

input/output pads (*TA* and *TB*) are available on opposite sides of the ASIC so that multiple chips can be operated as a daisy chain.

The channel architecture is composed of a low voltage section followed by a high voltage one. Since the high voltage devices are only used in the final stages of the channel, the low voltage and the high voltage sections have been geometrically separated inside the ASIC (Fig. 4) as described in Section VII. When a channel is selected, the low voltage section, built in an isolated well and operated between 0 V (DG) and 1.8 V (DS), receives the two arbitrary patterns (*A* and *B* in Fig. 3) and performs a low-voltage-to-current conversion. Currents are then mirrored using high-voltage MOSFETs and converted into high voltage digital signals. The output voltage levels can be arbitrarily set by changing the voltage supply values. Seven independent supply voltages are required in order to operate sLine as described in Section IV. The low voltage section also includes the cells of the two shift registers which are distributed in the channels (*Dual SR Cell* in Fig. 3).

IV. High Voltage Design Consideration

In order to be able to arbitrarily set the high-voltage output switching levels within ±16 V, independently on both sections *A* and *B*, particular attention must be paid to understand the several wells available in the technology. Wells have different characteristics and incorrect biasing of the p-n junctions at the well boundaries must be avoided. A supply voltage start-up sequence has been defined and implemented on the ASIC printed circuit board to avoid uncontrolled transient behaviors.

Fig. 4 shows a typical high voltage process cross-section where, for simplicity, the Shallow Trench Isolations have been omitted. Constraints on the levels of the required supply voltages are shown in Fig. 5. In sLine the reference voltage is digital ground *(DG)* and a total of seven supply voltages (*DS*, *HDG*, *HDS*, *HDGFA*, *HDGFB*, *HDSFA*, *HDSFB*) are required to bias correctly the wells shown in Fig. 4. While the low voltage section is operated between 0 V and 1.8 V, the wells of the high voltage section can operate at different supply voltages, as described in Section V. *HDS* and *HDG* are respectively the highest and the lowest voltage applied to the circuit and can be adjusted according to the application. *HDS* must be set higher than DS and *HDG* must be set negative and lower than DG. Their difference ΔVH can be as high as 32 V. The difference ΔV_{out} between the ASIC output levels *HDSF* and *HDGF* must be smaller than ΔVH and can be arbitrarily set between 1.8 V and 32 V. Note that *HDSF* and *HDGF* can also be set both positive or negative.

V. Level Shifting Cell

256 level-shifting cells are present inside the ASIC. Fig. 6 shows a simplified schematic of the cell.

A differential pair designed in the low-voltage section of the channel receives the low-voltage input pattern. According to the input pattern, the current in the tail transistor M_{TAIL} is steered into one of the two branches and then mirrored into the high-voltage section through the high-voltage transistors M_{L1}, M_{M1}, M_{L2} and M_{M2}.

The high-voltage signal at node *v* is then regenerated with a high-voltage inverter and sent to the *HV Buffer* at the output. The *HV Buffer* is composed of two inverters optimized to minimize delay and increase speed. Its output stage is built in isolated p and n wells translating the *HV Buffer* input pattern to arbitrary output levels *HDSF* and *HDGF*.

The boundary between the low-voltage and high-voltage sections is represented by the transistor pair M_{CS}. These

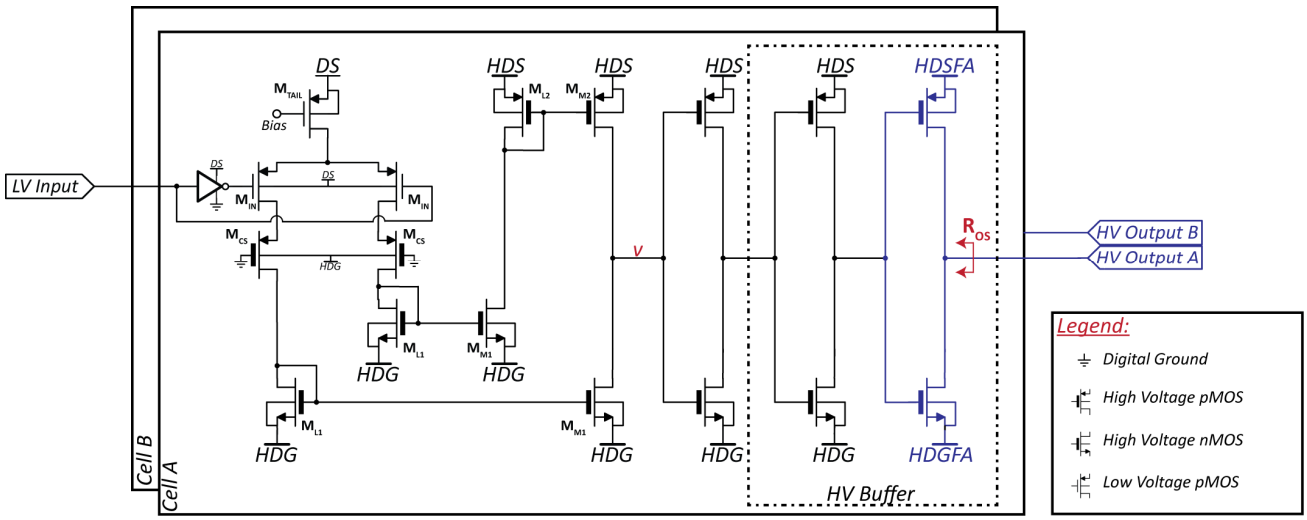

Fig. 6: sLine simplified Level Shifting Cell schematic.

MOSFETs must be high-voltage devices and they must be biased in order to avoid the drain of M_{IN} being biased below *DG*. For this reason the gates of M_{CS} have been connected to *DG*.

TSMC 0.18 µm HV LDD-MOS technology allows symmetric and asymmetric high-voltage MOSFETs. Because of their smaller capacitance and minimum length, asymmetric devices have been used for the cascode MOSFETs M_{CS} and in the mirrors M_{L1}, and M_{M1} in order to reduce the total delay.

Typical load capacitance for our applications can be as high as 1 nF. With this large capacitive load, an output time constant of 100 ns is required to achieve rise and fall times within 5 % of the final value in 300 ns. The output time constant depends on the maximum load capacitance $C_{LOAD,max}$ and on the output resistance R_{OS} of the output *HV buffer* according to the formula in (1).

$$\tau = R_{OS} \cdot C_{LOAD,\max} \tag{1}$$

For a capacitive load of 1 nF an output resistance smaller than 100 Ω is required. When the output value is high R_{OS} will be determined by the output resistance of the pMOS in the output inverter, instead when the output value is low R_{OS} will be determined by the output resistance of the nMOS.

When the final output value has been reached the driving transistor is in the linear region. The equivalent output resistance R_{OS} is small and inversely proportional to the transistor V_{GS}. Note also that for given output levels *HDSF* and *HDGF,* by increasing the voltage difference (called *HVO* in Fig. 5) between *HDSF* and *HDS,* and *HDGF* and *HDG*, respectively, the output resistance R_{OS} and the delay decrease. This feature is discussed in the next section. The size of the output transistors has been chosen as a compromise between output delay and transition speed.

VI. Simulation Results

In this section the switching speed, the delay and the power consumption of the ASIC are analyzed as a function of the biasing voltages.

The switching speed of the output voltage depends on the ΔVH difference between *HDS* and *HDG*. An example of the simulated behavior of sLine showing this feature is reported in Fig. 7. Here a comparison between the behaviors of the ASIC operated at ΔVH equal to 30 V (Fig. 7a) and ΔVH equal to 10 V (Fig. 7b), are presented. In the simulation the clock (*SC*) period is 8 µs. The output of channel 0 is connected to a 1 nF capacitor, while the output of channel 1 has been kept floating. This figure shows also that the output voltages *HDSFA (HDSFB)* and *HDGFA (HDGFB)* can be set differently. As shown in Fig. 7a (*CH1A),* when the supply voltages *HDS* and *HDG* are ±15 V, ΔV_{out} is 30 V and a capacitive load of 1 nF is present, the time rise and fall time are 260 ns and 270 ns, respectively. These results lead to a R_{OS} of 90 Ω. Keeping the supply voltages *HDS* and *HDG* at ±15 V, the value of ΔV_{out} has negligible impact on the speed of the output signal (Fig. 7a *CH1B*). Instead (Fig. 7b *CH1A*), when the supply voltages *HDS* and *HDG* are ±5 V, ΔV_{out} is 5 V and a capacitive load of 1 nF is present, the rise time and fall time are 420 ns and 400 ns, respectively. In this condition the R_{OS} is about 140 Ω. The dependence of the switching speed on the difference between *HDS* and *HDG* is apparent and a plot of the R_{OS} versus ΔVH is reported in Fig. 7c.

The input to output delay is also affected by the value of ΔVH. Increasing ΔVH the delay is reduced and a minimum delay of 55 ns can be reached. The influence of ΔVH on the delay is shown in Fig. 7c.

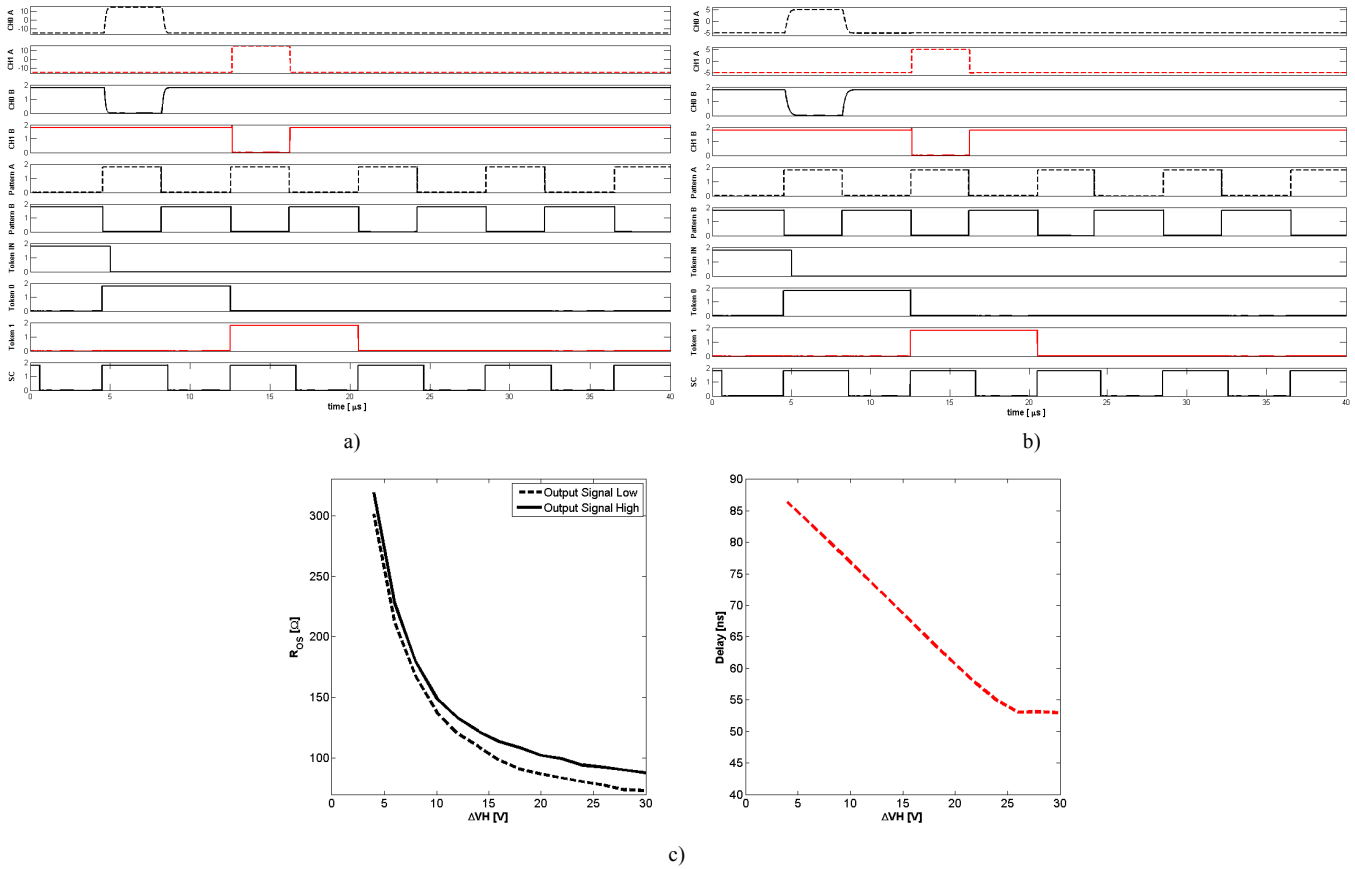

Fig. 7: Transient behavior of signals in sLine when ΔVH is equal to 30V *(a)* and 10V *(b)* and simulated output resistance R_{OS} and delay as function of ΔVH *(c)* .

The ASIC power consumption depends on the output switching speed. According to the required frame rate and the capacitive load imposed by the size of the sensor, the minimum required switching speed should be selected, reducing ΔVH to minimize power consumption. Considering a period of 8 µs and assuming a maximum load of 1 nF, to reach rise and fall times of 300 ns at full swing of 32 V, the average energy dissipation is 2 µJ. Since in each period two transitions are present, this result leads to an energy dissipation of 1 µJ/transition. When sLine is used to control one XCPS matrix of 256 x 384 pixels, at the LCLS pulse rate of 120Hz, it dissipates a power of 1mW/channel.

VII. Layout

The ASIC has been fabricated in TSMC 0.18 µm HV 1P6M LDD-MOS technology. It has 128 dual channels and a size of 3.4×6.9 mm^2.

To minimize latch-up effect, each high voltage MOSFET has its own guard ring. The low voltage section of the circuit is laid out in a separate well closer to the input pads. It has been possible to divide geometrically the ASIC layout floor plan between the low voltage and the high voltage sections because HV MOSFETs are used just in the final stages of the channel. The channel pitch is 36 µm while four rows of staggered output pads have been provided to accommodate two outputs every 56 µm as required by XCPS.

The sLine layout is shown in Fig. 8.

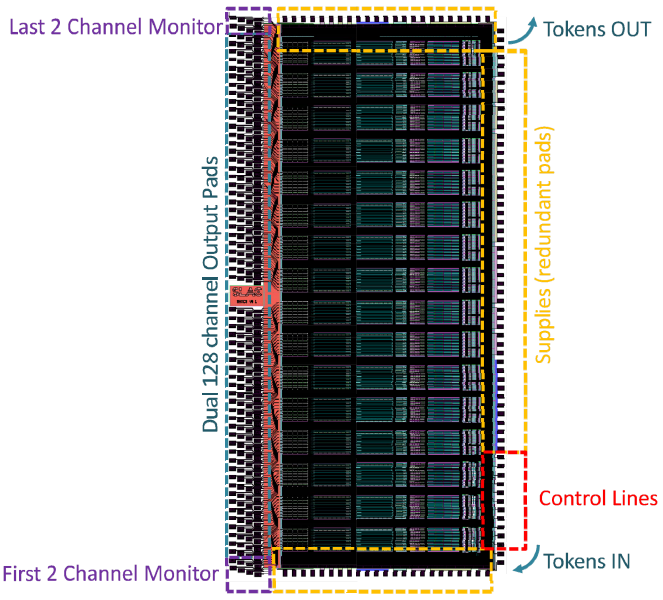

Fig. 8: sLine ASIC Layout.

VIII. Experimental Results

As an example of the performance achievable with sLine, some measurements from the set of characterization tests performed are reported. Fig. 9 shows the response for a 27 V swing in a 1 µs period with and without a capacitive load connected at the output of a channel. For a 1 nF load the waveform shows a T_{rise} and T_{fall} of about 300 ns, which corresponds to a R_{OS} of about 100 Ω.

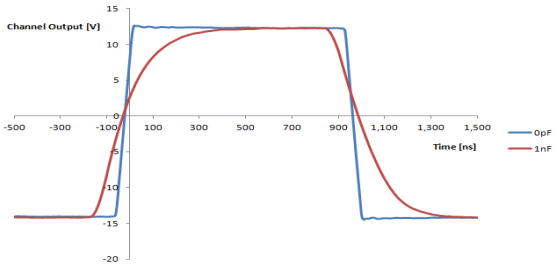

Fig. 9: Measured response for a 27 V swing with no load and with a 1nF load.

Fig. 10 shows a detail of a transition edge for a ±1 V swing and various capacitive loads measured with a Δ*VH* of 10 V. At low Δ*VH* the value of R_{OS} increases. As apparent from the figure, in this condition, for a maximum load of 1nF, the T_{rise} and T_{fall} are on the order of 600 ns which corresponds to a worst case R_{OS} of about 200 Ω.

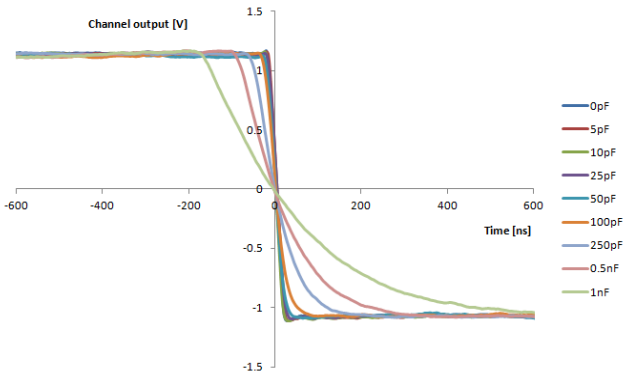

Fig. 10: Measured response for a ±1 V swing with different loads.

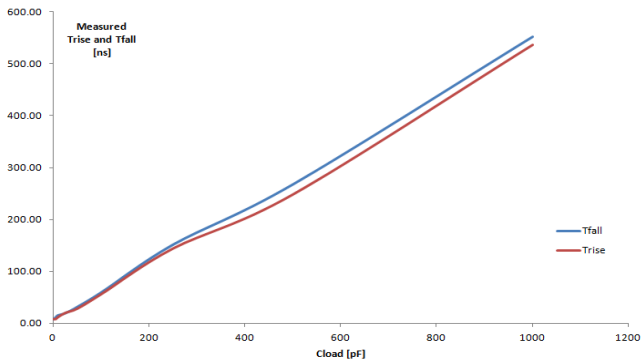

Fig. 11: Measured T_{rise} and T_{fall}. Worst case scenario.

Fig. 11 shows the dependence of T_{rise} and T_{fall} on the output load for minimum output swing.

IX. Conclusion

sLine is a high voltage switcher ASIC that complements the eLine class of multichannel time-variant integrating front-end ASICs that SLAC has developed to satisfy the demanding experiments at LCLS. The class is optimized for the readout of high capacitance 2D sensors with column-parallel readout and rolling shutter. sLine has been designed to control the selection of the sensor rows which typically require high voltages switched in short times.

The ASIC is able to switch 32 V on a 1 nF capacitive load at a speed of 300 ns (Tab. I). At these biasing conditions the power consumption is about 1 mW/channel.

Output switching levels can be arbitrarily adjusted within 32 V.

TABLE I
sLine Performance

Technology	TSMC 0.18µm High Voltage LDD - MOS
Die Area	3.4×6.9mm^2
Power Consumption	1mW/channel (in XCPS applications)
T_{rise}	300 ns
T_{fall}	300 ns
Output Swing	from 1.8V to 32V adjustable

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