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Characterization of Epitaxial Film Silicon Solar Cells Grown on Seeded Display Glass

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***Abstract* — We report characterization of epitaxial film crystal silicon (c-Si) solar cells with open-circuit voltages (V_{oc}) above 560 mV. The 2-um absorber cells are grown by low-temperature (<750 ˚C) hot-wire CVD (HWCVD) on Corning® EAGLE XG® display glass coated with a layer-transferred (LT) Si seed. The high V_{oc} is a result of low-defect epitaxial Si (epi-Si) growth and effective hydrogen passivation of defects. The quality of epitaxial growth by HWCVD on seeded glass substrates depends on the crystallographic quality of the seed and the morphology of the growth surface. Complete heterojunction cells consist of glass/c-Si LT seed/ epi n^+ Si:P/epi n^- Si:P/intrinsic a-Si:H/p^+ a-Si:H/ITO. Similar devices grown on electronically 'dead' n^+ wafers have given V_{oc} ~ 630 mV and ~8% efficiency with no light trapping features. Here we study the effects of the seed surface polish on epi-Si quality, how hydrogenation influences the device character, and the dominant junction transport physics.**

***Index Terms* — epitaxial layers, glass, silicon, solar energy.**

I. Introduction

The commercial photovoltaic market continues to be dominated by crystalline silicon wafer technology. However, epitaxial film-silicon on seeded low-cost substrates ("epi on seed") is a viable technology that could provide reduced manufacturing costs without sacrificing efficiency. Our group is exploring growth of epitaxial films on low-cost, seeded-substrates by hot-wire CVD (HWCVD). HWCVD allows nearly defect free epitaxial growth on wafers at deposition rates > 1.8 µm/min nearly 300 to 400 ˚C below typical chemical vapor deposition epitaxy[1]. The lower HWCVD growth temperature allows low-cost, low-temperature substrates, such as display glass, to be used as the substrate for large area crystal film silicon solar modules. Though NREL has investigated a variety of homo- and heteroepitaxial seeds on glass substrates, this contribution will focus mainly on layer-transfer (LT) c-Si films oxide-bonded to Corning® EAGLE XG® glass (hereafter SiOG) [2, 3]. Our study explores the influence of the surface preparation of the seed layer to obtain low-defect density epitaxial films, and compares material quality and device characterization between SiOG and wafer-based devices. Not surprisingly seed layer surface preparation greatly influences the epi-Si and device quality. We find that with a seed layer surface roughness nearly 10x rougher than a wafer, we get about 10x more dislocations and a lower V_{oc} compared to epi-Si devices grown on prime polished n^+ wafers. Yet, the V_{oc} obtained in our preliminary study are the highest reported for crystal Si films on display glass.

II. Experiment

Two types of substrates are explored in this study: 1) electronically 'dead' n^+ Si:P wafers with a prime surface polish in which photo generated carriers have minimal chance to be collected; and 2) LT c-Si films oxide-bonded to Corning® EAGLE XG® glass (SiOG).

Epitaxial films are grown on the LT seed layer by HWCVD using a gas mixture of SiH_4, H_2, and PH_3 over the temperature range of 650 – 830 ˚C. Emitters are formed by growing a heterojunction structure with hydrogenated amorphous Si [i a-Si:H (~5 nm), p a-Si:H:B (~15 nm)] in separate HWCVD deposition chambers.

An In_2O_3:Sn film provides a transparent conducting contacting layer and an antireflective coating. Device mesas are photolithographically defined and isolated with reactive ion etching using SF_6 gas. Back contacts are formed to a grown-in, heavily doped back surface field layer (Fig. 1). For epi-Si devices on 'dead' wafer, contact is made directly to the highly conducting wafer and no n+ layer is grown. Measurements of illuminated current density vs voltage (JV) are done with a calibrated AM1.5 solar simulator to give the operating parameters for the

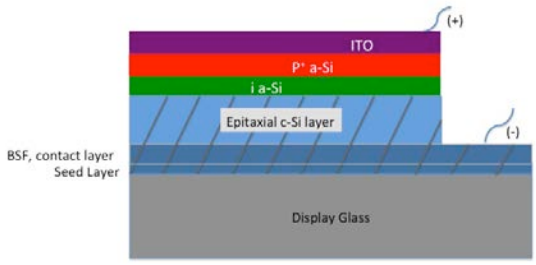

Fig. 1. Device schematic.

solar cell. Light and dark JV measurements are made between 150 K – 350 K with a Linkam Scientific cryostat and a Keithley 6517B electrometer. Quantum efficiency (QE), capacitance vs voltage (C/V) measurements are made with custom equipment.

III. Seed Preparation

The LT seed layers were exfoliated from wafers following a hydrogen implant to a specified depth and annealing to form hydrogen platelets. Before the seed layer is exfoliated, the wafers are oxide-bonded to display glass. The exposed surface (cut layer) of the exfoliated seed is quite rough (see Fig. 2 (left)) with an average surface roughness of about 8 nm, compared to < 0.1 nm average surface roughness of the polished wafers. Silicon on insulator (SOI) wafers formed from either smart cut technology or by porous silicon layer transfer, when used in the IC industry, are commonly heated to 1150 ˚C in 80 Torr hydrogen for 1 hour to dramatically reduce the surface RMS roughness to below 0.1 nm [4]. A similar high T anneal was used by Gordon et al. to smooth exfoliated seeds on spinel glass-ceramic substrates before 1130 °C epitaxial growth [5]. On SOI and glass-ceramic, the substrate can withstand the high annealing temperatures necessary for surface reconstruction of the

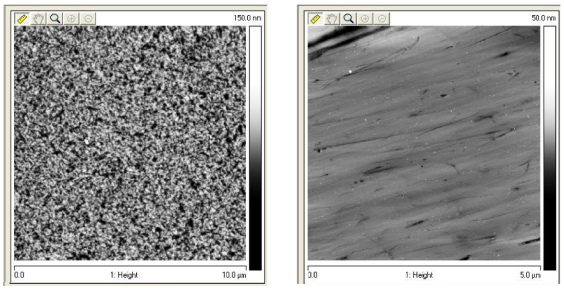

Fig. 2 AFM images of (left) as cut SiOG and (right) after CMP.

seed layer. Corning® EAGLE XG® glass, used in this study, is far less costly than the glass-ceramic, but has an annealing temperature of 722 ˚C and a softening point of 971 ˚C. Even though the price point for this type of glass is low enough for use in low-cost solar modules and the working temperatures are compatible with HWCVD epitaxy, the display glass cannot sustain a high-temperature hydrogen anneal necessary for surface reconstruction. We therefore explored two low-temperature techniques to smooth the surface of the seed layer for epitaxial growth. Our first approach was to perform a chemical/mechanical polish (CMP) on the seed, being careful not to grind away the entire 600-nm-thick as-cut seed layer. Removing about 400 nm of c-Si reduced the average surface roughness to 1 nm. However, polishing introduced groves into the surface of the seeds, as visible by AFM (Fig. 2 (right)). Our next approach was to anneal the seeds in hydrogen at 800 ˚C for 30 mins. This proved insufficient to improve the surface roughness of either the as-cut or polished seed layers.

IV. Epitaxial Films On Seeds

Epitaxial films are grown on the polished seed layers by placing them on a vertically-oriented heater in the HWCVD epitaxial reactor and heating to just below the unsupported deformation point of the 1" x 0.45" glass substrate. We measure this maximum sustainable temperature to be about 775 ˚C by using *in situ* spectroscopic ellipsometry[6]. Our previous research indicated that oxide growth on the surface prior to epi-Si deposition induces dislocations in the epi film that propagate through the film to the surface [7]. We therefore start our epi-Si growth with oxygen-filtered silane. We then use a SiH_4/ PH_3 mixture, without filtering, to form the n^+/n^- layers. Optical and scanning electron microscopy (SEM) images of the surface of the epi-Si films show sparse ($<10^4$ cm^{-2}) crystallographic pits and defect densities. Electron-beam induced current (EBIC) images on fully processed devices show active defect densities on the order of 10^4 – 10^5 cm^{-2}. TEM studies show these defects are predominately dislocations and twins.

V. Hydrogenation

Once the n^+/n^- epitaxial films are grown, the samples are hydrogenated in a custom-built remote plasma, rapid thermal annealing system. As-grown films have about

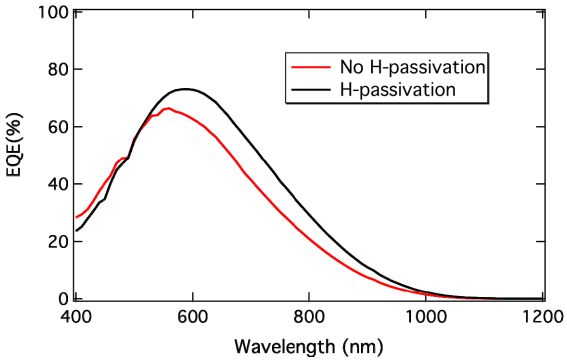

Fig. 3 External quantum efficiency with and without hydrogen passivation.

$2x10^{17}$ cm^{-3} H somewhat uniformly distributed throughout the film (determined by SIMS). After hydrogenation, H

concentrations increase ~10x in the top 1µm of the film and decrease to ~4 x10^{17} cm^{-3} near the back of the film. Hydrogenation improves both J_{sc} and V_{oc}. Fig. 3 shows typical EQE data for nominally identical devices on n+ wafers with and without hydrogenation.

The QE in the 400 – 550 nm range is almost identical before and after hydrogenation, however there is a pronounced increase in the QE for the hydrogenated sample beyond 550 nm out to 1000 nm. A fit to the QE data in the IR region indicates an increase in the effective diffusion length (L_{eff}) in the bulk with hydrogenation[8]. Minority carrier lifetimes, when measured on bare epi-Si films by resonance-coupled photoconductive decay (RCPCD), are about 10-15 ns, corroborating QE-determined L_{eff} measurements of about 3-5 µm. These data indicate an improvement in the bulk of the epi, but not a significant change near the surface of the epi-Si films with hydrogenation.

VI. Device Fabrication and Characterization

Following hydrogen passivation of the epi-Si layer, emitter heterojunction layers of a-Si (i) and a-Si:H (p^+) are deposited by HWCVD in a separate deposition chamber after an air break and dilute HF etch. A 70 nm ITO layer is then deposited by reactive evaporation of an In/Sn compound to give a contact and Anti-Reflection layer. Devices are defined by photolithography, and then a wet chemical etch is used to remove the ITO and a dry reactive ion etch (RIE) removes the n^- layer down to the n^+ back contact layer (see Fig. 1). This n^+ layer is

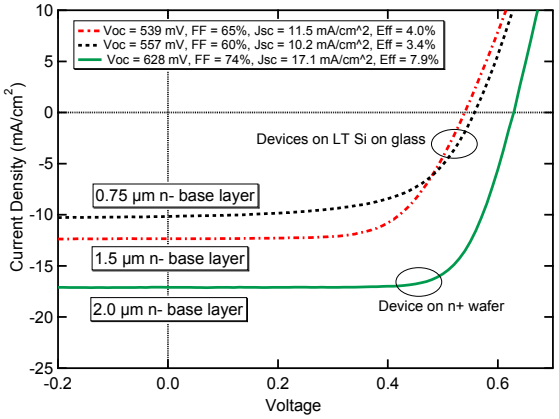

Fig. 4 Current density vs voltage for several devices described in the text.

necessarily thick (~2 µm) to provide a large RIE process window in order to stop the RIE etch within the n^+ layer. A thicker n+ layer provides more lateral conduction to the back contact and thus a lower R_{series}, but it also introduces a larger 'dead' layer in the device that absorbs light without providing carriers that contribute to the current. Fig. 4 shows typical JV curves for heterojunction devices on glass substrates and on a 'dead' n+ wafer.

The relatively high open circuit voltages (630 mV for n^+ 'dead' wafer devices and 560 mV for SiOG devices) indicate high quality material (L_{eff}/W >3) and junction formation, whereas the low fill factors show that our R_{series} remains too high despite the thick n^+ layer. R_{series} is much larger in the SiOG devices compared with the wafer devices (Fig. 4) due to inadequate n+ doping in the back contact layer, which contributes to the lower FF. However, the lower V_{oc} values for SiOG devices are a result of shorter diffusion lengths and a defective junction surface due to a higher dislocation density in the SiOG epi-Si layers. These dislocations may act to shunt the

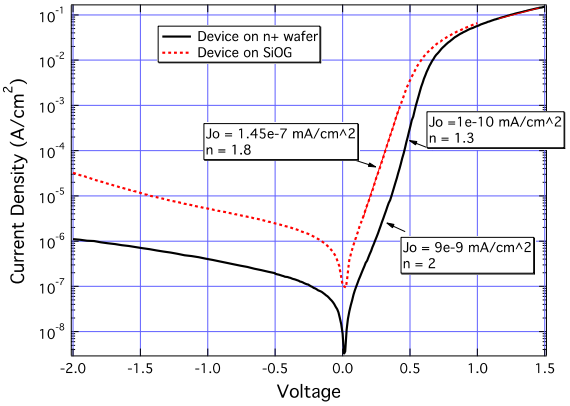

Fig. 5 Dark current density vs voltage data for SiOG device and device on n^+ wafer.

device and/or introduce recombination centers within the depletion region [9]. Both of these effects result in a higher dark saturation current density (Fig. 5), higher

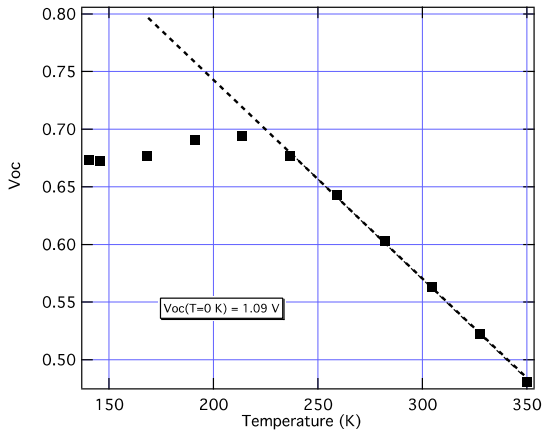

Fig. 6 Temperature corrected Voc vs Temperature data for a device on SiOG.

ideality factors near V_{oc} (Fig. 5) and higher surface recombination velocities (S_p) at the heterojunction interface (see below) in SiOG devices compared with wafer based devices. The dark JV data of Fig. 5 reveal that our devices on n+ wafers show the typical voltage dependence in forward bias as high efficiency wafer-based heterojunction devices[10]. However, our SiOG devices show forward bias JV(Temperature) characteristics typical of surface dominated recombination. To verify this, Fig. 6 shows V_{oc} vs Temperature data for a SiOG device. The temperature-corrected V_{oc} at T=0 K is less than the bandgap of silicon, indicating interface recombination likely dominates junction transport[11]. Combining V_{oc} vs J_{sc} data with a built-in potential value measured by capacitance vs voltage data (not shown), we find front surface interface recombination velocities much higher in SiOG devices, compared with low-defect density wafer based devices confirming that surface recombination dominates in SiOG devices.

These preliminary results on high V_{oc} SiOG devices are encouraging for this technology. However, much work is needed to reduce defects to increase both the bulk and surface quality in these devices.

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