Transistor operation and mobility enhancement in top-gated LaAlO$_3$ / SrTiO$_3$ heterostructures

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(Dated: June 17, 2013)

Abstract

We report the operation of LaAlO$_3$ / SrTiO$_3$ depletion mode top-gated junction field-effect transistors using a range of LaAlO$_3$ thicknesses as the top gate insulator. Gated Hall bars show near ideal transistor characteristics at room temperature with on-off ratios greater than 1000. Lower temperature measurements demonstrate a systematic increase in the Hall mobility as the sheet carrier density in the channel is depleted via the top gate, providing a route to higher mobility, lower density electron gases in this system.

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The electric field-effect has been successfully applied in a top-gate geometry to create normally-off transistors in undoped $SrTiO_3$ (STO).[1, 2] Diverse properties have been studied including superconductivity,[3, 4] thermo-electricity,[5] Kondo physics,[6] and percolation effects.[7] The normally-on interface between $LaAlO_3$ (LAO) and TiO_2 terminated (100) STO [8] has also been electrostatically modulated from the back-side using the STO substrate as the gate dielectric.[9–17] Although back-gating is rather robust and reliable, it simultaneously changes many parameters, most notably the confining electric field strength at the interface, Hall mobility and sheet carrier density.[11] Hence back-gating by itself does not allow low sheet carrier densities to be reached while maintaining relatively high Hall mobilities. Nor can the Rashba spin-orbit coupling be controlled independently of the sheet carrier density. Top-gating is a natural complimentary technique to tune the electronic properties: as is well-known in conventional semiconductor systems both the top- and back-gate geometries change the confining potential of the electron gas, but the spatial extent of the envelope electron wavefunction is altered in quite distinct ways for the two cases.[18]

The challenges of switching on devices at low temperatures with a top gate in STO,[2] can be mitigated by using the depletion mode of junction gate field-effect transistors. Somewhat surprisingly however, given the attractively large band-gap of the over-layer in LAO/STO heterostructures, top-gate depletion devices have only recently been demonstrated by Förg et al.[19] over a temperature range 173 K $\leq T \leq$ 373 K. These devices had a fixed LAO thickness, $d_{LAO} = 9$ unit cells (uc), and short (20 μm - 200 μm) and wide (1600 μm) channels, to enable device operation with a reduced channel resistance and gate leakage. However the two-probe device geometry prevented the determination of the sheet carrier density, n, and hence the Hall mobility. Here we employed micrometer-scale Hall bars to enable precise Hall measurements, and study the field effect on the carrier density, for various d_{LAO}. Ideal transistor operation with top-gating was demonstrated, as evidenced by the direct scaling of the mobile sheet carrier density obtained from the Hall effect with the expected modulation by the top-gate voltage, V_{GS}. A sheet carrier density modulation of up to 1.7×10^{13} cm^{-2} was achieved with V_{GS} in the range -1 V $\leq V_{GS} \leq$ +1 V and 2 K $\leq T \leq$ 300 K. Notably, at lower temperatures the Hall mobility was significantly enhanced with field effect depletion of the electron gas, demonstrating the potential of top-gating to reach low sheet carrier density and high mobilities.

The LAO/STO heterostructures were fabricated by pulsed laser deposition on TiO_2 termi-

nated STO (100) substrates using a pre-deposited amorphous AlO_x hard mask to define the Hall bar as described elsewhere.[11] The LAO thicknesses were in the range 4 uc $\leq d_{LAO} \leq$ 22 uc. The channel length covered by the gate was 400 μm, and the channel width in the range $W = 5-200$ μm. The top electrode was formed using *ex-situ* sputtered Au with thickness ~ 100 nm, and the source and drain were contacted with Al ultrasonic wirebonding. Figure 1(a) and (b) shows an optical image of a typical device, showing the source, drain and gate contacts, together with a schematic device cross-section. All transport measurements were carried out with a semiconductor parameter analyzer in DC mode, and capacitance measurements were made using a LCR meter. When the devices were on, the gate leakage current I_G was always significantly smaller than the drain current I_D, an example of which is shown by the $I-V$ characteristics in Fig. 1(c). The gate leakage shows a similar form to previous studies.[20]

Clear normally-on transistor characteristics at $T = 300$ K are shown in Fig. 2 for the case of $d_{LAO} = 16$ uc. Pinch-off is observed for -0.8 V $\leq V_{GS} \leq +1.2$ V, with a clear saturation at higher V_{DS}. Differentiating these data to obtain the channel conductance $g_D = \frac{dI_D}{dV_{DS}}$, and extrapolating to zero g_D, we find the pinch-off voltage V_P as a function of V_{GS}, as shown in the inset of Fig. 2(b). The corresponding current at $V_{DS} = V_P$, $I_{D,sat}$, defines the co-ordinates $(V_P, I_{D,sat})$ for a fixed V_{GS}, as shown by the circles in Fig. 2(a). The threshold voltage could be obtained as $V_{Th} = -1.15 \pm 0.05$ V by fitting the $V_P - V_{GS}$ data to the relationship $V_P = V_{GS} + V_{Th}$.[21] Taking a transfer curve at a source-drain voltage of $V_{DS} = 2$ V, as shown in Fig. 2(b), essentially ideal quadratic form of $I_D - V_{GS}$ is found, as expected from the gradual-channel model in the saturation regime.[21] These data allow a clear extrapolation of the threshold voltage as shown, giving $V_{Th} = -1.1 \pm 0.1$ V. The good agreement between these two V_{Th} values, obtained by two different analysis methods, suggests that the mobile carriers in the channel are ideally tuned by V_{GS}, with on-off current ratio's of greater than 1000 being achievable. Small hysteresis could be observed between increasing and decreasing V_{DS} in the transfer characteristics, as shown for the case of $V_{GS} = +1.2$ V in Fig. 2(a), where the difference in I_D between the increasing and decreasing sweep of V_{DS} is of the scale of 10 nA.

We systematically varied d_{LAO}, and were able to achieve transistor operation over the thickness range 4 uc $\leq d_{LAO} \leq$ 22 uc. The scaling of $V_{Th}(d_{LAO})$ is shown in Fig. 3. V_{Th} does not scale monotonically with d_{LAO}, as would be the case for constant sheet carrier density,

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via the relation $V_{\text{Th}} = -e d_{\text{LAO}} n(V_{\text{GS}} = 0)/\varepsilon_0 \varepsilon_r$, here e is the electronic charge, ε_0 and ε_r are the vacuum and LAO relative permittivities respectively, and the sign convention is taken such that $n > 0$ and $V_{\text{Th}} < 0$. It is notable that a systematic variation of the transport properties has been seen in this thickness regime elsewhere.[20, 22, 23] In order to more carefully examine this issue, we characterized several samples at lower temperatures where the Hall effect could be more reliably measured to directly measure the sheet carrier density change, and relate it to the capacitive character of the gate dielectric, since $\Delta n/\Delta V_{\text{GS}} = C_{\text{eff}}$. Here the effective capacitance C_{eff} is modeled as a 'dead' layer with thickness d_{dead} and dielectric constant $\varepsilon_{\text{dead}}$ in series with a bulk-like LAO layer with dielectric constant $\varepsilon_{\text{bulk}}$. From a simple series capacitor model $d_{\text{LAO}}/\varepsilon_{\text{eff}} = (d_{\text{LAO}} - d_{\text{dead}})/\varepsilon_{\text{bulk}} + d_{\text{dead}}/\varepsilon_{\text{dead}}$. We note that the dead layer thickness also includes possible suppression of the dielectric properties at the Au/LAO interface.[24] Assuming otherwise ideal capacitor behavior, $\Delta n/\Delta V_{\text{GS}}$ for various d_{LAO} can be used to extract $\varepsilon_{\text{eff}}(d_{\text{LAO}})$, and estimate $\varepsilon_{\text{dead}}$, $\varepsilon_{\text{bulk}}$ and d_{dead}. The measured $\varepsilon_{\text{eff}}(d_{\text{LAO}})$ is shown in Fig. 3, together with a theoretical fit which gives $\varepsilon_{\text{dead}} \sim 4.3$, $\varepsilon_{\text{bulk}} \sim 21.6$ and $d_{\text{dead}} \sim 4.3$ uc. These estimates, in particular the value of $\varepsilon_{\text{bulk}}$ emphasize that the atomic scale nature of interface between the gate and the electron gas.

With the establishment of robust transistor operation at room temperature, it is important to consider if the top-gating geometry can be successfully applied at lower temperatures. Figure 4(a) shows clearly that n can be ideally tuned with the top gate in a $d_{\text{LAO}} = 16$ uc, $W = 5\ \mu\text{m}$ sample at $T = 2$ K, where we compare the n variation from the Hall effect to that predicted from the measured device capacitance (940 pF with top-gated channel area 0.0504 mm^2) at $V_{\text{GS}} = 0$ V (solid line), assuming that $n = 0$ cm^{-2} at $V_{\text{GS}} = V_{\text{Th}} = -2$ V. Here the capacitance was measured in a frequency range of 20-100 Hz with an AC modulation voltage of 50 mV. In this range the loss tangent was < 0.04 and the gate leak conduction is negligibly small. In addition to the good agreement between the capacitance data and the Hall effect, as n was depleted the Hall mobility μ showed a clear increase: the opposite tendency compared to back-gate field effect modulation,[11] as shown in Fig. 4(b).

The dramatic asymmetry in the mobility modulation between back- and top-gating can be understood by considering the action of the gate voltages on the confined electron gas. For negative back-gating the applied electric field tends to confine the electrons closer to the interface where they are scattered more strongly.[11] In the top gate geometry by contrast, the center of weight of the envelope wavefunction of the electron gas is pushed away from

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the interface as the electron gas is depleted and the self-consistent confining electric field is reduced.[18] This results in a local three-dimensional electron density that becomes smaller, and located in the less disordered bulk STO as $V_{\mathrm{GS}} \to V_{\mathrm{Th}}$, producing the observed enhancement of the Hall mobility as n is decreased. The significance here is that the systematic n suppression achieved by the top gate voltage can provide access to a regime with both smaller carrier density and less disorder (higher mobility), where other methods have experienced difficulties in approaching this regime. By combining the top-gate with an additional back-gate at low temperatures, we can also envisage independently tuning the sheet carrier density and Hall mobility to control the electronic character of this fascinating system.

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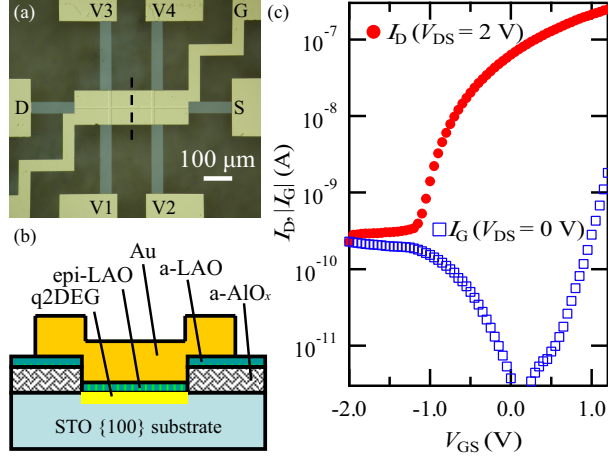[24] M. Stengel and N. A. Spaldin, Nature **443**, 679 (2006).

FIG. 1: (color online) (a) Optical microscope image of a device with central channel dimensions 5 μm $\times$ 150 μm between the centers of the voltage contacts (V1, V2) and (V3, V4). Source, gate and drain are labeled S, G and D respectively. (b) Schematic cross-section of the device (not to scale) taken along the dashed line in (a). "a" and "epi" refer to amorphous and epitaxial layers in the cross-section, and q2DEG is the electron gas. The amorphous AlO_x thickness is ~ 50 nm. (c) $I_D - V_{GS}$ and $I_G - V_{GS}$ characteristics for a typical device. Here $d_{LAO} = 16$ uc, and $T = 300$ K.
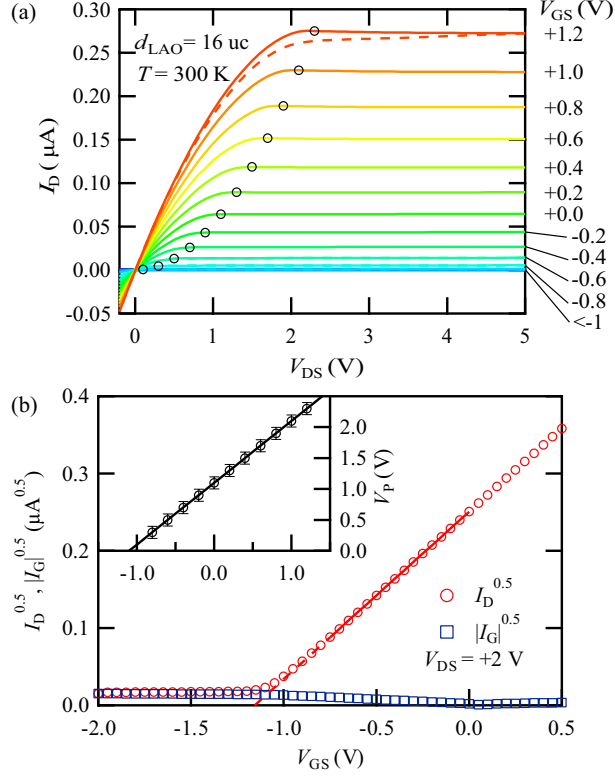
FIG. 2: (color online) (a) Transistor operation of a $d_{\mathrm{LAO}} = 16$ uc device at room temperature, for various V_{GS} taken in 0.2 V steps. All data are taken with increasing V_{DS} except for the dashed line at $V_{\mathrm{GS}} = 1.2$ V, which is for decreasing V_{DS}. Circles mark the co-ordinates $(V_{\mathrm{P}}, I_{\mathrm{D,sat}})$ on the respective traces. $W = 100$ μm. (b) $\sqrt{I_{\mathrm{D}}}$-V_{GS} plot, showing linear behavior in the saturation region. The abscissa intercept of the linear fit gives $V_{\mathrm{Th}} = -1.15 \pm 0.05$ V for this device, where the error bar is associated with the uncertainty given by the finite gate leakage. Inset: $V_{\mathrm{P}} - V_{\mathrm{GS}}$ (open circles) obtained from the $g_{\mathrm{D}} - V_{\mathrm{GS}}$ intercepts. Line is a best fit to the form $V_{\mathrm{P}} = V_{\mathrm{GS}} + V_{\mathrm{Th}}$, where V_{Th} is the fit parameter.
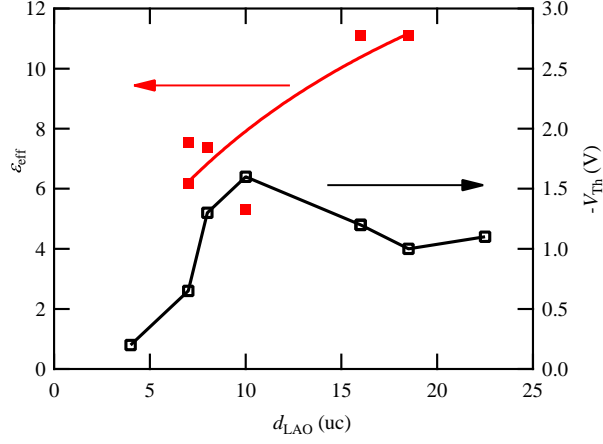
FIG. 3: (color online) Scaling of V_{Th} (right axis) at $T = 300$ K and ε_{eff} at $T \sim 100$ K (left axis) with d_{LAO}. Lines between V_{Th} data are guides to the eye. For the ε_{eff} data the line is a best fit to a series dead layer model giving $\varepsilon_{\text{bulk}} = 21.6$, $\varepsilon_{\text{dead}} = 4.3$ and $d_{\text{dead}} = 4.3$ uc. $W = 5$ μm for all devices.
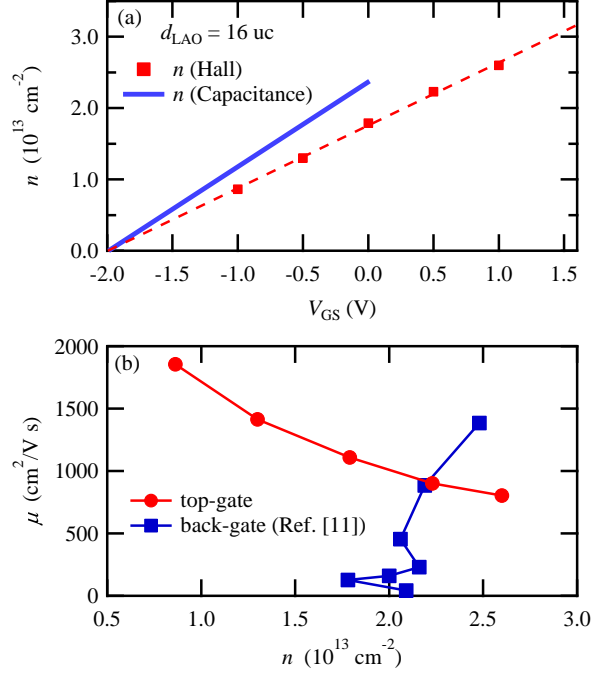
FIG. 4: (color online) (a) Control of the sheet carrier density n with V_{GS} at $T = 2$ K. Solid line shows the ideal predicted rate of carrier density tuning based on the capacitance measurements at $T \sim 150$ K, taking $n = 0$ cm^{-2} at $V_{GS} = V_{Th} = -2$ V. (b) Hall mobility enhancement with top-gate depletion of n at $T = 2$ K. Back-gate mobility suppression data from Ref. [11]. LAO thickness, $d_{LAO} = 16$ uc, $W = 5$ μm.