Low Cost Lithography Tool for High Brightness LED Manufacturing

FINAL REPORT

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Low Cost Lithography Tool for High Brightness LED Manufacturing

The Department of Energy identified low-cost manufacturing tools as a key element to the successful introduction of high brightness LEDs to the commercial marketplace. Lithography is a key component in LED manufacturing. Lithography is performed approximately 6 times per LED. Less expensive tools with higher yields and higher throughputs are essential to high volume LED manufacturing.

Project Overview

The objective of this activity was to address the need for improved manufacturing tools for LEDs. Improvements include lower cost (both capital equipment cost reductions and cost-of-ownership reductions), better automation and better yields. To meet the DOE objective of $1-2/kilolumen, it will be necessary to develop these highly automated manufacturing tools. Lithography is used extensively in the fabrication of high-brightness LEDs, but the tools used to date are not scalable to high-volume manufacturing.

This activity addressed the LED lithography process. During R&D and low volume manufacturing, most LED companies use contact-printers. However, several industries have shown that these printers are incompatible with high volume manufacturing and the LED industry needs to evolve to projection steppers. The need for projection lithography tools for LED manufacturing is identified in the Solid State Lighting Manufacturing Roadmap Draft, June 2009[1]. The Roadmap states that Projection tools are needed by 2011, figure 1, below. This work will modify a stepper, originally designed for semiconductor manufacturing, for use in LED manufacturing. ***This work addresses improvements to yield, material handling, automation and throughput for LED manufacturing while reducing the capital equipment cost.***

Category	Item	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
Equipment	Lithography	Contact											
				Projection									
	Thinning & Dicing	?											
	Wafer Inspection	?											
	Die Inspection	?											
	Die Attach	?											
	Device Inspection (Vf/Efficacy/Color)	High speed test (TBD)											
				Link device-level and wafer-level data									

Figure 1: Reprinted from the DOE Solid State Lighting Manufacturing Roadmap Draft[4]. The need for Projection Lithography for high volume manufacturing is identified as being needed by 2011.

[1] http://apps1.eere.energy.gov/buildings/publications/pdfs/ssl/ssl_manufacturing-roadmap.pdf

This project will directly address four areas of the stepper performance:

- Cost of Ownership (COO)
- Yield Improvements
- Automation Improvements
- CapEx reduction

These objectives align with the 2009 SSL Manufacturing Roadmap, subtask 2.3.3.

This final report will focus on the work performed during the period January 1, 2012 through June 30, 2012. Details on the period from March 2010 through December 2011 can be found in earlier annual reports.

Technical Approach and Work Plan

Cost of Ownership (COO) Improvements: Throughput

The Cost of Ownership is driven primarily by the initial capital equipment cost, the cost of operating the tool and the throughput of the tool. While we are planning on some improvements to tool cost operation, these costs are small and their impact to COO will also be small. The capital equipment cost will be addressed in the "CapEx Reductions" section. In this section, we will primarily focus on the throughput improvements.

Our updated throughput improvement goals are driven by new customer requirements and are based upon a specific tool configuration and have been defined with our customers. For 2-inch substrates, the original throughput of the tool was 86-wafers/hour and our goal was to increase this in two stages. The first stage would have a throughput goal of 95-wafers/hour and the second stage would have a final goal of 115-wafers/hour. For four-inch substrates, the initial throughput was 65-wafers/hour, with a first stage goal of 70-wafers/hour and a final goal of 80-wafers/hour. In summary, for 2-inch wafers, our goal is a 33% increase in throughput, and for 4-inch wafers, our goal is a 23% increase in throughput.

Throughput improvements come from two sources: a brighter light source (for faster resist exposures) and less overhead time between exposures. The time between exposures is dominated by wafer transport time, alignment time, wafer handling time, wafer set up, etc.

Non Exposure Related Throughput Improvements

An analysis of the tool's wafer-exposure-sequence shows that a significant amount of time is spent on correcting the wafer rotation. Wafer rotation is controlled by our "theta-stage". On semiconductor wafers, the alignment marks are very carefully located and the amount of wafer rotation required for alignment is minimal (often zero). However, on sapphire substrates, the dies are not well aligned to wafer fiducials, resulting in the need for large wafer rotations. We needed make the wafer rotation both longer-travel, as well as higher speed. To achieve this, a great deal of work was done to develop a higher speed "theta stage", which include higher speed motor, new controller, new mechanics, new electronics and new software. We have been able to reduce the theta rotation and pre-alignment time by approximately 0.7 seconds.

With this improvement and several other software improvements (to reduce processing time), we have been able to achieve a throughput for our off-axis EGA alignment routine to be 104-wafers/hour for 2-inch wafers and 79-wafers/hour for 4-inch wafers, which exceeded our "stage-one" goals and is close to our "stage 2" goals.

The final throughput increases to meet our stage 2 goals are expected to come from the new, brighter LED illuminator that we investigated in this activity. The new illuminator is LED based, and using published data from our LED supplier; we expect to increase the brightness of our illuminator, which will directly lead to reduced exposure times and an increase in throughput. Our goal was to increase the brightness of the source by > 10% which would be sufficient to meet our Stage 2 goals.

Exposure Related Throughput Improvements (Improved Source)

The current lithography tool uses a mercury arc lamp. We have analyzed the optical properties required from our source for improved throughput. A larger light source is insufficient; it is possible to obtain a larger lamp that emits more power, but the power emitted per unit area (which is known as the “brightness”) is not increased. To obtain a higher throughput tool, we need a brighter source and one does not exist for our lithography tool.

Recent improvements in LED technology have led us to believe that an LED light source can be more bright (and certainly more efficient) than a mercury arc lamp. Changing our source to an LED based source will require a complete re-design of our “light engine”—the light source and the optics that couple the source to the optical system of the lithography tool. We have completed a concept design for this LED based illuminator, and a drawing from Zemax (an optical design software code) is shown in figure 2.

The key risks in an LED illuminator are:

1) Thermal management of the LED source
2) Seamless replacement of the mercury source with the LED source.

Thermal management of the LED source is critical for a number of reasons. First, when LEDs get too hot, their lifetimes are severely impacted. Second, as the LEDs temperature rise, their emissions shifts to longer wavelengths and their bandwidths broaden. This wavelength shift affects the resist response.

It is imperative that the LED wavelength be constant over the lifetime of their use. If the LED wavelength shifts over time, then, the tool performance will also shift. Semiconductor and LED manufacturers will not tolerate a time-dependent variation to the tool performance.

It is equally imperative that the LED emission wavelength match the mercury arc lamp emission wavelength—at least match its center wavelength. UV photoresists have been optimized over time for use at 365 nm—the Mercury (Hg) i-line emission. All resists have different chemistries, and as a result, perform differently. As the source wavelength shifts from 365 nm, some resists are more sensitive (i.e., absorb more and consequently, will have shorter exposure times and give the tool a higher throughput) and other resists are less sensitive (which will lead to less absorption and lower throughput). Operating at different wavelengths would necessitate the need for device manufacturers to re-calibrate and re-qualify tools for different resist and source combinations. In manufacturing environments where a combination of tools with different sources exists, it would become unmanageable for the factory to maintain different “recipes” for exposure, depending upon which tools and resists are being used.

LEDs typically have a wider bandwidth than an Hg arc lamp. A high pressure Hg arc lamp will have a FWHM of approximately 6 nm centered at 365 nm, whereas the FWHM of an LED source is usually 9-10 nm. We have shown with numerical modeling that, as long as the center wavelengths match-up to within 1-2 nm, the larger LED bandwidth is not an issue.

Finally, for the LED to replace the Hg lamp in the illuminator, it is necessary that the final resist profiles be identical. Semiconductor and LED manufacturers have spent considerable resources to optimize their exposures to get precisely the correct resist profiles for their manufacturing process. If the resist profiles from the different sources do not match, then, the LED illuminator will be rejected.

In this final report, we describe our work on characterizing the use of the LED illuminator. We discuss the lifetime of the LED source as well as the resist exposures we have obtained. During the period of January 1, 2012, to June 30, 2012, this has been our primary focus in this program.

In our 2011 annual report, we described the LED illuminator in some detail. That section is repeated below. At the end of this section, we discuss our lifetime and resist exposure results.

From an optical design point of view, a key invention was the coupling of the LED array to a light pipe. This allowed us to reduce optical costs and improve LED light collection efficiency. The Zemax optical design illustrated in figure 2 uses a fold mirror, but this is optional.

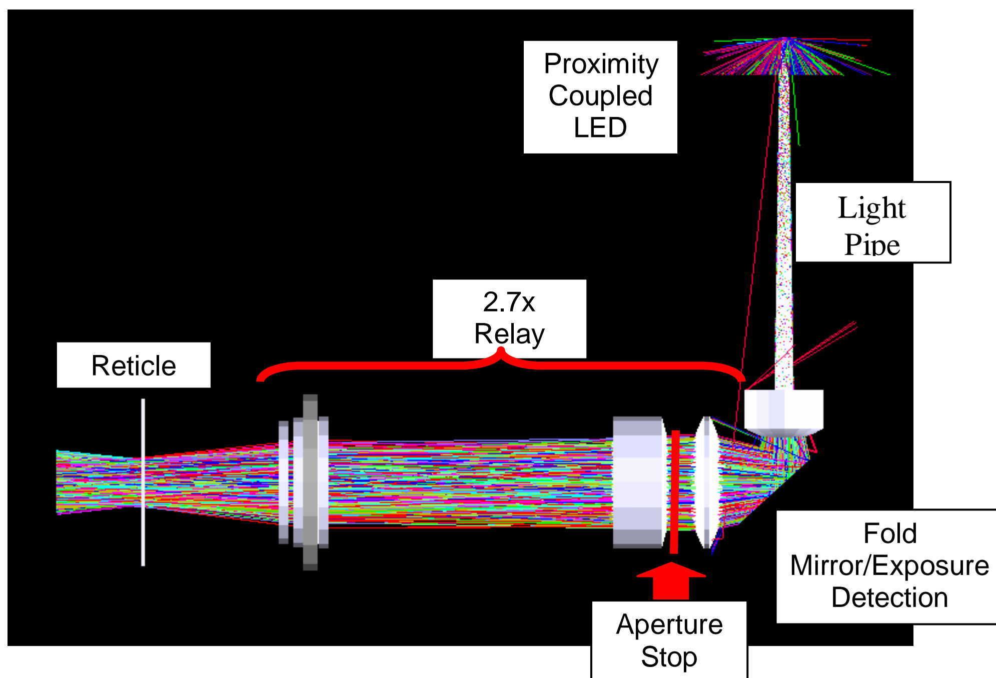


Figure 2: Optical design for the LED illuminator.

Last year, we reported on the light uniformity from a 2x5 input array of 1x1 mm^2 LEDs; specifically, we modeled a 2x5 array of LEDs, placed at the input to the light pipe, and found it to be acceptable.

In last year's report, we indicated that we had significant success with LEDs operating at 395 nm (our goal is to operate at 365 nm). Based upon that work we were confident that we would be able to meet our goal of higher irradiance (watts/cm2) at the wafer plane but at the time of the report, we did not have credible 365-nm die.

Working with Nichia, we were able to obtain high-brightness "365-nm" chips. In particular, we are currently evaluating an array of twenty-one, 1x1 mm die, figure 3. The specifications for these die were 365-nm +/- 5 nm. While we needed a significantly tighter distribution of center

emission of the die (i.e., 365-nm +/- 1 nm during operation), we felt that we could use these die for initial characterizations.

The individual die in the arrays we received and tested had a central emission wavelength of 365.5 nm when operated at low power and at room temperature. The central wavelength shifted to longer wavelengths (367.5 nm) during actual operation. Based upon our need to match the wavelength of the Hg lamp, and the wavelength shift during operation, we will need die that have a central emission wavelength of approximately 364 nm (+/- 1 nm) while at room temperature and at low power.

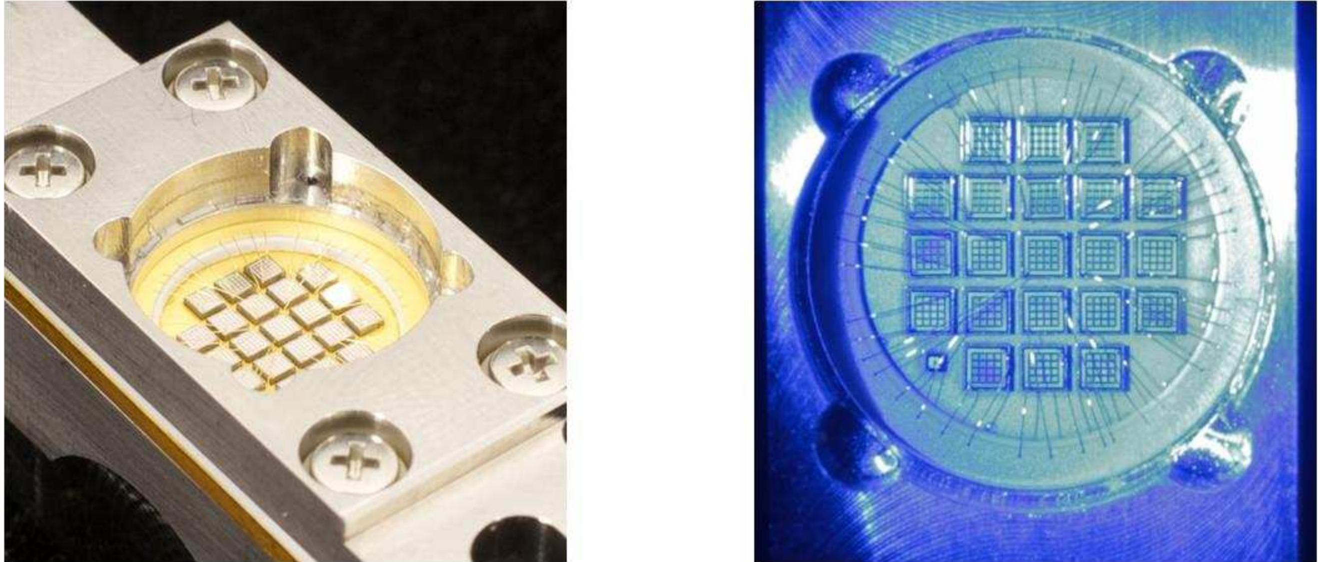
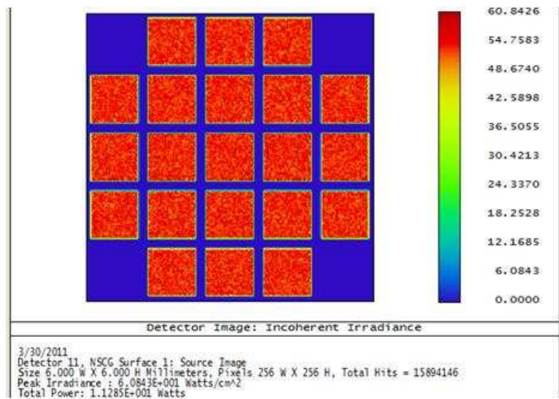
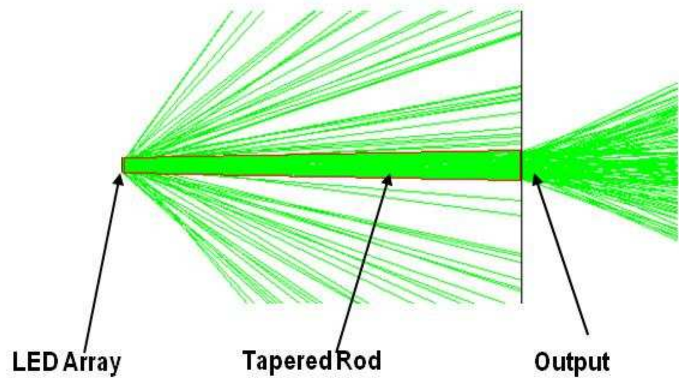


Figure 3: Left photo is an oblique view of the 21-die array. Right photo is a top view of the array. Each die is spec'ed to emit 0.6 watts of 365-nm radiation.

The water-cooled die array is well constructed and is driven with an input drive current of 1 Amp per die (21 Amps total). Each die will emit approximately 0.6 watts (a total emission of 12-13 watts per array). Our goal is to obtain 18 watts from the integrated module. Based upon our discussions in early 2011, we expected this (or a similar) array to be able to emit 18+ watts by Q4/2011. This was sufficient for us to precede with characterization of the emission characteristics of the LED array.

We optically modeled the output of the 21-die array, coupled to a tapered homogenizer rod. Figure 4 illustrates the optical modeling, with the 21 die array shown, proximity coupled to the input of a tapered homogenizer rod. Figure 5 illustrates the calculated uniformity from the output of the homogenizer rod, with intensity profiles illustrated in Figure 6. Figure 6 is a “line-out” of the calculated intensity uniformity at the exit of the homogenizer rod, through the center of the rod, in both the “x” and “y” directions. The uniformity goal of 2% is easily met.





Source Array

Optical Model

Figure 4. The 21-die array of 365-nm LEDs is illustrated on the left side. The array is proximity coupled to a tapered homogenizer rod (right figure). The output of the homogenizer rod is uniform.

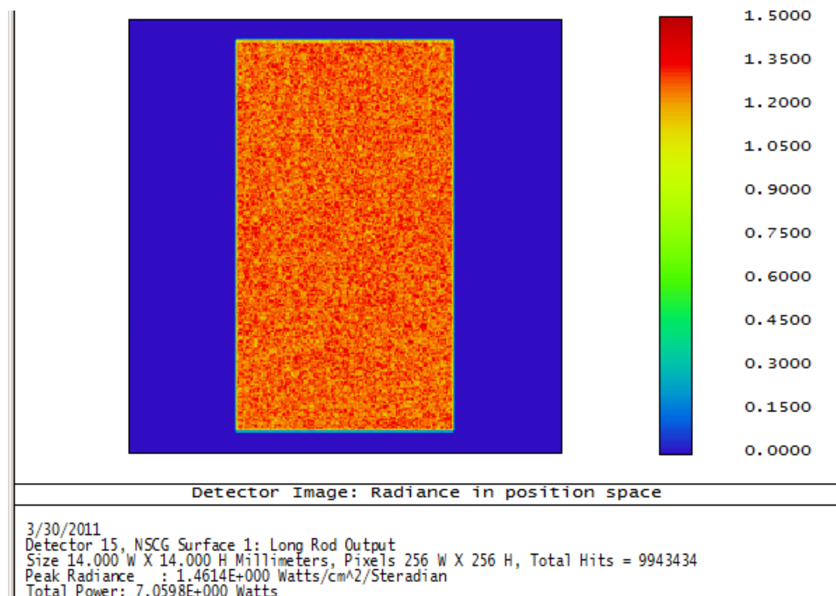


Figure 5. The output of the homogenizer rod is illustrated in this figure. 1 million rays were emitted from the LED array to calculate the uniformity.

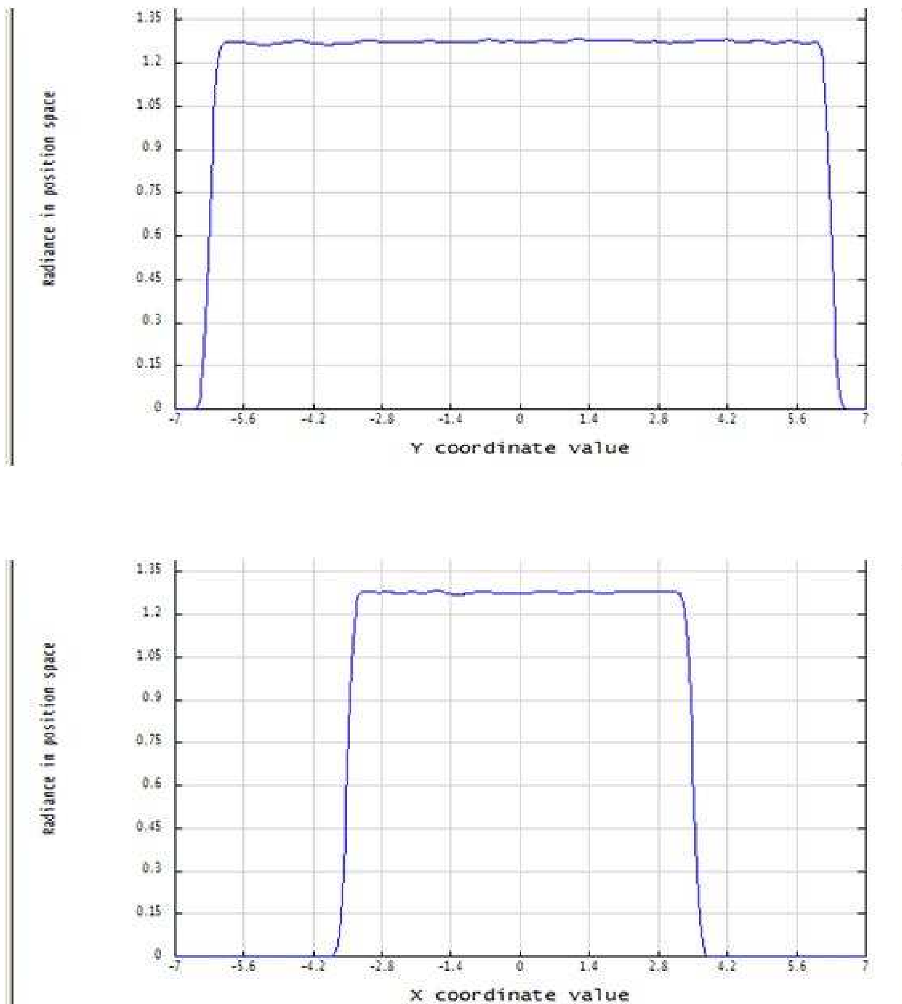


Figure 6: Intensity line outs at the output of the homogenizer rod (figure 5) illustrating that the uniformity requirement can be met.

We initiated a LED module lifetime tests. We began by taking 12 modules (each with a water-cooled, 21-die array) and measuring their spectrum and power emission.

We then took the 12 modules and created three sets of four modules each, Figure 7. We took 4 modules and ran them at 21 Amps, as our baseline. We took 4 modules and removed their glass cover plate and ran them at 21 Amps. Finally, we took 4 modules, removed their glass cover plate and bathed them with flowing nitrogen, while running at 21 Amps.

All twelve modules were proximity coupled to a tapered homogenizer rod, and the output of the rod was monitored using a photodetector with a small aperture. The data from the photodetector was logged and stored. We cycled the current to the modules in pulsed mode, similar to the operating conditions in our tool (1/4 second "on", with ~1/2 second "off"). We then monitored the emission vs. time, and re-measure the spectrum periodically (initially, monthly).

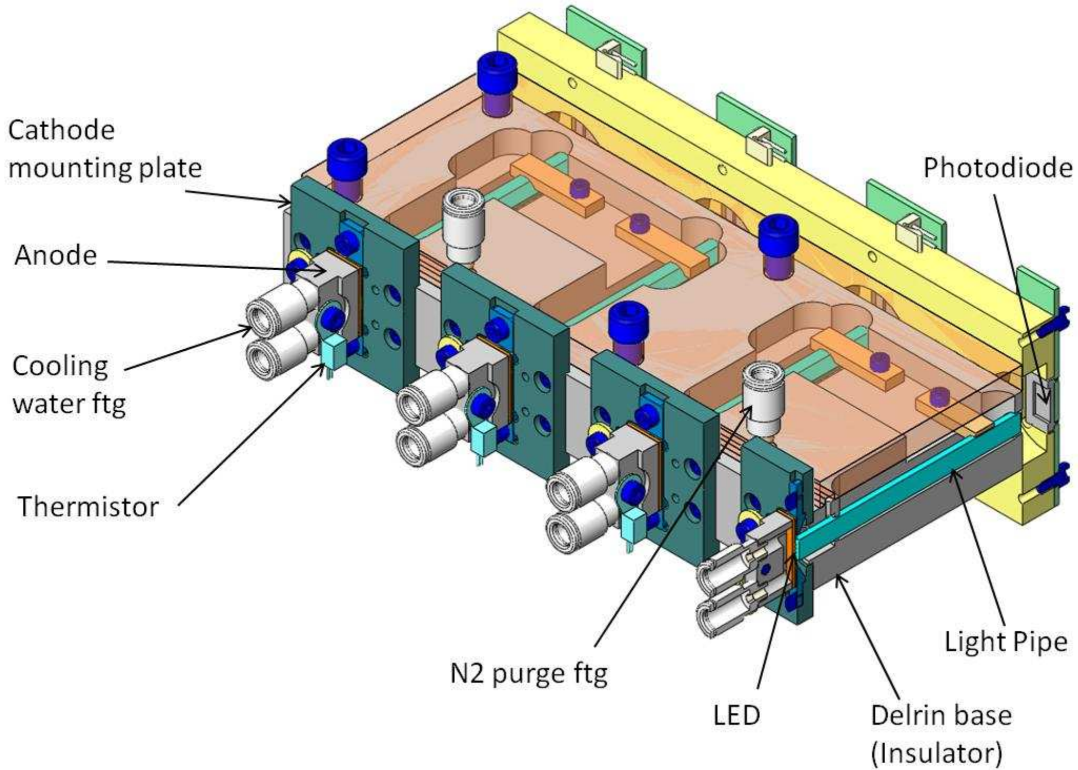


Figure 7 illustrating a 4-module array in our test station.

We noted a considerable decrease in the emission power for the four modules with flowing nitrogen. When inspecting the tapered homogenizer rod, we noted that there is considerable color degradation at the input. This degradation is not evident on the homogenizer rods for the other 8 modules, nor did the output power of the other 8 modules decrease. We suspect that the degradation is due contamination in the flowing nitrogen gas. If the nitrogen contains hydrocarbons, the 365-nm radiation is sufficiently energetic to “break” the hydrocarbons which can then coat the glass rod. In time, the hydrocarbons build up in thickness and continuously absorb additional radiation. Fortunately, the hydrocarbons on the glass input are easily cleaned, but this test illustrates that it is not practical to flow nitrogen into the LED source area unless the nitrogen is free of hydrocarbons.

The other 8 modules had no appreciable power loss during the life time tests to date.

In parallel with the LED lifetime testing, we began to design the mechanical and electrical components of the LED illuminator.

The LED mechanical design (which we are currently using in a bread-board system and is currently installed on an engineering lithography tool) is illustrated in Figure 8.

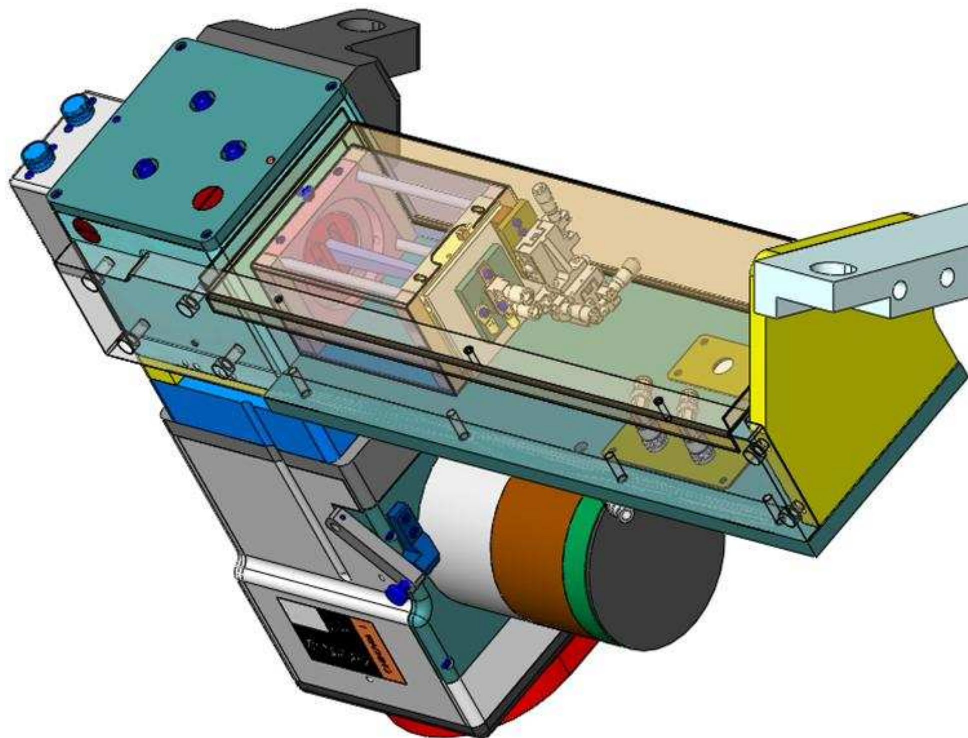


Figure 8. Mechanical design of the Breadboad illuminator.

In Figure 9, we show the LED Breadboard illuminator superimposed on the mechanical system for the current illuminator. The large cylindrical shape in the upper right is the current Mercury Arc Lamp housing, which will be removed when the LED illuminator is installed. As can be seen, the new LED illuminator is smaller than the existing Hg lamp illuminator.

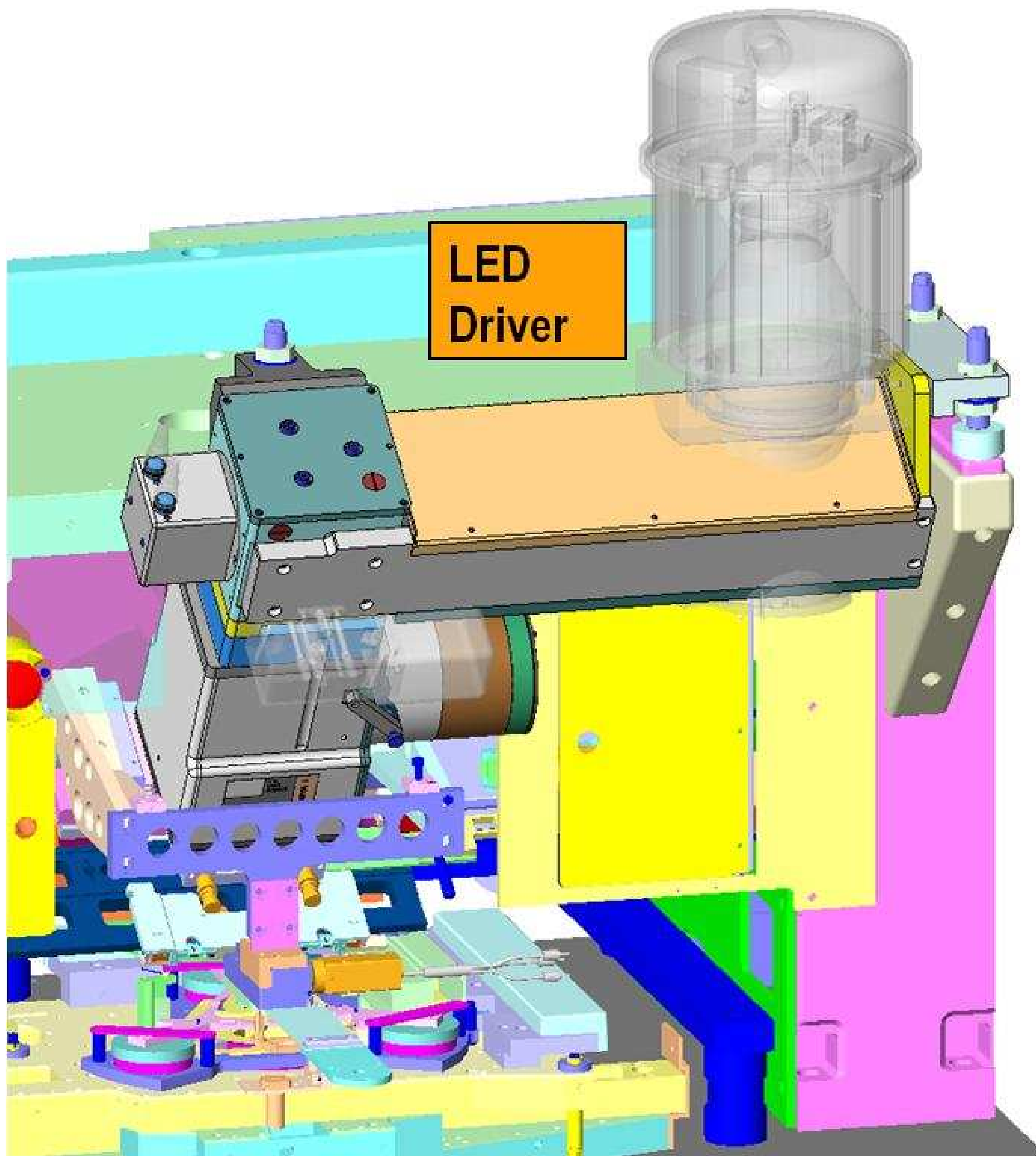


Figure 9 illustrates the location of the new LED illuminator on the tool, with the old Mercury Arc lamp in its current place (upper gray cylinder). The new LED illuminator is much more compact.

The Light Pipe assembly (that couples the LED module to the rest of the illumination system) is illustrated in Figure 10.

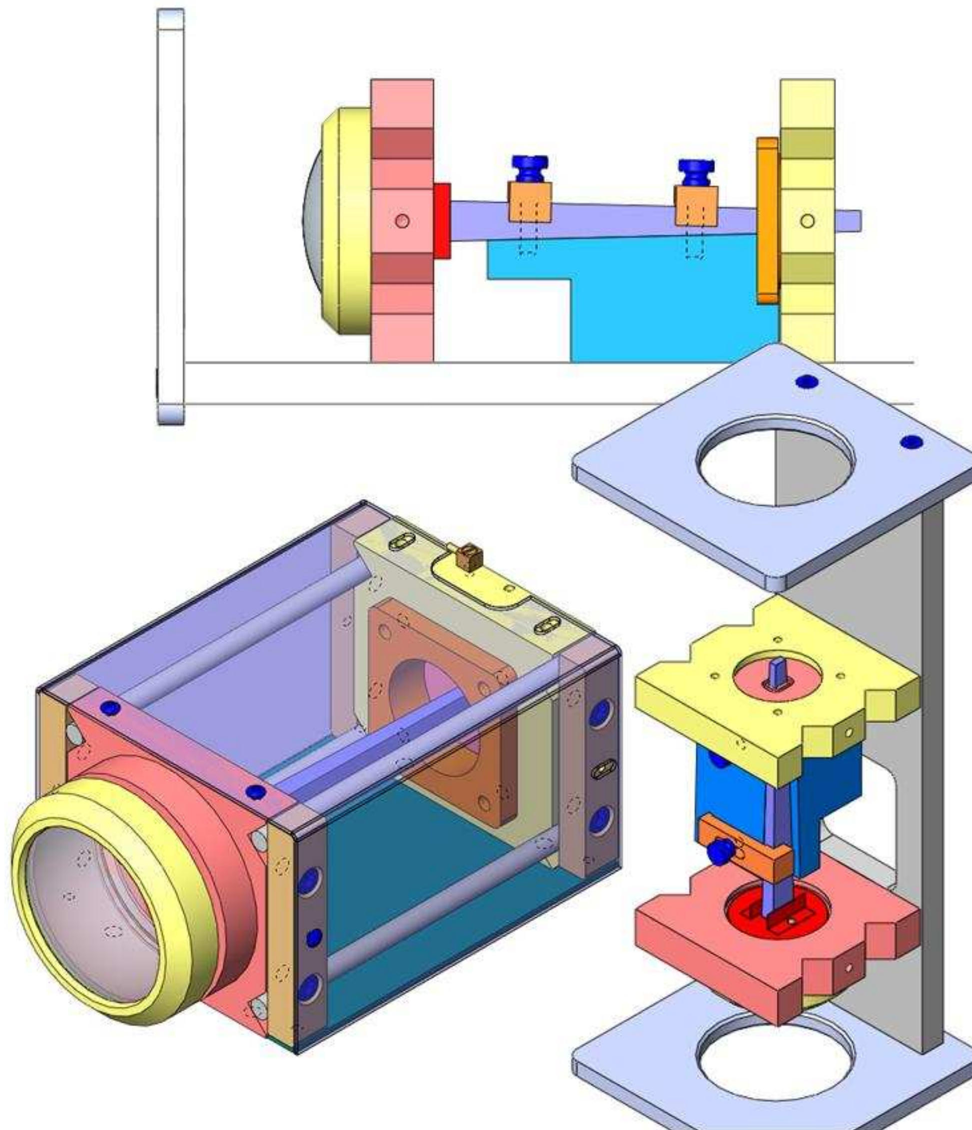


Figure 10: The components of the light pipe assembly.

LED Illuminator Evaluation Results: Resist Exposures

We fabricated the LED illuminator discussed in the previous section and installed it onto a lithography tool at Ultratech. Then, we characterized a number of different resists that are typical of those used by our customers in the LED manufacturing community and compared the results to exposures from a conventional Hg arc lamp. The resists we characterized include:

OiR906-10i (1 micron thick)
OiR906-10i (3 microns thick)
AZGXR601 (3 microns thick)
AZ12XT (11 microns thick)
AZnLOF2020 (3 microns thick)
AZ15nXT (7.5 microns thick)
AZnLOF 2035 (7 microns thick)

These resists cover both positive and negative acting resists, and different thicknesses that are used at different process steps. Typically, thinner resists are used for PSS layers, and thicker resists are used for contact or current distribution layers.

At low power and at room temperature, the LEDs used in these experiments were typically centered at 365.5 nm. However, at full power, the temperature rose to 367.5 nm. It was difficult to obtain LEDs so that they would emit at the correct wavelength while being operated at full power. However, we felt that we could still accurately identify the performance and/or limitations of the LED illuminator with proper procedures.

We began by measuring the appropriate “dose to clear” for each resist and thickness. The “dose to clear” is the minimum exposure required to remove the photoresist with a specific development time. Because the wavelength of the LED was slightly longer than the Hg lamp, we expected that the baseline “dose to clear” might be somewhat different. We then normalized all of our exposures to this new “dose to clear” at the LED wavelength.

Our first data from resist exposures included CD uniformity across the field. Figure 11 illustrates the CD uniformity for the OiR906-10i resist (3 microns thick). Two micron spaces were printed in the resist and CD uniformity was measured from the center of the field to the edges. The horizontal axis plots the focal offset of the tool. This illustrates the depth of focus for the process. Along the horizontal axis, -2.5 microns represents the “best focus” point in the exposure matrix. Notice that, from “best focus” (i.e., -2.5 microns) to the edge of the acceptable focus (+3.5 microns) the tool is exhibiting a depth of focus in excess of +/- 6 microns (12 microns total). This compared favorably to exposures with a Hg lamp and is an acceptable result.

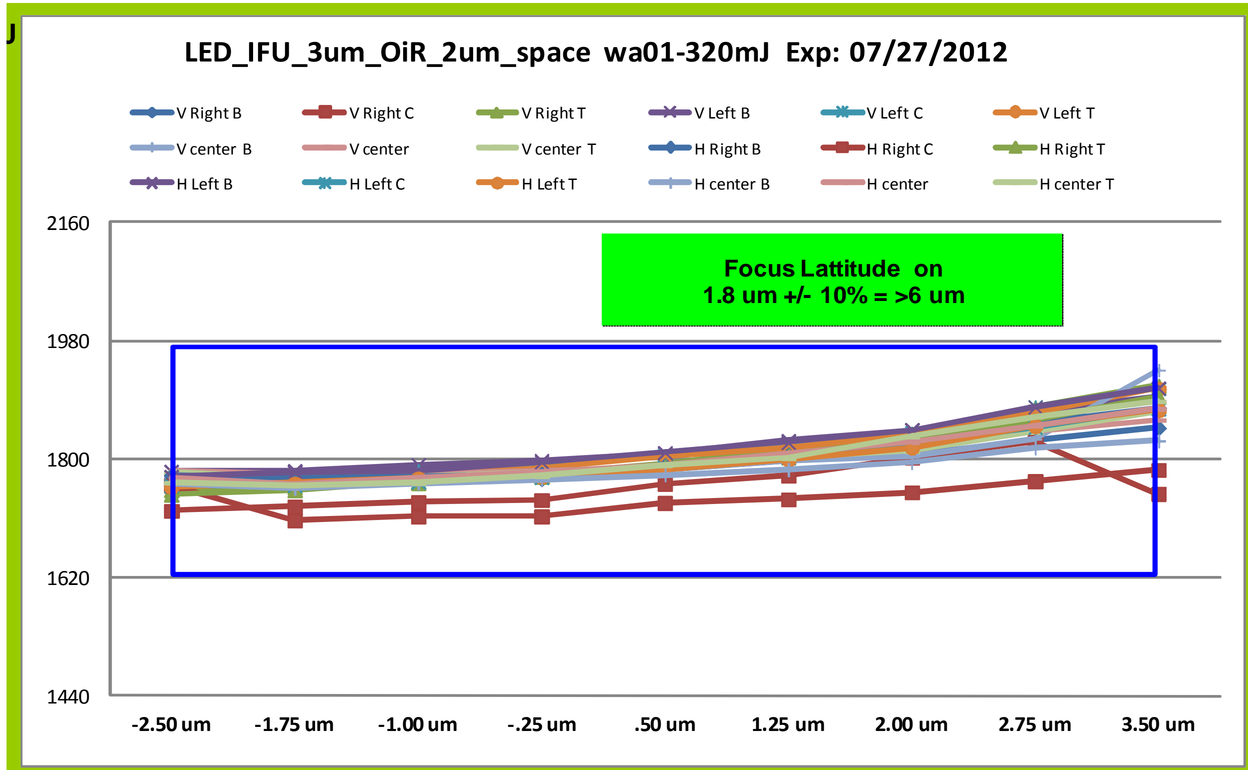


Figure 11. The focus latitude is measured for OiR resist. Best performance is obtained at the focal setting of -2.5 microns, which is the center of the focal depth. The entire focal depth is +/- 6 microns.

Figure 12 shows a summary of “resist exposure margin” tests. Exposure Margin is the effective process range in exposure dosage. Nominal dosages and exposure margins were determined by extensive SEM analysis of the line profiles. Horizontal and vertical lines were printed and analyzed in our SEM. Linewidths were plotted as a function of exposure dosage, and from that, the “nominal” dose and “exposure margin” was calculated. For manufacturing purposes, it is expected to have an exposure margin > +/- 35%. All of these resists meet this criterion when exposed with Hg lamps. From the figure below, we see that some resists do not meet this criterion when exposed with the LED illuminator. The reasons for this are unknown.

LED Illuminator Resist Test Summary

Date: 8/8/2012

		OiR906-10i 1 µm	OiR906-10i 3 µm	AZGXR601 3 µm	AZ12XT 11 µm	AZnLOF2020 3 µm	AZ15nXT 7.5 µm	AZnLOF2035 7µm	COMMENTS
Item 1	Actual Resist Thickness (from ETA-Optik)	1.05 um	2.61 um	2.85 um	11.30 um	2.85 um	7.49 um	6.80 um	6" wafer
	E_0, Dose to Clear (Dose to Retain)	75 mJ	185 mJ	80 mJ	140 mJ	125 mJ	130 mJ	160 mJ	
	CD Target (space)	1.0 um	2.0 um	2.0 um	4.0 um	2.0 um	3.0 um	3.0 um	
	Nominal Dose (per Vertical CD)	140 mJ	310 mJ	95 mJ	160 mJ	240 mJ	290 mJ	210 mJ	Refer to Images
	Exposure Margin, mJ (CD Target +/- 10%)	50 mJ	210 mJ	25 mJ	30 mJ	100 mJ	80 mJ	200 mJ	
	Exposure Margin, %	**36%**	**68%**	***26%***	***19%***	**42%**	**28%**	***95%***	
	CD Exposure Bias, um/mJ	.0040 um/mJ	.0019 um/mJ	.0160 um/mJ	.0267 um/mJ	.0040 um/mJ	.0075 um/mJ	.0030 um/mJ	

Figure 12. Resist exposure margins are measured for a variety of resists. Exposure margins are defined by the greatest change in exposure that will still produce lines with a CD within 10% of the target. These resists typically have margins > 35% with the Hg lamp illuminator.

SEM micrographs illustrated an unusual behavior for the LED exposed resists which we do not understand. Normally, resist profiles appear to be “box-like”. The edges are nearly square and symmetrical. Several of the resist profiles generated with the LED illuminator appear to be “tilted” in one direction, but not on all of them. Figure 13 (A,B) illustrates the resist profile that we have seen on some resists using the LED illuminator. These results were not seen on a Hg arc lamp illuminator. Until we understand the root cause of these resist profiles, it is unlikely that an LED illuminator can be used to replace the Hg lamp.

Figure 13A. Examples of acceptable profiles on AZ2020nLOF resist. Resist profiles are typically “box like”, with some slight undercutting at the base of the line. Notice that the lines are symmetrical.

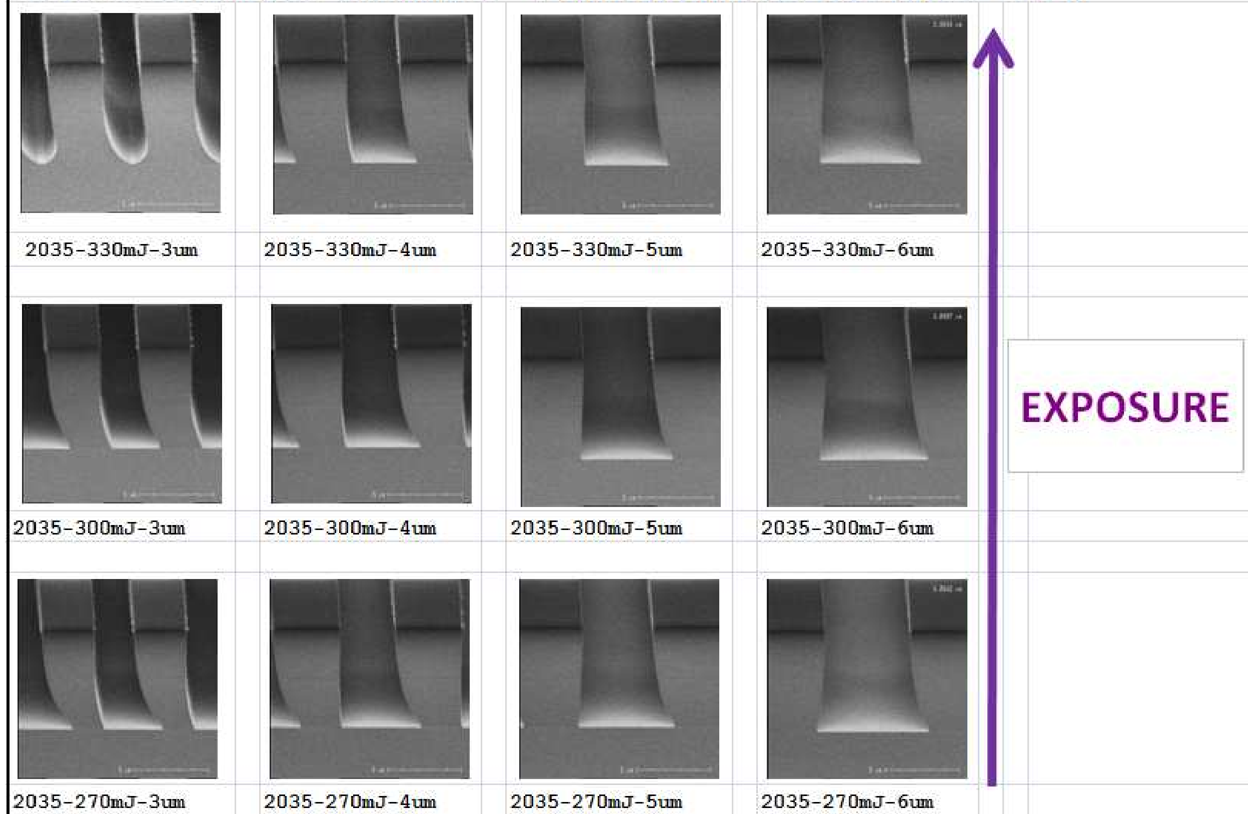


Figure 13B. Example of odd profiles on AZ2035nLOF resist with the LED illuminator. Notice that the lines are not symmetrical. The reasons for this are unknown at this time.

We also compared "top down" SEM micrographs of hole-type patterns taken with both the LED illuminator and the Hg illuminator. These hole-type patterns are used to create PSS structures in LEDs. The results are shown in figure 14. The LED exposures are on the left side, whereas the Hg exposures are on the right side. What is evident is that the LED holes are asymmetric when compared to the Hg exposures. Notice, in particular, the top row exposures.

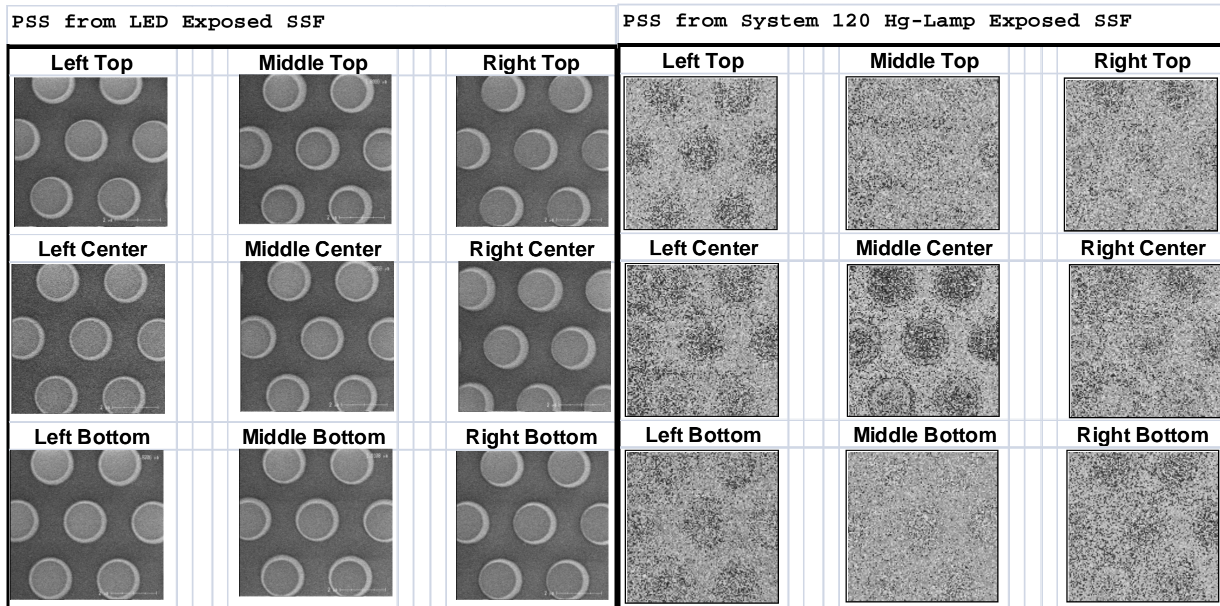


Figure 14. The "top-down" SEM micrographs on the left are from an LED exposure, whereas, the micrographs on the right are from a Hg arc lamp exposure. The pattern produced cylinders in thick resist. Notice that the Hg lamp exposures are symmetrical. In the top row of the LED exposures, the right side shows an asymmetry.

Our conclusion from our resist evaluation is that the replacement of the Hg arc lamp with the LED illuminator is not straightforward. There is something unusual occurring which is degrading the profile of the resists. This needs to be fully characterized and understood before an LED illuminator can be introduced into semiconductor manufacturing.

LED Illuminator Evaluation Results: Life Time tests

It was determined early that the LED performance as a function of time needed to be characterized under what we considered to be "normal operating conditions". The 21 die array that we planned to use for the Illuminator would be driven at 21 amps. The array would also be water cooled. Power to the LED array was cycled similarly to actual production conditions.

We used a water chiller to maintain the water temperature to the LED array at a constant temperature. We operated the LEDs at 21 Amps. We monitored the light emission, the wavelength and the spectral bandwidth as a function of time. We also ran tests where we reduced the water cooling temperature and reduced the drive current. With these tests, we were able to obtain a good understanding of the LED performance over its lifetime.

Power:
On our testbed, we were able to monitor the power emitted from individual die arrays. Operating at full power (21 Amps) and with a cooling water temperature of 23oC, the LED output degraded at a rate of 0.16% per day. The lifetime of the array (defined as the number of days to drop to 80% of the output) would then be 125 days.

By changing the water cooling temperature to 10oC, the LED output degraded at a rate of 0.11% per day, which increased the lifetime to 180 days (figure 15).

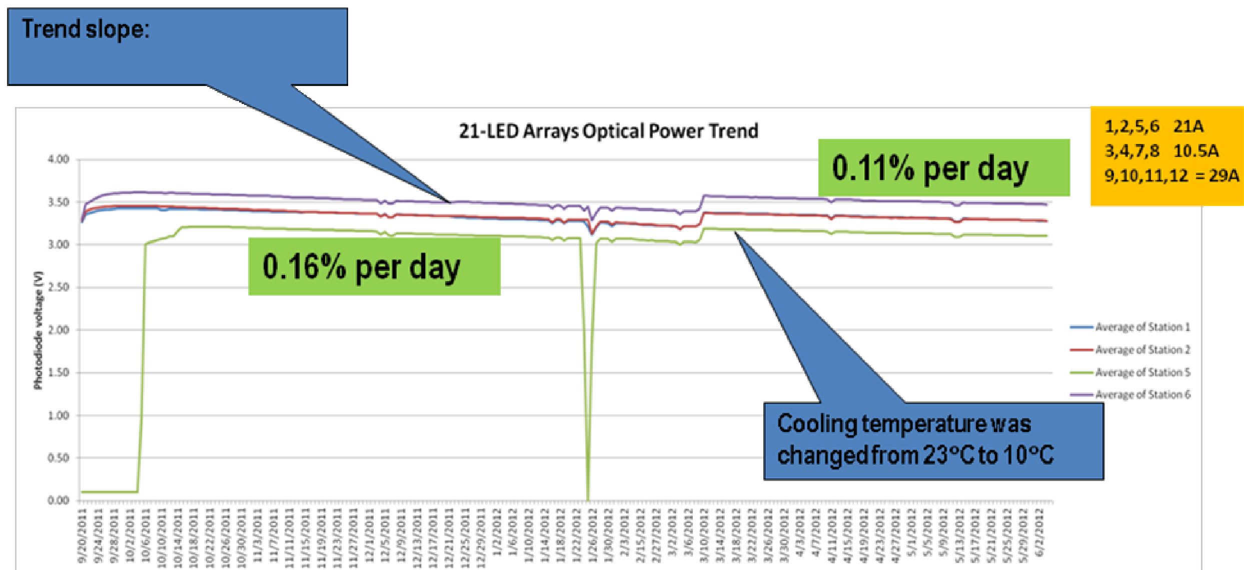


Figure 15. The output of the standard LED array is monitored under standard operating conditions (i.e., 23oC water cooling temperature and full current; power cycled ½ second on, ¼ second off). The decay of the array is 0.16%/day, which would lead to a life expectancy of only 125 days. By decreasing the water cooling temperature to 10oC, the lifetime increased to 180 days.

Another lifetime test was performed by reducing the drive current in half, and reducing the water temperature to 10oC. The lifetime is increased to 333 days, figure 16.

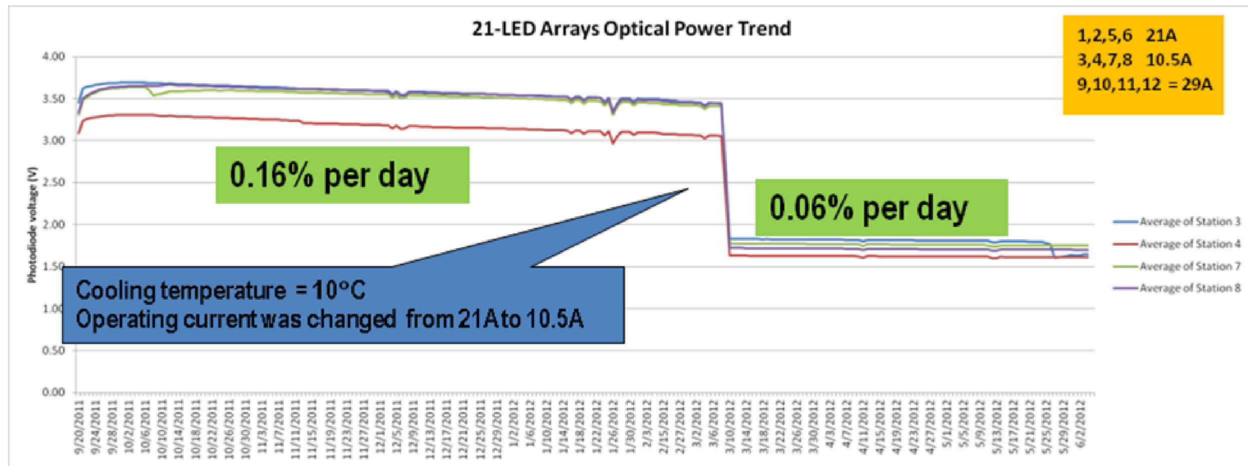


Figure 16. The output of the standard LED array is monitored under standard operating conditions (i.e., 23oC water cooling temperature and full current; power cycled ½ second on, ¼ second off). By decreasing the water cooling temperature to 10oC, and reducing the operating current in half, the lifetime increased to 333 days.

We also noted that reducing the water cooling temperature reduced the wavelength shift of the LEDs. This is illustrated in figure 17. Initially, the LEDs wavelength increased from the spec (at room temperature) of 365.5 nm, to 367.25 nm (at full power operation). But, reducing the water cooling temperature to 10oC, dropped the emission wavelength to approximately 366.75 nm.

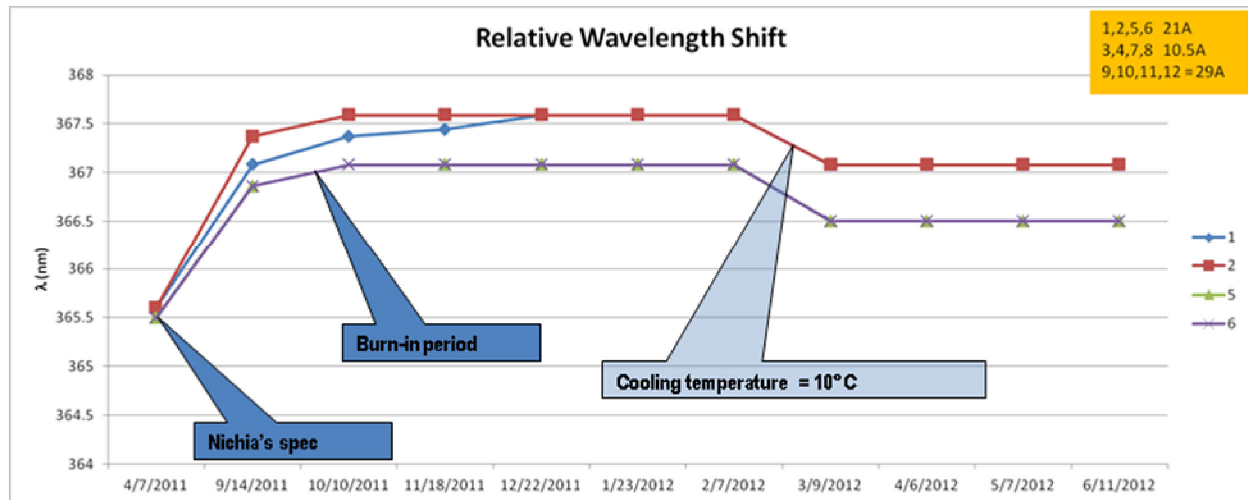


Figure 17. The center wavelength of the LED array is compared to its emission at room temperature and low power (i.e., Nichia's spec), vs. nominal operating conditions and the conditions with lower cooling water temperature.

Reducing the drive current while maintaining the water cooling temperature at 10oC had an even more dramatic effect on the wavelength, figure 18. At half input power and with 10oC water cooling, the emission wavelength dropped down to the initial room temperature specs.

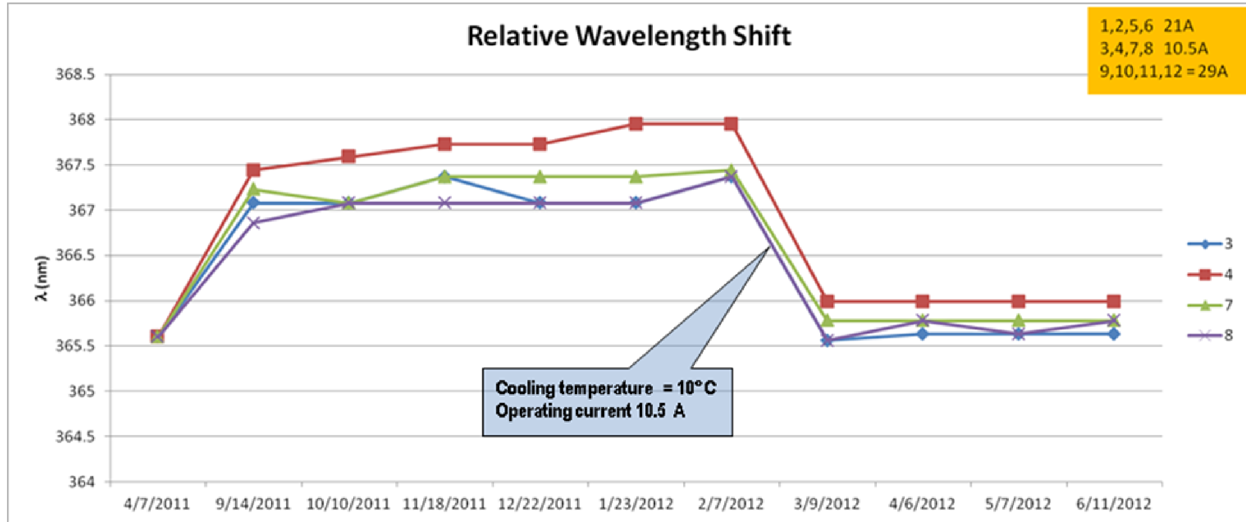


Figure 18. Reducing the drive current and the water cooling temperature reduced the wavelength shift so that the emission was comparable to that when the device is operated at room temperature.

The emission spectrum was sensitive to drive conditions. By reducing the current to 10.5 Amps, and reducing the cooling water temperature to 10oC, the FWHM dropped from 10 nm to 8 nm, figure 19. Fortunately, we determined from numerical calculations that the increase in the emission spectrum was probably insignificant.

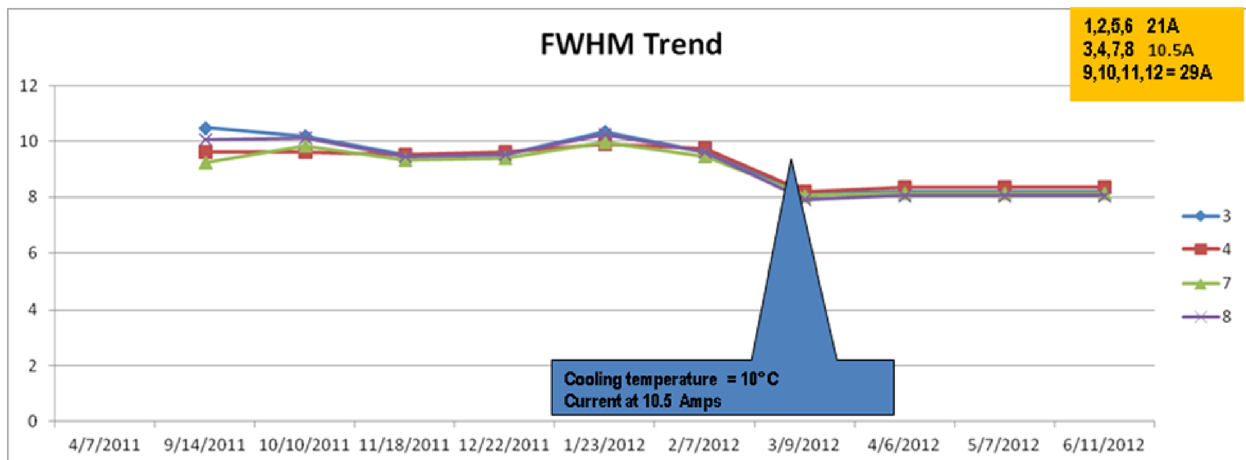


Figure 19. The emission spectrum (FWHM) is plotted for two different water temperatures: 23oC and 10oC.

Our conclusions from these life-time tests were that, we could build an LED illuminator to meet our spectral needs provided that the initial (room temperature) wavelengths of the die were between 363 and 364 nm. By driving them at a slightly reduced power and using 10oC water to cool the device, the emission would be at 365 nm.

However, the emitted power of these die were still less than our goal. At the beginning of the project, we understood that these die were emitting 12-14 Watts of integrated power, and the roadmap indicated that the die would emit > 18 watts by the end of our investigation period. We needed 18 watts (minimum) for the LED die to replace the Hg lamp. Unfortunately, at the conclusion of the investigation, the power emitted from the devices has not increased sufficiently and the throughput from an LED illuminator would be reduced from the throughput of a Hg lamp illuminator.

Yield Improvements

We have made considerable improvements to LED manufacturing Yields using our Projection Lithography tool.

As reported earlier and illustrated in the following illustration, lithography is used several times in the manufacturing of the LED. This illustration, figure 20, shows lithography being used 5 times, but we have learned of some manufacturers using lithography 6 or more times.

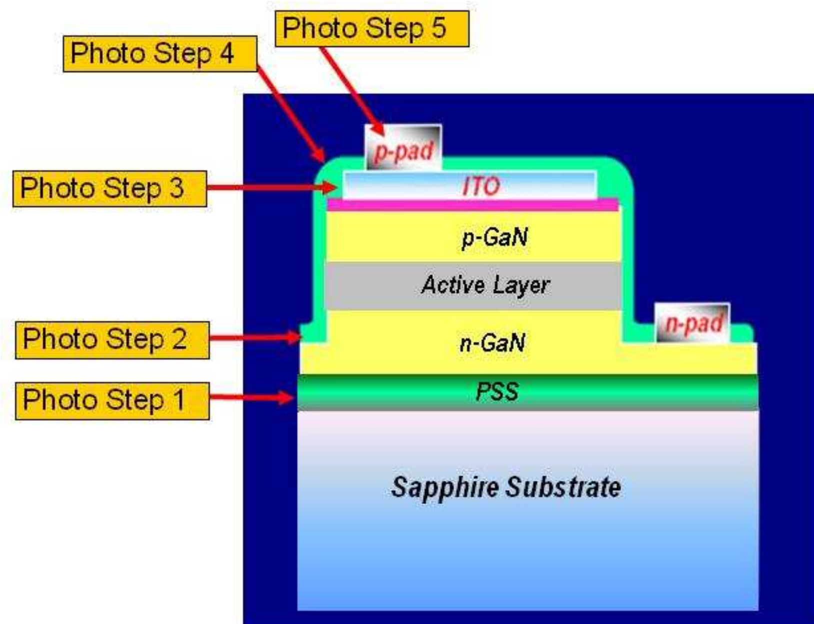
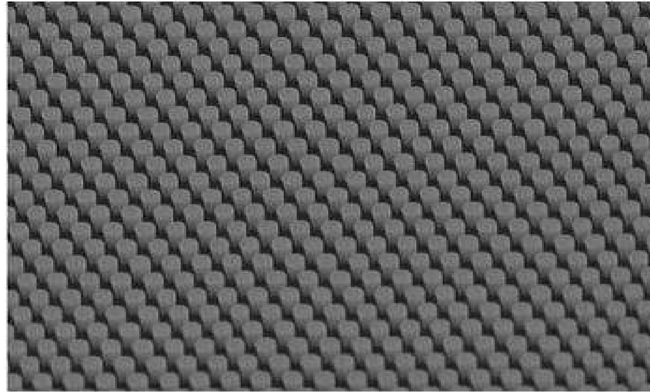


Figure 20: An illustration highlighting the various lithography steps during LED manufacturing.

The first photolithography step is at the patterned sapphire substrate (PSS) layer. These are typically small structures (1-2 microns in diameter, on a 2-3 micron pitch), about 3 microns tall (figure 21). Generally, this is the most demanding photolithography step in the LED manufacturing line, but is also the most tolerant of single defects. While it is critical to produce features of the correct dimensions, the absence of a single “dot” does not affect the performance of the LED. But, traditional proximity print aligners are incapable of producing these structures because of the warpage of the substrate. The warpage of the Sapphire substrate after the MOCVD deposition is typically ~50 microns for 2-inch wafers (more warpage for larger wafers), which creates gap-control issues in an aligner. When trying to print PSS type structures using an aligner, the print quality (dot diameter and spacing width) changes considerably as the gap changes. Hence, a Sapphire substrate printed with an aligner will have large areas where the PSS pattern prints poorly. As a result, the Ultratech projection lithography tool has became the tool of record at most LED manufacturing sites in the world for PSS layer patterning.

Major LED manufacturers have reported an increase in LED output efficiency of 15-20% using the PSS structures that are fabricated with Ultratech tools.



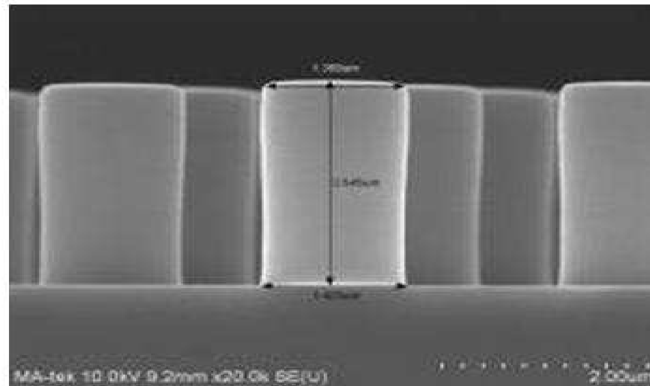


Figure 21: SEM micrographs of PSS structures defined on an Ultratech Stepper tool. The posts are typically about 1-2 microns in diameter, with approximately 1 micron between posts.

From figure 20, lithography step 2 defines the Mesa layer, which is typically features that are several tens of microns in size.

Lithography Step 3 is defining the ITO structures. Here, the use of the projection lithography tool is very dramatic. In results from our customers, we find that the ITO fingers defined by our steppers are much more clearly defined (Figure 22).

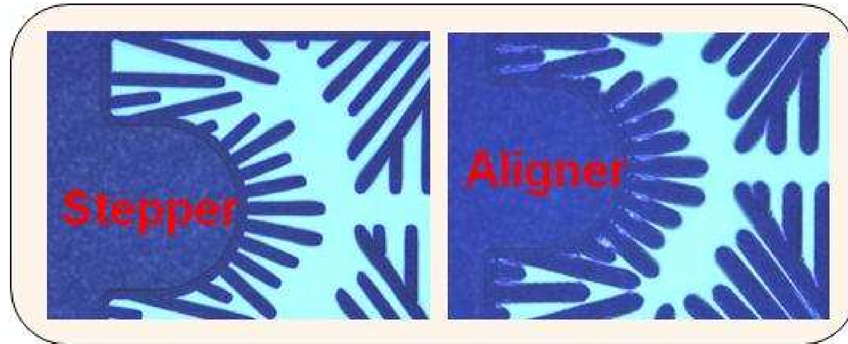


Figure 22: ITO fingers are used to help spread the current across the pGaN layers. The ITO defined using an Aligner is poorly defined, compared to the fingers printed with a Stepper. This results in improved LED efficiency.

The performance improvement on LEDs using projection lithography (rather than aligners) for the ITO layer is shown in Figure 23, where we see better LED emission with smaller fingers (smaller fingers do not print as well on aligners as they do on steppers). As a result, LED manufacturers are seeing 6-10% LED emission improvements from their devices whose ITO layers are patterned with steppers.

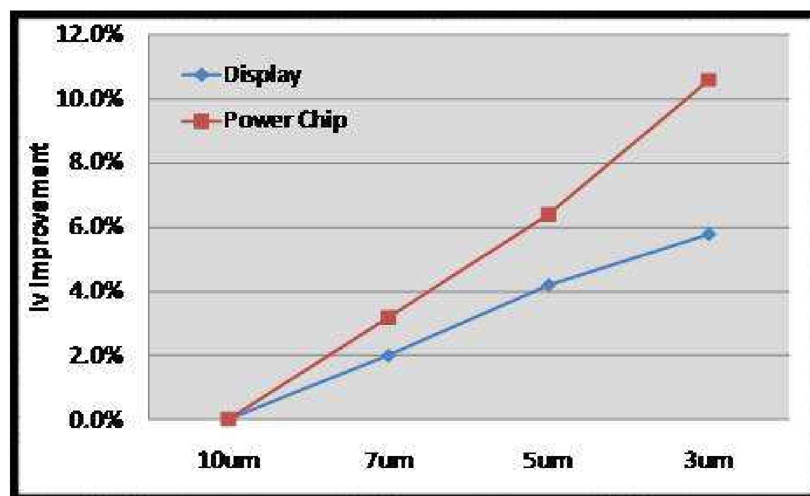


Figure 23: LED device performance improvements resulting from lithography using an Ultratech Stepper vs. an Aligner.

Lithography layers 4 and 5 include the current blocking layers and the final contact pad layers.

The results for using a projection lithography stepper vs. an aligner, is both improved device output (up to 30%) as well as improved yields. Actual yield data from a customer is shown in Figure 24, where the customer ran several thousand wafers (for power LEDs for consumer lighting) through two process lines: one using aligners for layers 2, 3 and 5, whereas, the second line using steppers for all layers. The results are dramatic; on 2-inch wafers, the customer reported a remarkable 7% yield improvement. This is so large that the calculated Return-on-Investment for purchasing a stepper is only 3 months!

Another customer reported the results of "re-work rate" for using the Ultratech Stepper, vs. a Nikon stepper for the most critical layers. The customer found that the Nikon stepper had a re-work rate of over 35%, whereas, the Ultratech stepper has a re-work rate less than 2%. This is an incredible difference and is likely because of all the LED specific improvements that have been integrated into the Ultratech Stepper tool as a result of this DOE program.

In short, the DOE program has allowed us to offer to the industry, a lithography tool that produces LEDs with up to 30% more output, have 10x less re-work rate (than other steppers), and have 7% higher final yields (than aligners). All this means better, brighter and less expensive LEDs.

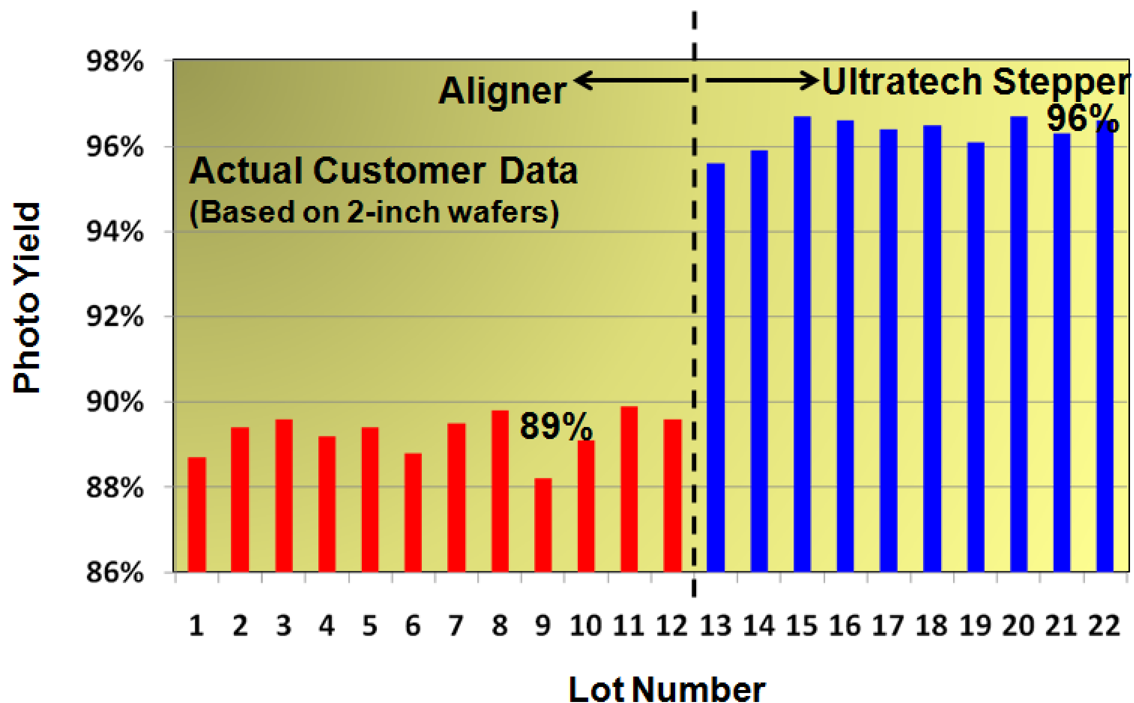


Figure 24: Yield results for production lots of LEDs made on an Aligner and made on an Ultratech Stepper. The yields form the Ultratech Stepper are 7% higher.

Warped Wafer Handling Improvements

GaN on Sapphire substrates are severely warped by the GaN deposition process. This makes robotic handling of the substrates difficult. Warpages in excess of 100 microns has been reported by customers for 2 and 4 inch wafers.

Ultratech has developed a variety of warped-wafer handling systems for Silicon wafers and has used this fundamental technology to develop a warped-wafer handling system for Sapphire substrates. This has greatly improved the robotic capabilities of our tools and allowed them to be fully automated in a manufacturing environment. The warped-wafer handling capabilities improve factory automation, reduces tool down time and improves yields.

We evaluated a number of wafers from LED manufacturers so that we can determine the type of warped wafer handling that would be required. The measurements were made on a custom tooling device designed by Ultratech for this purpose. The table below summarizes the measurements made on 2, 4 and 6-inch wafers.

			Wafer Profile Measurements (um)		
Date Measured	**Wafer ID**	**Wafer Size**	**Min**	**Max**	**Range**
May, 2011	N1106061	2"	-2.9	4.0	6.9
May, 2011	N11060604	2"	-5.0	2.4	7.4
May, 2011	N/A	4"	-15.0	-0.2	14.8
May, 2011	N/A	6"	-90.0	-4.5	85.5
October, 2011	S26525610	2"	-100.0	-12.0	88.0
October, 2011	S2625612	2"	-100.0	-12.0	88.0

We polled our customers and found that they expected wafer warpage to have the following maximum values:

Current structures:
- 2” wafers: 100 microns
- 4” wafers: 140 microns

Future structures:
- 2” wafers: 120 microns
- 4” wafers: 200 microns

A key performance requirement for the end effector is to:

1) Pick up and transport the warped wafer without dropping it
2) Deliver the warped wafer to the desired location within location tolerances.

This second requirement is often overlooked. During the wafer transport, it is necessary to place it in the appropriate location. If the wafer is placed in the wrong location, it may become difficult

(if not impossible) to continue processing the wafer. For example, if the wafer slipped on the end effector, and then the robot tries to load the wafer into a cassette, it may be possible for the edge of the wafer to hit the edge of the cassette, causing the wafer to fall to the floor. Additionally, there are times when the end effector must place the wafer precisely on the stage of the lithography tool within the capture window of the machine-vision system.

With these requirements and measurements, we developed a new end effector for the HB LED market. The end effector (used for robotic pick up and transportation) has three raised areas to create three points of contact on the warped wafer. It also has reduced channel areas that will make it easier for the wafer to make a seal and create a vacuum. This new design is illustrated in figure 25.

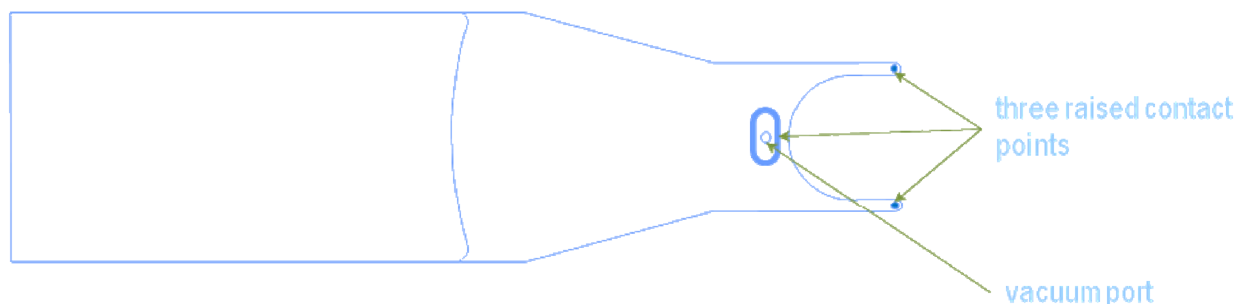


Figure 25. New End effector design for warped sapphire wafers.

The table below illustrates the wafer placement accuracy of wafers picked up and placed on the lithography tool. For the tool, we need the wafers placed to within +/- 100 microns in both x and y. It should be noted that several of the wafers in this table could not be picked up or located with a standard end effector.

			New End Effector Design	
Substrate	Wafer ID	Wafer Size	X 3Sigma (um)	Y 3Sigma (um)
Silicon	N/A	2	44.275	65.236
Silicon	N/A	4	42.052	51.467
Silicon	N/A	6	16.534	19.795
Sapphire	S2625610	2	90.224	57.522
Sapphire	S2625612	2	60.223	23.184
Sapphire	C0206054-Wafer #1	2	60.556	56.864
Sapphire	Wafer #2	2	36.331	47.754
Sapphire	Wafer #3	2	110.468	56.234
Sapphire	Wafer #4	2	101.851	52.9
Sapphire	Wafer #5	2	65.801	44.581

As of February 28, this new end effector design has been delivered to our customers and is being used in manufacturing.

CapEx Reductions

The original selling price of the lithography tool as designed for semiconductor applications was in excess of $1.5M. However, in discussions with our customers, we quickly learned that there was a “price ceiling” of approximately $1M for this tool. It became imperative that we reduce the capital cost of the tool.

The primary driver for the price of the tool is materials cost (labor represents a small percentage of the tool price). To reduce the tool price by ~33%, we need to reduce the materials cost by ~33%. This initiated a massive review of all components of the lithography tool and subjected each part to a cost-reduction analysis. Additionally, LED manufacturing specification requirements were accessed to determine if some features could be eliminated.

As of this writing, we have been able to reduce the materials cost of the tool by more than 25%. This reduction is slightly less than our goal when we began this project. However, the reason for the higher materials cost is that the LED market required that we add features to the tool (such as the Universal Wafer Chuck and the Off-axis IR camera). When these (and other) new features are removed, we are at approximately 30% cost reduction. The current list price for the tool with the additional features is $1.1M, which is sufficiently close to our target price.

Progress

Significant progress to date has been achieved on this project. Summarizing from above, we have:

- LED Illuminator
  - Completed concept design
  - Completed wavelength analysis
  - Completed uniformity analysis
  - Completed power requirement analysis
  - Completed source architecture concept
  - Found vendor with the technology to package the required source: completed
  - Characterized the LED performance: completed
  - Completed Lifetime testing
  - Completed Performance testing
  - Built a prototype LED illuminator and installed it on a stepper: completed
- Software
  - Throughput improvements completed
  - Yield improvements completed
  - Automation improvements completed
- Yield Improvements
  - New, off axis, IR alignment system with large depth of focus for better alignment, producing higher yields: completed

    - Higher yields inherent with Steppers vs. Aligners, but much lower re-work rate on Ultratech Steppers (vs. Nikon Steppers) because of all the LED specific "substrate handling" improvements: completed
    - Warped Wafer Handling system: completed
- CapEx reductions
    - Reduced CapEx by approximately 25% (however, in an "apples to apples" comparison, the reduction is closer to 30%). Completed
- Additional Activities
    - Low cost integrated enclosure completed
    - Modified fast shutter completed
    - Extended theta range on chuck completed
    - Universal Wafer size chuck completed

Summary

Our goal was to introduce a lithography tool with a specific set of capabilities to the LED community, and with a price tag of under $1M; a 33% reduction in the Capital Equipment cost. Since that time, we have learned of additional features that the LED community requires, which raised the price target. In an "apples to apples" comparison, we have successfully met the price reduction target. However, the additional features requested (or required) by the LED community have driven the price up so that the Capital Equipment cost is now approximately $1.1M. Given the yield improvements that the Stepper provides over aligners, our customers in the LED community have found this acceptable.

Also at the beginning of the program, we set very aggressive throughput goals for the tool. We wanted to increase the throughput of the tool by 25-35% (depending upon wafer size). We nearly met this goal. We fell slightly short of our goal because we weren't able to introduce the higher brightness source that we planned. Even so, our throughput increased by 20-30%.

At the beginning of this activity, we identified the new, high brightness, LED illuminator as the largest risk in the project. We were convinced that the project was worth doing even if this single aspect of the program failed. We learned a great deal about LED performance, and the demanding requirements of the lithography industry. As of this date, LEDs for 365 nm lithography are not ready yet. The greatest limitation seems to be the willingness of vendors to provide 365 nm LEDs; most vendors will provide a wide distribution of wavelengths around 365 nm (+/- 5 nm), which is unacceptable for lithography. We have also found some curious resist profiles using the LED illuminator. The root cause of this has not been determined. If the power and wavelength issues could be resolved, we are convinced that the profile issues could be adequately investigated and resolved.

Milestones and Deliverables

- **LED Illuminator:**
    - Concept design review — Completed
    - Prototype design & procurement completed — Completed
    - Prototype integration & testing completed — Completed
    - Resist characterization — Completed
    - Production design & procurement completed — Completed
    - Production integration and testing completed — Completed
    - Product release to manufacturing — Docs completed

- **Low Cost Integrated Enclosure:**
    - Prototype design & procurement — Completed
    - Prototype integration & testing — Completed
    - Install & test a beta system in the field — Completed
    - Documentation completed — Completed

- **Universal Wafer Size Change:**

- Design Completed Completed
- Procurement, integration & testing completed Completed
- Documentation completed Completed

- **IR Camera Cost Reduction**
  - Design completed Completed
  - Procurement, integration & testing completed Completed
  - Documentation and release Completed

- **Throughput Improvements (non-LED illuminator)**
  - Throughput analysis completed Completed
  - Theta stage improvement for accuracy & throughput Completed
  - Throughput enhancements and testing Completed

- **Warped Wafer Handling**:
  - Project Requirements Completed
  - Project Plan Completed
  - Designed solution Completed
  - Completed and released to customers Completed

- **Additional Cost Reductions**:
  - Analysis and proposals Completed

Conference Proceedings

No publications were made during this year.

Patents

No patent applications were made during the course of this activity.