NREL **National Renewable Energy Laboratory**

Innovation for Our Energy Future

15th Workshop on Crystalline Silicon Solar Cells and Modules: Materials and Processes

Extended Abstracts and Papers

Workshop Chairman/Editor: B.L. Sopori

Program Committee:
M. Al-Jassim, J. Kalejs, J. Rand, T. Saitoh,
R. Sinton, M. Stavola, R. Swanson, T. Tan,
E. Weber, J. Werner, and B. Sopori

Vail Cascade Resort
Vail, Colorado
August 7–10, 2005

15th Workshop on Crystalline Silicon Solar Cells and Modules: Materials and Processes

Extended Abstracts and Papers

Workshop Chairman/Editor: B.L. Sopori

Program Committee:
M. Al-Jassim, J. Kalejs, J. Rand, T. Saitoh,
R. Sinton, M. Stavola, R. Swanson, T. Tan,
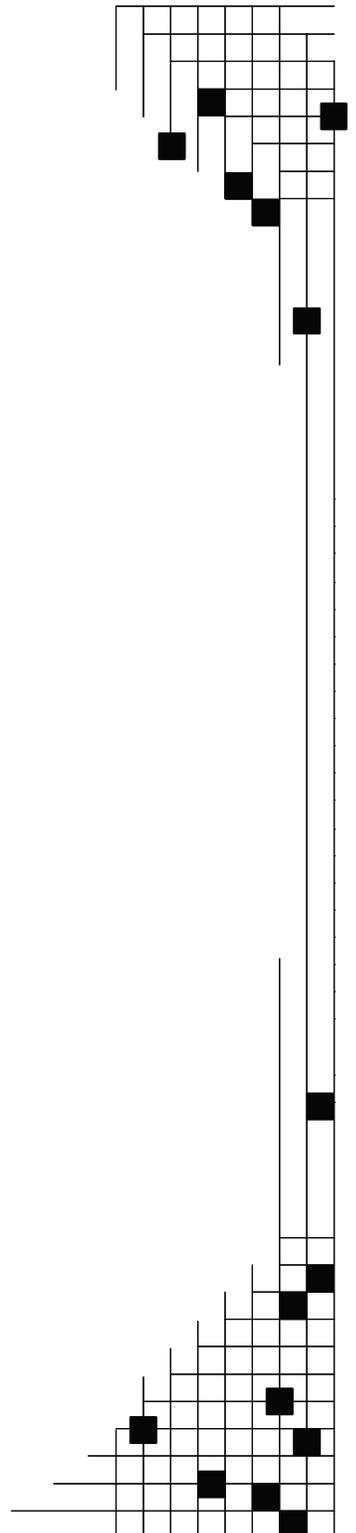E. Weber, J. Werner, and B. Sopori

Vail Cascade Resort
Vail, Colorado
August 7–10, 2005

National Renewable Energy Laboratory
1617 Cole Boulevard, Golden, Colorado 80401-3393
303-275-3000 • www.nrel.gov

Operated for the U.S. Department of Energy
Office of Energy Efficiency and Renewable Energy
by Midwest Research Institute • Battelle

Contract No. DE-AC36-99-GO10337

15th Workshop on
Crystalline Silicon Solar Cells & Modules:
Materials and Processes
August 7 – 10, 2005

TABLE OF CONTENTS

Silicon Workshop: Providing the Scientific Basis for Industrial Success

Bhushan Sopori
National Renewable Energy Laboratory

The silicon photovoltaic (PV-Si) industry has undergone rapid growth in the last few years, leading to new production capabilities that will exceed GW/yr and take us to multi-GW production in the near future. This rapid growth was fostered by many technical achievements and breakthroughs in the science and technology of photovoltaics. Some of these technologies were developed by the industry itself while others were adopted from R&D performed at various universities and academic institutions. These technical and scientific advances have occurred around the globe and, in many cases, were prompted by strong government assistance. In the United States, NREL/DOE offers many programs that support Si research and development. One of them is the Silicon Workshop, which is geared to help the PV-Si industry by (i) bringing together the industry, research, and academic communities, (ii) disseminating scientific and technical information by nurturing collective views on critical research areas, and (iii) providing feedback to NREL/DOE on important research tasks, as seen by the community. I (and the entire program committee) hope that the Silicon Workshop has contributed significantly toward the success of PV industry and will continue to do so in the future.

The silicon workshop started in late 1980's when NREL/DOE initiated a program heavily oriented to investigating the fundamentals of solar cell processing of low-cost (defected and impure) silicon wafers via the fundamentals of gettering and passivation. Accordingly, the early workshops were entitled "Role of Point Defects in Si Solar Cell Processing". This was the time when Si solar cell community was learning to view phosphorus diffusion and Al alloying not only as junction and contact formation processes, respectively, but as a means of mitigating effects of impurities and defects through gettering and passivation. Because the microelectronics industry had already commercialized gettering technologies, it was essential to import this art/science, as much as possible, from the gurus in the microelectronics industry. It was also necessary to entice microelectronics specialists to join the PV research teams (in spite of the dwindling budgets). The workshop started as gathering of SERI/DOE subcontractors in Si solar cell processing to discuss how to maximize research output for shrinking budgets. Each year since then, the meeting of these minds analyzed the scientific and technological progress; collectively we identified the critical technology areas, and determined potential solutions to industrial bottlenecks.

During the last 14 workshops, the title of the workshop changed to reflect increasing emphasis on industrial issues – attempting to guide the basic research toward solving industrial problems.

Now the workshop provides an informal avenue to assess the accomplishments in the PV field and to find solutions to advance the crucial technologies. This is done in Colorado – away from the humdrum of day-to-day chores in the various companies/research labs. The strength of the workshop is determined by its participants. We have been fortunate to benefit from the enthusiastic participation of invited speakers, poster presentations, and general attendence from industry, universities, and research laboratories worldwide, providing the mix of personalities that make this workshop special and especially useful and interesting. One of important parts of

the workshop agenda is the Summary of the Discussion Sessions, which highlights salient features of the discussions and provides a list of tasks that should be supported by NREL/DOE as future R&D. In keeping with the tradition of guiding the fundamental research, the theme of this year's workshop is "Providing the Scientific Basis for Industrial Success".

I am so grateful to the members of our Program Committee who spend a lot of time identifying topics for special sessions, invite suitable speakers, and develop a technically challenging program. This workshop deviates very significantly from traditional conferences— it is informal, provides ample time for discussion, and (something that is very dear to me) provides opportunities for younger scientists/engineers to freely express their views. In fact, many of our invited review talks are given by graduate students (who do a wonderful job in presenting unbiased reviews of the subject).

Our workshop also looks into the future to promote participation of younger scientists and engineers. This event is primarily supported by the PV industry, which makes contributions that pay for the financial support of the graduate students. I am very thankful to the contributors who invest in the future of PV. Each year the workshop recognizes both the contributors and the recipients of the Graduate Student Awards.

Many people find the workshop proceedings very useful. For this 15th workshop, as a memorabilia, we have put all these proceedings together in a memory stick. I am sure many of you will cherish it as much as I will.

The program committee has selected several special sessions to address issues such as availability of poly feedstock, challenges in using thinner wafers, critical modules issues, and novel processing and cell design approaches. I hope you will find this year's workshop enlightening.

This year we dedicate the session on Impurity & Defect Engineering to Prof. Jim Corbett, who has made enormous contributions in this area and was one of the strongest supporters of the workshop. I have learned a lot from him and have greatly appreciated the humility of such a great scholar and gentleman. I am thankful to Stefan Estreicher for suggesting this dedication to Prof. Corbett.

p-type vs. n-type Silicon Wafers: Prospects for High-efficiency, Commercial Silicon Solar Cells

J.E. Cotter, J.H. Guo, P.J. Cousins, M.D. Abbott, F.W. Chen and K.C. Fisher
Centre of Excellence for Advanced Silicon Photovoltaics and Photonics
University of New South Wales, Sydney, Australia 2052

Abstract

Chemical and crystallographic defects are a reality of solar grade silicon wafers and industrial production processes. Long overlooked, phosphorus as a dopant in silicon wafers is an excellent way to mitigate recombination associated with these defects. This paper details the connection between defect recombination and solar cell terminal characteristics, for one specific case of high hole lifetime and low electron lifetime. It then looks at a detailed case study of the impact of diffusion induced dislocations on the recombination statistics in n-type and p-type silicon wafers and the terminal characteristics of high-efficiency, double-sided buried silicon solar cells made on both types of wafers. Several additional short case studies examine the recombination associated with other industrially relevant situations - process-induced dislocations, surface passivation and unwanted contamination. On the whole, n-type silicon wafers are more tolerant to chemical and crystallographic defects, and as such, they have exceptional potential as a wafer for high-efficiency, commercial silicon solar cells.

1. Introduction

N-type Czochralski and multicrystalline silicon materials, associated process technologies and solar cell designs have received considerable attention recently, for a number of reasons. Several researchers have reported very high pre- and post-processing lifetimes in both cast multicrystalline [1] and Chochralski materials [2]. Many have noted the performance stability of various phosphorus-doped Czochralski silicon wafers under illumination, in contrast to the industry-standard boron-doped Cz wafers [3, 4]. MacDonald [5] and Martinuzzi [6] have catalogued electron and hole lifetimes for a variety of chemical impurities and discussed the implications for silicon solar cells. More recently, research groups are reporting good initial solar cell efficiencies on various designs and based on various process techniques [7, 2, 8, 9, 10, 11]. Sanyo [12] and SunPower, Inc. [13] have demonstrated efficiencies over 20% in large area n-type Czochralski and solar grade float zoned wafers using vastly different solar cell technologies. There certainly appears to be excellent potential for commercial grade, n-type silicon wafers as a basis for high-efficiency commercial silicon solar cells.

The technical underpinning for optimism regarding commercial n-type silicon wafers over similar p-type silicon wafers is that, for many defects relevant to commercial grade silicon wafers, hole lifetimes are higher than electron lifetimes, in some cases, orders of magnitude higher. A casual look at the familiar low-injection, minority-carrier diffusion length $L \equiv \sqrt{D \cdot \tau}$ hints at a very important design issue for silicon solar cells - which are better, electrons or holes, as minority charge carriers? Electrons have higher mobility/diffusivity by a factor of about 3, so in materials and processes that are free from any defects whatsoever, electrons, and therefore p-type silicon wafers, have the advantage. Today's commercial grade silicon wafers and industrial processes, however, are not free from defects. Chemical impurities, precipitates, complexes, and crystal imperfections are so common that 15+ years of intensive effort by numerous researchers [14] has been devoted to understanding and mitigating those defects. This raises the main question of this paper: Given defected silicon wafers and industrial process that introduce defects, which is better, n-type or p-type silicon? We acknowledge the broader context of the p-versus-n wafer question. Issues such as processing technology (boron diffusion is particularly tricky, for example), equipment and capital investment, wafer cost, yield and availability, market acceptance, etc. are all important, however, they are outside the scope of this paper.

This paper first ties together the nature of asymmetric Shockley-Reed-Hall (a-SRH) recombination to a solar cell's performance, namely its lighted J-V, dark log(J)-V and dark local ideality factor (m-V) curves. For a typical a-SRH recombination process, wafer polarity matters a great deal to the solar cell's performance. We then describe a case study that traces from a specific process-induced defect - diffusion-induced misfit dislocations - through the photoconductance lifetime and finally to the final solar cell terminal characteristics of side-by-side, p-type and n-type buried contact silicon solar cells. We then look at photoconductance lifetime studies of several industrially relevant situations - process-induced dislocations, surface passivation and furnace contamination. In all cases, there is a clear bias toward high hole lifetimes and low electron lifetimes, which suggests that given the defected nature of solar grade silicon wafers and industrial processes, the n-type solar grade wafers hold a significant advantage over their p-type counterparts.

2. Asymmetric Shockley-Reed-Hall Recombination and Solar Cell Terminal Characteristics

Robinson et al. [15] and Cousins et al. [16] observed and explained the effect that a-SRH has on passivated-emitter rear locally diffused (PERL) and double sided buried contact (DSBC) solar cells, respectively. For a SRH recombination centre, at one fixed energy, the well-known SRH recombination rate expression applies

$$U_t = \frac{(n \cdot p - n_i^2)}{\tau_h \cdot (n + n_1) + \tau_e \cdot (p + p_1)}, \text{ where } \quad \tau_h \equiv \frac{1}{v_{th} \cdot N_t \cdot \sigma_h} \quad \text{and} \quad \tau_e \equiv \frac{1}{v_{th} \cdot N_t \cdot \sigma_e}.$$

Here, τ_h and τ_e are the hole and electron lifetimes, which depend on both the density of defect states N_t and the capture cross sections of electrons and holes σ_e, σ_h, respectively. We refer to the case where the majority and minority carrier lifetimes differ significantly as asymmetric Shockley-Reed-Hall recombination, specifically $\tau_{Majority} \gg \tau_{minority}$. a-SRH recombination is illustrated in Figure 1a, which shows the total and components of normalised recombination $U/\Delta n$ (expressed as inverse lifetime) for a few cases of a-SRH and including a small component emitter recombination. Curve A shows the total recombination in a p-type wafer with simple (ie. traps at a single energy level) a-SRH recombination ($\tau_h \gg \tau_e$). Curve B shows the total recombination in a p-type wafer with a more-natural a-SRH recombination (traps distributed over a spectrum of energy levels). Curve C shows the total recombination in an n-type wafer for both types of a-SRH used for Curves A and B (again for $\tau_h \gg \tau_e$) and Curve D shows the total recombination for no a-SRH recombination (emitter recombination only), which represents the unaffected case.

Except for the omission of junction recombination, which occurs at the cleaved edge of the device [18], Figure 1a is fairly typical of high-efficiency double-sided buried contact solar cells (DSBC) made at UNSW. The SRH recombination rate is dominated by the minority carrier lifetime at lower injection levels and by the sum of minority and majority carrier lifetimes at higher injection levels, which is well understood, however, it is important to point out that the inflection point between these two regimes does not necessarily occur at the high-low injection boundary (ie. at the wafer doping level), as can be clearly seen in Figure 1a. The inflection occurs at a point that depends on the a-SRH statistics (including the wafer doping level) and other recombination processes occurring in the device. Importantly for high-efficiency commercial silicon devices, the inflection point can occur at or above the one-sun operating injection level of a silicon solar cell, where it has a significant negative impact on the terminal characteristics of a solar cell.

(a)   *(b)*   *(c)*
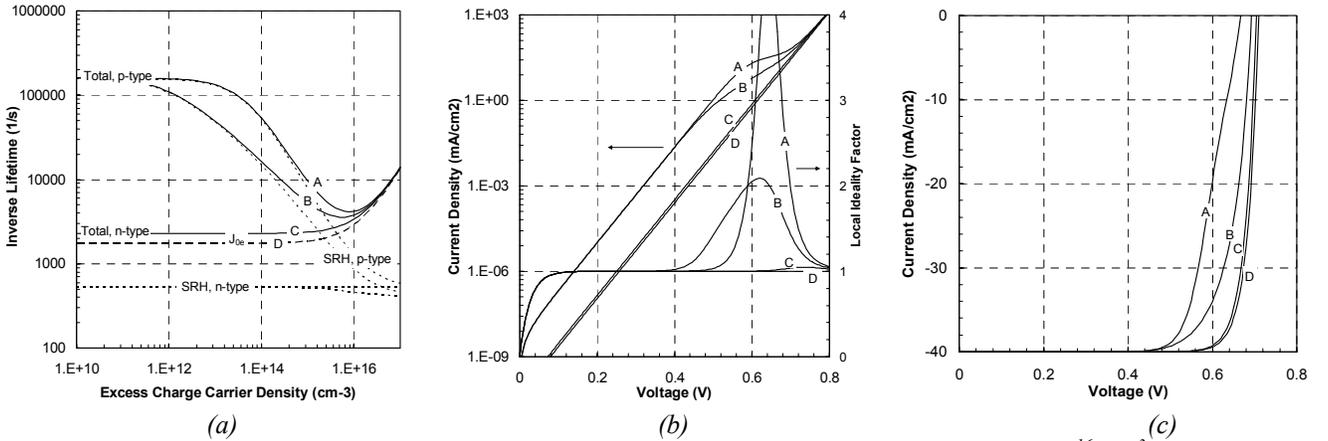
Figure 1. (a) Simulated total and components of recombination n-type and p-type ($N_a = N_d = 1.5 \times 10^{16}$ cm^{-3}) silicon wafers, expressed as inverse lifetime, including a-SRH recombination ($\tau_p \gg \tau_n$) and emitter recombination ($J_{0e} = 4.8 \times 10^{-14}$ A/cm^2); (b) the resulting dark log(J)-V and dark m-V curves; and (c) the resulting lighted J-V curves.

The simulation in Figure 1a can be recast as implied current-voltage curves to illustrate this key point, using

$$iV = \frac{k \cdot T}{q} \ln\left(\frac{n \cdot p}{n_i^2}\right) \quad \text{and} \quad iJ = q \cdot W \cdot (U_t + U_e)$$

where iV and iJ are the implied voltage and implied current determined by the injection level and the recombination rates U_t and U_e, which are the a-SRH and emitter recombination rates, respectively. W is the device thickness. Figure 1b shows the

resulting transformation as dark current-voltage (log(J)-V) and local ideality factor curves (m-V), and Figure 1c shows an illuminated current-voltage (J-V) curve, assuming a constant value for light-generated current density (J_{sc} = 40 mA/cm^2). The influence of the a-SRH recombination process can be seen clearly in the terminal characteristics of a solar cell: a characteristic shift to higher voltage at higher current in the dark log(J)-V curves, a "hump" in the dark m-V curves and a soft fill factor in the lighted J-V curves.

Comparison of Curves A-D in Figure 1c clearly shows the negative impact that a-SRH recombination can have on the terminal electrical characteristics of a solar cell, but more importantly, it illustrates the difference that wafer type makes in terms of mitigating this type of recombination. For this case, where $\tau_p \gg \tau_n$, the p-type solar cell is adversely affected (Curves A and B) compared to the case with no a-SHR recombination (Curve D), whereas the n-type solar cell is hardly affected (Curve C). This situation is illustrated in the following case study.

3. A Case Study - Misfit Dislocations and the DSBC Solar Cell

One of the best demonstrations of the link between manufacturing considerations and solar cell performance, as it relates to the a-SRH argument outlined in the previous section, is the story of boron diffusions in high-efficiency Buried Contact (BC) Solar Cells. The double-sided buried contact solar cell suffered from poor fill factor and a characteristic hump in the m-V curve that was initially attributed to floating junction shunting [17]. McIntosh et al. [18] first attributed the poor fill factor to the heavy boron groove diffusion, and Cousins et al. [19] later identified boron diffusion-induced misfit dislocations as the specific a-SRH recombination centre responsible for the poor performance. Guo [20], working in parallel on n-type high-efficiency interdigitated backside BC (IBBC) solar cells and using identical boron groove diffusions, first pointed out the absence of the deleterious effects of a-SRH recombination in working solar cells using J-V and m-V analysis.

Misfit dislocations form due to stress gradients that arise from dopant concentration gradients, such as those typically found in solid-state diffusions. Stress on the silicon lattice is caused by atomic radius mismatch between silicon and the dopant atom (the covalent radii of boron and phosphorus are 0.88 Å and 1.06 Å respectively, compared to 1.18 Å for silicon), resulting in a localised contraction of the silicon lattice around the substitutional dopant atoms. For low concentrations of dopant atoms, the lattice accommodates this stress elastically, however, when the total concentration of dopants exceeds a critical concentration the lattice can no longer accommodate elastically, and misfit dislocations are generated. These diffusion-induced misfit dislocations are half-loop dislocations nucleated at the diffusion surface in the <110> directions consisting of two screw dislocations perpendicular to the diffusion surface and an edge dislocation line parallel to the diffusion surface in the <110> direction. At diffusion temperatures, the two screw dislocations glide out of the wafers edge within seconds, and the edge dislocation lines glide into the substrate in response to the stress gradient governed by the diffusion profile. The collision of several edge dislocations forms a cross-hatch dislocation network characteristic of diffusion-induced misfit dislocations. Figure 2 shows the characteristic cross-hatch pattern that results from Yang defect etching (CrO$_3$:HF) [21] of the surfaces and cross-sections heavily boron and phosphorus diffused silicon wafers.

| (a) | (b) | (c) |
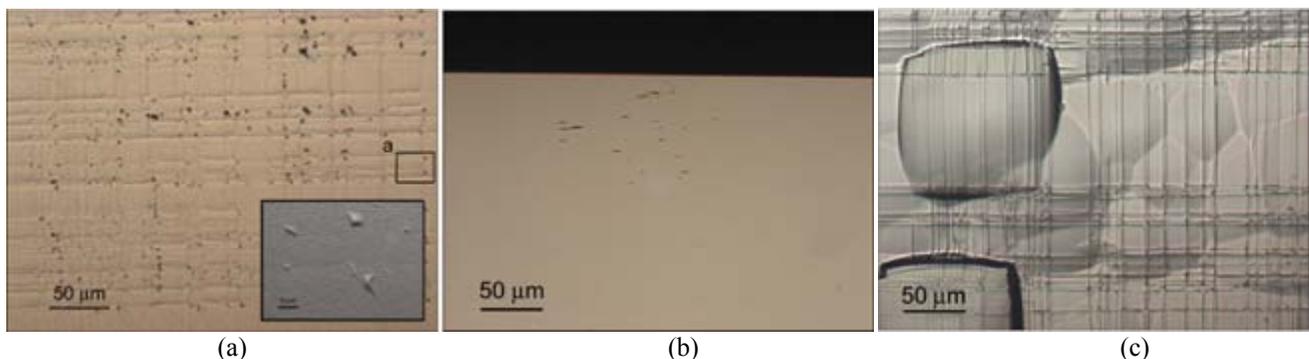
Figure 2. Photo of the misfit dislocation networks observed for phosphorus and boron diffusions as revealed by Yang etching (a) heavy boron diffusion, observed on the plan-view, (100) surface, (b) heavy boron diffusion, observed on the cross-section (110) surface cross-section, and (c) heavy phosphorus diffusion, observed on the plan-view, (100) surface.

Figure 3a shows the recombination characteristics for heavily boron diffused p-type and n-type silicon wafers that are known to produce dislocation networks like those shown in Figure 2. Figure 3b shows a similar plot of lightly boron diffused p-type and n-type silicon wafers known to not produce dislocation networks. The correlation between the boron process (heavy or light), the misfit dislocation (present or absent) and the a-SRH recombination (present or absent) is reasonably clear - Cousins [19] provides more detail for both phosphorus and boron diffusions. The key observations to make in the graphs in Figure 3 are the reduced overall recombination in n-type wafers and the absence of the strong a-SRH

behaviour for the boron diffusions made on the n-type wafers, because hole lifetimes are significantly greater than electron lifetimes for these defects.

(a) (b)
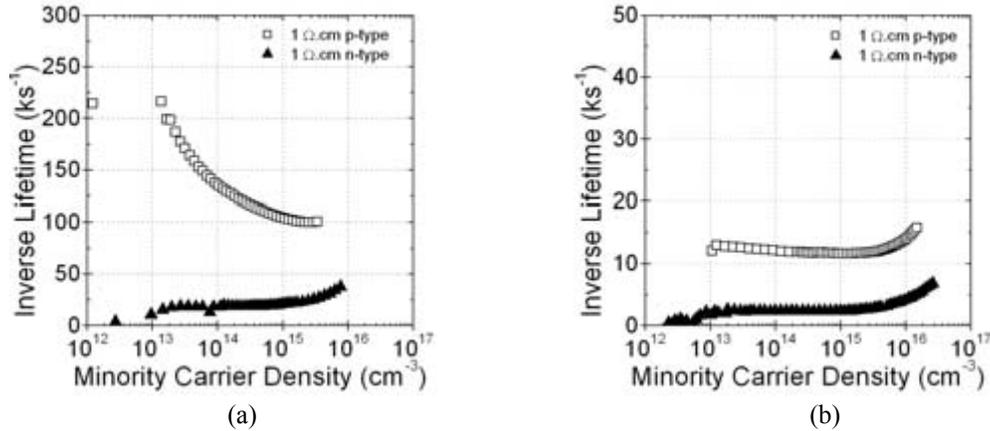
Figure 3. Photoconductance measurements of inverse lifetime for diffusions in p-type and n-type FZ silicon demonstrating the presence or absence of a-SRH resulting from (a) heavy boron diffusions (~20 Ω/sq.) known to produce a misfit-dislocation network (per Figure 2) and (b) light, well-controlled boron diffusion (~100 Ω/sq.) known to be free of a diffusion-induced misfit dislocation network.

Fortunately, the DSBC solar cell design is ideal for making a direct comparison of solar cell terminal characteristics of solar cells made side-by-side on n-type and p-type silicon wafers. The DSBC processing sequence can be applied to either type of wafer without significant changes in the processing sequence - diffusions, oxidations, even metallisation processes can be applied with good effect to both types of wafers run in split batches. Also, the heavy boron diffusion characterised in Figure 2a and Figure 3a is typical of the heavy boron diffusion process used in the "groove diffusion" step and is known to produce diffusion-induced misfit dislocations. Such a side-by-side comparison of terminal characteristics of p-type and n-type solar cells is shown in Figure 4.

(a) *(b)* *(c)*
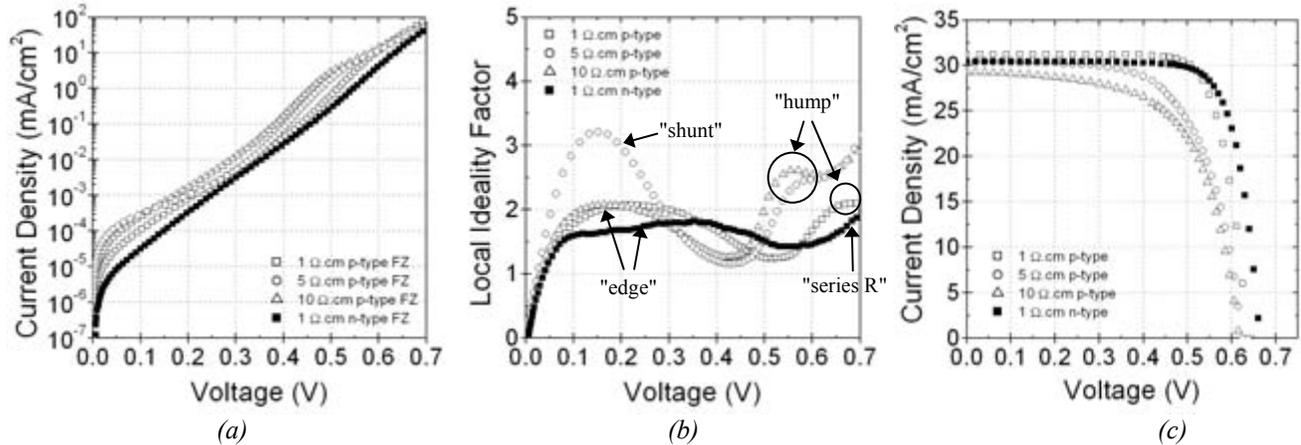
Figure 4. Dark ln(J)-V, dark m-V, and lighted J-V curves of a split batch of DSBC solar cells made on various p-type and n-type silicon substrates.

The m-V curves represent the keystone of this discussion. Firstly, however, several features commonly found in m-V curves that are not relevant in the current discussion should be pointed out. At low voltages, an ohmic shunt can be seen in one of the p-type solar cells, while the other three solar cells exhibit edge-induced junction recombination because of their relatively large perimeter compared to their area [18]. Also, at high voltages, all four solar cells exhibit series resistance. What is most relevant is that all three p-type devices show the hump that is characteristic of the a-SRH recombination process induced by heavy boron groove diffusions (see Figure 1b) and that the n-type solar cell does not exhibit the hump. All four solar cells used boron groove diffusions that are known to introduce diffusion-induced misfit dislocations, yet only the p-type solar cells are affected by their presence.

Furthermore, the hump peaks at a voltage that is governed by SRH statistics, so the shift in the peak with wafer resistivity observed in Figure 4b provides additional support that the hump is due to a-SRH recombination. More importantly, the

hump, which is tied to the transition in the a-SRH recombination statistics as described in the previous section, occurs roughly around the operating point of the solar cell and adversely affects all of the key terminal characteristics of the p-type solar cells, especially fill factor, as can be seen in Figure 4c, but not the n-type solar cells.

The case of the solar cell fabricated on the p-type 1 Ω.cm wafer deserves extra discussion. The fill factor of this particular solar cell looks comparable to the n-type case. However the a-SRH effect on fill factor is not apparent in the p-type solar cell because the inflection point described above occurs at around 675 mV (note the peak of the associated hump in Figure 4b), which is well above its open circuit voltage of the solar cell. Importantly, the voltage characteristics of this solar cell *are* degraded by the a-SRH recombination, as can be seen by comparing voltages with the n-type solar cell, which, incidentally, has a base doping level that is lower by a factor of 3.

4. Other Industrially Relevant Cases

Float zoned wafers can be made with nearly zero density of any chemical point defects, complexes, and extended defects, and laboratory processing can be controlled to a high degree to avoid contamination and extended defect formation and provide superior surface passivation - thereby avoiding the deleterious effects of a-SRH recombination. For example, PERL solar cells made on FZ wafers in the laboratory have demonstrated this [22].

Solar grade wafers and high-volume, low-cost manufacturing processes, however, do not afford the same wafer quality and process control. Multicrystalline silicon wafers are riddled with a diverse population of chemical impurities and complexes, dislocations and stacking faults, twins and grain boundaries and surfaces. Industrial processes can subject the wafer to intrinsic (thermal expansion) and extrinsic (stress from coatings and diffusions) stresses and contamination that contribute further to this diverse population of defects.

The previous discussion provides one good basis for answering the p-versus-n question, but diffusion induced misfit-dislocations are only one entry in the catalogue of SRH recombination centres that might be found in solar grade silicon wafers and/or induced by industrial solar cell fabrication processes. More information is needed about the nature of defects common to silicon solar cells.

MacDonald [5] and Martinuzzi [6] have presented short tables of chemical impurities commonly found in multicrystalline silicon wafers. Many of the usual suspects - Fe, Ti, V, Cr, Mo, Co, FeB, CrB - show asymmetric capture cross sections with high hole lifetimes and low electron lifetimes, although some do not. As far as these elements are concerned, at least, using phosphorus instead of boron as a dopant has good potential to mitigate the a-SRH recombination effect described above. This section looks at the nature of a few other defects that are relevant to the industrial manufacture of silicon solar cells - dislocations, surfaces and furnace contamination - with the aim of providing additional insight into the p-versus-n question.

4.1 Laser-induced Dislocations

Dislocations can be induced by any number of industrial process steps that place the silicon wafer under stress. Furnace loading and unloading, oxidation of textured surfaces, and laser ablation, for example, are well known to induce local dislocations which can glide a considerable distance during subsequent thermal treatments. The DSBC and IBBC process sequences use laser ablation, so the impact of laser-induced dislocations is of importance to these types of solar cells. Here we look the recombination statistics of laser-induced dislocations, and generalise to dislocations generated by other processes.

The laser ablation process is used to make the grooves of DSBC and IBBC solar cells. The silicon wafer is heated in a local area well above the melting temperature of silicon (1410°C) in a very short time (a few microseconds). The molten silicon is ejected from the wafer leaving a groove behind the path of the laser. The ablation process creates a thin layer of damage on the walls of the groove that is normally removed using a sodium-hydroxide etch. If the damaged layer is not removed properly, these dislocations will glide into the bulk of the wafer during subsequent thermal processes.

Figure 5 shows three such grooves. A typical front electrode grid was laser scribed into a split batch of p-type and n-type silicon wafers that were sodium-hydroxide etched for different times and then subjected to a thermal treatment at 1000°C for 2 hours in an inert ambient. A Yang etch was used to delineate the dislocations, which are clearly visible in Figure 5a and b, but not in Figure 5c, which was sufficiently etched to remove the damage layer.

(a)   *(b)*   *(c)*
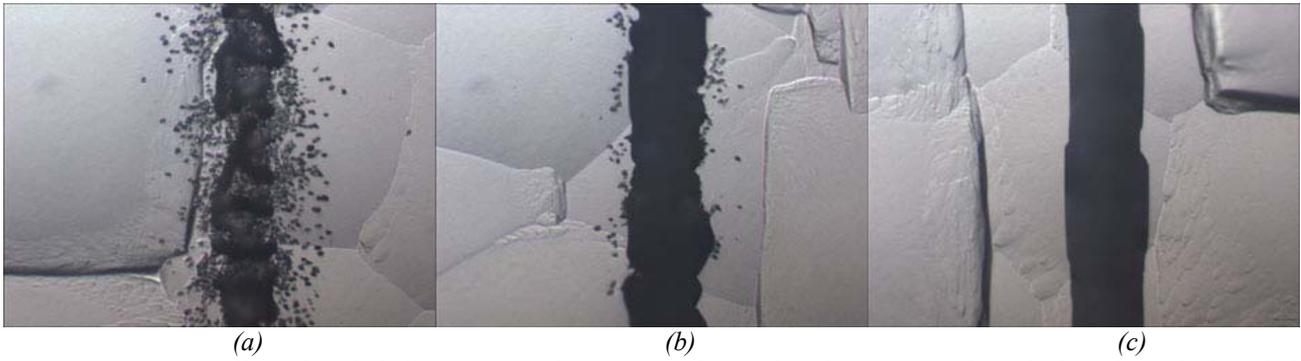
Figure 5. Intentionally induced dislocations on laser-grooved samples that were sodium hydroxide etched and then subjected to a thermal cycle (a) 0 minutes etch (b) 12 minutes etch and (c) 20 minutes etch.

A second split batch of p-type and n-type wafers was processed identically and then phosphorus diffused and oxidised to provide a high-quality surface passivation. The finished wafers were then characterised using the photoconductance lifetime technique. The data are shown in Figure 6.

(a)   (b)
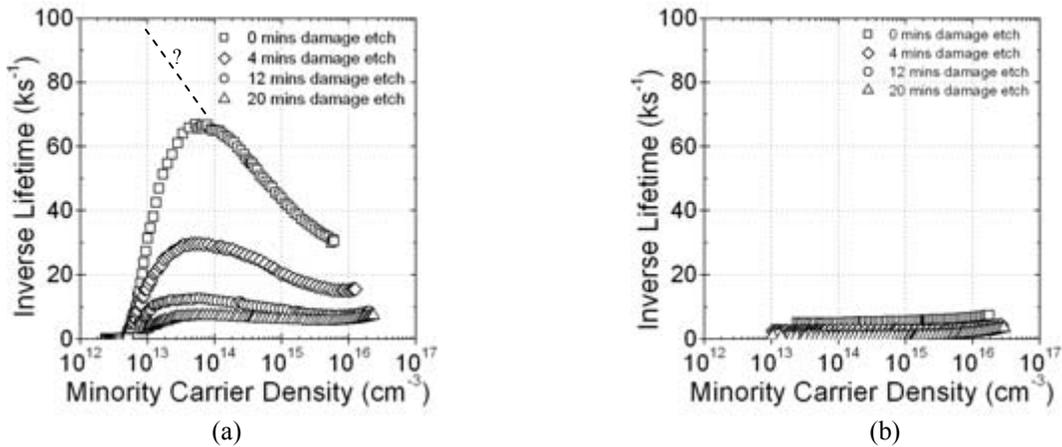
Figure 6. Photoconductance measurements of the laser-scribed wafers showing the dominance of the a-SRH recombination in the p-type samples (a) and the absence of a-SRH recombination in the n-type samples (b).

The difference in the recombination statistics of the p-type and n-type samples is remarkable. The n-type wafers are nearly completely insensitive to the presence of the dislocations, supporting very high effective lifetimes even for the worst case, whereas the p-type wafers are highly sensitive and show low lifetimes, the full impact of which is masked by the depletion region modulation effect [23] at injection levels below about 10^{13} cm^{-3}.

The misfit- and laser-induced dislocations both show high hole lifetimes and low electron lifetimes, and it is reasonable to expect that dislocations induced by other processes would behave similarly. Therefore, for materials and processes where dislocations might be present or introduced (for example, multicrystalline silicon wafers or rapid furnace loading and unloading processes), the n-type wafer has a clear advantage in terms mitigating the associated recombination.

4.2 Wafer Surfaces

Surfaces are a well-studied source of recombination in silicon solar cells. The ratio of hole to electron lifetimes is already known to be much greater than 1 for silicon surface states passivated by both silicon dioxide and silicon nitride [24]. We confirm this understanding again here in order to draw attention to the importance considering surface recombination when addressing the p-versus-n question.

The photoconductance lifetime graphs in Figure 7 show the recombination statistics for three cases of p-type and n-type surfaces: (a) direct passivation by thermally grown silicon dioxide; (b) direct passivation by PECVD silicon nitride; and (c) passivation by PECVD silicon nitride of boron and phosphorus diffused surfaces. The graphs show that in all cases, the ratio of hole lifetimes to electron lifetimes is greater than one. Thus, as far as silicon surfaces are concerned, the n-type surface has a clear advantage in terms of mitigating the associated recombination.
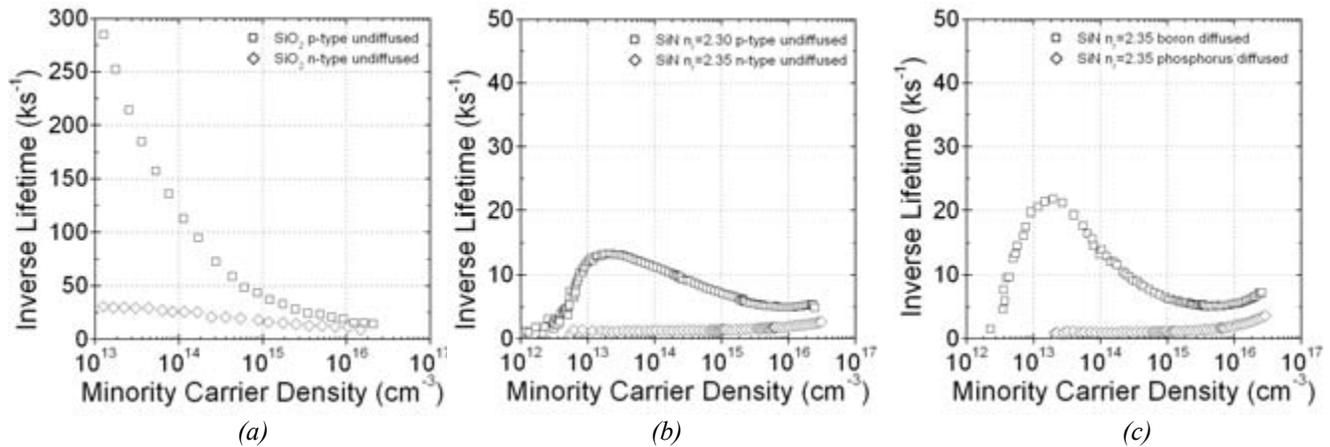
Figure 7. Photoconductance measurements of surface recombination in p-type and n-type FZ silicon wafers (a) direct passivation of 1 Ω.cm, p-type and n-type wafers with thermally grown silicon dioxide; (b) direct passivation of 1 Ω.cm, p-type and n-type wafers with PECVED silicon nitride; (c) passivation of light phosphorus and boron diffusions (~100 Ω/sq.) on a 1 Ω.cm, n-type silicon wafer with PECVD silicon nitride.

4.3 Contamination

Wafer contamination is a spurious problem that kills wafer lifetime and degrades solar cell performance. The list of sources of chemical contaminants is endless - poor quality water, poor handling, furnace cross contamination, particles from clothing and hair. Clean room facilities and procedures go a long way to solving contamination problems, of course, in fact PERL silicon solar cells routinely achieve >24% in quite rudimentary clean facilities.

Despite our best efforts, diffusion and oxidation furnaces at UNSW occasionally become contaminated by unknown chemical impurities. One particular split batch of three 1 Ω.cm p-type and three 1 Ω.cm n-type float zone solar cells was rejected after phosphorus diffusion and oxidation due to an unexpected contamination that was detected by routine photoconductance lifetime monitoring. Figure 8 shows the photoconductance lifetime measurements of that batch. The variability in the recombination statistics of the p-type samples is consistent with this type of contamination problem. The important things to note are the tight distribution of the recombination statistics for the three n-type wafers (the three curves overlap to within the width of the border of the symbols used in the graph), the much lower overall recombination for the n-type wafers and the absence of a strong a-SRH behaviour in the curves. This strongly suggests that the n-type wafers are largely unaffected by the contamination problem in sharp contrast to the p-type wafers. Therefore, n-type silicon wafers have clear advantage in terms of this particular contamination problem, and likely in the more general case, in terms of mitigating the recombination associated with contamination.
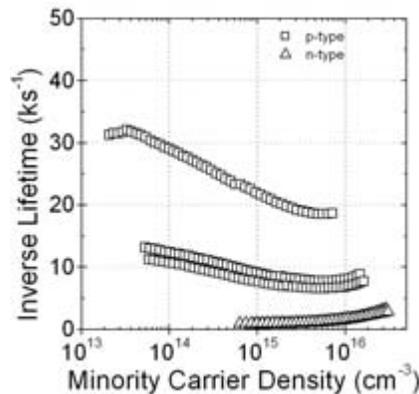
Figure 8. Photoconductance measurements of p-type and n-type silicon wafers unintentionally contaminated during a phosphorus diffusion and thermal oxidation process sequence.

5. Conclusion

N-type silicon wafers offer a significant opportunity for commercial, high-efficiency silicon solar cells. Lifetimes and device characteristics have been proved to be stable under illumination. High lifetimes have been reported in

multicrystalline, Czochralski and float zoned wafers, and high efficiency solar cells are now being reported in solar cells made on n-type wafers. As for feedstock considerations, the growing list of defects that exhibit high hole lifetime and low electron lifetime, and the impact that the associated a-SRH recombination has on the terminal characteristics of solar cells, suggests that n-type silicon wafers are better suited for high-efficiency, commercial silicon solar cells. As for industrial manufacturing processes, the excellent tolerance of n-type wafers to induced or introduced defects suggest the same again. Overall, in terms of the electrical requirements of a solar grade wafer for industrial high-efficiency silicon solar cells, n-type wafers seem to hold a significant advantage over p-type wafers.

Issues in the broader context of the p-versus-n question do not seem terrible. N-type wafers are not significantly more expensive than p-type wafers. Module manufacturing technology should cope with n-type solar cells, and system integrators should have no problem with n-type modules. Perhaps the largest issue is manufacturing technology, specifically forming the p+ emitter and metallisation. Boron diffusion, while more difficult than phosphorus diffusion, is not impossible, with a little care, and good results with printed and plated metallisation are already being reported. New device concepts and designs based on n-type solar cells are already springing up. Given the demonstrated potential, n-type silicon wafers are an opportunity for high-efficiency commercial silicon solar cells that is not to be missed.

References

1   A. Cuevas, S. Riepe, M. J. Kerr, D. H. Macdonald, G. Coletti and F. Ferrazza, "N-type multicrystalline silicon: a stable, high lifetime material," *Proceedings of the Third WCPVEC*, Osaka, Japan, 11-18 May, 2003, pp. 1312-1315.
2   J.H. Guo and J.E. Cotter, "Laser-grooved Backside Contact Solar Cells with 680 mV Open-circuit Voltage," *IEEE Transactions on Electronic Devices*, vol.51(12), pp.2186-2192, 2004.
3   S.W. Glunz, et al., "Comparison of Boron- and Gallium-doped p-Type Czochralski Silicon for Photovoltaic Applications", *Progress in Photovoltaics: Research and Applications*, Vol. 7, pp 237-240, 2000.
4   J. H. Guo, B. S. Tjahjono, and J. E. Cotter, "19.2% Efficiency N-type Laser-grooved Silicon Solar Cells," *Proc. 31st IEEE Photovoltaic Specialists Conference*, Orlando, FL, 2005.
5   D. Macdonald and L.J. Geerligs, "Recombination Activity of Interstitial Iron and other Transition Metal Point Defects in p- and n-type Crystalline Silicon," *Applied Physics Letters*, Vol. 85, No. 18, pp. 4061-4063, 2004.
6   S. Martinuzzi et al. "n-type Multicrystalline Silicon Wafers for Solar Cells," *Proc. 31st IEEE Photovoltaic Specialists Conference*, Orlando, FL, 2005.
7   A. Cuevas, C. Samundsett, M. J. Kerr, D. H. Macdonald, H. Mäckel and P.P. Altermatt, "Back junction solar cells on n-type multicrystalline and CZ silicon wafers," *Proceedings of the Third WCPVEC*, Osaka, Japan, 11-18 May, 2003, pp.963-966.
8   J. Zhao et al., " "High Efficiency Rear Emitter PERT Solar Cells on n-type FZ Single Crystalline Silicon Substrates," *Proceedings of the 20th EUPVSEC*, Barcelona, Spain, 2005.
9   J. Libel, et al., "n-type Multicrystalline Silicon Solar Cells with BBr3-diffused Front Junction," *Proc. 31st IEEE Photovoltaic Specialists Conference*, Orlando, FL, 2005.
10 C. Schmiga, et al., "Solar Cells on n-type Silicon Materials with Screen-printed Rear Aluminium-p+ Emitter," *Proceedings of the 20th EUPVSEC*, Barcelona, Spain, 2005.
11 S. Martinuzzi, et al., "n-type Multicrystalline Silicon for Solar Cells," *Proceedings of the 20th EUPVSEC*, Barcelona, Spain, 2005.
12 M. Tanaka et al., "Development of HIT Solar Cells with More than 21% Conversion Efficiency and Commercialization of Highest Performance HIT Modules," *Proceedings of the Third WCPEC*, Osaka Japan, 2003, pp. 955-958.
13 W.P. Mulligan, et al., "Manufacture of Solar Cells with 21% Efficiency," *Proceedings of the 19th EUPVSEC*, Paris, France, 2004, pp. 387-390.
14 For example, the proceedings of this annual workshop.
15 S.J. Robinson, A.G. Aberle and M.A. Green, "Recombination saturation effects in silicon solar cells," *IEEE Transactions on Electron Devices*, ED-41(9), pp. 1556-1559, 1994
16 P.J. Cousins, C.B. Honsberg, A.B. Sproul and J.E. Cotter, "The effect of SRH on the fill factor of double sided buried contact solar cells," *Proceedings of the Australian and New Zealand Solar Energy Society Conference*, New Castle, 2002.
17 C.B. Honsberg et al., "High-efficiency, Low-cost Buried Contact Silicon Solar Cells," Proceedings of the 24th IEEE PVSC, Hawaii, 1994, p 1473-1476.
18 K.R. McIntosh, "Lumps, humps and bumps : three detrimental effects in the current-voltage curve of silicon solar cells," PhD Thesis, UNSW, 2001
19 P. J. Cousins and J. E. Cotter, "Misfit dislocations generated during non-ideal boron and phosphorus diffusion and their effect on high-efficiency silicon solar cells", 31st IEEE Photovoltaics Specialists Conference, Orlando, FL, January 2005.
20 J.H. Guo, "High Efficiency n-type Laser-grooved Buried Contact Silicon Solar Cells," PhD Thesis, University of New South Wales, 2004.
21 K.H. Yang, "An etch for delineation of defects in silicon," Journal of Electrochemical Society: Solid-State Science and Technology, 131(5), pp. 1140-1145, 1984.
22 J. Zhao, A. Wang and M.A. Green, "24.5% efficiency silicon PERT cells on MCZ substrates and 24.7% efficiency PERL cells on FZ substrates," Progress in Photovoltaics: Research and Applications Vol. 7, pp. 471-474, 1999.
23 P. J. Cousins, D. H. Neuhaus and J. E. Cotter, "Experimental verification of the effect of depletion-region modulation on photoconductance lifetime measurements", *Journal of Applied Physics*, 95(4), pp. 1854-1858, 2004.
24 A.G. Aberle, *Crystalline Silicon Solar Cells; Advanced Surface Passivation and Analysis*, Centre for Photovoltaic Engineering, University of New South Wales (Sydney, 1999)

Designs and Fabrication Technologies for Future Commercial Crystalline Si Solar Cells

Ajeet Rohatgi

University Center of Excellence for Photovoltaics Research and Education
School of Electrical and Computer Engineering
Georgia Institute of Technology, Atlanta, GA 30332-0250

ABSTRACT

The cost of photovoltaic (PV) systems is expected to decrease by a factor of two to four within the next two decades, making PV a very attractive and cost-effective solution to the energy and environmental problems. This cost reduction will happen by combination of economy of scales due to market expansion, smart integration of PV into residential and commercial buildings, and technical innovations leading to low-cost, high-performance solar cells. Since 1979, each doubling of cumulative PV module production has been accompanied by a 20% reduction in module price. Our calculations show that if this learning rate continues for the next two decades, the cost of PV module could reach the \$1.00/Wp target by 2015 at 40% annual growth, or by 2021 for 20% annual growth. Crystalline Si has been the champion of the PV industry and accounts for almost 95% of the PV modules produced today. Crystalline Si is primarily responsible for the greater than 30%/yr growth in PV in recent years, which reached almost 60% in 2004. In spite of competition and constant threat from other materials and technologies, Si has shown an uncanny ability to reinvent itself when challenged. We show that 20%-efficient Si cells from 100 μm thick Si wafers can reduce the direct manufacturing cost to \$0.62/W for a 500 MW$_p$ production line. Current production Si solar cell efficiencies range from 13 to 20% with the majority of the solar cells around 14-15% made by traditional screen-printing technology. Meanwhile, Interdigitated Back Contact (IBC) cells from SunPower and HIT cells from Sanyo are approaching the 20% efficiency level in production, which has increased the pressure and competition for higher efficiency manufacturable Si solar cells at a reasonable cost. This paper reviews some of the recent developments and outlines some approaches, cell designs, and process technologies that can lead to higher performance commercial crystalline Si solar cells.

1. <u>Model calculations to establish a roadmap for achieving 20% efficient commercial Si solar cells</u>

Figure 1 shows that 20%-efficient Si cells from 100 μm thick Si wafers can reduce the direct manufacturing cost to \$0.62/W, for a 500 MW$_p$ production line with wafers, cell, and module yields of 92, 95, and 98%, respectively. Even though laboratory scale Si solar cell efficiencies have reached 24.7%, the efficiency of most production cells is below 16%. Unfortunately, laboratory scale cells are too expensive and industrial cells are not efficient enough to meet the target of \$1.00/W$_p$ for PV modules as shown in Fig. 1. A detailed examination of the laboratory and industrial cells reveals that the efficiency gap
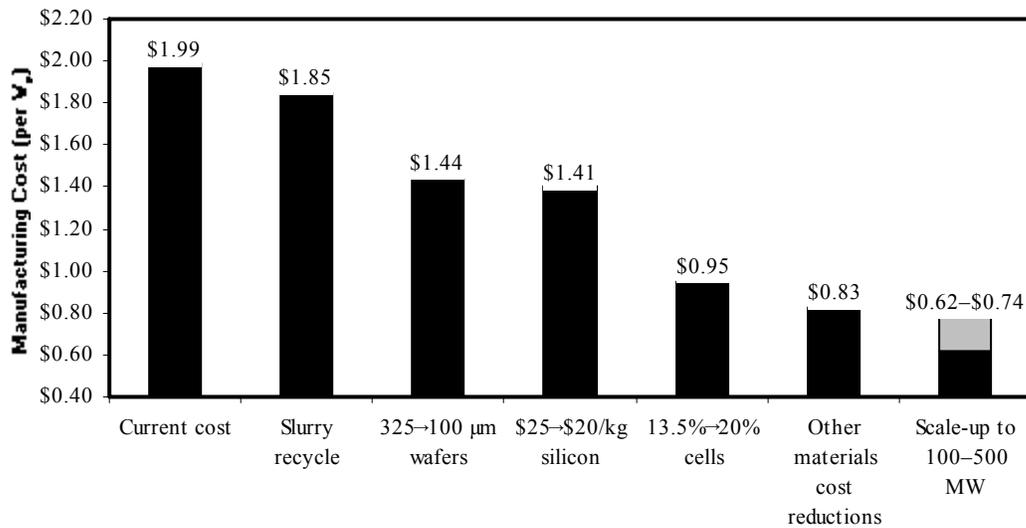
Fig. 1 Economic roadmap detailing how PV module manufacturing cost can be reduced to under $0.80/W with 20%-efficient 100 μm thick c-Si solar cells.

between the two is the result of the use of lower cost Si materials in production and the absence of (or lower quality) advanced design features such as 1) effective front and rear passivation, 2) effective light trapping via good front surface texturing and a back surface reflector, 3) reduced shading and contact recombination, 4) selective emitter formation, and 5) higher diffusion length to cell thickness ratio. In Fig. 2 we present model calculations in the form of a roadmap to demonstrate how we can raise the efficiency of a screen-printed production cells from 13.4 to 20%. Each bar in the roadmap represents the need for low-cost technology development that will be discussed in the remainder of this paper.
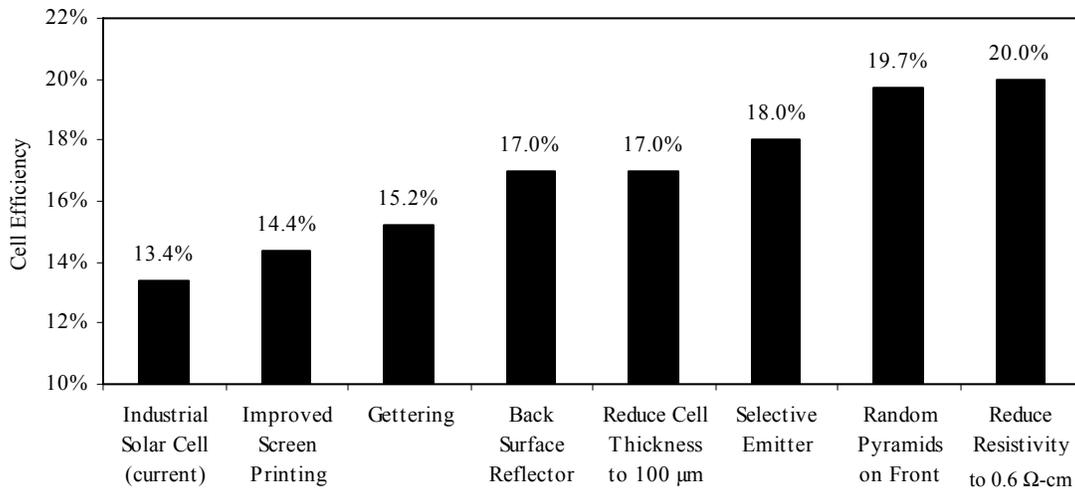
Fig. 2 Technology roadmap to achieve 20%-efficienct solar cells using a combination of manufacturable technologies.

2. Lifetime enhancement during cell processing

The calculations in Fig. 2 assume a uniform bulk lifetime of 100 µs, which is much higher than the as-grown lifetime in many of the PV grade Si materials, including Czochralski Si, cast mc-Si, and ribbon Si, used in production. Fortunately, most cell processes involve P diffusion, Al alloying and SiN antireflection (AR) coating, which are known to assist in impurity gettering and H passivation. However, the degree of lifetime enhancement is still highly process specific, even though there has been significant improvement in understanding and implementation of these techniques. Figure 3 shows the enhancement in bulk lifetime of PV grade Si materials during processing of screen-printed cells in our lab, which involved P diffused emitter, plasma-enhanced chemical vapor deposited (PECVD) SiN AR coating, Al-doped back surface field, and co-firing of screen-printed Ag and Al contacts. As expected, the

Fig. 3 Enhancement in bulk lifetime of PV grade Si materials through manufacturable gettering and passivation treatments at Georgia Tech.

impact of each process step on lifetime enhancement is material specific. However, most cases, we were able to achieve ≥100 µs lifetime. In general, cast mc-Si shows greater response to P diffusion gettering and Al alloying induced gettering because of the presence of metallic impurities such as Fe. Ribbon Si materials respond more favorably to SiN deposition and annealing induced H passivation of defects. In our study, we found

that several process-related modifications contributed to the final lifetime of ≥100 µs in most materials. These modifications include a) short NH_3 pretreatment in the PECVD reactor prior to SiN deposition, b) deposition of SiN at low-frequency (50 KHz) at ~430°C, c) rapid co-firing of screen-printed contacts, and d) rapid cooling of contacts after firing. NH_3 pretreatment and low-frequency SiN deposition provide an additional source of H for defect passivation in a thin Si region just below the SiN layer due to ion damage-induced adsorption of H atoms. Rapid firing enhances the degree of defect hydrogenation because of the competition between the

Fig. 4 Lifetime enhancement in EFG Si due to a short SiN-induced hydrogenation firing cycle in RTP.

13

supply of H to the defect and release of the H from defect during the firing process. Fourier Transform Infrared Spectroscopy measurements show that the release of H from SiN layer slows rapidly with firing time but the dehydrogenation from the defect continues at the same pace. Rapid cooling after the firing also improves hydrogenation for the same reason. Therefore, a shorter firing cycle is much more effective [Fig. 4]. Most cell processes should incorporate the above guidelines for lifetime enhancement. In the future, efforts should be made to investigate even shorter firing times, below 1 s, to determine if managing the competition between the supply and loss of H from the defect can give even further enhancement in lifetime.

3. Non Uniformity in Material Quality

Multicrystalline Si materials account for almost 60% of the PV modules produced today. However, both cast and ribbon Si wafers suffer from spatially inhomogeneous defect distributions that could have a detrimental effect on V_{oc} and cell performance. This effect is caused by diodes associated with high recombination regions or "bad regions" that act in parallel with good regions to reduce V_{oc}. Figure 5 shows an LBIC map of a 4 cm^2 String Ribbon Si solar cell where 38% of the device area has a very low lifetime ($\tau_1 <$ 5 μs) while the rest of the cell had a lifetime of $\tau_o \geq$ 100 μs. A companion cell on the same wafer with no detectable bad regions had a V_{oc} of 605 mV, as opposed to 578 mV for the cell in Fig. 5. Model calculations in Fig. 6, show that the area fraction of bad regions and their recombination strength R=(1- L_{eff1}/L_{eff0}) can account for this loss in V_{oc}. Figure 6 reveals that we need to reduce the area fraction of bad regions, with a recombination strength of ≤0.80, to <5% to avoid any appreciable loss in performance due to nonuniformity. Notice that R varies between 0 and 1, and a high R value corresponds to greater recombination activity in the bad region. Though gettering and passivation techniques have improved, they are not yet able to eliminate the loss due to inhomogeneity in many cells. Most studies suggest that the bad regions generally contain impurities precipitated at dislocation tangles after cell processing. There is a need to understand an improve defect engineering and defect management to prevent the formation of such regions.

Cell 1
V_{OC} = 616 mV
LBIC = 0.568 A/W

Cell 3
V_{OC} = 578 mV
LBIC = 0.454 A/W
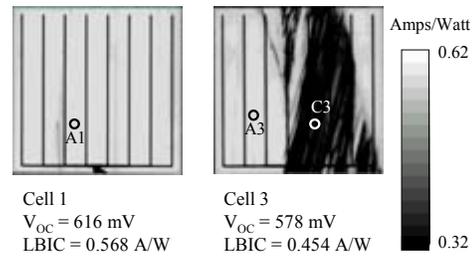
Fig. 5 LBIC maps of a 4 cm^2 String Ribbon Si solar cells (a) without and (b) with regions with high recombination activity that lower LBIC response and V_{oc}.
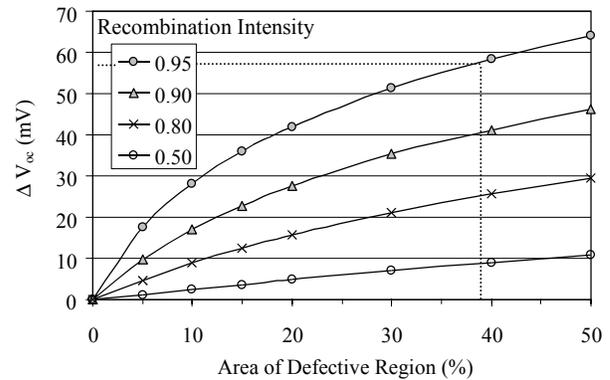
Fig. 6 Calculated loss in V_{oc} as a function of defective area with different recombination intensity.

Rapid thermal processing using intense light may be able to dissociate impurity precipitates and getter them out of the active bulk region if the thermal budget is appropriate. However, nonideal thermal processing can do more harm than good because dissociated metal impurities could end up in the bulk region rather than at the surfaces. The best way to alleviate this problem is to minimize impurity incorporation during crystal growth and cell processing.

4. Improved Back Surface Passivation and Light Trapping

Our roadmap for industrially feasible 20%-efficient cells in Fig. 2 calls for a BSRV of ≤200 cm/s and a BSR of > 95%. Most industrial solar cells today use full area screen-printed Al on the back, which forms an Al-BSF upon firing. However, this scheme produces a BSRV of ≥600 cm/s on 1 Ω-cm Si with a BSR value of ~65% [1], which is not sufficient for 18-20%-efficient cells. We have performed theoretical calculations that reveal that a 60 μm thick Al layer fired 875°C can produce an Al-BSF with a BSRV of 100 cm/s. We also have demonstrated that the combination screen-printing and RTP can lead to a uniform Al-BSF layer with BSRV values as low as 200 cm/s [2]. However, we have found experimentally that the conditions that should lead BRSV values of 100 cm/s cannot be achieved by screen-printing because of the formation of Al bubbles that are created by Al-Si melt agglomeration and significantly degrade the quality of the Al-BSF. Figure 7 shows an experimentally determined curve that maps the allowed combination of Al thickness and firing temperatures before the onset of bubble formation. In addition, an Al layer thickness of 60 μm will lead to significant warping of thin wafers (<200 μm), and is therefore not compatible with the roadmap in Fig. 2. Thus we must find an alternative to the full area Al rear contact.
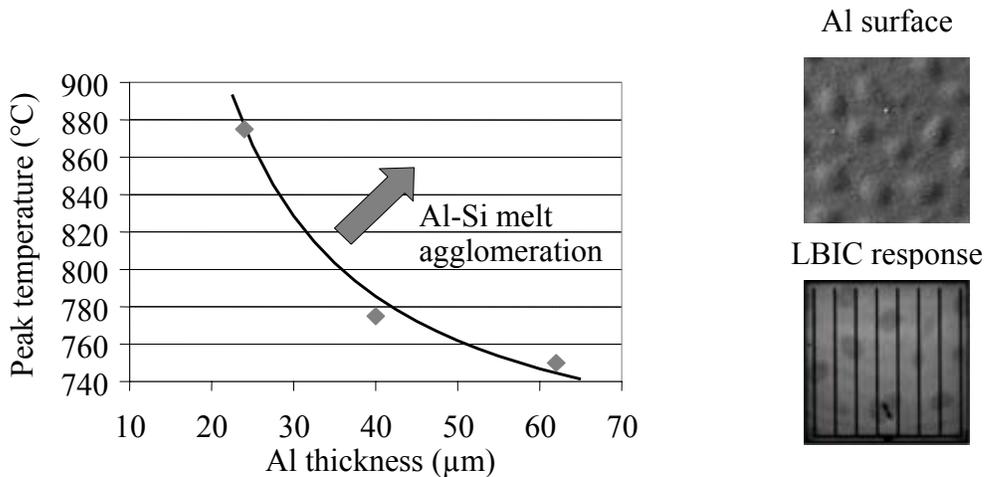
Fig. 7. Highest alloying temperature and corresponding Al thickness (measured after firing) where the agglomeration of Al-Si melt can be avoided. Images on the right show Al agglomerates protruding the Al surface and the effect of the Al agglomerates on LBIC response.

The Fraunhofer Institute for Solar Energy Systems (ISE) has conducted an excellent and comprehensive study of alternatives to the full Al-BSF [3] that includes dielectric

passivation with a local back surface field (LBSF, PERL) dielectric passivation with ohmic contacts (PERC), dielectric passivation with laser-fired contacts (LFC) and full area boron-BSF. Table 1 summarizes their results of BSRV and BSR values for various schemes that are superior to the screen-printed Al-BSF. Using PC1D and the BSR and BSRV values for LFC through a dielectric, cell efficiencies were calculated for 250 and 50 μm thick Si with a textured front surface. It was found that the Al-BSF would produce cell efficiencies below 20%, while the efficiency of LFC cells would

Table 1 Back surface recombination velocity (S_{back}) and back surface internal reflectance (R_{back}) for various back surface passivation schemes [3].

Structure	R_{back} (%)	S_{back} (cm/s)
LBSF (105 nm oxide)	94.5	60
LFC (105 nm oxide)	95.5	110
PERC (105 nm oxide)	95.0	200
Diffused B-BSF	71	430
Screen-printed Al-BSF	65	750
Evaporated Ohmic Al contact	83	10^7

exceed 20% for both thicknesses. This was also demonstrated experimentally by cell fabrication.

Even though the above results have been demonstrated in the laboratory, they are not yet being implemented in production because of some challenges associated with the LFC process and the preservation of the dielectric passivation during contact firing. The rear dielectric needs to satisfy three criteria: Si/dielectric interface quality should be excellent, it should remain unaffected by firing, and the dielectric stack should provide good BSR. Glunz et al. [4] have shown that a stack composed of SiO_2 (100 Å)/SiN (200 Å)/SiO_2 (500 Å) can satisfy these requirements. The 100 Å thin oxide provides effective surface passivation, the SiN layer prevents degradation of the passivation during firing (and may even enhance passivation), and the 500 Å oxide on top of the SiN and underneath an Al layer improves the reflectance of the stack above 90%. Figure 8 shows a potentially manufacturable process for a triple dielectric stack cell design with contact openings on the rear. The process sequence starts with PECVD deposition
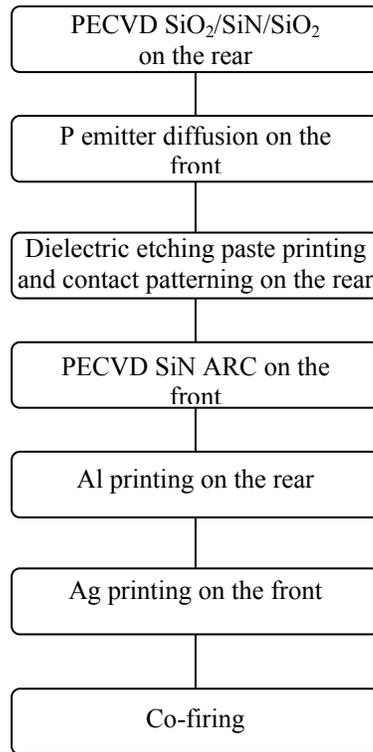
Fig. 8 Potentially manufacturable process for a triple dielectric stack cell with screen-printed contacts.

of the triple dielectric passivation of the stack on the rear followed by phosphorus diffusion. The stack prevents phosphorus diffusion on the backside and the nitride layer prevents degradation of the passivation quality. Holes are opened through the dielectric stack by deposition of a special screen-printed paste, which upon firing at 400°C dissolves the dielectric stack underneath the screen-printed pattern (Fig. 9(a)). The pattern can also be opened by laser scribing through the rear stack (Fig. 9(b)). The rest of the process is identical to conventional Si cells in which PECVD SiN is deposited on the

(a)   (b)
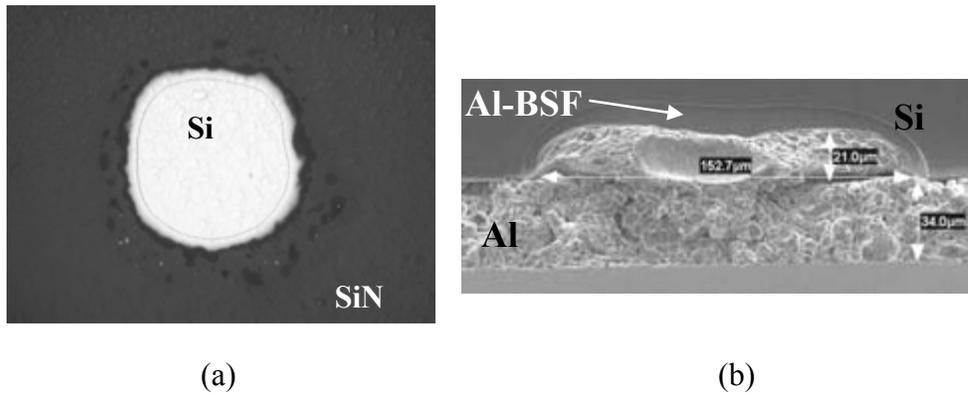
Fig. 9 Two technologies to open contact windows through dielectric layers (a) screen printing and baking a special dielectric etching paste, and (b) laser scribing through the dielectric and Si followed by screen printing and firing of Al.

front followed by screen-printing of the Ag grid on the front and full Al on the rear. Contacts are co-fired forming the local Al-BSF through the openings in the dielectric and an Al/dielectric stack/Si mirror in the remaining area. One needs to choose the appropriate Al paste (low frit content) that does not fire through the dielectric on the rear. Another fabrication approach to the above high efficiency cell designs involves plated contacts and screen-printing paste that can etch through the dielectric. In this case a unique diffusion call STAR [4] is used to achieve simultaneous diffusion of P on the front and B on the rear along with a high quality thin passivating oxide on both surfaces. The STAR diffusion can be followed by deposition of SiN on both sides and printing of the dielectric etching paste to open a grid pattern on the front and a pattern of points on the rear. Then Ni-Cu contacts can be plated.

5. Formation of Screen Printed Contacts to a High Sheet Resistance Emitter

Most commercial Si cells today are made with screen printed contact that force the emitter sheet resistance to be in the range of 30 to 60 Ω/sq in order to achieve FFs $\geq$ 0.75. However, the roadmap in Fig. 2 showed that we not only need to raise the emitter sheet resistance to the range of 80 to 100 Ω/sq. but also achieve FFs of ~0.78 to obtain 18-20% efficient cells. This is a challenging task because detailed analysis of the contact interface reveals that screen-printed contact technology does not produce a full area contact. Instead, the interface consists of randomly precipitated Ag crystallites embedded in the Si surface, and separated from the Ag grid by a glass layer. Carriers must tunnel through
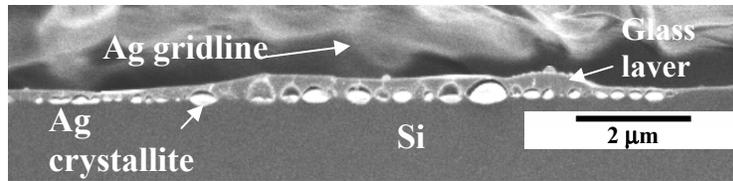
Fig. 10 Cross-sectional SEM micrograph of the screen printed showing small spherical Ag particles and a thin glass frit layer that give rise to high FFs on ~100 Ω/sq. emitters

this glass layer to be collected by the grid. Increasing the emitter sheet resistance is difficult because a low surface concentration increases the contact resistance between the Ag crystallites and the Si emitter. In addition, some Ag crystallites become large and may shunt or introduce junction leakage because of the shallow junction depth in lightly doped emitters. All of these factors tend to lower the FF and prevent the use of high sheet resistance emitters in commercial cells.

V_{OC} (mV)	643.2
J_{SC} (mA/cm^2)	37.78
FF	0.781
Eff. (%)	19.0
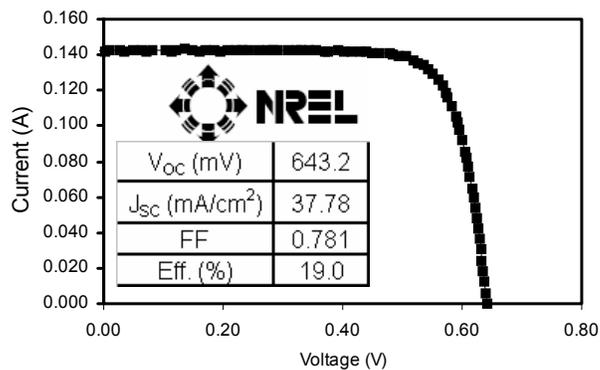
Fig. 11 I-V measurement by NREL for the 19.0% textured front and back 100-Ω/sq emitter cell on 0.6 Ω-cm float zone Si.

In an attempt to make good ohmic contact to high sheet resistance emitters, we investigated the impact of paste constituents on the contact interface. The objective was to identify the paste chemistry and firing combination that can produce a large number of small Ag crystallites in conjunction with a thin glass layer. Fig. 10 shows that small to medium size spherical Ag particles, a glass frit with a high glass transition temperature, and rapid firing tend to produce the contact interface that can give high FFs on ~100 Ω/sq. emitters. We also found that a rapidly crystallizing glass that solidifies just below the peak firing temperature also helps in obtaining the desirable interface. Figure 11 shows that we were able to achieve 19%-efficienct 4 cm^2 solar cells with FFs of ~0.78 on 0.6Ω-cm float zone Si using screen printed contacts on a ~100 Ω/sq. emitter. More research needs to be conducted on this topic to improve the reproducibility of high FFs on the high sheet resistance emitter and transfer the technology to large area devices. Recently, Tool et al [5] demonstrated a 17%-efficienct large area mc-Si solar cell with screen-printed contacts on an 80 Ω/sq. emitter.
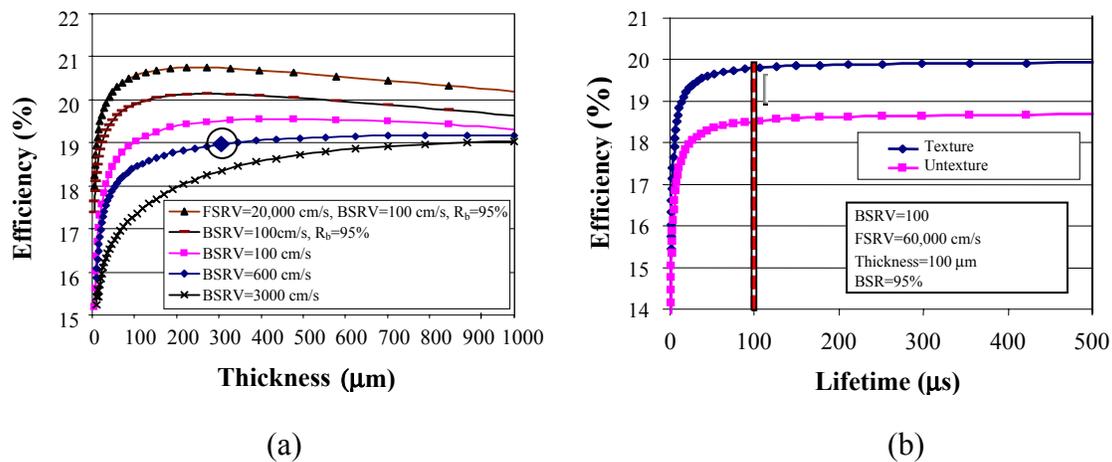
Fig. 12 Simulated curves of screen-printed solar cell efficiency plotted as a function of (a) base thickness and BSRV, and (b) bulk lifetime.

6. Cell Designs and Structures for ≥20%-efficient Commercial Si Solar Cells

In the previous sections we showed that we fabricated 4 cm^2 cells with screen-printed contacts and an efficiency of 19% on 0.6 Ω-cm float zone Si using a high sheet resistance emitter and 4.5% grid shading. The process sequence involved 90-100 Ω/sq. emitter diffusion, single layer SiN deposition on the textured emitter surface by PECVD, screen printing of the Ag on the front and full area coverage of Al on the rear followed by rapid co-firing in a belt furnace and a 400°C forming gas anneal. In the remainder of this section, the 19%-efficient cell will be used as a launching pad to illustrate the cell designs and technologies that can lead to ≥20%-efficient commercial Si cells. Detailed analysis of this cell showed that improvement of the BSR of 65% and the BSRV of 600 cm/s would lead to significant performance enhancement. Figure 12 (a) and (b) show PC1D calculations and cell designs that can lead to ≥20%-efficient simple and manufacturable Si cells. In Fig. 12 (a), cell efficiency is plotted as a function of base thickness and BSRV, and the 19%-efficent cell is marked by an open circle. The calculations reveal that
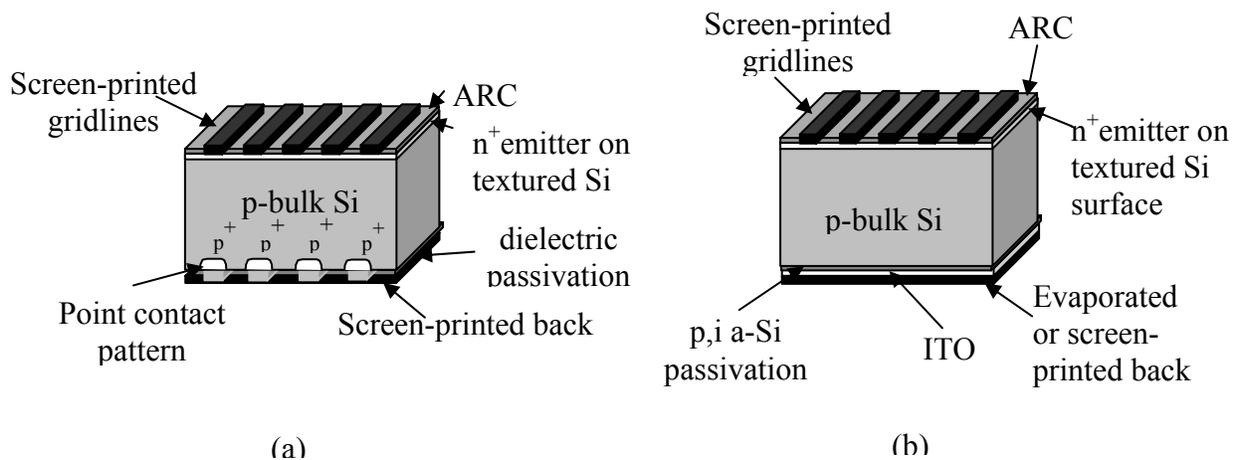
Fig. 13 Schematic of cell designs that can reduce BSRV and increase BSR to produce ≥20%-efficient screen-printed cells with (a) dielectric passivation and a local Al-BSF, and (b) a p,i stack of a-Si with ITO and an evaporated or screen-printed metal back contact.

19

if we can simply reduce the BSRV to 100 cm/s, cell efficiency can approach 19.5%, and if the BSR value can be increased to 95% the efficiency can exceed 20%. It is also interesting to note that for 0.6 Ω-cm float zone Si with a bulk lifetime of 250 μs, efficiency becomes relatively insensitive to thickness in the range of 100 to 300 μm. Thus a reduction of the cell thickness by a factor of three can be tolerated without any loss in cell performance, resulting in a substantial cost reduction. Figure 13 shows a schematic of two cell designs that can produce $\geq$20%-efficient screen-printed cells. These cell designs are composed of the front portion of our 19%-efficienct cell with the back contact altered to give BSRV values below 200 cm/s. One scheme (Fig. 13 (a)) involves a dielectric stack with point contact openings, capped with screen printed Al as pointed out is Section 4. The second approach (Fig. 13 (b)) involves deposition of 10-20 nm of p and i a-Si layers on the back, capped with conductive ITO and an evaporated or screen-printed metal paste that can be fired at low temperature. This technology has been shown to produce BSRV values $\leq$125 cm/s [6]. Model calculations in Fig. 12(b) show that if a lower quality Si material (τ=100 μs as shown in Fig. 3) is used instead of FZ Si, cell efficiencies will decreases only somewhat because the thin cell has a high BSR value (95%) and a low BSRV value (100 cm/s). However, if the material cannot be textured, the efficiency could decrease to ~18.5% with this technology.

7. Simplified Interdigitated Back Contact Structures

The IBC cell concept has been around for several decades. This cell design offers many advantages over conventional cells including elimination of shading losses, reduced heavy doping effects, high metal coverage on the rear to reduce series resistance, reduced front surface recombination velocity, simple co-planar interconnects, and the use of thin wafers. There are three basic IBC configurations: front dielectric passivated (FDP), front floating junction (FFJ), and front surface field (FSF). Significant progress has been reported in this area. Ohtsuka et al. [7] reported a simulated efficiency limit of 24.3% for FDP-IBC cells while SunPower recently produced 22.5%-efficient FSF-IBC cells on 160 μm-thick FZ Si. The processing sequence to achieve this cell design involves three high temperature steps including B diffusion, P diffusion, and thermal oxidation, along with low-cost patterning of contacts and possibly metal plating. In this process, the use of thin wafers and the large number processing steps can lead to yield problems.
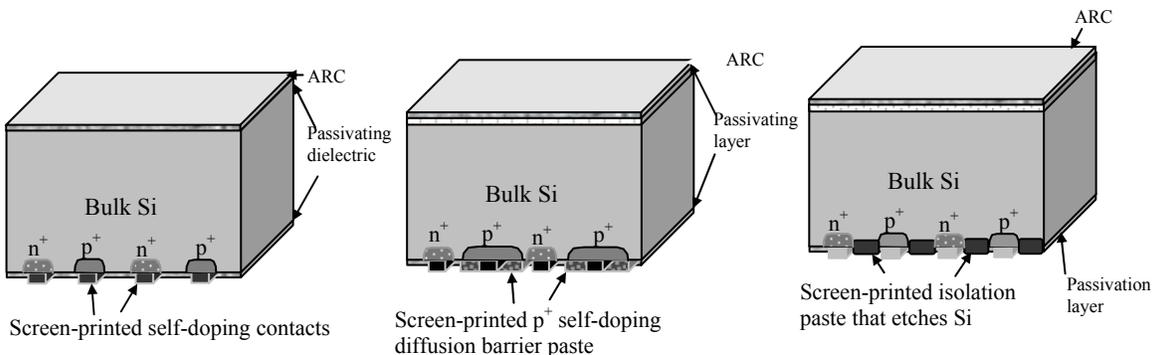
Figure 14 Three simplified IBC cell designs that can be achieved using low-cost technologies if appropriate screen printing pastes are developed.

Efforts to produce IBC cells using very low cost processing have not yet succeeded but should be continued.

Figure 14 shows three simplified IBC cell designs that can be achieved using low-cost technologies. Screen printed self doping Ag and Al pastes can be printed in an interdigitated manner and fired through an oxide/nitride dielectric on the rear, while the front oxide passivation is protected by oxide/nitride stack [3]. This technology requires further development of phosphorus self-doping Ag paste to achieve sufficient phosphorus doping using fritted Ag paste and normal firing times and temperatures. The second low-cost approach to IBC cells involves using a boron self doping phosphorus diffusion barrier. In this case the diffusion barrier is printed first followed by a phosphorus diffusion step during which boron is diffused underneath the barrier [8]. Then the passivating dielectrics can be deposited on both sides after removing the diffusion glass. Finally Ag and Al pastes are screen-printed interdigitatively and fired through the dielectric so that Ag makes contact to the n^+ region and Al punches through the diffusion barrier and the passivating dielectric to contact the p^+-region. The third approach to low-cost IBC cells involves using a screen printable paste that can etch the dielectric and the underlying silicon wafer. In this approach, phosphorus diffusion is performed first on both sides of the wafer. Then the Si etching paste is used to etch regions between the n^+ and p^+ and the passivating dielectric is deposited on both sides. After that, Ag and Al gridlines are printed interdigitatively and fired through the dielectric to form p+ regions and ohmic contacts simultaneously.

Figure 15 shows an IBC structure using a-Si layers on crystalline Si (HIT technology). In this structure the front surface is coated with intrinsic a-Si and a SiN AR coating. On the back surface, the intrinsic a-Si is deposited first, followed by interdigitated depositions of n and p –Si layers that are isolated from each other. Contacts to the a-Si n and p layers are made by deposition of ITO and screen-printed metal contacts.
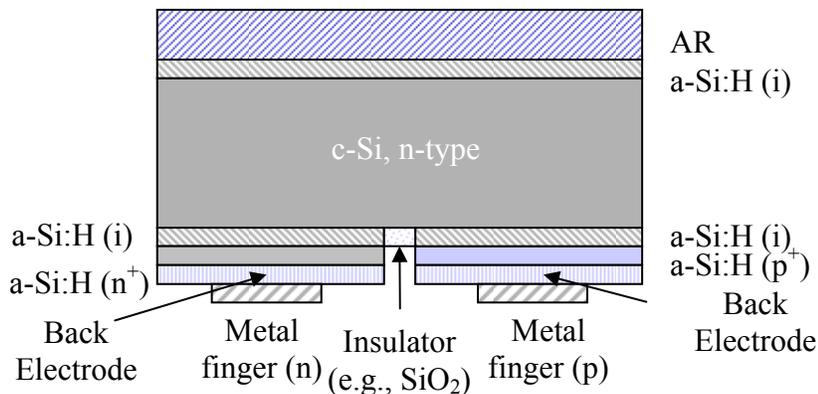
Fig. 15 IBC structure using a-Si layers for heterojunctions and surface passivation on crystalline Si (HIT technology).

7. Conclusions

Greater than 20%-efficient cells from Sanyo and SunPower have ignited the race for high-efficiency cells. However the challenge is how to get to high-efficiency cells with high manufacturing yield. This paper reviews some of the recent progress in commercial Si solar cell technologies that can contribute to high-efficiency Si cells. Model calculations were performed to establish the requirements for material and device parameters that can lead to high-efficiency cells. These calculations suggest that we should make a long-term target of 20%-efficient Si cells on 100 μm thick Si using low-cost technologies. This will require a bulk lifetime of ≥100 μs, efficient light trapping, excellent back surface passivation, and good quality contacts. Selected solar cell designs and low-cost technologies were discussed that have the potential for 100 μm thick 20%-effient cells, and approaches and process sequences are discussed that can reach this target at low cost. Some of the outlined approaches involve the development of novel screen-printing pastes, the use of HIT type structures involving the combinations of a-Si and c-Si, dielectric surface passivation, and low-cost IBC structures. Based on the recent success in each of these areas, it is very likely that some combination of advanced design features attained by low-cost technologies will lead to cost-effective Si PV in the near future.

Acknowledgement

8. References

[1] M. Hilali, et al. "High-efficiency (19%) screen-printed textured cells on float-zone silicon with high sheet-resistance emitters," submitted to Appl. Phys. Lett**.**

[2] S. Narasimha and A. Rohatgi, "Optimized aluminum back surface field techniques for silicon solar cells", in *Proc. of 26th IEEE PVSC.*, 1997, pp. 63-66.

[3] S.W. Glunz et al. "Comparison of different dielectric passivation layers for application in industrially feasible high-efficiency crystalline silicon solar cells," *Presented at the 20th E-PVSEC*, 2005.

[4] T. Krygrowski, et al., "A novel processing technology for high-efficiency silicon solar cells," J. Electroch. Soc. 146, (1999) pp. 1141-1146.

[5] C.J. Tool et al., "17% mc-Si solar cell efficiency using full in-line processing with improved texturing and screen-printed contacts on high-ohmic emitters," *Presented at the 20th E-PVSEC*, 2005.

[6] M. Schaper et al., "20.1%-efficient crystalline silicon solar cell with amorphous silicon rear-surface passivation," *Prog. Photovolt: Res. Appl.* **13**, (2005) pp. 381–386.

[7] H. Ohtsuka, et al. "Three-dimensional numerical analysis of contact geometry in back-contact solar cells" *Prog. Photovolt: Res. Appl.* 2, (1994) pp. 275–285.

[8] P. Hacke, et al. "Application of a boron source diffusion barrier for the fabrication of back contact silicon solar cells," in *Proc. of 31st IEEE PVSC.,* 2005, pp. 1181-1184.

Atomic Structure and Electronic Properties of c-Si/a-Si:H Interfaces in Silicon Heterojunction Solar Cells

Yanfa Yan, Q. Wang, M. Page, E. Iwaniczko, D. Levi, M.M. Al-Jassim, Howard. M. Branz, and T.H. Wang

National Renewable Energy Laboratory, Golden, CO 80401

Abstract

The atomic structure and electronic properties of c-Si/a-Si:H interfaces in Si heterojunction (SHJ) solar cells are investigated by high-resolution transmission electron microscopy (HRTEM), atomic-resolution Z-contrast imaging, and electron energy loss spectroscopy (EELS). Atomically abrupt and flat c-Si/a-Si:H interfaces are found in all high-performance SHJ devices. These atomically abrupt and flat c-Si/a-Si:H interfaces can be realized by two approaches. At a substrate temperature below 150°C, the hydrogenated amorphous Silicon (a-Si:H) layer can be grown by hot-wire chemical vapor deposition (HWCVD) from pure silane. Alternatively, at a higher substrate temperature of 200°C the c-Si substrate can be treated by H-diluted NH_3 and then followed by H_2 etching, prior to the a-Si:H deposition.

Introduction

SHJ solar cells have attracted great attention since the report of high performance of Sanyo's HIT cells [1]. The superior performance of the SHJ structure is believed to be the results of the excellent passivation of c-Si surface by the a-Si:H layer, which is used both as the front junction emitter, and as a full contact back-surface-field (BSF). Surface passivation of c-Si is a critical process for many applications, especially high-efficiency silicon solar cells. The surface states often act as recombination centers for the charge carriers. The reduction of excess carrier loss at the c-Si surface, a key feature of an SHJ solar cell, is one of the critical issues to improve the device performances [2]. Thin films of a-Si:H are widely used for thin-film photovoltaics [3] and many other applications. It has a higher H content and bigger bandgap than c-Si. These make it a promising candidate for surface passivation of c-Si and capable of replacing traditional dielectrics such as SiO_2 and Si_3N_4. Sanyo's HIT structure has demonstrated the excellent passivation capability of a-Si:H, as well as good carrier transport ability. However, it has been challenging for other group to obtain high performance of heterojunction solar cells with either plasma enhanced chemical vapor deposition (PECVD) or HWCVD. We believe that this is because direct deposition of a-Si:H on a hydrophobic c-Si surface can lead to a mixed phase or epitaxial Si growth with some degree of structural defects [4].

Recently, NREL has achieved high-performance SHJ solar cells by HWCVD. The a-Si:H layers have been obtained by two different approaches. The first is that the a-Si layer is directly deposited by HWCVD at a low substrate temperature, i.e., lower than 150°C. The second is that the c-Si substrate is treated by H-diluted NH_3, prior to the a-Si deposition at a relatively higher substrate temperature, 200°C. The first approach has produced SHJ device efficiency of 16.9% with a high V_{oc} of 652 mV on a planar p-type

float-zone (FZ) silicon substrates with an HWCVD a-Si:H(n) emitter and screen-printed Al as the BSF back contact. It has also produced a V_{oc} of 691 mV for a double-heterojunction SHJ on a planar n-type FZ-Si substrate with HWCVD a-Si:H as both the emitter and the BSF back contact [5]. The second approach has yielded an efficiency of 13.4% on a non-textured single-sided heterojunction solar cell on a p-type Czochralski (CZ) Si with an Al-BSF.

In this paper, we investigate the atomic structure and the electronic properties of the c-Si/a-Si:H interfaces in these SHJ solar cells by HRTEM, atomic-resolution Z-contrast imaging, and EELS. We find that all the high-performance SHJ devices grown by either approach exhibit an abrupt and atomically flat c-Si/a-Si:H interface.

Experimental

The a-Si:H layers were grown by the HWCVD technique from pure silane, as described elsewhere [6]. Because the undoped intrinsic a-Si:H layers normally have a far lower density of defects and a slightly larger energy gap than doped a-Si:H layers, the undoped intrinsic a-Si:H is believed to provide better pasivation effects than doped a-Si:H. Therefore, the NREL SHJ solar cells contain a thin (~5 nm) intrinsic a-Si:H layer, which is generally interposed between the base wafer and the heavily doped emitter. Details of the NREL device fabrication process are described elsewhere [7-9]. TEM samples were prepared by cleaving the SHJ devices. HRTEM, atomic Z-contrast images, and EELS were taken in a Tecnai TF20-UT microscope equipped with a Gatan Image Filtering (GIF) system, operated at 200 kV. The Z-contrast images were formed by scanning a 1.36-Å probe across a specimen and recording the transmitted high-angle scattering with an annular detector (inner angle ~45 mrad). The image intensity can be described approximately as a convolution between the electron probe and an object function. Thus, the Z-contrast image gives a directly interpretable, atomic resolution map of the columnar scattering cross-section in which the resolution is limited by the size of the electron probe [10,11].

Results and Discussion
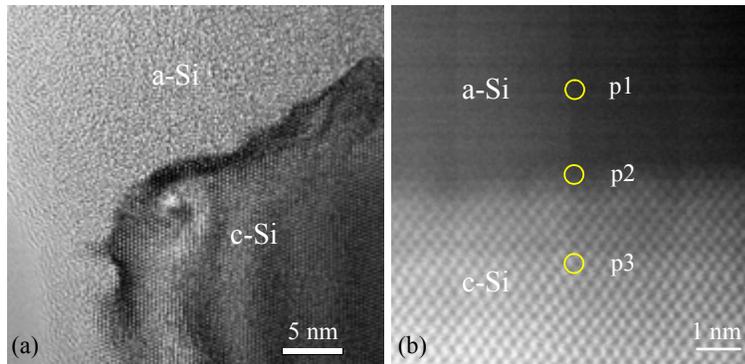
FIG. 1. (a) HRTEM image and (b) Z-contrast image of the front c-Si/a-Si:H interface in a double-heterojunction SHJ solar cell.

We first report the results obtained from the device with an a-Si:H layer grown without surface pretreatment by HWCVD at below 150°C. Figures 1(a) and 1(b) show a HRTEM image and a Z-contrast image of the front (100)c-Si/a-Si:H interface in a double-heterojunction SHJ solar cell with a high V_{oc} of 680 mV. The electron beam is along the [110] zone axis. The intrinsic and doped a-Si layers are not distinguishable in the images. Each bright spot in the Z-contrast image shown in Fig. 1(b) directly represents two closely spaced Si columns. The images reveal that the interface is abrupt and flat. To understand the electronic structure change across the interface, EELS spectra were taken at different points around the interface.
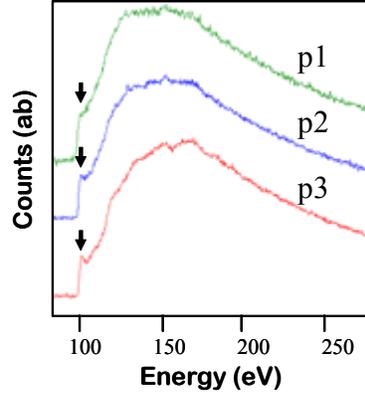
FIG. 2. Si-L edges spectra taken from different points around the c-Si/a-Si:H interface shown in Fig. 1(b).

Figure 2 shows the Si-L edges spectra taken from three points indicated as p1, p2, and p3 in Fig. 1(b). Point 1 is inside the a-Si:H layer, point 2 is at the interface, and point 3 is inside the c-Si. It is seen that the intensity of the first peak (as indicated by black arrows) is reduced as the electron beam is moved from the c-Si area to the interface. It is further reduced when the electron beam is moved into the a-Si:H layer. The Si-L edges spectra represent the transition from the Si $2p$ band to the conduction band. The intensity reduction of the first peak indicates that the density of states is reduced around the minimum of the conduction band. The reduction at the interface and in the a-Si is likely caused by the disorder. Thus, the intensity of this peak tells us the quality of the a-Si:H layer, i.e., the lower the intensity, the more disorder, i.e., the better a-Si. The EELS spectra shown in Fig. 2 indicate that a high quality a-Si:H layer is achieved.
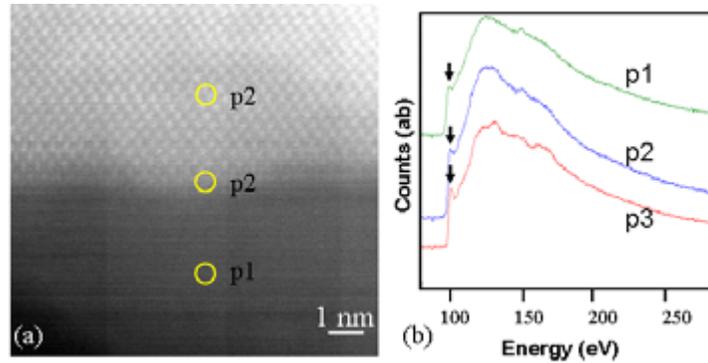
FIG. 3. (a) Z-contrast of the back c-Si/a-Si:H interface in a double-heterojunction SHJ solar cell and (b) Si-L edges spectra taken at three different points around the interface.

In Fig. 3(a), we show a Z-contrast of the back c-Si/a-Si:H interface in a double-hetero junction SHJ solar cell. It reveals that the c-Si/a-Si:H interface at the back side is also abrupt and flat. Figure 3(b) shows the Si-L edges spectra taken at three different points around the interface. Point 1 is inside the a-Si:H layer, point 2 is at the interface, and point 3 is inside the c-Si. It is seen again that the intensity of the first peak, as indicated by black arrows, is reduced as the electron beam is moved from the c-Si area to the interface. However, the intensity reduction in the a-Si:H area is not as great as that in Fig. 2. This might suggest some residual ordering in the a-Si:H layer, which should be removed to improve the quality of this a-Si:H layer.
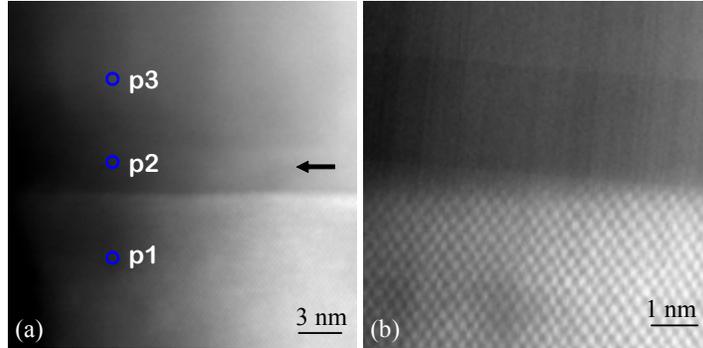
FIG. 4. (a) lower magnification and (b) higher magnification Z-contrast images of c-Si/s-Si:H interface in a NH_3 treated device.
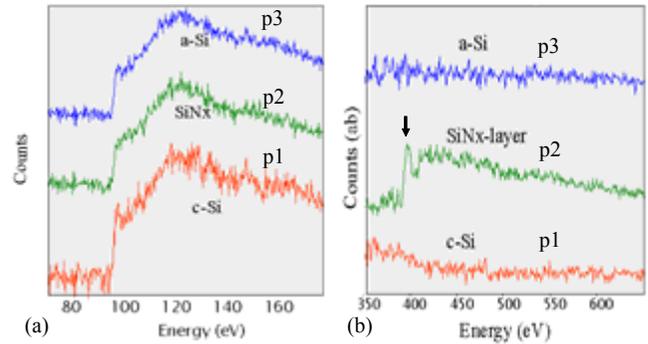
FIG. 5. (a) Si-L edges and (b) N-K edges spectra taken at three different points around the interface, shown in Fig. 4(a).

We now report the results obtained from devices with a-Si:H layers grown at higher temperature (200°C) after the c-Si substrates were treated by H-diluted NH_3. We used a tantalum 0.5-mm-diameter wires heated to about 2000°C by an ac power supply. Surface treatment was performed by introducing H-diluted NH_3 gases with the hot filament on. A p-type c-Si wafer of (100) orientation was used for the cell process. Figures 4(a) and 4(b) show a lower magnification and a higher magnification Z-contrast image, respectively, of the c-Si/s-Si:H interface in a NH_3 treated device. Figure 4(a) reveals clearly that there is an inter-layer with a thickness of about 3 nm lying in between the c-Si and a-Si:H. We found that this layer is SiN_x. To obtain the chemical composition and electronic information around the interface, Si-L edges and N-K edges spectra were taken at different points around the interface. Figures 5(a) and 5(b) show the Si-L edges and N-K

edges spectra taken at three points around the interface. The N-K edge peak is only seen at the inter-layer, indicating that the NH_3 treatment produces an amorphous SiN_x layer. This amorphous layer prevents epitaxy and ensures the deposition of a-Si:H at 200°C by HWCVD.

Though the SiN_x layer formed by NH_3 treatment ensures the abrupt growth of a-Si:H, this layer itself is harmful to device performance because it is highly resistive. The existence of this SiN_x layer often leads to low short-circuit current (Jsc) and fill factor (FF). We find that this layer can be thinned by H_2 etching immediately after the NH_3 treatment. With optimized etching time, this layer can be thinned down to about one monolayer, but this amount is still enough to ensure the growth of a-Si:H on the wafer.
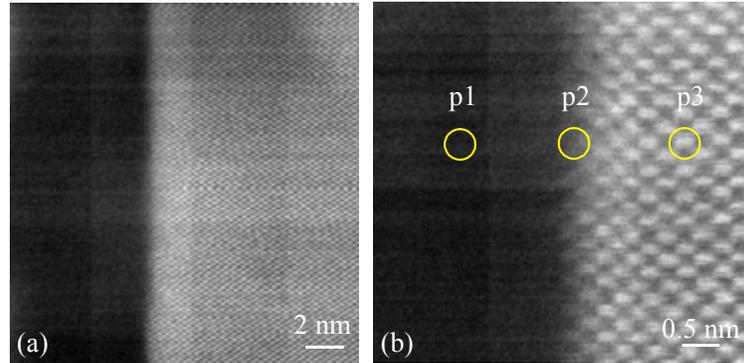
FIG. 6. (a) Lower and (b) higher magnification Z-contrast images of c-Si/a-Si:H interface from a device by NH_3 treatment, followed by 50 second H_2 etching.
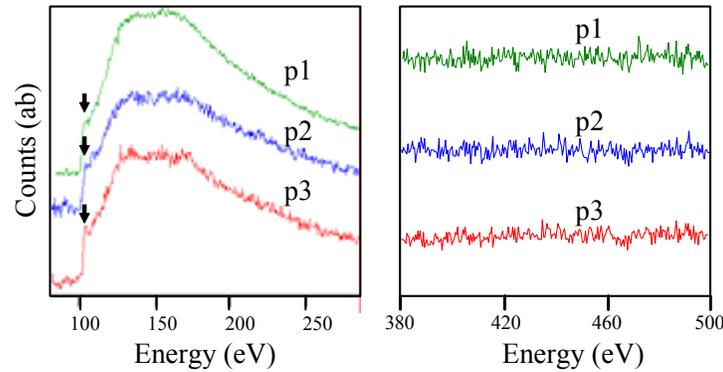
FIG. 7. Si-L edge and (b) N-K edge spectra taken at three different points around the interface, shown in Fig. 6(b).

Figures 6(a) and 6(b) show a lower- and higher-magnification Z-contrast image of the c-Si/s-Si:H interfaces, respectively, with the c-Si surface pretreated by H-diluted NH_3 and followed by 50 second H_2 etching before a-Si:H deposition. Fiure. 6(a) reveals clearly that the inter-layer is no longer visible. The high-magnification Z-contrast image in Fig. 6(b) reveals that the c-Si/s-Si:H interface is atomically abrupt and flat. To obtain the chemical composition and electronic information around the interface, Si-L edges and N-K edges spectra were taken at different points around the interface. Figures 7(a) and 7(b) show the Si-L edge and N-K edge spectra taken at three points around the interface. The

N-K edge peak is no longer seen at any position. This confirms that the SiN$_x$ layer has successfully thinned down to our detection limit.   However, the ability to grow a-Si:H abruptly on the wafer is still maintained. The Si-L edge spectra also show that high quality of the a-Si:H is also achieved with this higher temperature if pretreatment is used.

Summary

We have investigated the atomic structure and electronic properties of c-Si/a-Si:H interfaces in Si SHJ solar cells by HRTEM, atomic-resolution Z-contrast imaging, and EELS. The a-Si:H layers were grown by two approaches. In the first the a-Si:H layer is grown by HWCVD at a low substrate temperature, i.e., lower than 150°C. In the second the c-Si substrate is treated by H-diluted NH$_3$ and then followed by H$_2$ etching, prior to the a-Si deposition at a relatively higher substrate temperature, 200°C. We found that atomically abrupt and flat c-Si/a-Si interfaces were achieved using both approaches.

Acknowledgements

References

[1] M. Taguchi, K. Kawamoto, S. Tsuge, T. Baba, H. Sa-kata, M. Morizane, K. Uchihashi, N. Nakamura, S. Kiyama, and O. Oota, *Prog. Photovolt: Res. Appl*. **8,** 2000, pp. 503-513.
[2] T. Wang, Q. Wang, M. Page, and T. Ciszek, Thin Solid Films, **430**, 261 (2003).
[3] J. Yang and S. Guha, Mat. Res. Soc. Proc, **557**, 239 (1999).
[4] T. H. Wang, Q. Wang, E. Iwaniczko, M. R. Page, D. H. Levi, Y. Yan, C. W. Teplin, X. Z. Wu, and H. M. Branz, in *Proceedings of the 19th EUPVSEC Conference,* Paris, France 2004), to be published, (2004).
[5] T.H. Wang, M.R. Page, E. Iwaniczko, Y. Xu, Q. Wang, Y. Yan, D. Levi, V. Yelundur*, L. Roybal, R. Bauer, A. Rohatgi, H.M. Branz, in this proceedings
[6] Jian Hu, Howard M. Branz, Richard S. Crandall, Scott Ward and Qi Wang, Thin Solid Film, **430**, 249 (2003).
[7] M.R. Page, E. Iwaniczko, Q. Wang, D.H. Levi, Y. Yan, H.M. Branz, V. Yelundur, A. Rohatgi, and T.H. Wang, *14th Workshop on Crystalline Silicon Solar Cells and Modules,* Winter Park, CO, August 8-11, 2004; NREL/BK-520-36622, pp. 246-249.
[8] T.H. Wang, E. Iwaniczko, M.R. Page, D.H. Levi, Y. Yan, H.M. Branz, and Q. Wang, V. Yelundur and A. Rohatgi, 31st IEEE Photovoltaics Specialists Conference and Exhibition Lake Buena Vista, Florida January 3–7, 2005.
[9] Q. Wang, M. Page, Y. Yan, and T. Wang, 31st IEEE Photovoltaics Specialists Conference and Exhibition Lake Buena Vista, Florida January 3–7, 2005.
[10] S.J. Pennycook and D.E. Jesson, Phys. Rev. Lett., **64**, 938; (1990).
[11] S.J. Pennycook and P.D. Nellist, J. Microsc. **190**, 159 (1998).

Design and Operational Considerations for
Crystalline Silicon PV Modules

Adrianne Kimber
Powerlight
2954 San Pablo Ave.
Berkeley, CA 94702

ABSTRACT

The presentation will describe issues and concerns for crystalline silicon PV cells and modules from the systems design, manufacturing and operations perspective. Some background will be given on PowerLight, our requirements for module qualification and testing in the design phase, and our experience in maintaining and tracking the performance of fielded modules. The talk will focus on current module issues that impact our business, including module construction and ratings and recent reliability issues encountered in the field.

Modeling CZ Crystal Growth and Casting Process for Solar Cells

Koichi KAKIMOTO, Lijun LIU and Satoshi NAKANO

Research Institute for Applied Mechanics, Kyushu University
6-1, Kasuga-Koen, Kasuga 816-8580, JAPAN

Abstract

This paper reports three-dimensional calculation of a Czochralski furnace and transient phenomena of casting process of silicon for solar cells. The three-dimensional calculation predicted the temperature distribution in the furnace with transverse magnetic fields, which affects distribution of voids, which is formed by aggregation of vacancies. The calculation regarding the solar cells predicted temperature distribution, interface shape and flow velocity in the melt as a function of time of solidification. Moreover, iron distribution in the crystal was able to calculate by using transient calculation of solidification. Distribution of iron in silicon crystal is determined by solidification process, which includes segregation process, and diffusion process after solidification.

1. Introduction

The CZ growth method has for several decades been the most widely used technique for growing high-quality bulk crystals of silicon. The thermal field in and the oxygen incorporated into a grown crystal, the melt-crystal interface and the melt flow motion in the crucible have significant effects on the formation of micro-defects and crystal quality in a CZ growth process. It is therefore important to elucidate and control the heat, mass and oxygen transfers, as well as the melt-crystal interface shape, in a CZ growth furnace. With the increasing capacity of modern computer and computation technology, application of numerical simulation has become an effective and essential tool for analysis and design optimization of a CZ growth system to improve silicon crystal quality. On the other hand, different configurations of magnetic field were investigated and applied as an effective method to control the heat, mass and oxygen transfers in a CZ growth[1-7].

Over the past two decades, there have been many works on numerical analyses of CZ crystal growth processes using various models[8-17]. Most of these models can be generally divided into two types: local models[8-11] and 2D global models[12-15]. However, actually, since all constituents of a CZ furnace are closely related to each other through different forms of heat transfer by melt convection, solid conduction and thermal radiation, the CZ growth furnace is a highly nonlinear and strongly conjugated thermal system. Knowledge of heat transport throughout the entire furnace is thus required. On the other hand, the melt flow in a crucible and, hence, the thermal field within the growth furnace are principally three-dimensional, especially in cases under the influence of any

asymmetric external fields, such as in a TMCZ configuration. Therefore, 3D global analysis of a CZ growth system is necessary for a better understanding of realistic phenomena and insight physics of the growth process and, hence, for process improvement. A coupled 2D/3D model[16, 17)] was developed in recent years to solve these problems. In this kind of models, a local 3D analysis is carried out with thermal boundary conditions obtained from a quasi-2D global modeling. Obviously, the 3D effects of the thermal system, especially the 3D melt flow, can not be taken into account in the quasi-2D global modeling, and the thermal boundary conditions for the 3D local analysis can only be given in 2D. Furthermore, how to give the thermal boundary conditions for the 3D local analysis from the solution of a quasi-2D global modeling still remains a problem under discussion, since it was found[16)] that the type of thermal boundary conditions (fixed temperature or heat flux) has a strong influence on the 3D results of the interface shape and on the melt convection in a crucible.

Liu and Kakimoto[18)] recently proposed a 3D global model that makes 3D global modeling feasible with moderate requirements of computer resources and computation time. All convective and conductive heat transfers, radiative heat exchanges between diffuse surfaces and the Navier-Stokes equations for the melt phase are all coupled and solved together with a finite volume method in a 3D way. All the above-mentioned difficulties in the existing models are thus solved. In this paper, the validation of the model was demonstrated. Some results obtained most recently using this 3D global model were reported for a silicon TMCZ growth configuration.

Liu and Kakimoto also developed static and dynamic codes of casting process for silicon solar cells. This code can calculate solid-liquid interface shape, impurity distribution in both crystal and the melt during solidification by changing heater power imposed.
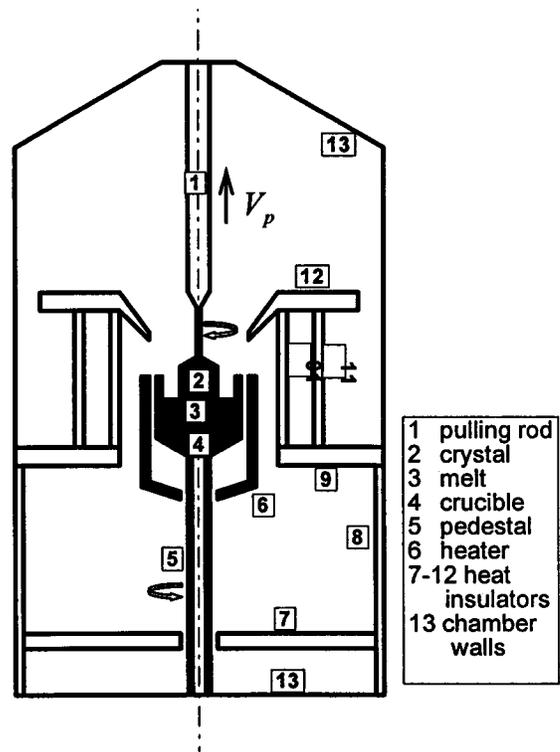
Fig. 1 Configuration and domain partition of a typical Czochralski growth furnace: 3D domain (gray) and 2D domain (open).

31

2. Model description and governing equations under influence of a magnetic field

The configuration of a small CZ furnace that was investigated in this study is illustrated in Fig. 1. The growth process is assumed to be quasi-steady. All of the constituents of the furnace are subdivided into a set of block regions as shown in the figure. Each block region is covered by a structured grid. In order to perform 3D global modeling with moderate requirements of computer memory and computation time, a mixed 2D/3D finite volume scheme was developed[18]. Following this scheme, the components in the core region of the furnace, namely, the 3D domain, are discretized in a three-dimensional way. The domains away from the core region, namely, the 2D domain, are discretized in a two-dimensional way. In Fig. 1,
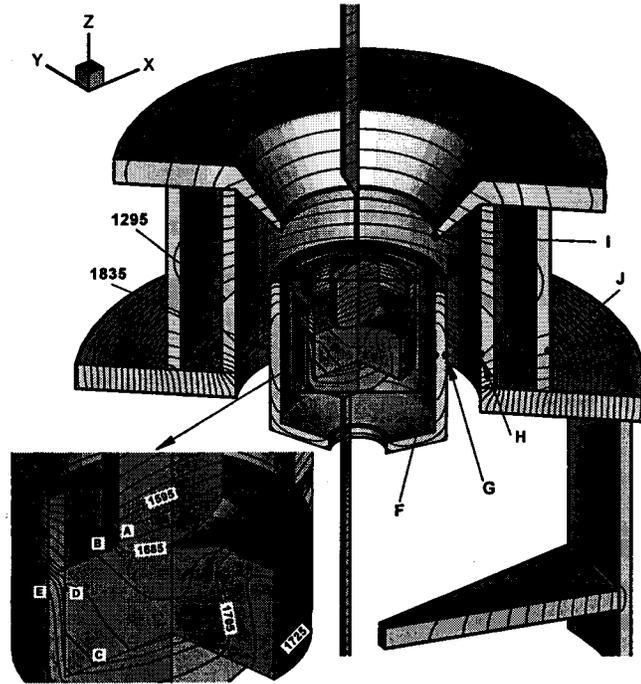
Fig. 2 Temperature distribution in a furnace in a transverse magnetic field. Temperature distribution in the furnace and locations under consideration. Isotherms are plotted every $30\,K$ in solids and every $10\,K$ in the melt.

for an example, the 3D domain includes the crystal, melt, crucible and heater. The other regions in the furnace are included in the 2D domain.

The calculation of view factors in the radiation modeling is reported elsewhere in detail. Details of the model, including treatments of boundary conditions, were published elsewhere[18].

3. Computation results for model validation

A test growth process was numerically simulated to demonstrate the validity of the proposed model[18]. The configuration of the growth furnace is as shown in Fig. 1. The furnace is in a transverse magnetic field with non-rotating crystal and crucible. The magnetic field is applied in the x-direction with an intensity of 0.3 T. The crystal, melt, crucible, heater and heat insulators were included in the 3D domain.

Figure 2 shows the temperature distributions in the melt as well as in solid

components in the furnace. Three-dimensional features can be obviously seen in the core region of the furnace, especially in the melt. The core region of the furnace must be treated in 3D but the heat insulators away from the core region can be treated in 2D in order to save computation resources, demonstrating that the proposal of 2D domain and 3D domain in establishing our 3D global model is reasonable.

(a)   (b)
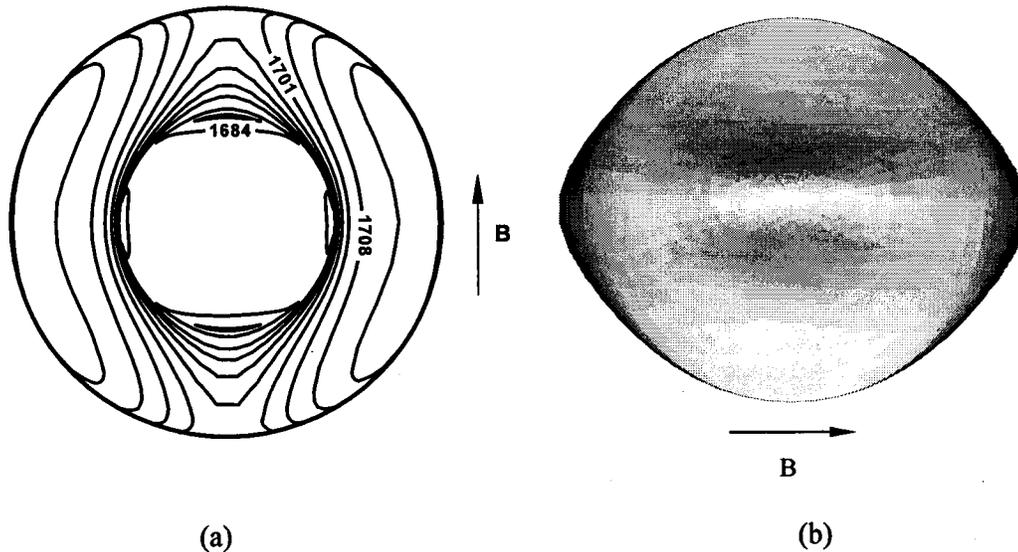
Fig. 3 (a) Calculated temperature distribution at solid-liquid and liquid-gas interface. (b) Calculated interface shape.

The melt-crystal interface shape was found to be 3D in this growth process, which can be observed in Fig. 2. In Fig. 3, a top view of the interface with identification to the isothermal surface of the melting temperature of silicon is shown. These results are in good agreement with the experimental research of Kajigaya et al.[19]. In their experiment, ellipsoid crystals with 3D interface shapes were grown in a transverse magnetic field with the same intensity under a condition without seed rotation.
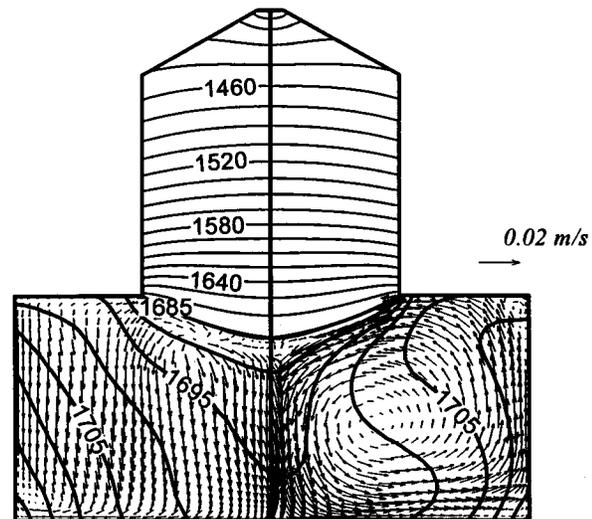
Fig. 4 Melt convection, thermal field and melt-crystal interface profiles in symmetric planes $x = 0$ (right) and $y = 0$ (left). Isotherms are plotted every $5 K$ in the melt and every $15 K$ in the crystal.

33

4. Numerical analysis of a TMCZ growth

Some results of the melt convection, thermal field and melt-crystal interface shape were shown in Fig. 4 and Fig. 5(a) for a TMCZ configuration with rotating crucible and crystal rotation[3]. The transverse magnetic field is $0.1T$ oriented in the x-direction. The rotation rates of crystal and crucible are $-30\,rpm$ and $5\,rpm$, respectively. Figure 4 shows the melt convection, thermal field and melt-crystal interface profiles in symmetric planes $x = 0$ (perpendicular to the magnetic field) and $y = 0$ (parallel to the magnetic field). A strong vortex occupies plane $x = 0$, while, in plane $y = 0$, the melt flows downward to the crucible bottom with a complex pattern right under the melt-crystal interface. Accordingly, the temperature distributions in plane $x = 0$ and plane $y = 0$, which are dominated by the flow pattern of melt, are distinctly different. However, even

(a)   (b)
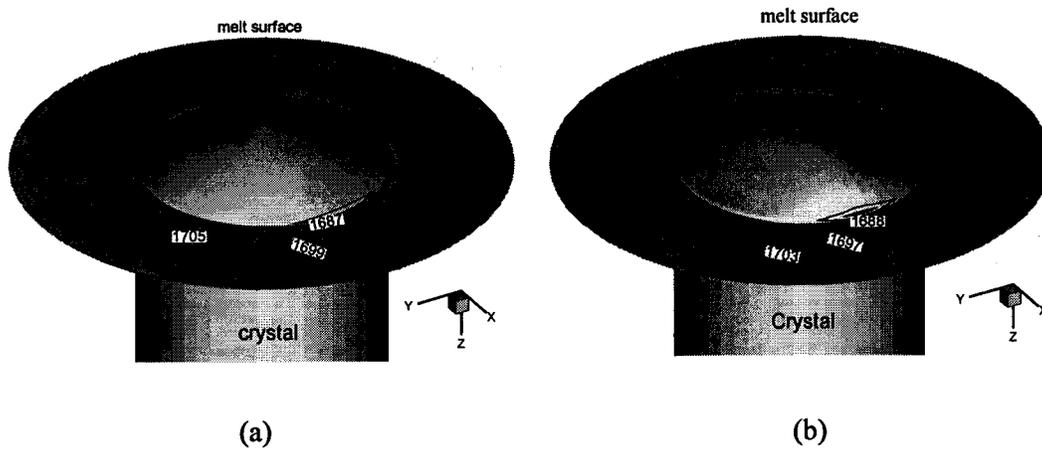
Fig. 5   A 3D view of the melt-crystal interface and the temperature distribution on the melt top surface as well as on the interface. Isotherms are plotted every $3\,K$. (a) rotating crucible and crystal;   (b) non-rotating crucible and crystal.

though the flow and thermal field of melt are obviously three-dimensional, the melt-crystal interface profiles in the two orthogonal planes are almost symmetric, as shown in Fig. 5.

Figure 5 (a) is a 3D view of the melt-crystal interface shape and the temperature distribution on the melt top surface as well as on the melt-crystal interface. For the sake of comparison, the corresponding results were also shown in Fig. 5 (b) for the case in which the crystal and crucible are not rotating.   As can be noted in these figures, differing from the three-dimensional interface shape shown in Fig. 5 (b), the deflection of melt-crystal interface shape is almost uniform over circumference in Fig. 5 (a).   This indicates that the crystal and crucible rotations homogenize the melt-crystal interface deflection over circumference.

5. Static and dynamic modeling of casting process for solar cells

Casting process is one of the promising method for production of silicon crystals with reasonable const performance and quality. We developed two codes of casting process for silicon solar cells. One is static, which can calculate temperature distribution, interface shape, flow velocity in quasi-static condition. Figure 6 shows grid and temperature distribution of a furnace for casting silicon. We can recognize the multi heater system in the furnace and temperature distribution in a whole furnace. Figures 7 (a) and (b) show the temperature distributions prior to solidification and after solidification. The interface shape after solidification is recognized to convex to the melt, which is qualitatively identical to experiment.

The other code, which we call dynamic code can calculate interface shape between a solid-liquid interface, flow velocity and temperature distribution in a whole furnace as a function of time during solidification. Moreover, growth velocity, iron distribution, and fraction solidified as a function of imposed power of heater in a furnace. Therefore, we can calculate dynamic response of the system, which includes incubation time of solidification. Furthermore, impurity distribution can be calculated which includes the effect of both solidification with segregation process and cooling process, since cooling process strongly affects impurity distribution in a grown crystal. The calculated growth

(a)   (b)
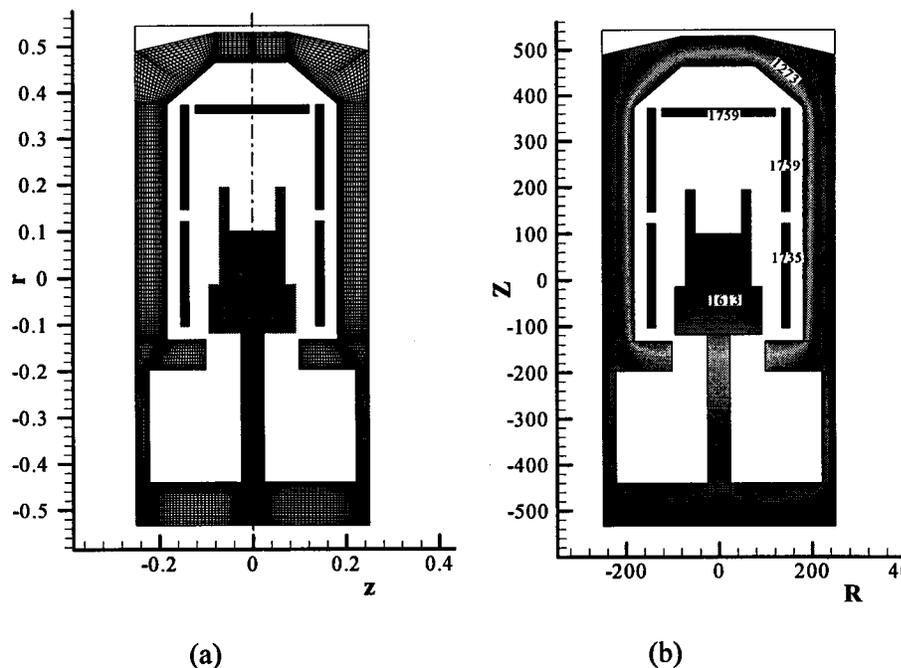
Fig. 6   (a) Grid of calculation.   (b)   Calculated temperature distribution in a whole furnace.

35

rate increases monotonically when we impose linear decrease of heater power as a function of time. Since size of this system is small, heat capacity of the furnace is not so large compared a furnace for production. Consequently, the growth rate can increase monotonically, however the condition is more complex for a large furnace.

(a)   (b)
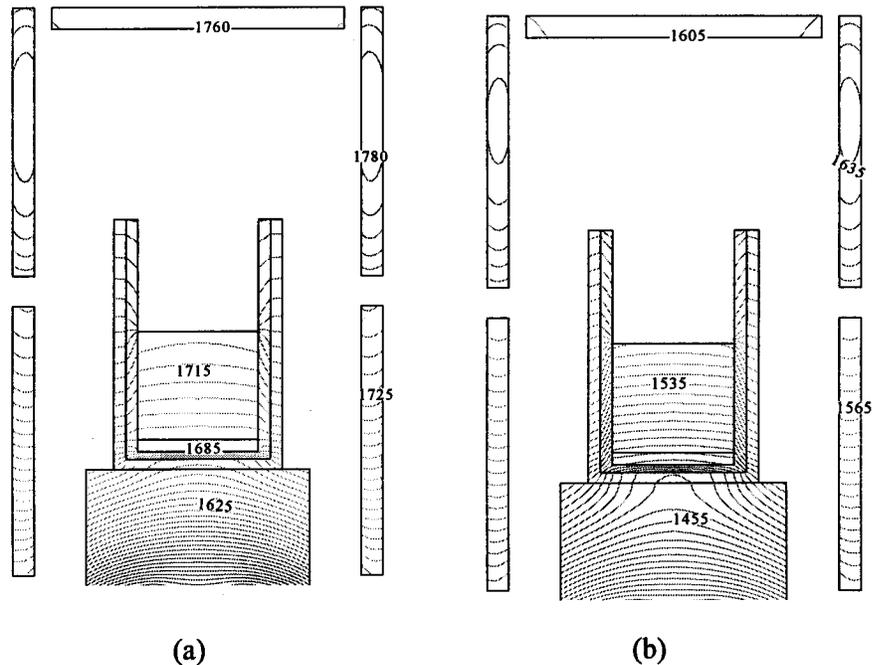
Fig. 7   Temperature distribution in a furnace. (a) Beginning of solidification. (b) After solidification.

6.   Conclusions

A 3D global model was developed for analyzing the heat, mass and oxygen transfers in a silicon CZ configuration with moderate requirements of computer memory and computation time. The model was demonstrated to be valid and reasonable. Some results obtained recently using this 3D global model were introduced for a silicon TMCZ growth. The model showed powerful capability in analyzing heat, mass and oxygen transfers in a CZ configuration. A casting process for solar cells can be calculated dynamically. The code can calculate impurity concentration during solidification and cooling process. Moreover, the code can calculate how temperature in a furnace changes as a function of time by changing heater power imposed.

References

1) N. Kobayashi: J. Cryst. Growth, 108 (1991) 240.
2) B.C. Sim, I.K. Lee, K.H. Kim, H.W. Lee: J. Cryst. Growth, 275 (2005) 455.
3) L.J. Liu, K. Kakimoto: Cryst. Res. Technol, 40 (2005) 347.
4) A. Krauze, A. Muiznieks, A. Muhlbauer, Th. Wetzel, W.v. Ammon: J. Cryst. Growth, 262 (2004) 157.
5) D. Vizman, S. Eichler, J. Friedrich, G. Müller: J. Cryst. Growth, 266 (2004) 396.
6) M. Watanabe, M. Eguchi, T. Hibiya: Jpn. J. Appl. Phys., 38 (1999) L10.
7) M. Watanabe, M. Eguchi, W. Wang, T. Hibiya, S. Kuragaki: J. Cryst. Growth, 237 (2002) 1657.
8) N. Kobayashi: J. Crystal Growth, 43 (1978) 3573.
9) A. Krauze, A. Muiznieks, A. Muhlbauer, Th. Wetzel, W.v. Ammon: J. Crystal Growth, 262 (2004) 157.
10) K. Kakimoto, L.J. Liu: Cryst. Res. Technol., 38 (2003) 716.
11) J.J. Derby, R.A. Brown: J. Crystal Growth, 74 (1986) 605.
12) L.J. Atherton, J.J. Derby, R.A. Brown: J. Crystal Growth, 84 (1987) 57.
13) F. Dupret, P. Nicodeme, Y. Ryckmans, P. Wouters, M.J. Crochet: Int. J. Heat Mass Transfer, 33 (1990) 1849.
14) M. Li, Y. Li, N. Imaishi, T. Tsukada: J. Crystal Growth, 234 (2002) 32.
15) V.V. Kalaev, I. Yu. Evstratov, Yu. N. Makarov: J. Crystal Growth, 249 (2003) 87.
16) D. Vizman, S. Eichler, J. Friedrich, G. Müller: J. Cryst. Growth, 266 (2004) 396.
17) V.V. Kalaev, D.P. Lukanin, V.A. Zabelin, Yu. N. Makarov, J. Virbulis, E. Dornberger, W. von Ammon: J. Crystal Growth, 250 (2003) 203.
18) L.J. Liu, K. Kakimoto: Int. J. Heat Mass Transfer, (2005), in press.
19) T. Kajigaya, T. Kimura, Y. Kadota: J. Crystal Growth, 112 (1991) 123.

Application of Numerical Simulation of Directional Solidification Processes for Improving Crystal Quality

T. Saitoh and I. Yamaga[1]
Tokyo University of Agriculture and Technology
Koganei, Tokyo 184-8588, Japan
[1]Dai-ichi Dentsu, Ltd., Chofu 182-0034, Tokyo, Japan

Summary

Since the first paper on casting process in 1976 [1], several solidification processes have been developed by industry including casting (Wacker, now Deutch Solar) [2], Heat Exchanger Method (Crystal Systems, transferred to GT Solar) [3], Electromagnetic Casting (Sumitomo Sitix, now SUMCO Solar) [4, 5] and so forth. In recent PV market, multicrystalline Si wafers produced by the processes play a major role to fabricate solar cells due to the cost-effectiveness. However, the rapid market growth using the Si wafers might be suppressed by the shortage of Si feedstocks.

One of the solutions to solve the material issue is to make highly efficient cells using higher-quality Si wafers. Limit cell efficiency is realized if the minority-carrier lifetimes are achieved to a millisecond level. A small furnace experiment using a crucible size of 155 mm square is described, which includes the investigation of the effect of temperature gradient on crystal quality of solidified Si ingots [6]. Using two kinds of solidification technologies, the target diffusion length of 600 µm was achieved. As for the multicrystalline Si (mc-Si) wafers, such a high lifetime was reported by P-gettering and H-passivation of the mc-Si wafers grown in the small solidification furnace [7-8]. Using the high-quality mc-Si wafers, very high cell efficiencies close to 20 % were achieved at Fraunhofer Solar Energy Institute [9].

The quality of the multicrystalline Si ingots has been improved by trial and error experiments on solidification conditions. To avoid the troublesome efforts, numerical approach was successfully applied for the SOPLIN process to simulate the temperature distribution in furnaces and the solidification velocity of the ingots [10]. Detailed understanding of the directional solidification is a key element to produce higher-quality mc-Si ingots and to design a commercial solidification furnace. The heat transfer in the process has also been investigated by applying fluid dynamics software [11-12]. In this paper, the complex heat transfer in the furnace is analyzed by optimizing numerical simulation including mesh settings and comparing simulated temperature distribution and solidified thickness with measured ones.

A heat transfer model of the process was developed using a fluid dynamics software "PHOENICS" commercialized by CHAM Corp. [13]. The furnace consists of rectangular silica crucible and circular heater, carbon insulators and water-cooled chamber. Si charge was melted in an isothermal condition and then solidified by lowering the crucible/carbon block and also decreasing the heater temperature. The physical properties of carbon and silica materials were provided by the manufacturers. The better mesh setting was obtained

by using narrower spacing near the surfaces of the insulators, heater, silica crucible, cooling block and Si ingot. The simulated temperature distribution was compared with the measured values using thermocouples inserted in a model carbon block. As an example, simulated temperature distributions in the furnace were introduced for nucleation and final stages of the solidification at heater temperatures of 1470 and 1450 C. The temperature distribution in the molten silicon was convex, which is caused by heat transfer from the heater to the crucible side via thermal radiation. Using the FD software, a flow pattern of Argon gas in the furnace could be observed. The pattern included a local cyclic flow due to the confined furnace structure and the convection along the crucible and heater walls. The control of the Ar gas flow is important to suppress the carbon contamination in the silicon ingot from the ambient.

Based on the numerical simulation, a production-level solidification furnace was designed and constructed. The temperature gradient of the furnace was about half of that of the small furnace, but good-quality, 250 kg Si ingots were successfully fabricated. The average diffusion length of the ingots was 250 μm and cell efficiencies using the Si wafers were the same level as compared with the commercial cells. Understanding of the irregular pattern of the diffusion length is to be investigated by taking account of dislocation multiplication, constitutional supercooling and more precise temperature control.

Acknowledgements

References

[1] H. Fischer and W. Pshunder, Proc. of 12th IEEE Photovoltaic Specialists Conference 1976, p.86

[2] D. Helmreich, Silicon Processing for Photovoltaics II, C. P. Khattak and K. V. Ravi, Elsevier Science Pub., 1987

[3] C. P. Khattak and F. Schmid, Proc. of 13th IEEE Photovoltaic Specialists Conference, 1978, p.137

[4] T. F. Ciszek, J. Electrochem. Soc. 132 (1985) 963.

[5] K. Kaneko, R. Kawamura and T. Misaewa, Proc. of 1st World Conference on Photovoltaic Energy Conversion, 1994, p. 30.

[6] T. Eguchi et al., presented at 15th Photovoltaic Science and Engineering Conference, Shanghai, Oct. 2005, paper number PV0396-02.

[7] M. Dhamrin et al., presented at 19th European Photovoltaic Solar Energy Conference and Exhibition, Paris, June 2004

[8] J. Henze et al., presented at 20th European Photovoltaic Solar Energy Conference and Exhibition, Barcelona, June 2005.

[9] O. Schulz et al., presented at 20th European Photovoltaic Solar Energy Conference and Exhibition, Barcelona, June 2005.

[10] D. Franke et al., Solar Energy Materials & Solar Cells 72 (2002) 83-92

[11] E. A. Meese et al., presented at 19th European Photovoltaic Solar Energy Conference and Exhibition, Paris, June 2004.

[12] B. Jones et al., presented at 20th European Photovoltaic Solar Energy Conference and Exhibition, Barcelona, June 2005

[13] PHOENICS Version 3.6, 2005, CHAM Japan

Application of Numerical Simulation of Directional Solidification Processes for Improving Crystal Quality

T. Saitoh and I. Yamaga[1]
Tokyo University of Agriculture and Technology,
Koganei, Tokyo 184-8588, Japan
[1]Dai-ichi Dentsu, Ltd., Chofu 182-0034, Tokyo, Japan

Outline of this presentation

- **Introduction**
- **Small furnace results**
- **Numerical simulation of solidification furnace**
- **Design of a commercial furnace**
- **Future issue for quality improvement**

History of Multicrystalline Si Ingot Developments

Initial developments
- **Cast process by AEG Telefunken in 1975**
- **Heat Exchanger Method by Crystal Systems in 1976**
  (Technology transfer to GT Solar in 1990's)

Japanese contributions
- **NEC under Sunshine Project in 1976**
- **Technology transfer to Sumitomo Sitix in late 1970's**
- **EMC by Sumitomo Sitix (SUMCO Solar) in 1980's**
- **Kawasaki Steel (JFE Steel) in late 1990's**
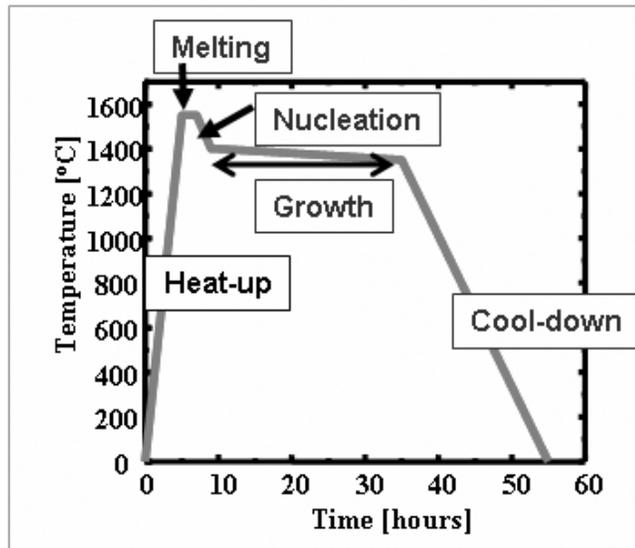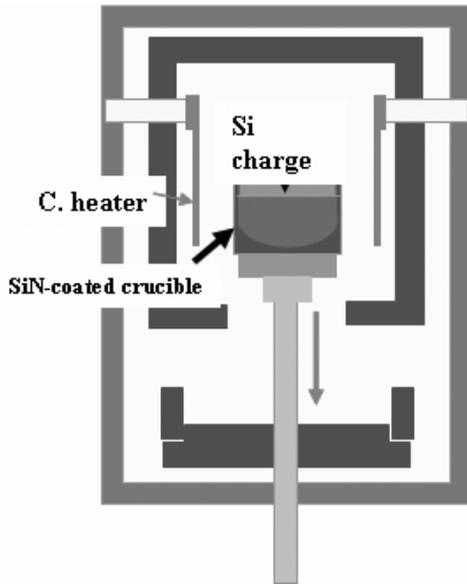
Growth furnace and process of mc-Si ingots Using 10kg solidification furnace
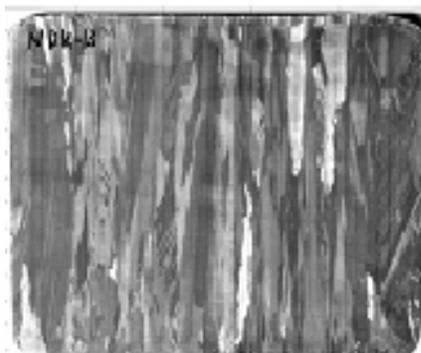
Vertical cross section
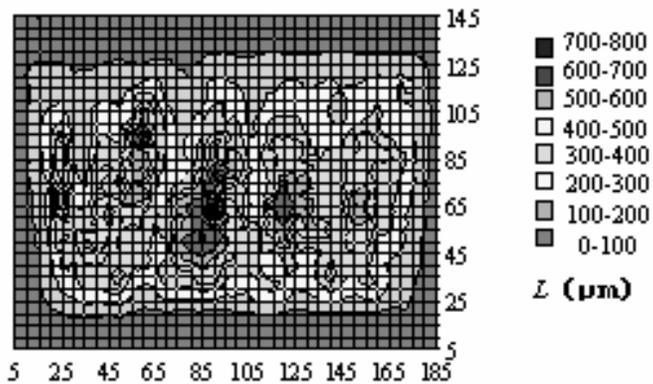
Diffusion length map of the Vertical cross section

Effects of P-gettering and H-passivation

(Case 1) P-gettering and furnace gas anneal (TUAT)

Legend:
- Before P-gettering
- After P-gettering
- After FGA
- Resistivity(Ω·cm)

Y-axis left: Effective lifetime [μs]
Y-axis right: Resistivity [Ωcm]
X-axis: Wafer Number (10, 50, 90, 130, 170)

$\rho = 1\,\Omega\cdot cm$
$D = 30\ cm^2/s$
$\tau = 100\ \mu s$
Then
$L = 550\ \mu m$
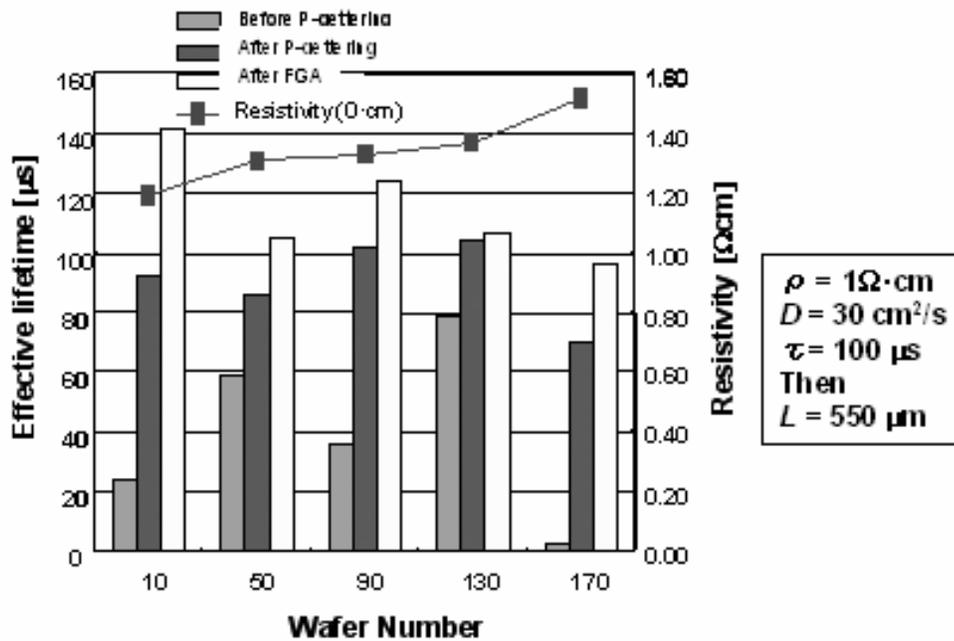
(Case 2) P-gettering and SiN-hydrogenation (FISE)

Y-axis: Area-averaged lifetime τ [μs]
X-axis: As grown, P-gettering, P-gett. + H-pass.

Bar labels:
Ga 2.2 Ωcm (top)
Ga 6.4 Ωcm (center)
Ga 7.7 Ωcm (bottom)
B 1.1 Ωcm (top)
B 1.3 Ωcm (center)
B 1.5 Ωcm (bottom)

Ga-doped mcSi wafers (7.1 Ωcm, 1065 cm²) after P-gettering and H-passivation.
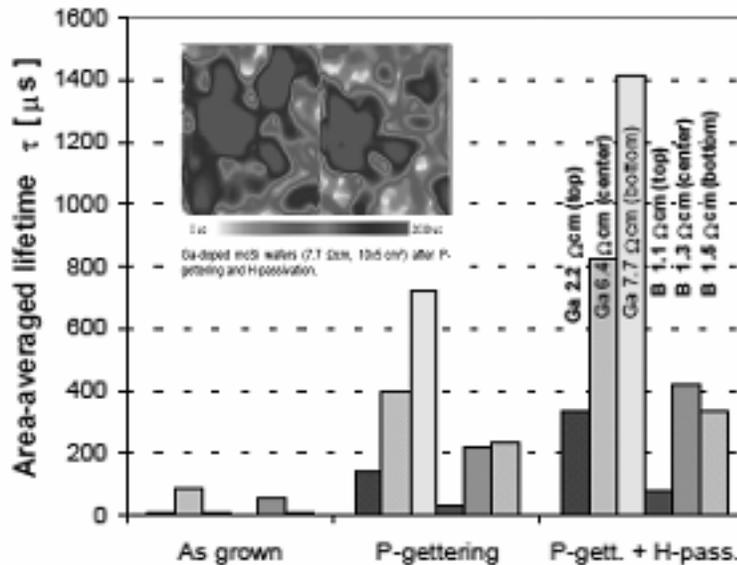
Millisecond Area-Averaged Lifetimes in Gallium-Doped p-Type Multicrystalline Silicon

J. Henze[1], C. Schmiga[1], M. Dhamrin[2], T. Saitoh[2], I. Yamaga[3], J. Schmidt[1]

20th EUPVSEC in Barcelona, 2005

42

High-efficiency solar cell process for lowly doped multicrystalline silicon

Oliver Schultz[1]*, S.W. Glunz[1], D. Kray[1], M. Dhamrin[2], I. Yamaga[3], T. Saitoh[2], G.P. Willeke[1]

[1]Fraunhofer ISE, Heidenhofstr. 2, 79110 Freiburg, Germany,

[2]Tokyo University of Agriculture and Technology, Tokyo 184-8588, Japan

[3]Dai-ichi Kiden Co., 1-54-1, Shimo-ishihara , Chofu, Tokyo 182-0034, Japan
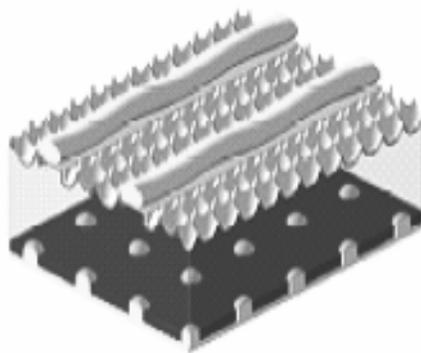
Fig. 4: Applied cell structure for high-efficiency solar cells from mono- and multicrystalline silicon. The front surface is plasma-textured and covered by a double-layer antireflection coating. The rear surface is covered by a wet oxide and contacted with the LFC-process.

Table 1: Solar cell results on FZ and multicrystalline material.

Best solar cells (1 cm²)

material	ρ [Ω cm]	V_{oc} [mV]	j_{sc} [mA/cm²]	FF [%]	η [%]
FZ	1	657	39.7	81.7	21.3
FZ	4	639	40.0	79.6	20.3
FZ	9	645	40.4	78.2	20.4
Boron-mc	1.2	640	38.8	80.0	19.9
Gallium-mc	5	623	39.3	79.5	19.5

Average values and standard deviation.

material	Amount of cells	Contact pitch [µm]	ρ [Ω cm]	V_{oc} [mV]	j_{sc} [mA/cm²]	FF [%]	η [%]
FZ	72	500	1	655 ± 4	39.3 ± 0.4	79.0 ± 1.9	20.4 ± 0.6
FZ	33	500	4	634 ± 2	39.9 ± 0.2	78.1 ± 0.8	19.7 ± 0.3
FZ	34	500	9	636 ± 5	40.1 ± 0.3	76.9 ± 1.1	19.6 ± 0.4
Boron-mc	32	250	1.2	618 ± 15	37.6 ± 0.9	77.8 ± 1.7	18.1 ± 1.1
Gallium-mc	30	250	5	608 ± 11	38.7 ± 0.5	76.2 ± 2.0	18.0 ± 0.9
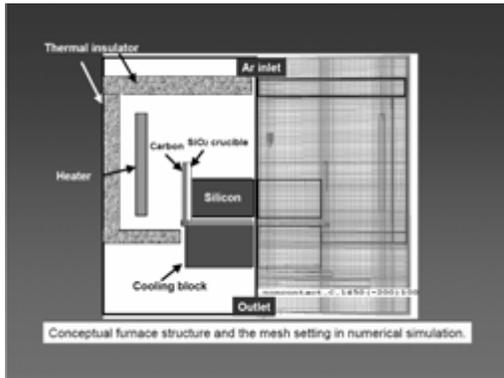
Conceptual furnace structure and the mesh settings
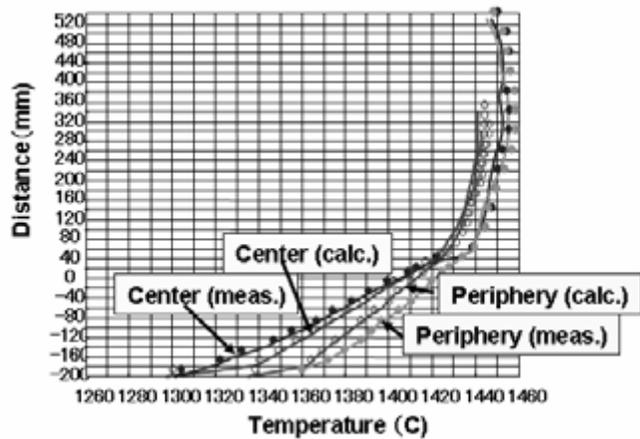
Comparison between simulated and calculated temperature distribution using a carbon block
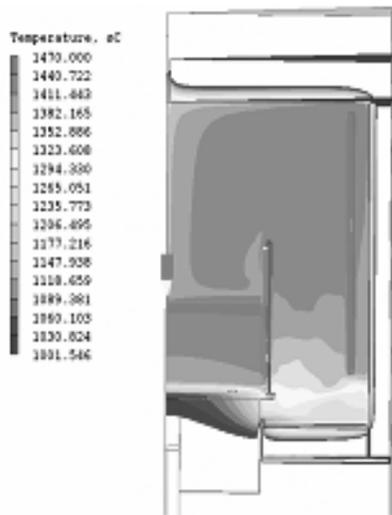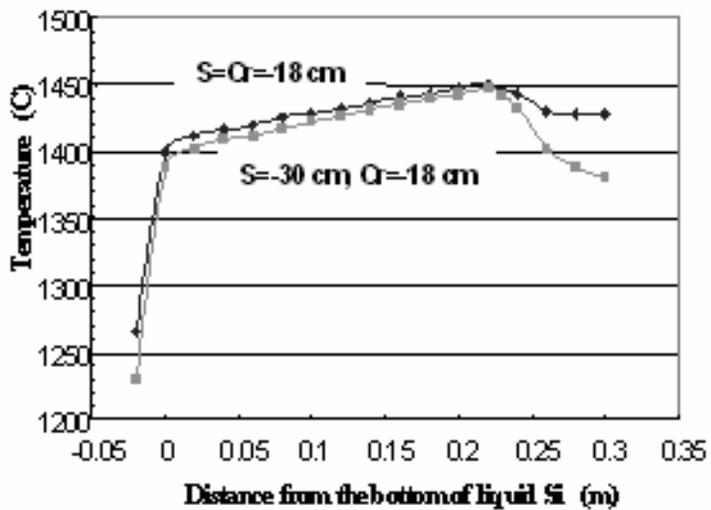
(a) Contour map (b) Central position

Simulated temperature distribution in a solidification furnace for a nucleation stage at a heater temperature of 1470C and a crucible lowering of 18 cm.
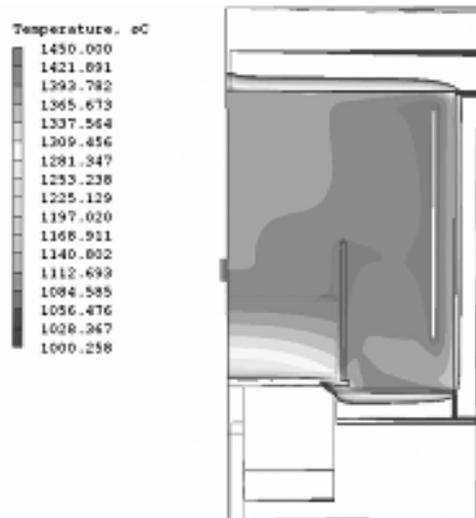
Simulated temperature distribution in a furnace for a final stage of the solidification at a heater temperature of 1450C and a crucible lowering of 20 cm.
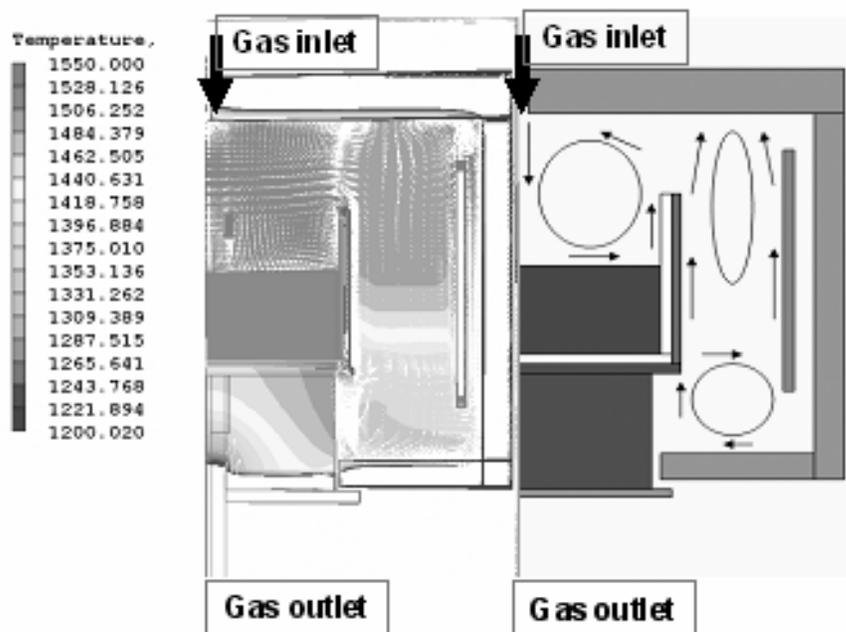
Temperature distribution   **Flow pattern of Ar gas**

Simulated temperature distribution and Ar gas flow pattern in a solidification furnace for a Si melting step at a heater temperature of 1550C.

Features
- **250 kg ingot**
- **Front loading**
- **Small size**
- **Unique heater**
- **Short cycle time**
- **Easy maintenance**

Overview of commercial 250 kg solidification furnace constructed by Dai-Ichi Kiden Corp.
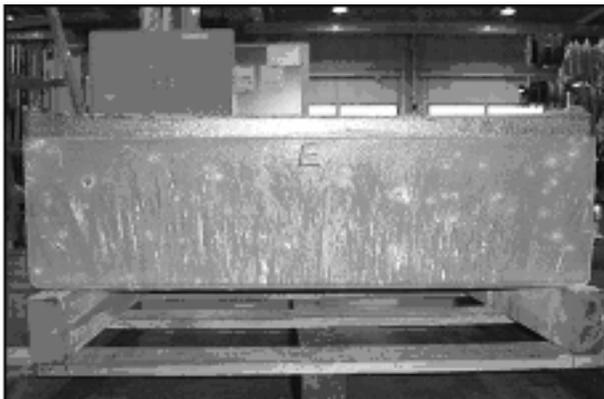
(a) Side view of the ingot
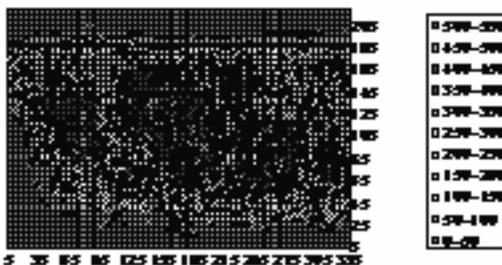
(b) Diffusion length map of the half ingot

Side view and diffusion length map of directionally solidified 250 kg multicrystalline Si ingots

Future Issues

- **Detailed understanding of vertical diffusion length maps**
- **Dislocation multiplication during solidification**
- **How to model the constitutional supercooling ?**
- **Time-dependent simulation during solidification**
- **Precise control of directional solidification**
- **Elimination of contamination from ambient and Si_3N_4 coating**

Solar Industry Crystalline Silicon Initiative:
A Step on the Road to Our Solar Power Future

Allen Barnett, Electrical and Computer Engineering, University of Delaware

Rhone Resch, Solar Energy Industries Association, Washington, DC

Introduction

The attendees at the 14th Crystalline Silicon Workshop recommended that this initiative be developed. Following is a summary of the present recommendations that are circulating in Washington. The process, present status and next steps will be discussed. Recommendations for Research Priorities and improved traction in Washington will be solicited.

Objectives of the Initiative

The Crystalline Silicon Initiative is an industry-led collaboration designed to reduce the cost, increase the efficiency, and improve the manufacturing of crystalline silicon solar power. The Initiative targets the material that accounts for more than 90% of photovoltaic (PV) production worldwide. The figure includes the 2015 goals for system and electricity costs. By 2015, the Initiative will:

* Reduce solar electricity costs to less than 6¢/kWh

* Start solar power on a path to deliver half of all new U.S. electricity generation by 2025

* Increase performance by 50%, with modules to reach 18% efficiency

* Cut system manufacturing costs dramatically

* Decrease price to consumers by 40% from today's $6.10 per watt

* Reclaim global market leadership in the United States

* Reestablish U.S. technological leadership in PV materials, equipment, and production processes that will serve the booming world market for PV.
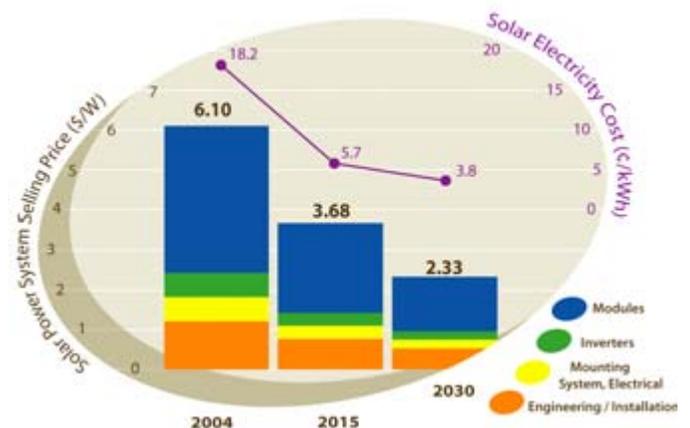
Importance of the Initiative for the United States

* World PV shipments grew by 60% in 2004, and demand continues to be strong in 2005. The industry now generates more than $6 billion in revenues annually. The figure below shows the potential for PV growth projected by the PV Industry Roadmap.

* PV sales are driven by innovative technology and manufacturing, which improve PV cost and performance, and by strong market development programs.

* U.S. market share of this worldwide boom dropped to less than 12% last year, the lowest level ever; Europe and Japan garnered almost 26% and 52%, respectively, of a market once dominated by the United States.

- Market incentives in a few states, such as California, helped U.S. sales, but imported PV is gaining ground. We are importing a product that America invented, giving up domestic jobs and hurting our balance of trade.

- The Initiative is a strategic research investment for the United States to rebuild a strong market position in an industry where we expect to add 42,000 jobs by 2015, and to double in size again by 2020—if we invest in both R&D and market development.

- The result will be an industry whose products increase energy security, boost domestic economic development, lower peak power costs, improve grid stability, reduce air pollution, cut greenhouse gas emissions, and lower water consumption for power generation.

Research Priorities

The Initiative will fund a focused research effort that will be a 50/50 cost-share with industry. The target will be new areas of research that have emerged recently or have been overlooked by past research. The cutting edge of crystalline silicon science and engineering will be explored, leading to advances for both the semiconductor and photovoltaic power industry. Key research areas and essential goals—based on input from industry, universities, and national laboratories—include advances in cost and performance of silicon wafers, PV cells, and PV modules:

- Novel breakthrough designs and processes

- Improved impurity and defect engineering for higher performance at lower materials costs

- Methods to minimize power losses created by incorporating large-area cells into modules

- Products that last for 30 years and are simple to install and operate

- New hydrogen-passivation processes and equipment

- New silicon production processes

- Thinner materials and larger cells

- New capital equipment capable of high-volume manufacturing, and sophisticated in-process diagnostics

- New processes and machine tools to create the next generation of manufacturing technology

- Innovations to reduce optical losses

- New or improved electrical contact systems

- Industry, university, and national laboratory partnerships for new crystalline silicon advances.

The Initiative

	Cell Efficiency (%)	Module Efficiency (%)	Electricity Costs (¢/kWh)	Annual Generation (MW)
Now	18*	12	18	139
Near- to Mid-Term	24*	18	6	2500**
Long-Term	29	25	4	Majority of Annual Generation by 2025

* laboratory
** by 2015
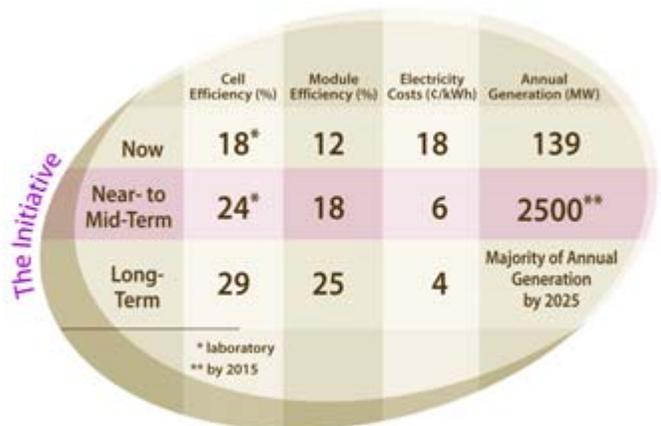
This figure to the right illustrates the near-term impact of the Initiative and its connection to the long-term potential expected from basic research and development.

Solar Energy Industries Association's Process.
Before the formal meeting held in Florida in January 2005, some 23 organizations were involved, with 19 written and 7 verbal inputs. The formal meeting had 50 attendees from 26 organizations. And the last draft generated 31 responses, indicating a very high level of participation and contribution.

EUROPEAN PHOTOVOLTAIC RTD AND DEMONSTRATION PROGRAMME

P Menna
European Commission
Directorate General for Energy and Transport
Brussels (Belgium)

ABSTRACT: The EU RTD programme has been tackling the RTD agenda for the PV sector at several levels and now has a suite of projects which cover the different main strategic lines of the programme. .At the technology level, the projects are researching new higher efficiency PV modules and system components, which can be produced at lower costs. (DG RTD)At the system level it is demonstrating innovative, simple and more cost effective approaches to the integration of system components, such as higher voltage module arrangements to match more efficient and lower cost integrated inverters. At the market level the programme is demonstrating the benefits which can be achieved by building systems in a context which achieves a critical mass of activities in terms of design, procurement, installation procedures, and eventually operation and maintenance. This provides important insights into the ways to achieve economies of scale and business advantages in the future. At the level of building integration, the programme has been pioneering through demonstrating the potential of using PV systems in highly efficient and well managed buildings.
Keywords: R&D and Demonstration Programmes; Strategy; Dissemination

1 INTRODUCTION

Europe's energy system is characterised by a heavy dependence on imported fossil fuels, an ever increasing demand for electricity, and emissions of CO_2 which are still too high compared with our Kyoto commitments. Currently, the European Union imports about 50% of its energy needs. This figure is predicted to rise to 70% at the horizon 2030, with an increasing share for fossil fuels, unless bold measures are adopted [1].

Renewables and energy efficiency measures represent an important way to bring to Europe not only environmental benefits, but also the other important advantages of improved security of supply, due to reduced need for imported hydrocarbons and technological development, which would also allow us to pursue the Lisbon Agenda. Furthermore, because renewables and energy efficiency measures are more labour intensive than conventional energy supply, they also bring an increased employment.

The European policies for the renewable energy sector, which are of direct relevance to the solar photovoltaic sector, were first set is the White Paper on renewable energy, which was adopted in November 1997 [2]. This document established the ambitious target of 12% for the contribution of renewable sources of energy to the European Union gross energy consumption in the year 2010, and an equally ambitious target of 3000 MW of photovoltaic power to be installed by the same date. Further clarifications on EU policies for the renewable energy sector are contained in the Green Paper on the Security of Energy Supplies, which was launched in November 2000 [1]. Subsequently, the Commission published its first report on the progress which had been achieved towards the objectives given in the White Paper [3].

Recently, the EU has put in place a new regulatory framework, with a view to accelerating the growth of EU markets for renewable electricity. In this context, the most important instrument is the Directive on electricity production from renewable energy sources, which set a community EU-25 target of 21% of the electricity consumed in 2010 to be produced from renewable energy sources [4].

More recently, the Commission has reported on the share of renewable sources in the energy balance of the EU Member States [5]. This Communication shows that only four Member States have actively adopted measures which are effective enough to put them on line to meet their renewable energy and green electricity commitments. For the rest of Europe the picture is not so good. The other Member States must therefore act more quickly and introduce more ambitious policies if the EU is to meet its overall targets.

The latest available market analysis shows that the cumulated installed European photovoltaic capacity in 2004 surpassed the 1 000 MW figure [6]. The European market growth prospects, mostly driven by Germany, remain positive, so that the 3 000 MW target for the year 2010 appears within reach. However, in the same year 2004, because the demand was higher than the production, Europe became for the first year a net importer of technology. The European photovoltaic turnover has been estimated to be close to € 2 billion and the number of employees about 23 000, including manufacture, R&D, installation and distribution [6]. It is vital that the PV industry continue to grow in ways which will ensure that the maximum possible number of jobs is created within the EU. Since solar photovoltaic, as many of the renewable energy sources, is still relatively new to the market, there is a need for a targeted legislative and commercial infrastructure to encourage rapid market growth. At the same time, there is still a need for high profile demonstrations and promotional activities to raise the confidence of investors. The Commission is therefore active in both these areas, with the clear purpose of increasing the share of renewable energy sources in the energy mixes of the EU Member States.

2 LEGAL INSTRUMENTS

During the recent years, the Commission has proposed a considerable number of legal instruments, adopted by the European Parliament and Council, to promote renewable energy and energy efficiency. The most relevant for the PV sector are reported in the following.

2.1 The Green Electricity Directive

The Directive 2001/77/EC on the promotion of electricity produced from renewable energy sources, sets a legal framework for the future development of the renewable electricity (RES-E) markets in the EU [4].

The Member States are now obliged to establish national targets, which are designed to ensure that the future consumption of RES-E in the EU-25 will rise from 14% in 1997 to 21% by 2010.

The Commission will monitor the progress made towards these targets. The Directive abstains from proposing a harmonised Community wide support scheme for RES-E, but obliges the Commission to report by October 2005, on the experiences gained in the Member States with their different support schemes.

The Directive further obliges Member States to assure guaranteed grid access for RES-E, to issue guarantees of origin for RES-E, and to ensure that the calculation of the costs of connecting new producers of RES-E to the grid and of transmitting green electricity are transparent and non-discriminatory.

Finally, the Directive obliges EU Member States to simplify the administrative procedures associated with installing RES-E generators and connecting them to the grid. This is very important for the PV sector, because it does not make great sense to use the same level of administrative procedure for a typical 3 kW PV generator as would be used for a 300 MW conventional generator.

2.2 Directive on the Energy Performance of Buildings

The Directive 2002/91/EC on energy performance of buildings includes a methodology for establishing integrated building energy performance standards, that takes into account on-site energy production, for example through the use of solar technologies [7]. The transposition of this Directive into National laws in the Member States will provide a valuable opportunity for the PV industry. It gives the possibility to demonstrate to building owners and users that PV can contribute to reducing the 40% of EU final energy consumption, which is currently consumed in buildings.

3 COMMUNICATION ON RENEWABLES

More recently, in a Communication to the Council and the Parliament, the Commission has reported on the share of renewable sources in the energy balance of the Member States [5]. The Commission analysed the current situation and listed the actions that have been undertaken to promote renewable energy in Europe. Concluding that current progress is still not fast enough to ensure EU

targets for 2010 will be achieved on time, the Commission calls on Member States to do more and proposes that more action should be taken at Member State level, particularly by those Member States which are falling behind. In the same Communication, the Commission also committed itself to carry out regular reviews of progress in the development of renewable energy sources. The first review will be completed by October of this year with a view to opening a debate in order to set in 2007 a target for the period after 2010, starting the process for establishing a longer term perspective for renewable energy.

4. PHOTOVOLTAIC RTD AND DEMONSTRATION PROGRAMME

The European Commission has been supporting research and development in the PV sector in Europe for more than 20 years, helping in providing a framework within which researchers and industrialists can work together to develop new applications for PV technologies. In terms of research objectives, a combination of actions is needed to address the PV sector, and these are primarily related to cost reduction: (1) fundamental research aimed at achieving relevant progress either through reducing manufacturing costs or through increasing the efficiency of the PV cells, and (2) integrated research and demonstration, including the development of system design options and concepts, with a view to expanding the market and providing a basis for economies of scale in PV module production. Through a series of RTD framework programmes (FP), the Commission has maintained long term support for the development of the full range of PV devices, including crystalline and thin film solar cells, PV modules and balance of systems components.

4.1 RTD and Demonstration within FP5 (1998-2002)

The 5th Framework Programme, coordinated by the European Commission, was tailored in short to medium term and medium to long term activities for the Research and Demonstration in the Photovoltaic sector. In total almost 100 PV projects were started between 1999 and 2003.

In the short to medium term timeframe, 40 projects were launched in Europe, for a total cost of more than €150 M and an EC contribution close to €45 M. The activities with an expected impact in the medium to long term correspond to more than 60 projects with over €65 M contribution. In a previous paper we provided more details on the main results of the 5th Framework Programme for the Research and Demonstration in the Photovoltaic sector [8].

4.2 The 6th Framework Programme (2003-2006) (FP6)

For the research actions on PV supported under FP6, the focus has been put on the development and demonstration of integrated approaches to new system

design options and concepts, with a strong emphasis on cost reduction.

In the short to medium term, priority has been given to innovative production concepts for high efficiency cells/modules to be integrated into larger scale photovoltaic production facilities to lower the cost; and including low cost integrated components or devices for PV generators; large area, low cost photovoltaic modules for building integrated PV and autonomous solar electricity generation systems; integration of photovoltaic installations in generation schemes to feed local distribution grids and development of new devices and systems to manage these installations.

The medium to long term part of the programme has focused on innovative concepts and fundamental materials research for the next generation of PV technologies; thin film PV technology; PV processing and automated manufacturing technologies; PV components and systems -balance of systems and the research for innovative applications of PV in buildings and the built environment.

As a result of the calls launched so far under the FP6 Programme for both short-to-medium and medium-to-long term , 19 PV projects for a total cost of €145 million and an EC contribution higher than €73 million have been already started or are going to be soon finalized.

In addition, some of the projects supported under the new CONCERTO initiative (launched with the FP6 TREN 2nd call) include demonstrations of innovative PV systems, for a total of 2.9 MW of power and an additional support for the PV sector of about €14 million.

To provide some concrete examples of the projects already launched under FP6, in the short-to-medium term programme, *PV MIPS* is useful to mention. It is an integrated project aimed at the development and demonstration of a new generation of PV modules with integrated power conversion system, to reduce the cost of the electricity generated by grid connected systems The project outcome embraces the high-voltage module with integrated inverter without transformer. This approach offers tremendous advantages when used with high-voltage thin-film modules. For crystalline silicon modules an integrated, two-stage inverter is also being developed and demonstrated within the same project The research will have a strong focus on building integrated PV, because the potential for these applications is especially high in the dense populated areas of Europe.

For the medium to long term programme it is worth to mention the integrated project CRYSTAL CLEAR which deals with crystalline silicon photovoltaics. The objectives of the project are research, development, and integration of innovative manufacturing technologies which allow solar modules to be produced at a cost of 1 EUR/Wp in next generation plants; improvement of the environmental profile of solar modules by the reduction of materials consumption, replacement of materials and designing for recycling; enhancement of the applicability of modules and strengthening of the competitive position of photovoltaics by tailoring to customer needs and improving product lifetime and reliability. Also worth to recall is the integrated project FULLSPECTRUM which

pursues a better exploitation of the FULL solar SPECTRUM by further developing concepts already scientifically proven and by proving new ones.

5. INTELLIGENT ENERGY – EUROPE PROGRAMME

The Intelligent Energy - Europe programme (2003-2006), which is a non-technological programme aiming to tackle market barriers, has now launched two Calls for proposals, and will launch its third call in the autumn of 2005, with a deadline in early 2006. In the first Call, PV was included mainly in the vertical action dealing with renewable electricity, and this led to proposals aiming to tackle market barriers in line with the EU Directive on electricity from renewable energy sources. It also resulted in projects aiming to bring together PV market actors with a view to raising awareness as well as the sharing of knowledge and experience.

More recently the second Call included PV in the context of the vertical action on small scale renewable energy systems. The aim here was to focus on promoting the market for systems which are sold directly to end users and building owners.

The third call, which is scheduled to be launched in the second half of September with a deadline 3-4 months later, is expected open almost all of the vertical key actions, and will therefore invite proposals which address all forms of market barriers to the use of PV electricity.

In addition, a number of actions under the COOPENER field have addressed issues related to the promotion of electricity services for poverty alleviation and sustainable development, and these have included work which is directly related to the future use of PV systems for electricity supply in the poorest areas of developing countries. The main aims of COOPENER are to build local capacity in the areas of energy policy and regulation with a view to creating a more attractive business environment for the provision of sustainable energy services for poverty alleviation. This implies work on local regulations and policies related to energy, and on other regulations, such as import taxes, which can inhibit the commercial viability of renewable energy systems.

6 TECHNOLOGY PLATFORM ON PHOTOVOLTAIC

The *Technology Platform on Photovoltaic* is now operational and has established a new process allowing all of the interested parties in the PV sector to work together on a longer term basis with built in continuity, and with common aims.

The main role of the Platform is to implement a strategic plan to provide advice and expertise to decision makers allowing informed decisions to be made and to propose concrete actions. In ensuring stronger links and coordination between industry, research, market and policy, the Platform represents an important point for

initiatives involving all the main actors of the sector, also for the formulation of research programmes. The Platform is steered by a Committee of 20 members, appointed on an individual basis, representing the different views of the European PV sector (Industry, Research , Policy). The Platform is composed of four working groups (Policy, Market, Research and Developing Countries) supported by a secretariat and envisages the formation of a mirror group composed of representatives of the EU MSs.

7. LESSONS LEARNED

The EU RTD Framework programme have focused on tackling technological barriers to the growth of PV markets by supporting major initiatives aimed at developing new materials and devices, reducing the cost of the modules and systems, promoting a major market development. The cost-sharing basis of the support programme implies that the risks are also shared with both public and private sector organisations in the different Member States. Currently a substantial number of projects cover the different main strategic lines of the programme

7.1 Short to medium term RTD

Numerous projects started under the 5th Framework Programme (1998-2002) are now being completed so that it is possible to elaborate some preliminary statistics. First of all it is worth to note that about 90% of the projects initially launched are going to be successful completed. This is not obvious considering the gloomy economic situation, the fact that demonstration projects, which often have a total cost in the range of tens million euro, receives a maximum support of 35% and the procedural/administrative barriers to overcome at local/national level to complete the installations. It means that financially robust and very committed consortia have been partners in the projects.

At the system level, the programme is demonstrating innovative, simple and more cost effective approaches to the integration of system components, such as higher voltage module arrangements to match more efficient and lower cost integrated inverters, like the *PV MIPS* project already discussed above.

At the market level the programme is demonstrating the benefits which can be achieved by building systems in a context which reaches a critical mass of activities in terms of design, procurement, installation procedures, and eventually operation and maintenance. This provides important insights into the ways to achieve economies of scale and business advantages in the future.

For example, within the project *Universol (NNE5-2001-293)* fits within this category. With the completion of *Universol,* 24 PV systems for a total power of 850 kW have been installed in educational and cultural facilities located in four different European countries. The PV installations, which include advanced monitoring systems, provide an excellent tool to assess the behaviour of different technological approach in a variety of climatic conditions. It also helped institutions, municipalities and cultural centres to acquire a direct experience and know-how on the PV technology and disseminate these widely throughout Europe, in particular to students. Another example of this category of projects is *Mediterraneo (NNE5-2001-437).* By completing 22 installations for a total PV power of about 800 kW in the urban environment of France, Italy, Portugal and Spain, this project considerably increased the awareness of photovoltaic in the European cities built environment, helped increase the market for PV in Europe by achieving a significant reduction in the cost of grid-connected PV, developed standardized PV systems for building applications. This project also contributed to a further dissemination of PV systems especially in two countries (France and Portugal) with limited national support. In Spain it was possible to demonstrate some outstanding façade integrated systems. In terms of job creation, the project may have a high impact, because it is opening the door for follow-up installations.

At the level of building integration, the programme has been pioneering through demonstrating the potential of using PV systems in highly efficient and well managed buildings, with advanced ICT (Information Communication Technology) tools for building energy management). Here the potential for the technology is vast but largely unexplored, particularly for achieving a closer integration of PV electricity supply with the energy demand profiles over the day and over the year in different climate conditions, also including the Northern EU Member States. A good example of this category of project is *PV Nord* (*NNE5-2001-264*). Eight high-profile building projects have been completed in the Nordic countries and in the Netherlands, for a total power of 216 kW. All the systems and are operational and a high dissemination effort has been made. Worth to note the results achieved, among the others, with the management aspects of PV integration. Over the years, development activities have focused at aesthetics, design of the PV systems, cabling and PV claddings. Most of the industrial development work as well has been focussed on the PV aspects only. The result is that when the PV system is separated from the rest of the building management and service practices, there is a danger that the performance tracking and maintenance of the PV systems also becomes separated. Integration of the PV system into the building automation systems could be easily achieved, and thus increasing the usability and value of PV. The cost of doing this seems to be cheaper than adding extra monitoring equipment to the PV system. Thus, the combination of ICT and PV seems to be not a cost issue but mainly an issue of awareness.

7.2 Medium to long term RTD

At the technology level, the projects are researching new higher efficiency PV modules and system components, which can be produced at lower costs.

For example, the Ribbon-Growth-on-Substrate silicon wafer manufacturing technology was developed by Bayer AG as a very promising cost-effective, high-speed wafer manufacturing method. This approach has

the potential to half the silicon wafer manufacturing costs, as the costly wafer-cutting step is avoided and almost 100% of the silicon material is used in the form of wafers. Therefore the successful implementation of the technology will have a major impact on photovoltaic manufacturing costs as well as energy payback times.

The main challenge to face is the improvement of the as-grown electronic wafer characteristics by optimised solar cell process steps. For this purpose, the relation between chemical and crystallographic wafer parameters and solar cell process steps need to be well understood.

A cluster of six projects is focused on environmentally friendly mass manufacture of Chalcopyrite thin film solar cells at low cost.

References

[1] Green Paper on the Security of Energy Supplies European Commission COM(2000)769.

[2] Energy for the Future: Renewable Sources of Energy White Paper for a Community Strategy and Action Plan COM (97)599, 26.11.1997.

[3] Communication on the implementation of the community strategy and action plan on renewable energy sources (1998-2000) COM(2001)69, 16.02.2001.

[4] Directive 2001/77/EC on the promotion of electricity from renewable energy sources, 27 Sept 2001.

[5] Communication on the Share of Renewable Energy in the EU, COM(2004)366, 26.5.2004.

[6] Photovoltaic Energy Barometer, in Systèmes Solaires, **166** (2005) 37-52.

[7] Directive 2002/91/EC on the Energy Performance of Buildings, 16.12.2002.

[8] P Menna,, R Gambi, W Gillett, R Ostrom, H Scholz, 19th EPVSEC, Paris.7-11 June 2004, Conference Proceedings pag 3187-90 (ISBN 3-936-338-14-0 ISBN 88-89407-02-6).

U.S. Department of Energy
Energy Efficiency and Renewable Energy

DOE Photovoltaics Subprogram

Crystalline Silicon

Jeffrey Mazer

U.S. Department of Energy
Energy Efficiency and Renewable Energy

DOE Solar Program Budget ($ Thousands)

	2004	2005	2006
Photovoltaics	76500	77633	70642
CSP	5500	6000	10524
SH&L	3000	2900	2787

	2004	2005	2006
PV Fundamental Research*	29409	31903	29640
Crystalline Silicon Project **	3900	4860	4945
Measurement & Char	6780	6230	5855
Electronic Mat & Devices	9370	6860	6445
High Perf PV & Future Gen	4275	6140	5770
Solar Resource Char	590	450	420
Environmental H&S	440	420	400

* Includes system integration & coordination, earmarks, and cross-cutting.
** The Crystal Silicon Project started in FY 2005.

NREL Crystalline Silicon Project Activities

U.S. Department of Energy
Energy Efficiency and Renewable Energy

- **Advanced Si materials and structures at NREL:** collaboration with Si PV community to develop advanced thin-cell morphologies

- **Process integration at NREL:** development of a new suite of deposition, processing, and characterization tools for the S&TF

- **Center of Excellence at Georgia Tech:** development of advanced industrial processing methods, including improved screen printing and rapid thermal processing, with annual funding of $950 K

- **University subcontracts:** industry-selected topics for elucidation of defect physics and development of advanced processes; six new subcontracts – Georgia Inst Tech (2), Cal Inst Tech, UC Berkeley, Texas Tech, and NCSU – funded through Oct 2005 at $725 K.

- **New university solicitation:** in 2006 with funding ~ $1000 K

Programmatic Issues for Crystalline Silicon Project

U.S. Department of Energy
Energy Efficiency and Renewable Energy

- The first major system in the new S&TF will be a silicon cluster tool. However, there is insufficient funding for other capital equipment and for adequate S&TF staffing.

- NREL measurement and characterization capabilities are severely impacted by inadequate capital equipment upgrade

- Increased partnering with universities and industry, within the framework of SEIA's Crystalline Silicon Initiative (which calls for U.S. global market leadership, 18%-average efficiency modules, and $0.06/kWh systems by 2015)

DOE Photovoltaics Subprogram

Crystalline Silicon

Jeffrey Mazer

DOE Solar Program Budget
($ Thousands)

	2004	**2005**	**2006**
Photovoltaics	76500	77633	70642
CSP	5500	6000	10524
SH&L	3000	2900	2787

PV Fundamental Research ($ Thousands)

	2004	2005	2006
PV Fundamental Research *	**29409**	**31903**	**29640**
Crystalline Silicon Project * *	3900	4860	4945
Measurement & Char	6780	6230	5855
Electronic Mat & Devices	9370	6860	6445
High Perf PV & Future Gen	4275	6140	5770
Solar Resource Char	590	450	420
Environmental H&S	440	420	400

* Includes system integration & coordination, earmarks, and cross-cutting.

* * The Crystal Silicon Project started in FY 2005.

PV Fundamental Research in FY 2006 ($ Thousands)

- Solar Characterization, 420
- Environmental H&S, 400
- Electronic Materials & Devices, 6445
- Crystalline Si Project, 4945
- Measurement & Characterization, 5855
- High Performance PV & Future Gen, 5770

- **Advanced Si materials and structures at NREL:** collaboration with Si PV community to develop advanced thin-cell morphologies

- **Process integration at NREL:** development of a new suite of deposition, processing, and characterization tools for the S&TF

- **Center of Excellence at Georgia Tech:** development of advanced industrial processing methods, including improved screen printing and rapid thermal processing, with annual funding of $950 K

- **University subcontracts:** industry-selected topics for elucidation of defect physics and development of advanced processes; six new subcontracts – Georgia Inst Tech (2), Cal Inst Tech, UC Berkeley, Texas Tech, and NCSU – funded through Oct 2005 at $725 K.

- **New university solicitation:** in 2006 with funding ~ $1000 K

- The first major system in the new S&TF will be a silicon cluster tool. However, there is insufficient funding for other capital equipment and for adequate S&TF staffing.

- NREL measurement and characterization capabilities are severely impacted by inadequate capital equipment upgrade

- Increased partnering with universities and industry, within the framework of SEIA's Crystalline Silicon Initiative (which calls for U.S. global market leadership, 18%-average efficiency modules, and $0.06/kWh systems by 2015)

Transition metals in silicon solar cells: sources of contamination, interactions, defect engineering

A.A.Istratov, T.Buonassisi, M.Heuer, M.Pickett, and E.R.Weber

University of California, Berkeley, CA 94720

Transition metals in silicon is one of the most persistent problems in integrated circuits (IC) silicon technology and in silicon photovoltaics (PV). In the IC industry, the requirements to the level of purity of silicon with respect to transition metals have been steadily increasing with each next generation of integrated circuits, and currently are at a level of $10^9 - 10^{11}$ cm^{-3}, depending on the application. The level of attention to a particular metal historically depended on its impact on minority carrier lifetime, p-n junctions leakage current, and gate oxide integrity, as well as on its ubiquity in the production environment and availability of analytical tools to detect contamination with this particular metal species. For instance, iron has been recognized as the major contaminant several decades ago (see [1] for a review), whereas interest to the properties of copper in silicon has greatly increased only after copper metallization was implemented in the 1990s (see, e.g., [2, 3]).

Silicon photovoltaics is in a different situation than the IC industry. While reduction of the transition metal content through stricter contamination control would improve the efficiency of multicrystalline silicon solar cells, the cost of such measure is often prohibitive. The long-term goal of photovoltaic industry is to reduce cost of solar energy to make it competitive with traditional sources of electricity. Ultimately, this means lower material and production costs. There are various ways towards this objective. Some groups argue that thin silicon films on cheap substrate such as glass could be the technology of the future; others believe that the way to go is to fabricate low-cost solar cells with satisfactory efficiency using low-grade silicon feedstock and inexpensive processing. In either of these and others prospective technologies, recombination active defect clusters, which to a large degree are determined by transition metal contamination, limit the cell efficiency. Better established PV technologies, such as ribbon growth or ingot casting, are also affected by transition metals. Hence, there is a need to (a) understand the origins, distribution, and chemical state of metal contaminants in solar cells and their impact on solar cell efficiency, (b) improve existing techniques for passivation and gettering of transition metals and develop novel approaches to reduce recombination activity of solar cells, and (c) understand the limits how dirty the solar-grade feedstock can be to make cells with acceptable efficiency and find means to live with a higher metal content in the wafers.

In order to accomplish these tasks, one has to have suitable analytical techniques. Metrology tools used by the IC industry for contamination control (e.g., TXRF, lifetime measurement techniques with optical dissociation of FeB pairs, or DLTS) are best suited for detection of surface contaminants or for detection of interstitial or substitutional transition metals. This is the preferred metal state in high-quality single crystalline silicon due to usually low metal contamination levels (hence, a low driving force for precipitate nucleation) combined with a low density of heterogeneous nucleation sites. Application of these techniques to mc-Si typically reveals only low concentrations of isolated metal impurities, rarely more than $10^{11} - 10^{12}$ cm^{-3} [4, 5]; it was also noted that grains with poor electrical properties often had the lowest dissolved interstitial/substitutional metal concentration due to higher metal precipitation rate in these areas [6]. On

the other hand, recent neutron activation analyses [7-9] revealed that the total metal content of mc-Si is much higher, from 10^{12} to 10^{16} cm^{-3}, indicating that the majority of metals are not in easily detectable interstitial/substitutional state, but in clusters, precipitates, or metal inclusions. The minority carrier diffusion length in these materials is much higher than one would expect if all transition metals were homogeneously dissolved. This implies that the recombination activity of metal clusters/precipitates, measured per metal atom, is lower when the metals are precipitated.

Unfortunately, the level of understanding of electrical properties and of the nature of recombination activity of metal precipitates is poor. It is known that metal precipitates may form bandlike states in the silicon bandgap [10-13]; the origin of these bandlike states could be interface states formed at the precipitate/silicon interface, or bounding dislocations. The processes of recombination at metal precipitates do not easily lend themselves to computer modeling due to the complexity of the phenomena involved in trapping and recombination of carriers at the precipitates [14, 15]. Additionally, the macroscopic minority carrier diffusion length in samples with metal precipitates should also depend on their spatial distribution and spatial density.

Electrical properties of metal precipitates have been successfully studied in intentionally heavily contaminated and rapidly quenched high-quality FZ samples [10, 12, 13], in which metals form such high density ($10^{12} - 10^{14}$ cm^{-3}) of similar in size precipitates that they can be easily studied by DLTS and TEM. In solar cells, metals are often found in clusters at structural defects, may have sizes varied in a large range, and can be separated by hundreds of microns between clusters. It is very difficult to systematically analyze the structure, chemical nature, and recombination properties of such clusters using traditional tools [16]. Additionally, solar cells contain a wide variety of metal clusters of different shapes and chemical origins which simultaneously affect the electrical properties of the material.

Synchrotron radiation based x-ray microscopy tools, which have been first applied to solar cell by McHugo et al. [17-19], and were recently complemented by the XBIC technique [20-23], have been successfully used by our group in the last several years [20, 24-27], enable one to analyze the spatial distribution, chemical state, and recombination activity of metal clusters in mc-Si in situ, nondestructively, and selectively. Application of these techniques to a variety of mc-Si materials allowed us to understand the preferred state of metals in silicon and suggest typical pathways of metal contamination in solar cells. It was found that transition metal precipitates are found in practically all studied mc-Si materials, including block-cast, sheet, and ribbon materials. The density of metal precipitates correlates with the total metal content of the material (which to a large extent is determined by the quality of the feedstock used for its production), and with the thermal history of the material (samples which were cooled faster during growth tend to contain higher density of smaller precipitates). The majority of the precipitates contain transition metals with high diffusivity and solubility in silicon, such as Fe, Cu, Ni, or Co. Slowly diffusing metals, such as W or Ti, rarely form isolated precipitates, although can occasionally be observed in metal particles dominated by iron. All observed metal clusters can be divided in two groups: metal-silicide nanoprecipitates (typically less than 50-100 nm), which as a rule do not contain slowly-diffusing metals (although may contain co-precipitated Fe, Ni, or Co, particularly in intentionally contaminated samples), and large (often greater than a micron in size) metal clusters which contain oxidized iron often mixed with slowly diffusing metals such as Ti, W, or Ca.

The chemical state of transition metals has been a topic for discussion since 1999, when McHugo et al. [28] observed oxidized metal clusters in electromagnetic cast mc-Si. Since binding energy of metals to metal-oxides is much higher than to metal silicide, presence of oxidized

metal species could explain difficulties with removal of transition metals from mc-Si wafers by gettering. In order to predict response of metal clusters to rapid thermal anneals and gettering treatments, it was critical to understand the origin of the oxidized species and the likelihood of their formation inside of the silicon. The abundance of oxygen and dissolved metals in mc-Si is clearly a factor which favors the formation of metal oxides. However, analysis of thermodynamics of reactions of oxygen with metals in silicon revealed that oxygen is stronger bound to silicon than to the majority of metal species (with the exception of several heavy metals such as Hf or Zr) [26]. This implies that the reaction of oxidation of metals in silicon is less likely than the reverse reaction of reduction of metal oxides to metal silicides. Additionally, it would take a very long time, particularly for slow diffusing metals, to form a particle with the size over a micron. Therefore, we concluded that the oxidized particles are inclusions, which were introduced into the melt with the feedstock or from the growth interfaces, did not get completely dissolved in the silicon melt, and were trapped in the crystal. An additional fact supporting this model is the observation that only oxidized iron (which has the melting temperature higher than the melting point of silicon), but not oxidized copper (which has a lower melting temperature than silicon) inclusions were found [26, 27].

Metal clusters were found predominantly at grain boundaries, although some materials (such as sheet material) had metal clusters also at intragranular defects. We have indications that some grain boundaries are more preferred for metal precipitation than the others. This is probably determined by the degree of disorder at grain boundary interfaces and the amount of local strain, and seems to correlate with the index of the boundaries. Twin boundaries in string ribbon mc-Si seem to have the lowest probability of nucleating metal precipitates, and therefore have lower recombination activity than the other types of grain boundaries [29].

Once we have understood the spatial distribution of transition metal clusters and their chemical state, the pathways of metal contamination can be discussed in greater details. First of all, some transition metals are introduced together with the feedstock (either dissolved in the silicon or as metal particles). Recycled silicon feedstock has higher contamination levels than high quality electronic-grade silicon. Additionally, on the growth stage, metals can be introduced from the growth surfaces (dies, crucibles, belts, etc.), both by etching of the surfaces of crucibles of dies by molten silicon and by diffusion of impurities from furnace parts into the melt. Our recent analysis of the potential contamination from silicon-nitride crucible coating provides a good example (briefly described below, and presented in detail in a separate poster paper in these proceedings, [30]).

One of the implementations of casting technology used by the PV industry is directional solidification of silicon ingots in quartz or graphite crucibles coated with sintered silicon nitride layer. We have analyzed five different α-Si_3N_4 powders obtained from commercial vendors and from one of our industrial collaborators which is representative of the powder which they use to coat crucibles. μ-XRF and μ-XAS maps of the Si_3N_4 powder and cast mc-Si samples were compared. The chemical states of metals in the powders were similar, although the total metal content scaled proportionally to the purity of the powder. It was found that Si_3N_4 powder contained metal precipitates in the chemical state similar to what is found in cast mc-Si ingots: larger particles of a chemical state most similar to Fe_2O_3, and smaller particles of Fe+Cr+Ni (reminiscent of stainless steel) with iron in an Fe^0 charge state (such as in iron silicide, metallic iron, iron carbide, etc.). Other less-frequently-observed impurity-rich particles contain Cu, Zn, Ti, Cr, Ni, Co, or Ca. The density of metal precipitates in the ingots was higher in the areas near the sides and the bottom of the ingot, i.e., in the areas where ingot is in contact with the crucible, and diffusion

of impurities into the ingot is likely. Additionally, the top layer of the cast ingot contained high density of Si_3N_4 precipitates, which are typical only for the ingot-casting technology and are thought to be formed by precipitation of nitrogen dissolved from the crucible lining. All these factors indicate that Si_3N_4 crucible lining is a likely source of metal contamination, which occurs either through diffusion of metals from the crucible lining into the silicon ingot, or via slow dissolution or flaking off of the silicon nitride coating together with metal particles.

There are certainly ways how one can reduce process and equipment-originated contamination by using cleaner materials, or stricter contamination control in the production. On the other hand, the question which is often discussed is "how dirty is too dirty?", i.e., what metal content in the feedstock can be tolerated by solar cells, so that the efficiency losses due to metal contamination are offset by the lower cost of the cells. Practically, this implies that the existing gettering/passivation technologies should be optimized to make them robust against high metal contamination levels, and novel methods for reduction of the impact of transition metals on solar cell efficiency should be developed. We believe that these tasks open excellent opportunities for materials science research.

We see three means of reduction of the metal content or reduction of the impact of metals on solar cell performance: gettering, passivation, and defect engineering. These will be discussed below.

Gettering is removal of metals from the bulk of the wafers to the near-surface areas where they are less detrimental. It is limited by several factors. First, it is limited by the kinetics of dissolution and diffusion of metals towards the gettering layer [31]. Indeed, typical aluminum or phosphorus diffusion gettering is performed for a relatively short time (a few minutes) at temperatures from 700^oC to 1000^oC as it is combined with emitter diffusion or backside contact firing. In order to transport metals from metal precipitates to the gettering layer, they have to be dissolved and have to diffuse a distance which on average is equal to half of the wafer thickness. Under the condition when the total metal content of the wafer is much greater than the metal solubility at the gettering temperature, a complete gettering may take many hours. Indeed, the NAA study of Macdonald et al. [9] revealed that gettering during emitter diffusion removes only a fraction of the total metal content. The second factor limiting gettering is the capacity of the gettering layer, which is much thinner than the mc-Si wafer. Consequently, the metal concentration in the gettering layer increases much faster than it is decreases in the wafer, and equilibrium determined by the segregation coefficient between the gettering layer and the substrate can be established way before the metals get removed from the substrate [26, 32, 33]. Gettering efficiency can be further reduced by stabilization of some metal clusters by the strain fields of extended defects, or segregation of metals in the vicinity of structural defects. Despite these limitations, gettering is an efficient means to remove most recombination active interstitial or substitutional metals, leaving behind metal precipitates with lower recombination activity per metal atom. The key factor for the optimization of gettering is optimization of the gettering anneal as to reduce the probability of dissolution of the existing metal precipitates. Our analysis of samples processed by RTP at different temperatures indicates that lower processing temperatures and slower cooling is a good way to "minimize the damage" from dissolved metals and get the most from the gettering treatment. It should be kept in mind that dissolution of metal clusters can occur at any high-temperature step, and therefore every step has to be carefully optimized.

Hydrogen passivation. Despite the fact that hydrogen passivation is widely used by the photovoltaic industry to reduce recombination activity of defects, the physical phenomena involved in passivation of defects, and particularly of metal clusters, are poorly understood. It is

thought that the mechanism of passivation is the formation of metal-hydrogen complexes which substitute deep energy levels in the bandgap with shallow ones, or remove levels completely, thus reducing the recombination activity of the metals. However, the energy levels of interstitial/substitutional metals and metal-hydrogen complexes reported in the literature in the recent years reveal that metal-hydrogen complexes form multiple energy levels which are not necessarily shallower than the levels of the isolated metal species [34-43], see Fig. 1. Why is then hydrogen passivation works? Is it interaction of hydrogen with metal precipitates rather than with isolated metal species (which can be removed by gettering)? How does it depend on the chemical origin and size of metal clusters? Why some defects are passivated while others are not? There are many more questions than answers in hydrogen passivation of metal clusters, and there is a lot to be learned in this area. An interesting additional fact which was observed in our XRF analyses of hydrogenated samples is that heat treatment used during hydrogenation, either by remote plasma or by silicon nitridization, changes the distribution and size of metal clusters through a process similar to Ostwald ripening. It is not completely clear at this time if this is only the effect of a heat treatment applied during hydrogenation, or if hydrogen can stimulate dissociation of metal clusters and diffusion of metals.

Finally, the area of <u>defect engineering of metals</u> is extremely promising. It is now clear that the minority carrier diffusion length of metal-contaminated mc-Si depends not only on the total metal content, but also on the spatial distribution of metals. Generally, it is better to have a low density of relatively large metal precipitates as far away from the p-n junction as possible than all these metals dissolved in the interstitial form or spread through the sample in a high density of tiny clusters. We introduced the term "defect engineering of transition metals in solar cells" to describe the process of transformation of transition metals into their least recombination active state. This concept may appear to be similar to gettering, but there is one important difference. Gettering removes metals away from the device-active area by collecting them at intentionally created sinks. Defect engineering of metals does not remove metals from the device area (which in the case of a solar cell is the whole wafer thickness), but changes their distribution and/or chemical state.

We do not have a readily available answer how to achieve the goals of defect engineering, although the first results are promising [44]. It took over 40 years to develop gettering to its current state of understanding, and we expect that it will take substantial research efforts to develop good defect engineering techniques, which, when complemented with the existing and improved gettering and hydrogen passivation techniques, would allow the PV industry to use lower grade feedstock, thus reducing the production costs.

The possible ways how metals can be engineered in solar cells could include changing concentrations of silicon native defects (vacancies and interstitials), using sophisticated cooling profiles to stimulate growth of larger metal precipitates at the expense of smaller ones, or even utilizing formation of complexes between metals. The formation of such complexes is indeed possible: recently we discovered that under certain conditions iron, copper, and nickel tend to form a ternary compound instead of forming isolated or co-precipitated silicides [45]. The impact of these new compounds on recombination activity of metal clusters or on the stability of metal precipitates has yet to be studied.

To summarize, transition metals is one of chief recombination active defects in multicrystalline silicon solar cells, common to all technologies. Progress in understanding the spatial distribution, chemical state, and sources of metal contamination lead us to better understanding of the impact of metals on solar cell performance and opened new exciting areas of research such as

metal defect engineering. Improved understanding of the contamination pathways and behavior of metals in silicon is vital for further improvement of solar cell efficiency.

FIGURES
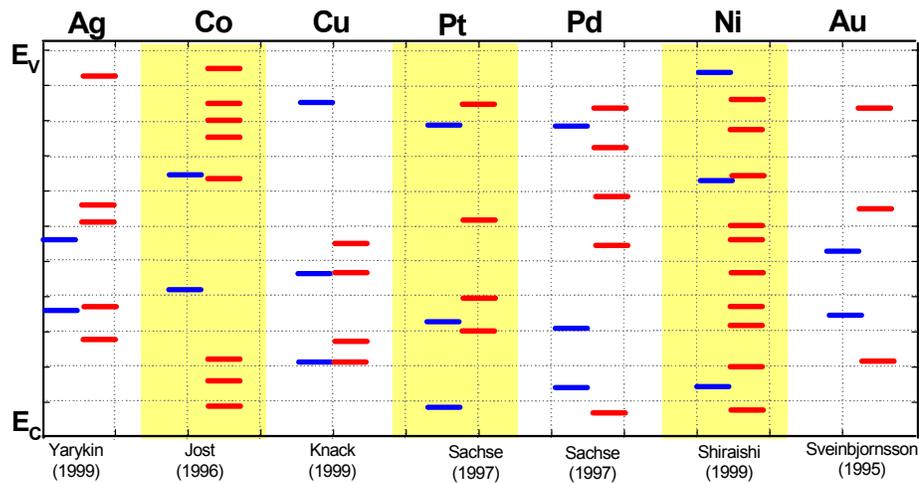
Fig. 1. Energy levels associated with several common transition metals in silicon and with complexes of these metals with hydrogen [34-43]. The (blue) bars on the left represent levels of the isolated interstitial or substitutional metal, the (red) bars on the right represent levels of complexes with hydrogen (which may consist of one, two, or three hydrogen levels). This plot shows that the model which assumes that hydrogenation either removes metal impurity levels completely, or converts them to shallow levels, is a significant oversimplification.

REFERENCES

1. A. A. Istratov, H. Hieslmair, and E. R. Weber, *Appl. Phys. A* **70**, 489 (2000).
2. M. B. Shabani, T. Yoshimi, and H. Abe, *J. Electrochem. Soc.* **143**, 2025 (1996).
3. A. A. Istratov and E. R. Weber, *J. Electrochem. Soc.* **149**, G21 (2002).
4. J. Cao, M. Prince, and J. P. Kalejs, *J. Cryst. Growth* **174**, 170 (1997).
5. Y. Yang, S. Mil'shtein, J. T. Borenstein, and J. I. Hanoka, *Appl. Phys. Lett.* **56**, 2222 (1990).
6. J. Bailey and E. R. Weber, *phys. stat. sol. (a)* **137**, 515 (1993).
7. A. A. Istratov, T. Buonassisi, R. J. McDonald, A. R. Smith, R. Schindler, J. A. Rand, J. P. Kalejs, and E. R. Weber, *J. Appl. Phys.* **94**, 6552 (2003).
8. D. Macdonald, A. Cuevas, A. Kinomura, Y. Nakano, and L. J. Geerligs, *J. Appl. Phys.* **97**, 33523 (2005).

9. D. Macdonald, A. Cuevas, A. Kinomura, and Y. Nakano, in *29th Photovoltaic Specialists Conference*, p. 285, IEEE, New Orleans, LA (2002).

10. W. Schröter, J. Kronewitz, U. Gnauert, F. Riedel, and M. Seibt, *Phys. Rev. B* **52**, 13726 (1995).

11. W. Schröter, V. Kveder, M. Seibt, H. Ewe, H. Hedemann, F. Riedel, and A. Sattler, *Mater. Sci. Engin. B* **72**, 80 (2000).

12. F. Riedel and W. Schröter, *Phys. Rev. B* **62**, 7150 (2000).

13. A. A. Istratov, H. Hedemann, M. Seibt, O. F. Vyvenko, W. Schröter, T. Heiser, C. Flink, H. Hieslmair, and E. R. Weber, *J. Electrochem. Soc.* **145**, 3889 (1998).

14. H. Hedemann and W. Schröter, *Solid State Phenom.* **57-58**, 293 (1997).

15. H. Hedemann and W. Schroeter, *J. de Physique III* **7**, 1389 (1997).

16. A. A. Istratov, H. Hieslmair, O. F. Vyvenko, E. R. Weber, and R. Schindler, *Solar Energy Materials & Solar Cells* **72**, 441 (2002).

17. S. A. McHugo, A. C. Thompson, I. Perichaud, and S. Martinuzzi, *Appl. Phys. Lett.* **72**, 3482 (1998).

18. S. A. McHugo, A. C. Thompson, C. Flink, E. R. Weber, G. Lamble, B. Gunion, A. Mac-Dowell, R. Celestre, H. A. Padmore, and Z. Hussain, *J. Cryst. Growth* **210**, 395 (2000).

19. S. A. McHugo, A. C. Thompson, A. Mohammed, G. Lamble, I. Perichaud, S. Martinuzzi, M. Werner, M. Rinio, W. Koch, H. U. Hoefs, and C. Haessler, *J. Appl. Phys.* **89**, 4282 (2001).

20. T. Buonassisi, I. A.A., M. D. Pickett, M. A. Marcus, G. Hahn, S. Riepe, J. Isenberg, W. Warta, G. Willike, T. F. Ciszek, and E. R. Weber, *Appl. Phys. Lett.*, in print (2005).

21. O. F. Vyvenko, T. Buonassisi, A. A. Istratov, H. Hieslmair, A. C. Thompson, R. Schindler, and E. R. Weber, *J.Appl.Phys.* **91**, 3614 (2002).

22. H. Hieslmair, A. A. Istratov, R. Sachdeva, and E. R. Weber, in *10-th workshop on crystalline silicon solar cell materials and processes,* B. L. Sopori, Editor, p. 162, NREL, Golden, CO (2000).

23. T. Buonassisi, A. A. Istratov, M. D. Pickett, M. A. Marcus, G. Hahn, S. Riepe, J. Isenberg, W. Warta, G. Willike, T. F. Ciszek, and E. R. Weber, in this volume.

24. O. F. Vyvenko, T. Buonassisi, A. A. Istratov, E. R. Weber, M. Kittler, and W. Seifert, *J. Phys.: Cond. Matter* **14**, 13079 (2002).

25. T. Buonassisi, O. F. Vyvenko, I. A.A., E. R. Weber, G. Hahn, D. Sontag, J. P. Rakotoniaina, O. Breitenstein, J. Isenberg, and R. Schindler, *J. Appl. Phys.* **95**, 1556 (2004).

26. T. Buonassisi, M. A. Marcus, A. A. Istratov, M. Heuer, T. F. Ciszek, B. Lai, C. Zhonghou, and E. R. Weber, *J. Appl. Phys.* **97**, 63503 (2005).

27. T. Buonassisi, A. A. Istratov, M. Heuer, M. A. Marcus, R. Jonczyk, J. Isenberg, B. Lai, C. Zhonghou, S. Heald, W. Warta, R. Schindler, G. Willeke, and E. R. Weber, *J. Appl. Phys.* **97**, 74901 (2005).

28. S. A. McHugo, A. C. Thompson, G. Lamble, C. Flink, and E. R. Weber, *Physica B* **273-274**, 371 (1999).

29. T. Buonassisi, G. Hahn, A. M. Gabor, J. Schischka, A. A. Istratov, M. D. Pickett, and E. R. Weber, in this volume.

30. T. Buonassisi, A. A. Istratov, M. D. Pickett, J. P. Rakotoniaina, O. Breitenstein, M. Marcus, S. Heald, and E. R. Weber, in this volume.

31. P. S. Plekhanov, R. Gafiteanu, U. M. Gosele, and T. Y. Tan, *J. Appl. Phys.* **86**, 2453 (1999).

32. S. M. Myers, M. Seibt, and W. Schröter, *J. Appl. Phys.* **88**, 3795 (2000).

33. H. Hieslmair, S. A. McHugo, A. A. Istratov, and E. R. Weber, in *Properties of Crystalline Silicon,* R. Hull, Editor, p. 775, INSPEC, Short Run Press, Exeter (1999).
34. N. Yarykin, J. U. Sachse, H. Lemke, and J. Weber, *Physical Review B-Condensed Matter* **59**, 5551 (1999).
35. W. Jost, J. Weber, and H. Lemke, *Semicond. Sci. Technol.* **11**, 525 (1996).
36. S. Knack, J. Weber, H. Lemke, and H. Riemann, *Physical Review B-Condensed Matter* **65**, 165203/1 (2002).
37. S. Knack, J. Weber, and H. Lemke, *Physica B* **273-274**, 387 (1999).
38. J. U. Sachse, E. O. Sveinbjornsson, W. Jest, J. Weber, and H. Lemke, *Phys. Rev. B* **55**, 16176 (1997).
39. M. Shiraishi, J. U. Sachse, H. Lemke, and J. Weber, *Mater. Sci. Eng. B* **58**, 130 (1999).
40. E. O. Sveinbjornsson and O. Engstrom, *Physical Review B-Condensed Matter* **52**, 4884 (1995).
41. J. U. Sachse, E. O. Sveinbjornsson, N. Yarykin, and J. Weber, *Materials Science & Engineering B* **58**, 134 (1999).
42. J. Weber, S. Knack, and J. U. Sachse, *Physica B* **273-274**, 429 (1999).
43. J. U. Sachse, J. Weber, and H. Lemke, *Physical Review B-Condensed Matter* **61**, 1924 (2000).
44. T. Buonassisi, A. A. Istratov, M. A. Marcus, B. Lai, Z. Cai, S. M. Heald, and E. R. Weber, *Nature Materials*, manuscript NM05030414 accepted for publication on 6/30/2005 (2005).
45. M. Heuer, T. Buonassisi, M. A. Marcus, A. A. Istratov, M. D. Pickett, and E. R. Weber, in this volume.

Nature of the metastable boron-oxygen complex in crystalline silicon

Richard Crandall

National Renewable Energy Laboratory, Golden, CO 80401

Abstract

I measured the rates of light-induced metastable defect formation and annealing in boron doped Czochralski silicon solar cells using transient capacitance techniques. These measurements also make the first determination of the number of metastable defects typically produced by illumination; less than 10 % of the boron doping. These measurements support a model of the defect involving an oxygen dimmer bound to a boron dopant.[2] In addition I was unsuccessful in measuring the defect transition level using light-flash deep-level transient-spectroscopy.

Introduction

The efficiency of crystalline solar cells made from boron-doped Czochralski silicon (Cz-Si) degrade by as much as 10 % during operation. This is a serious problem for the widespread use of low cost b-doped Cz-Si for photovoltaic, PV, applications. One must either use float zone c-Si to reduce the oxygen or another dopant for high efficiency cells. Both of which are costly for the industry

Approximately 90% of the present world solar cell production is based on boron-doped silicon with Czochralski silicon (Cz-Si) having about 40% of that market and low cost multicrystalline-Si (mc-Si) cells about 50%. Although the initial efficiency of the Cz-Si cells is higher than the mc-Si cells, the former degrade to nearly the efficiency of the later after a few hours of illumination. This is due to the fact that mc-Si cells are, in most cases, stable under illumination. Since, in general, Cz-Si is more costly than mc-Si, the future of solar grade Cz-Si depends crucially on whether it is useable for mass-production of high-efficiency solar cells or not. By annealing the Cz-Si cells to 200 ˚C for a few minutes, the original efficiency is restored. However, this cure is certainly not feasible in practice.

From varies investigations of this metastability, it has been established that it is only present when both B and O exist in the Si. A quadratic correlation of the relative number of defects/boron atom on the oxygen concentration has led researchers[1] to postulate that the defect is a BO_2 defect. However, its exact structure is unknown. In fact its charge state is also unknown although it is doubtful that it would be negative if charged since it would not then be an efficient recombination center.

Numerous researchers have performed a variety of measurements in an attempt to unravel the nature of the defect in hopes of curing the degradation. See Refs. [1] and [2] and references therein. A reduction in the minority-carrier lifetime or open-circuit voltage are the main tools used for study since these reduce the efficiency. Deep-level transient spectroscopy, DLTS, has so far been unsuccessful in measuring the energy level in light

degraded material. Thus one does not even know whether the defect lies above or below the Fermi level and what is its capture cross-section. Similarly the number of defects is unknown.

The generation and annealing kinetics of the defect have been studied by various authors. The latest results show that it has an activation energy of 1.3 eV and 0.4 eV for annealing and generation, respectively.[1]

By measuring the capacitance during annealing of the defects in a degraded boron-doped CZ-Si solar cell I have made the first determination of the charge state of the defect causing the metastability and determined its density. We find that the defect is positively charged which explains why it is a good minority carrier trap. In a degraded cell the defect density is at most a few percent of the boron density.

Experimental

Measurement technique

To determine the charge trapped on metastable defects, I apply the familiar junction-capacitance method. The capacitance is measured using a lock-in amplifier (Stanford Instruments Model 850) at a frequency of 100 kHz and an ac test voltage of about 0.03 V rms. The device is mounted on a heated sample holder capable of maintaining a stable temperature (+/- 0.1 K) between 100 K and 600 K.

The samples are standard p-type B-doped Cz-Si solar cells with B doping of 1.2 and 13 x 10^{+15} cm^{-3} and Al back contacts. The lightly doped sample used a P doped diffused junction whereas the heavily doped base used an amorphous silicon heterojunction for the emitter. [3]

I measure the annealing kinetics of the B-O metastable defects by means of the following procedure:

1) samples are heated to about 500 K at the reverse bias used for measurement until any defects present are annealed. This usually takes about 10 min.

2) the temperature is then lowered to the measurement temperature and the bias is changed to 0 or a small forward bias and the device is illuminated long enough to form the metastable defects. Typically a few minutes at high measurement temperature. I find that if the bias is not changed to collapse part of the depletion region, there is no measurable degradation; presumably because the photo-generated electrons are swept out of the depletion region before they can form a defect.

3) the light is then removed and simultaneously the bias is switched back to its initial reverse value and the capacitance is monitored until it returns to its initial value when all the metastable defects are removed. Figure 1 shows a typical transient for hole detrapping

Steps 2) and 3) are repeated at different temperatures. By this method the defect annealing energy is determined from an Arrhenius plot of the logarithm of the annealing time versus inverse temperature. The annealing time is determined from a fit of an

exponential decay of the form $\dfrac{\Delta C(t)}{C} = A\,e^{-\frac{t}{\tau}}$ where C is the initial capacitance and

ΔC(t) is the change in capacitance. For more details on this type of experiment see Ref. [4]

To determine the rate of degradation of a fully annealed cell I use the following procedure.

1) the capacitance is measured at reverse bias of, for example, -1 V.

2) Then the bias is switched to 0 or a small forward bias and the sample is illuminated, for example, 10 s.

3) The light is turned off and the bias is returned to its initial reverse value for capacitance measurement. Since this measurement takes less than 2 s there is no annealing of the defects produced by light.

The entire sequence is repeated at a variety of temperatures to determine the activation energy for degradation.

Results

Transient during Annealing

Figure 1 shows an annealing transient for a solar cell containing 1.3 x 10^{+16} cm^{-3} boron. The measurement temperature is 410 K. The bias during the illumination to cause degradation is 0 V and the bias during the transient is -1V. The illumination cycle is 200 s. The initial decrease in capacitance, ΔC(t)<0, at 1 s shows the depletion width initially widens owing to compensation of some of the original depletion charge. This indicates that holes (majority carriers) are deeply trapped. Any free holes are swept out at very short times. At longer times the holes are emitted from the traps until finally at 1000 s all holes are emitted and swept from the depletion width and the capacitance returns to its initial value.
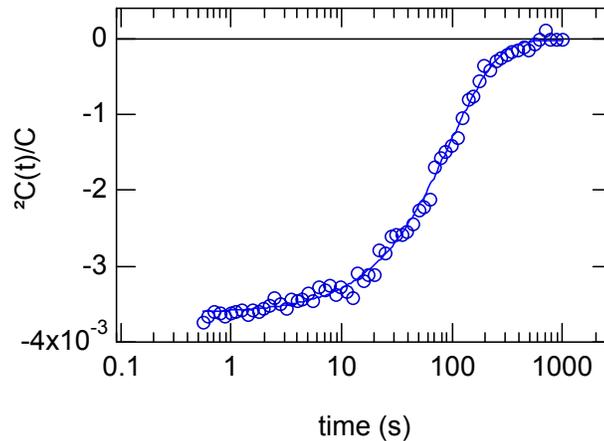
Figure. 1 Relative capacitance change versus annealing time at 410 K. Circles are measured values and the line is a fit to the data.

Using the depletion width approximation the trapped charge, N(t), is related to the

capacitance by: $\frac{N(t)}{N} = 2\frac{|^2\ C(t)|}{C}$ where

N is the depletion charge or density of boron. For this sample the boron concentration is $1.3 \times 10^{+16}$ cm^{-3}. Thus nearly 10^{+14} cm^{-3} defects are formed in this pulse. The initial value of the transient gives the maximum number of defects formed. This type of measurement is carried out at temperatures ranging between 370 and 440 K.

The solid line in the figure represents the function $\frac{^2\ C(t)}{C} = -\frac{N(t)}{2N}e^{-\frac{t}{\tau}}$ where t is the measuring time and τ the characteristic annealing time. For the data in Fig. 1 τ is 99 s. This function fits the well over the temperature range.

Figure. 2 Relative capacitance change versus annealing time at 410 K. Circles are measured values and the line is a fit to the data.

To determine the annealing activation energy the values of τ are plotted versus inverse measurement temperature to construct an Arrhenius plot. This plot is shown in Fig. 2. The annealing activation energy, ΔE_{act} is determined from the slope of the plot in the usual way. The activation energy of 1.3 eV is identical to the value determined by Schmidt and Bothe using minority-carrier lifetime as a measure of the defects.[1] The figure also shows a point, solid circle, for degradation at room temperature, but measured at elevated temperature. The agreement with the high temperature degradation shows that the temperature of degradation does not affect the annealing rate.

Degradation

A typical low temperature degradation transient is shown in Fig. 3. The transient initially rises above 0 indicating some electron trapping. Detailed analysis by varying bias and pulse conditions show that the electrons are trapped at the interface in the vicinity of the amorphous silicon heterojunction. It is unlikely that electron trapping at the interface is not part of defect formation. The decrease in capacitance appearing at long times shows that holes are trapped in the depletion region. As above, the depletion width approximation permits a determination of defects formed

Figure 3. Change in capacitance measured at reverse bias during light-induced charge trapping. Measurement temperature is 360 K. Illumination is 15 W cm^{-2}.

during degradation. At the longest time where the degradation saturates about 4 % of the initial boron can be converted to metastable defects. The solid curve in the figure is a fit of an exponential function similar to one used for annealing. From this function the degradation time is found to be 2060 s at 360 K.

By measuring degradation at a variety of temperatures and making an Arrhenius plot the degradation activation energy can be determined. Figure 4 shows the Arrhenius plot for degradation. The data from Schmidt and Bothe using minority-carrier lifetime to probe the defects is plotted for comparison.[1] From the capacitance the degradation activation energy is 0.17 eV. From the lifetime the activation energy is 0.4 eV. At first glance one might conclude that the two techniques measure different defects. However, I do not think this is the case since the data do not overlap in the same temperature range. By extrapolating the solid line fits to the data to high and low temperature one immediately sees that at high temperature process observed at low temperature is too fast to be a bottleneck affecting the capacitance measurements and at low temperature the process measured by capacitance is too fast to be a bottleneck affecting the lifetime measurements. I will say more about these two processes in the discussion.

Defect transition level

Rein and Glunz used advanced lifetime spectroscopy coupled with Schockley-Read-Hall analysis to determine the defects energy level in the gap.[5] They found that the level is 0.41 eV below the conduction band and that the level is an attractive Coulomb center. To my knowledge there are no reports of successfully using DLTS to measure the energy level.

The standard method of measuring energy levels is by using DLTS.[6] Using standard bias pulse DLTS will not work to find the defect energy since this method predominantly injects holes into the depletion region and the B-O defect should be an electron trap. However, one expects light-flash DLTS might be able to detect minority carrier, electron, traps since the light generates both electrons and holes.

I used a bias of -3 V and weak light flashes from 1 µs to 1 s and varied the temperature between 100 and 300 K. The entire capacitance transient to 10 s was measured and signal averaging increased the sensitivity to measure defects in concentrations as low as 10^{+12} cm^{-3}. Since the most recent estimates place the transition level at 0.5 eV, this temperature range was sufficient to detect this and deeper or shallower levels. Although I did observe shallow electron traps, these traps were present in either an annealed or fully degraded state.
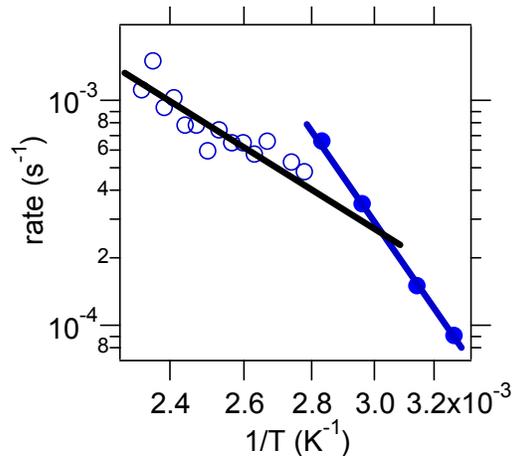
Figure 4. Arrhenius plot of the characteristic degradation time under illumination. The open circles are from capacitance measurements and the solid circles are from lifetime measurements.[1]

Discussion

The annealing behavior of the B-O defect studied by capacitance agreed well with the data determined by lifetime recovery.[1] The result that the defect has a net positive charge supports both the theory of Adey et al.[7] and Du et al.[2] who show that the defect consists of a negatively charged boron bound to a doubly positive charged oxygen dimer. Both models predict an annealing energy of about 1.3 eV.

The degradation data measured by capacitance, however, does not agree with the lifetime degradation measurement.[1] To resolve this discrepancy one needs the theory of Du et al.[2] who show that the initial steps in the defect formation, oxygen dimer diffusion,[7] have two activation energies. One is for hole capture by the positive oxygen dimer in the staggered configuration.[2] Typically charge capture by a repulsive barrier is about 0.4 eV.[8] Following this capture, the dimer reconfigures to the square configuration to continue diffusing. The predicted activation energy for this step is 0.17 eV is the same as measured by capacitance. Thus the lifetime and capacitance measurements are good support of the model of Du et al.[2]

To understand the failure to observe the defect transition level one again turns to the theory of.[2] They show that once an electron is not trapped by a well defined level of the defect but rather undergoes self trapping. First the electron is trapped at 0.2 eV below the conduction band. This level then moves rapidly below midgap before the electron is thermally emitted. Thus it will be difficult to observe in light-flash DLTS.

Summary

Using transient capacitance I measured an annealing activation of the B-O defect in CZ-Si. The value is 1.3 eV, the same as measured by transient lifetime measurements.[1] For defect formation the activation energy is 0.17 eV. This value is different from that measured by lifetime degradation.[1] because the former is measured at high temperature and the latter at low temperature. A search for the defects electron trapping level using light pulse DLTS was unsuccessful.

Acknowlegement

References

1.	Schmidt, J. and K. Bothe, *Structure and Transformation of the metastable B-O complex in Si.* Phys. Rev. B, 2004. 69: p. 024107.

2.	Du, M.-D., et al., *Self-trapping-enhanced carrier recombination at boron-oxygen complexes in Silicon*, in *15th Workshop on Crystalline Silicon Solar Cells and Modules: Materials and Processes*. 2005: Vail CO.

3.   Wang, Tihu et al., in *14th Workshop on Crystalline Silicon Solar Cells and Modules: Materials and Processes*. 2004: BreckenRidge CO..

4.   Crandall, R.S., *Meyer_Neldel Rule in Charge-Trapping Metastability in p-type Hydrogenated Amorphous Silicon.* Phys Rev. B, 2002. 66: p. 195210.

5.   Rein, S. and S.W. Glunz, *Electronic properties of the metastable defect in boron-doped Czochralski silicon: Unambiguous determination by advanced lifetime spectroscopy*. Appl. Phys. Lett., 2003. 82(7): p. 1054-1056.

6.   Lang, D.V., J. Appl. Phys., 1974. 45: p. 3023.

7.   Adey, J., et al., *Interstitial boron defects in Si.* Physica B-Condensed Matter, 2003. 340: p. 505-508.

8.   *Electronic Materials Science: For Integrated Circuits in Si and GaAs*, J. W. Mayer and S. S. Lau, Macmillan Publishing, New York, 1990.

PASSIVATING MULTI CRISTALLINE Si SOLAR CELLS USING SiN$_x$:H

I. G. Romijn, W. J. Soppe, H. C. Rieffe, W. C. Sinke, A. W. Weeber
ECN Solar Energy, P. O. Box 1, 1755 ZG Petten, The Netherlands
email: romijn@ecn.nl

ABSTRACT:

Passivating solar cells with SiN$_x$:H has been so far a scarcely understood effect that can only be optimized for cell production in an empirical way. In this study we determine the structural properties of SiN$_x$:H layers with Fourier Transform Infrared (FTIR) measurements and relate these to both the deposition parameters and its passivating qualities for solar cells. Furthermore we determined the relations between the hydrogen diffusion in the SiN$_x$:H and the structural properties of these layers.

The Si-N, Si-H and N-H bond densities for layers deposited with either nitrogen (N$_2$), ammonia (NH$_3$) or deuterated ammonia (ND$_3$|) and silane (SiH$_4$) are affected by the N/Si flow ratio and the pressure p in a similar way although the differences in dissociation energy and rate cause different deposition mechanisms. Comparing the Si-N and Si-H bond densities found for NH$_3$ and ND$_3$ grown layers, we find that roughly 25% of the hydrogen in the SiN$_x$:H layers stems from the ammonia precursor gas, while 75% stems from the silane.

We show that Si-N bond density is an important parameter governing both the bulk and surface passivation of the SiN$_x$:H layers. In spite of the different deposition mechanisms, the same relations hold between the H-diffusion coefficient, Si-N bond density and passivating qualities of SiN$_x$:H layers deposited with either N$_2$ or NH$_3$. The best bulk and surface passivating layers have a relatively low hydrogen diffusion coefficient due to a high Si-N bond density. We find optimum values for bulk and surface passivation for Si-N bond densities of $1.3*10^{23}$ cm^{-3}, regardless of the type of SiN$_x$:H used and regardless of the starting wafer quality. Lower Si-N bond densities result in layers with a more open structure and this will probably lead to H$_2$ formation during annealing. These H$_2$ molecules will effuse into the ambient during firing, and do not contribute to the passivation of solar cells. Higher Si-N bond densities result in a too dense structure, prohibiting an effective diffusion of H-atoms into the bulk of the solar cells. This study further indicates that FTIR analysis gives us a quick and reliable tool to check the quality and properties of SiN$_x$:H layers. This will allow optimization of SiN$_x$:H deposition systems without having to make complete solar cells.

1 INTRODUCTION

Hydrogenated amorphous silicon nitride layers (a-SiN$_x$:H) have become a very important part of modern silicon PV technology. They act as an anti-reflection coating and provide both bulk and surface passivation, important means for optimizing multi crystalline (mc) Si solar cells and obtaining high efficiencies [1]. The bulk, or defect passivation is achieved by driving hydrogen into the mc Si solar cells by a short thermal anneal [2,3,4]. At the same time, the surface passivation is improved by reducing the number of dangling bonds and creating a positive field effect by K+ centers [5].

On of the key issues of our research is to combine excellent bulk and surface passivation on low cost silicon with easy-to-handle gasses. Relations between structural properties and the quality of bulk and surface passivation of SiN$_x$:H need to be known for better understanding of the underlying physics. So far, passivation with SiN$_x$:H in industry has been a phenomenon that can only be optimized for cell production in an empirical way. This study provides means to determine passivating qualities of SiN$_x$:H independently of the deposition method and without making solar cells.

The amount of hydrogen diffusion from the SiN$_x$:H layer into the silicon wafer largely determines the quality of bulk passivation. Numerous generic studies of hydrogen diffusion in silicon nitride films have been reported [6,7,8,9], but studies on the relation between hydrogen diffusion in silicon nitride and bulk passivation are rather scarce [10,11]. The surface passivation is commonly related to the refractive index [5,12] and not to the structural properties. Only Mäckel and Lüdemann [13] and ECN [14] performed such a study. In recent publications, Weeber et al. [14,15] presented a systematic investigation on the bulk and surface passivating properties, the hydrogen loss mechanism in the SiN$_x$:H layer, and related these to the structural properties of the SiN$_x$:H deposited with SiH$_4$ and N$_2$. This first study is now extended to the use of NH$_3$ and deuterated ammonia (ND$_3$). The use of ND$_3$ sheds more light on the plasma chemistry and the deposition mechanisms of the SiN$_x$:H layer, while the use of both N$_2$ and NH$_3$ nitrides on solar cells reveals the structural properties of the SiN$_x$:H layers that govern its inherent passivating qualities independent of the deposition mechanisms.

2 EXPERIMENTAL

2.1 Approach
The physics behind the passivating properties of SiN$_x$:H layers is investigated in four steps:

- Deposition of layers on double polished Cz Si wafers for FTIR analysis to obtain bond densities, and relating those to the deposition parameters;
- Application of the examined layers to solar cells; determination of bulk passivating quality by measuring V$_{oc}$ and the Internal Quantum Efficiency at 1000 nm (IQE$_{(1000nm)}$), and relating these to the structural properties;
- Application of the examined layers to FZ Si wafers; determination of surface passivation by measuring the effective lifetime (τ_{eff}) using the Quasi Steady State Photo Conductance method [16] and relating these to the structural properties;
- Annealing of SiN$_x$ layers for increasing time periods at 800 ºC to determine H-diffusivity in the SiN$_x$:H layer and relate that to the structural properties of SiN$_x$:H;

2.2 Deposition of SiN$_x$:H layers
We deposited SiN$_x$:H layers with three different types of nitrogen-containing precursor gases; nitrogen (N$_2$), ammonia (NH$_3$) and deuterated ammonia (ND$_3$). This will allow us to determine whether fundamental relations exist independent of the process gases. Silane (SiH$_4$) was used as silicon precursor gas. The SiN$_x$:H layers were deposited using the in-line microwave remote Plasma Enhanced Chemical Vapor Deposition (MW RPECVD) system at ECN at different process parameters such as pressure and gas flows. This MW RPECVD has been co-developed with Roth and Rau [17].

2.3 FTIR analysis
We determined the bond densities (Si-H, Si-H and N-H) within the nitride layers using FTIR spectroscopy. From the transmission spectrum of the SiN$_x$:H layers deposited on Si substrates the absorption spectrum (k) of the single layer of SiN$_x$:H was calculated according to the method reported by Maley [18]. Subsequently, the bond densities are calculated by integrating the different absorption peaks and multiplying them with a proper proportionality constant [19,20].

2.4 Solar cells
The mc Si solar cells for the determination of the bulk passivation were made using neighboring wafers; the process sequence was: texturing using acidic etching, emitter formation using an infrared heated belt furnace, remote MW PECVD of SiN$_x$:H using the same deposition parameters as for the FTIR samples, metallization using screen printing and contact formation with an infrared heated belt furnace. IV measurements were performed with our Class A solar simulator according to the ASTM-E948 norm; the Internal Quantum Efficiency (IQE) was calculated from the spectral response and the reflectance.

3. EXPERIMENTAL RESULTS AND DISCUSSION

3.1 SiN$_x$:H structural properties related to the deposition parameters
In previous studies it was found that the mass density of the SiN$_x$:H layers is related to the Si-N bond density: layers containing more Si-N bonds have a higher mass density ρ, while those with relatively more Si-Si bonds are less dense and have a more porous structure [14, 21, 22].

In figure 1 and 2 the Si-N bond density for three nitrides deposited with NH$_3$, ND$_3$ and N$_2$ as precursor gasses are shown as a function of the N/Si gas flow ratio, and for different deposition pressures. For all nitrides the Si-N bond densities increase for increasing N/Si flow ratio, and are higher for lower deposition pressures. The refraction index n increases with decreasing Si-N bond density and decreasing N/Si flow ratio, which is shown qualitatively by the arrow in the graphs.
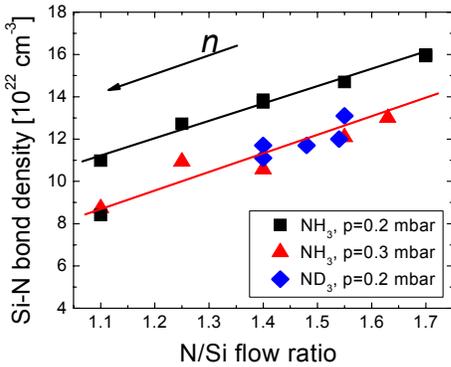
Figure 1: Si-N bond density versus the N/Si flow ratio for nitrides deposited with NH₃ and ND₃ at different pressures.
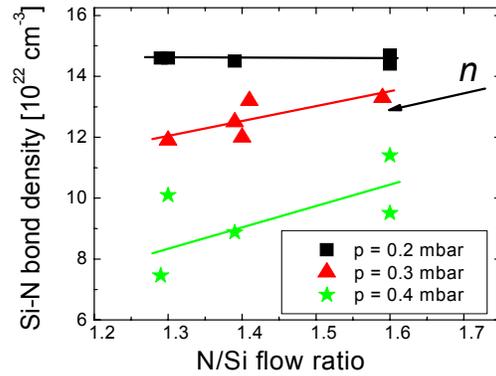
Figure 2: Si-N bond density vs N/Si flow ratio for nitrides deposited with N_2 at different pressures.

In figure 3 and 4 the Si-H and N-H bond densities of the same SiN_x:H layers are shown. For the Si-H and N-H bond densities of the NH_3 and ND_3 nitrides (figure 3) no pressure dependence is found; the Si-H bond density decreases, while the N-H bond density increases with increasing gas flow ratio. The Si-H and N-H bond densities of the N_2 nitrides however, do not significantly depend on the N/Si flow ratio. For these bond densities we see the pressure dependence as a main effect repeated. The points in figure 4 are averages over all values at a certain pressure.
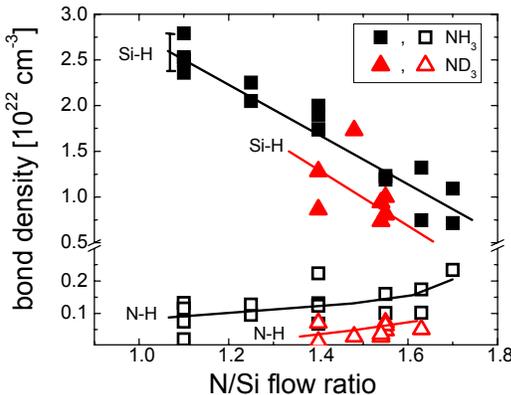
Figure 3: Si-H and N-H bond density versus the N/Si flow ratio for the NH₃ and ND₃ nitrides.
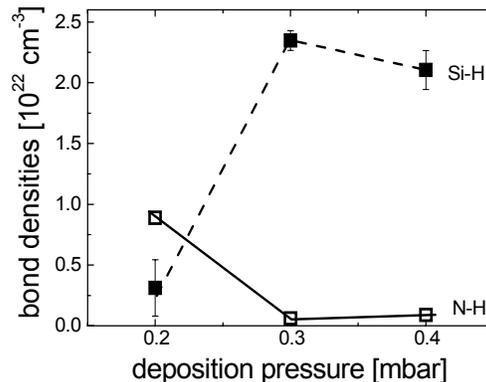
Figure 4: Si-H and N-H bond density versus the deposition pressure for N₂ nitrides.

The bond densities of the nitrides deposited with NH_3 (and ND_3) are stronger dependent on the flow ratio than those of nitrides deposited with N_2, especially at lower pressures (p = 0.2 mbar); the structural properties of N_2 layers depend mainly on the pressure. The increase in Si-N bond density (that we see for all nitrides) with increasing N/Si flow ratio is easily understood. At higher N/Si flow ratios relatively more reactive N-containing species are available; this will favor the formation of Si-N and N-H bonds over that of Si-Si and Si-H. The decrease in Si-H bonds with increasing N/Si flow ratio is only seen for the NH_3 and ND_3 nitrides. Mäckel and Lüdemann [13] found that the Si-N bond density increases (and the Si-H bond density decreases) with increasing N/Si atomic ratio in the layer. This corresponds to our results, since an increasing N/Si flow ratio will increase the N/Si atomic ratio in the layer.

The decrease of Si-N bond density for increasing pressures, also seen in all nitrides, is due to properties of our remote MW PECVD. In our system, the nitrogen containing gas is fed in near the plasma source, while the silane gas is fed in just above the samples. At the microwave source nitrogen (or ammonia) gas is dissociated by electron impact; while the silane in turn is dissociated by either electron impact or by interactions with N- or H- (in case of ammonia) radicals. Besides this, the dissociation of silane can be enhanced or even caused by the high temperatures in the deposition chamber. Higher pressures will confine the nitrogen plasma closer to the

plasma source, and less reactive N-containing species will reach the substrate. This will cause the formation of more Si-rich SiN_x:H layers that are less dense. A more detailed description of the plasma chemistry can be found in other publications [23,24].

The different flow and pressure dependence for both types of nitrides is caused by the difference in dissociation energy for N-N (9.81 eV) and H-NH$_2$ (4.65 eV) [25]. At low pressures, the degree of N$_2$ depletion will saturate for a certain microwave power; rendering the plasma independent on further increasing the N$_2$/SiH$_4$ flow ratio. Due to the lower ionization energy this maximum is not reached for NH$_3$. Within our processing parameters and the depletion of the NH$_3$ is close to 100% [17].

The lower Si-N bond density of the deuterated nitride, when compared to the nitride deposited with NH$_3$, is due to the difference in dissociation rate of NH$_3$ and ND$_3$. This dissociation rate depends on the vibration frequency of the N-D or N-H in the molecule, which is lower for N-D due to the larger mass. The Si-H bond density in the layers deposited with ND$_3$ is 75% of that in the corresponding layer deposited with NH$_3$, while the N-H bond density in layers made with ND$_3$ is hardly 50%. Since (in NH$_3$ and ND$_3$ nitrides) the majority of hydrogen is bonded to Si-atoms (see figure 3), this means that at least 25% of the hydrogen in the SiN_x:H layers stems from ammonia, while roughly 75% stems from silane.

In figure 5 the initial hydrogen fraction of all layers (deposited with N$_2$, NH$_3$ or ND$_3$) is shown against the Si-N bond density. We define the hydrogen fraction as:

$$\text{fraction H} = \frac{[Si\text{-}H] + [N\text{-}H]}{[Si\text{-}H] + [N\text{-}H] + [Si\text{-}N]} \qquad (1)$$
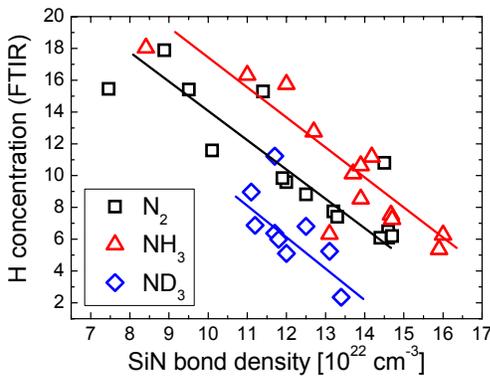
Figure 5: Total hydrogen concentration (calculated from bond densities) for the three different nitrides as a function of the Si-N bond density.

Although there is a lot of variation, the general trend is clear for all layers: with increasing Si-N bond density (and thus layer density) the total H-content decreases. For most SiN_x:H layers deposited with NH$_3$, more hydrogen is incorporated at the same Si-N bond densities than in layers deposited with N$_2$ or ND$_3$. As was found above, in layers deposited with ND$_3$ at least 25% of the hydrogen is replaced by deuterium. But, layers deposited with ND$_3$ also become less dense (lower Si-N bond density) using the same process parameters when compared with layers deposited with NH$_3$ due to the difference in dissociation rate, as was shown in figure 1. Both effects cause the H-content in ND$_3$ layers to be only 50% of the content in NH$_3$ layers at the same Si-N bond densities.

When N$_2$ is used instead of NH$_3$, the total H content decreases by roughly 25%. In this deposition, all hydrogen will stem from the silane; the 25% lower H-content is in agreement with the 25% difference in H-content between layers deposited with NH$_3$ and ND$_3$. This could mean that although the plasma chemistry is different, efficiency of hydrogen incorporation is approximately the same.

3.2 Bulk and surface passivation as a function of Si-N bond density

In previous publications we show that the Si-N bond density is a key parameter for bulk passivation [14,15,26]. Figure 6 shows the V_{oc} of cells made with SiN_x:H layers deposited with N$_2$ or NH$_3$. Wafers of average quality (A) and wafers of higher quality (B) were used. All values of V_{oc} are scaled to the maximum V_{oc} for each experimental run to be able to compare all the data.

From the figure it can be seen that:

- The V_{oc} for cells with SiN_x:H layers deposited with N$_2$ or NH$_3$ have the same dependence of the Si-N bond density.

- The maximum V_{oc} for both material qualities is found at the same Si-N bond density, viz. $1.3*10^{23}$ cm^{-3}. The difference is that for the better quality higher V_{oc} values are found for a broader range of Si-N bond densities.
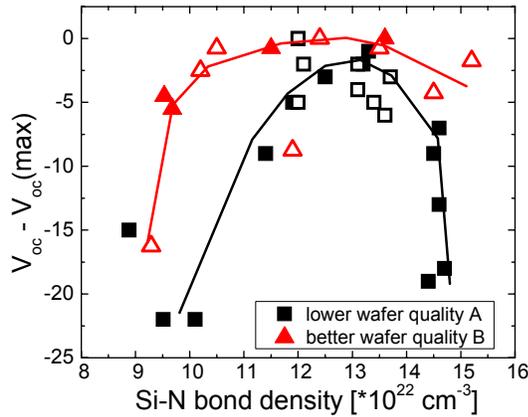
Figure 6: V_{oc}-V_{oc}(max) of mc-Si solar cells versus the Si-N bond density. The squares show the V_{oc} for cells made of average quality (A), the triangles show Voc for cells made of good wafer quality (B). Closed symbols: N_2 nitrides; open symbols: NH_3 nitrides. The lines are guides to the
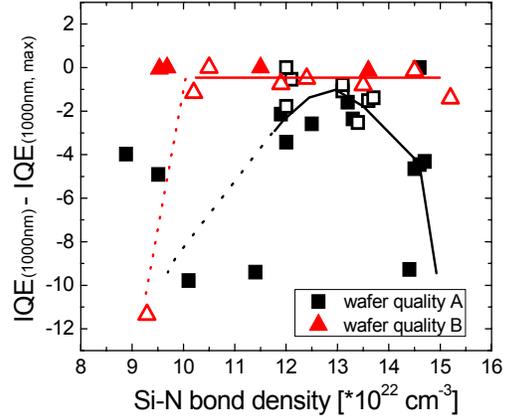
eye.

Figure 7: IQE at 1000 nm for the different solar cells. Again the difference between the different wafer qualities is clearly visible. Closed symbols: N_2 nitrides; open symbols: NH_3 nitrides. The lines are guides to the eye.

We were not able to make solar cells with [Si-N] < $9*10^{22}$ cm^{-3} or [Si-N] > $1.5*10^{23}$ cm^{-3}, because these layers became too inhomogeneous at larger areas.

V_{oc} is determined by both the bulk and surface passivation. To investigate the dependence of the Si-N bond density on bulk passivation the IQE at 1000 nm is shown in figure 7. When the wafer quality is lower (squares in graph 6 and 7), the V_{oc} follows the IQE at 1000 nm indicating V_{oc} is mainly influenced by the bulk properties of the solar cell. In the case of better wafer quality (triangles) however, the IQE remains constant down to very low Si-N bond densities ($1*10^{23}$ cm^{-3}). In this case, the bulk properties remain constant and smaller changes in V_{oc} (<5 mV) are caused by differences in surface passivation; the better surface passivation for Si-N bond densities around $1*10^{23}$ cm^{-3} will be confirmed below. At the lowest bond densities, the drop in IQE reflects a drastic reduction in bulk passivation; this results in an additional loss in V_{oc} of about 10 mV.

The amount of surface passivation can be determined by measuring the effective lifetime of charge carriers in FZ wafers coated with SiN$_x$:H layers. In figure 8 we show the effective lifetimes for N_2 (closed symbols), and some NH_3 (open symbols) grown nitrides with the different Si-N bond densities, before and after a very long anneal (60 min at 800 °C) for the N_2 nitrides, and a shorter anneal for the NH_3 nitrides.
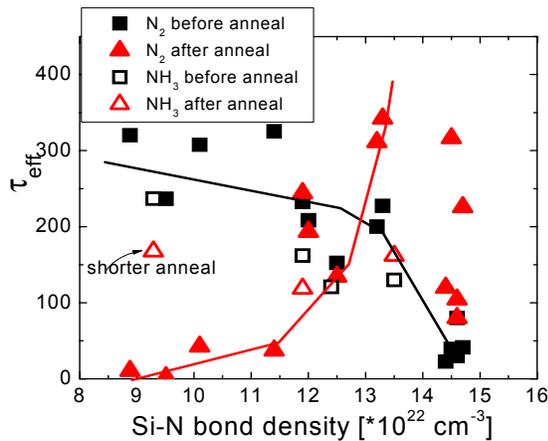
Figure 8: Effective lifetimes of charge carriers in FZ wafers with SiN$_x$:H layers before and after anneal (60 mins, 800 °C). N_2 nitrides: closed symbols, NH_3 nitrides: open symbols.

The figure shows that good initial surface passivation (large τ_{eff}) can be obtained for layers with low Si-N bond densities, but that this surface passivation is not thermally stable after a 60 minute anneal (although the much shorter firing of solar cells does not influence the τ_{eff} this much, see also arrow in figure 8 [23,27]). At high Si-N bond densities, the initial τ_{eff} is low, but after a long anneal the values improve drastically. Around [Si-N] ~ $1.3*10^{23}$ cm^{-3}, τ_{eff} remains constant at high values. At these bond densities, V_{oc} for wafers of good quality reaches its maximum (see figure 6, wafer quality B) that we contribute to the good and stable surface passivation. At higher Si-N bond densities there is a large variation in lifetime after annealing. This means that the best and most stable processing is found at a Si-N bond density of $1.3*10^{23}$ cm^{-3}, the same density as for best bulk passivation.

Combining the results for the bulk and surface passivation, we find optimum values for Si-N bond densities of $1.3*10^{23}$ cm^{-3} for both, regardless of the type of SiN$_x$:H used and regardless of the wafer quality.

3.3 Hydrogen diffusion in SiN$_x$:H layers.

In earlier publications we reported that the best surface and bulk passivation is found for denser layers, with a higher Si-N bond density ($1.3*10^{23}$ cm^{-3}), regardless of the initial amount of hydrogen. In these studies it was postulated that low Si-N bond densities result in more open structures that facilitate the formation of H$_2$ molecules that effuse into the ambient during anneal. This effused hydrogen will not contribute to the bulk passivation. In too dense layers ([Si-N] > $1.3*10^{23}$ cm^{-3}) the H-diffusion into the bulk of the solar cells during short anneals will be too small for good passivation [14,15,26]. In a recent publication, Dekkers et al [11] found that the mass density of the SiN$_x$:H layer governs the diffusion of hydrogen in the layer, denser layers prevent out-diffusion of molecular hydrogen. This publication confirms our earlier findings.

Our previous study on the H-diffusion in SiN$_x$:H and the related passivating properties was performed on SiN$_x$:H layers deposited with N$_2$ and SiH$_4$. This experiment is now extended with layers deposited with NH$_3$ and SiH$_4$. The diffusion of H in the NH$_3$ nitrides is monitored by measuring the Si-H and N-H bond densities as function of the anneal time at 800 ºC.
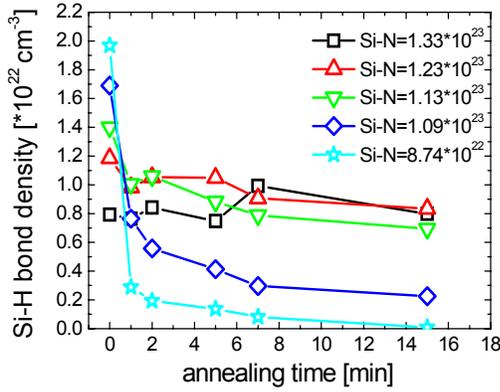
Figure 9: Change in Si-H bond density during anneal for different Si-N bond densities. All layers are deposited with NH$_3$ and SiH$_4$.
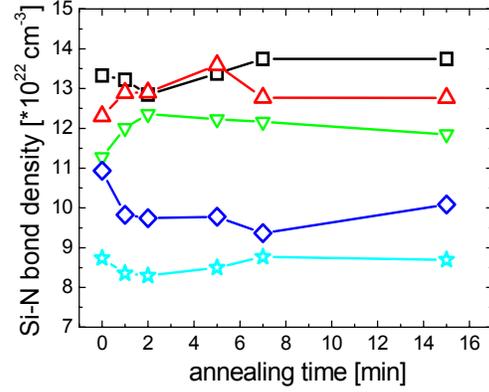
Figure 10: Change in Si-N bond density during anneal. All layers are deposited with NH$_3$ and SiH$_4$. The symbols correspond to those in figure 9.

In figure 9 the change in Si-H bond density upon annealing at 800 ºC is shown for layers with different Si-N bond densities, deposited with SiH$_4$ and NH$_3$. The N-H bond density shows similar behavior as a function of time. It is clear that layers with a high initial H-concentration (low Si-N bond density) loose most hydrogen during anneal. In figure 10 the change in Si-N bond density during the same anneal times is shown. Although some changes may be seen during the first anneal periods, the Si-N bond density remains approximately constant during anneal.

Similar to the N$_2$ nitrides [14,15], also in NH$_3$ nitrides the H-diffusion shows a strong time-dispersive (time dependent diffusion coefficient) behavior. This effect is well known for H diffusion in a-Si:H and can be described by [28]:

$$C_H = C_{H,0} \exp(-\pi^2 D_H t / L^2) \qquad (2)$$

$$D_H(t) = D_H(0)\{\omega t\}^{-\alpha} \qquad (3)$$

ω is the H attempt-to-diffuse frequency and α is the temperature dependent dispersion parameter ($0 < \alpha < 1$). More details about this dispersive character of H diffusion in SiN$_x$:H can be found in [24].

The initial diffusion coefficient D$_1$ of the hydrogen strongly depends on the Si-N bond density in the layers. In figure 11, these coefficients for Si-H for both N$_2$ and NH$_3$ nitrides are shown. The coefficients for N-H bond densities are similar, but harder to measure since the peak is much smaller and the error much larger. Although the hydrogen concentrations are quite different for N$_2$ and NH$_3$ nitrides (see figure 5), the diffusion coefficients are the same for both materials, and only depend on the Si-N bond densities.
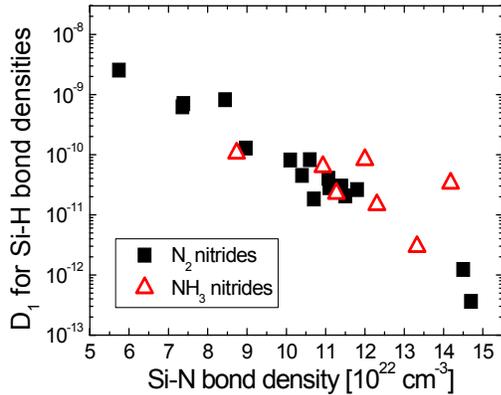
Figure 11: Initial Si-H diffusion coefficient D_1 as a function of Si-N bond density.
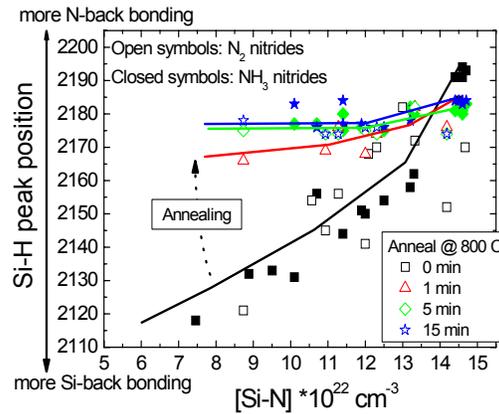
Figure 12: Shift in Si-H peak position as a function of annealing time.

A similar agreement between N_2 and NH_3 nitrides is also found for the shift in the Si-H peak position, shown in figure 12. The Si-H peak position is shown for both N_2 and NH_3 nitrides before and after annealing at several times. The Si-H peak position depends only on the Si-N bond density and the anneal times. The Si-H stretch vibration mode in SiN_x:H can occur at various frequencies between 2000 and 2300 cm^{-1}, depending on the back bonding of the concerning Si atom. If the back bonds are mainly Si atoms the vibration frequency is low (2000 cm^{-1} for H-Si-Si$_3$), in the case of mainly N atoms the vibration frequency is high (2220 cm^{-1} for H-Si-N$_3$) [21,22]. As expected, before annealing (t = 0; square symbols) we see that if the Si-N bond density is low, thus more Si in the layer, the Si-H back bonding is mainly silicon. When the Si-N bond density is high (more N in the layer), the Si-H back bonding is mainly nitrogen.

In figure 12 we see that after annealing the Si-H bonds with Si-rich back bonding disappear from all nitrides, only the Si-H bonds with N-rich back bonding remain. Indeed, figure 11 shows that SiN_x:H layers with low Si-N bond densities and thus more Si-rich back bonding have the highest Si-H diffusion coefficient. This stems from the more open and porous structure of the Si-rich layers. The strongest and most stable bonds are those around 2180 (H-Si-HN$_2$).

Although the N_2 and NH_3 nitrides are formed with different deposition mechanics and the initial hydrogen concentrations are not the same, the hydrogen diffusion and corresponding structural changes are the same for layers with the same Si-N bond density. In paragraph 3.2 we already showed that the bulk passivating properties of the two layers depend in the same way on the Si-N bond density; this fact can now be explained by the similar H diffusion from the SiN_x:H layer into the mc-silicon due to the same Si-N bond density in the layers.

4. CONCLUSIONS

We have shown that for SiN_x:H layers deposited with our remote MW PECVD system the N/Si flow ratio and the deposition pressure are important processing parameters. The Si-N, Si-H and N-H bond densities of layers deposited with N_2, NH_3 or ND_3 are related to N/Si flow ratio and the pressure p in a similar way, but the difference in dissociation energy and rate causes differences in the deposition mechanisms. Comparing the Si-N and Si-H bond densities found for NH_3 and ND_3 grown layers, we find that roughly 25% of the hydrogen in the SiN_x:H layers stems from the ammonia precursor gas, while 75% stems from the silane. This fact is confirmed by the 25% difference in H-content in N_2 and NH_3 layers.

Even though the N_2 and NH_3 nitrides are formed with different deposition mechanics and the initial hydrogen concentrations are not the same, the hydrogen diffusion and thus bulk passivation are the same for layers with the same Si-N bond density. Layers with low Si-N bond densities are porous with large hydrogen diffusion coefficients. During anneal the hydrogen will effuse into the ambient in molecular form and will not contribute to the passivation. Dense layers on the other hand, with high Si-N bond densities have very low diffusion coefficients. For too high Si-N bond densities the diffusion of the atomic hydrogen in the SiN_x:H layer will be too slow, resulting in less passivation during short anneals. The similar H-diffusion from the SiN_x:H layer explains the fact that we find optimum values for bulk passivation for the same Si-N bond densities of $1.3*10^{23}$ cm^{-3} for both N_2 and NH_3 nitrides and regardless of the starting wafer quality. Also the best surface passivation is found for both nitrides around this Si-N bond densities of $1.3*10^{23}$ cm^{-3}.

Consequently, the Si-N bond density found via the FTIR analysis is an important parameter for the solar cell characteristics, related to both the bulk and surface passivation of the SiN_x:H layers, regardless of the type of SiN_x:H. This study therefore indicates that FTIR analysis of the SiN_x:H layers gives us a quick and reliable tool to check the quality and properties of different SiN_x:H layers. This will allow optimization of SiN_x:H deposition processes and systems without having to make complete solar cells.

5   ACKNOWLEDGEMENTS

6   REFERENCES

[1]   S. Winderbaum, F. Yun, O. Reinhold, J. Vac. Sci.Techn. A 15, 1020 (1997).
[2]   Z. Chen, A. Rohatgi, R.O. Bell, J. P. Kalejs, Appl. Phys. Lett. 65, 2078 (1994)
[3]   F. Duerinckx, J. Szlufcik, Sol. Energy. Mat. Sol. Cells, 72, 231 (2002)
[4]   W.J. Soppe, C. Devilee, S.E.A. Schiermeier, J. Hong, W.M.M. Kessels, M.C.M. Van de Sanden, W.M. Arnoldbik, A.W. Weeber, *Proceedings of the 17th European Photovoltaic Solar Energy Conference, 22-26 October 2001, Munich, Germany*: 1543-1546
[5]   A. Aberle, Crystalline silicon solar cells – Advanced Surface Passivation and analysis, UNSW, Sydney (1999);   Progress in Photovoltaics: Research and Applications 8, 473 (2000)
[6]   W.M. Bik, R.N.H. Linssen, F.H.P.M. Habraken, W.F. van der Weg, A.E.T. Kuiper, Appl. Phys. Lett. 56, 2530 (1990)
[7]   M. Maeda and M. Itsumi, J. Appl. Phys. 84, 5243 (1998)
[8]   G. C. Yu and S.K. Yen, Appl. Surf. Sci. 201, 204 (2002)
[9]   C. Boehme and Lucovski, J. Non-Cryst. Sol. 299, 1157 (2002);   J. Appl. Phys. 88, 6055 (2000)
[10]   J. Hong, W.M.M. Kessels, W.J. Soppe, A.W. Weeber, W.M. Arnoldbik, M.C.M. Van de Sanden, J. Vac. Sci. Techn. B: 21, 2123 (2003)
[11]   H. F. W. Dekkers, L. Carnel, G. Beaucarne, W. Beyer, *Proceedings of the 20th European Photovoltaic Solar Energy Conference, 6-10 june 2005, Barcelona, Spain*
[12]   J. Tan, A. Cuevas, S. Winderbaum, K. Roth, *Proceedings of the 20th European Photovoltaic Solar Energy Conference, 6-10 june 2005, Barcelona, Spain*
[13]   H. Mäckel and R. Lüdemann, J. Appl. Phys. 92, 2602 (2002)
[14]   A.W. Weeber, H.C. Rieffe, W.C. Sinke, W.J. Soppe, *Proceedings of the 19th European Photovoltaic Solar Energy Conference, 7-11 june 2004, Paris, France:* p1005
[15]   A.W. Weeber, H.C. Rieffe, I.G. Romijn, W.C. Sinke, W.J. Soppe, *Proceedings of the 31st IEEE Photovoltaic Specialists Conference, 3-7 jan 2005, Orlando, USA*
[16]   R. A. Sinton, A. Cuevas, Appl. Phys. Lett 69, 2510 (1996)
[17]   W. J. Soppe, B.G. Duijvelaar, S.E.A. Schiermeier, A.W. Weeber, A. Steiner, F.M. Schuurmans, *Proceedings of the 16th European Photovoltaic Solar Energy Conference, 1-5 may 2000, Glasgow, Scotland*
[18]   N. Maley, Phys. Rev. B 46, 2078 (1992)
[19]   F. Giorgis, F. Giuliani, C.F. Pirri, E. Tresso, C. Summonte, R. Rizzoli, R. Gallloni, A. Desalvo, P. Rava, Phil. Mag. B 46, 2078 (1992)
[20]   E. Bustarret, M. Bensouda, M.C. Habrard, J. C. Bruyere, S. Poulin, S.C. Gujrathi, Phys. Rev. B 38, 8171.
[21]   W. J. Soppe, J. Hong, W.M.M. Kessels, M.C.M. van der Sanden, W.M. Arnoldbik, H. Schlemm, C. Devilee, H. Rieffe, S.E.A. Schiermeier, J.H. Bultman, A.W. Weeber, *Proceedings of the 29th IEEE Photovoltaic Specialists Conference, 20-24 may 2002*, New Orleans, USA
[22]   A.J.M. van Erven, Master Thesis, Eindhoven University of Technology
[23]   W. Soppe, H.C. Rieffe, A.W. Weeber, Progress in Photovoltaics: Research and Applications, in press
[24]   W. Soppe, H.C. Rieffe, I.G. Romijn, W.C. Sinke, A.W. Weeber, to be published
[25]   D. L. Lide, CRC Handbook of Chemistry and Physics, CRC Press, Boca Raton (1994)
[26]   I. G. Romijn, W.J. Soppe, H.C. Rieffe, A.R. Burgers, A.W. Weeber, *Proceedings of the 20th European Photovoltaic Solar Energy Conference, 6-10 june 2005, Barcelona, Spain*
[27]   A. Weeber, H.C. Rieffe, M.J.A.A. Goris, J. Hong, W.M.M. Kessels, M.C.M. van de Sanden, W.J. Soppe, *Proceedings of the 3rd World Conference on Photovoltaic Energy Conversion, 11-18 may 2003, Osaka, Japan*
[28]   W. Beyer, Sol. Energy Mat. Sol Cells 78, 235 (2003)

AKT

AKT Inc., an Applied Materials company

**AKT Thin Film
PECVD Deposition**

Robert Bachrach
7 August 2005

Part 1

External Use

Applied Materials Corporate Overview

- **FY04 New Orders**
  - $8,982 Million
- **FY04 Revenue**
  - $8,013 Million
- **Worldwide Employees**
  - Approximately 12,000
- **Worldwide Locations**
  - 14 Countries
  - >65 Sales and/or Service Locations
  - Manufacturing in North America, Europe and Israel
  - Development in North America, Asia, Europe and Israel
- **Gross RD&E Investment (5 years)**
  - $5,271 Million

External Use

Worldwide Semiconductor Production

History and Forecast

External Use

RD&E Investment

Revenue reported in accordance with SAB 101 beginning FY '01
Data prior to FY '99 does not include ETEC Systems

External Use

Wafer Fab Equipment Company Revenue — AKT

Total Revenue ($M)

- Applied Materials
- Tokyo Electron
- ASML
- Nikon
- KLA-Tencor
- Canon
- Novellus
- LAM

Source: Companies' Reports, VLSI Research 2/04

Envisioning the Future

External Use

Top 15 Worldwide Semiconductor Equipment Manufacturers — AKT

2004 Rank	CY2004 Sales ($M)*	Company
1	$8,163.10	Applied Materials
2	5,576.50	Tokyo Electron Ltd.
3	3,073.50	ASML
4	2,175.70	Advantest
5	1,991.10	Nikon Corporation
6	1,891.80	KLA-Tencor
7	1,851.20	Canon, Inc.
8	1,739.70	Hitachi High-Technologies Corp.
9	1,738.00	Dainippon Screen Mfg. Co., Ltd.
10	1,360.00	Lam Research Corporation
11	1,337.30	Novellus Systems, Inc.
12	1,146.30	Teradyne, Inc.
13	1,098.40	Ulvac, Inc.
14	861.80	ASM International N.V.
15	713.40	Agilent Technologies, Inc.

* Includes service and spares
Source: VLSI Research 5/05

Envisioning the Future

External Use

Served Available Market - Silicon — AKT

$ Billions

Forecast

- PDC*
- CMP
- Diff/Ox/RTP
- Ion Implant
- EPI
- PVD
- ECP
- CVD
- Dry Etch

1992 1993 1994 1995 1996 1997 1998 1999 2000 2001 2002 2003 2004F 2005F 2006F

* Note: Mask/Reticle and Wet Clean have been removed from all years;
PVD has been changed to include integrated application from 2001
Source: Applied Materials 5/04

Envisioning the Future

External Use

Served Available Market — AKT

$12.3 Billion

$7.6 Billion

CY 2002	CY 2006F	
	$1,701M	PDC*
	$1,015M	CMP
	$1,021M	Diff/Ox/RTP
$1,227M	$1,604M	Ion Implant
$666M		EPI
$676M	$1,289M	PVD
$961M		ECP
$1,544M	$2,355M	CVD
$1,643M	$2,753M	Dry Etch

$223M
$302M
$590M
$125M
$153M

* Note: Mask/Reticle and Wet Clean have been removed from all years;
PVD has been changed to include integrated application from 2001
Source: Applied Materials 5/04

Envisioning the Future

External Use

89

Slide 1: AKT's Current Focus

AKT — *AKT's Current Focus*

Products   **Technology**   **Customer Support**

Gen.5 PECVD
-Production Support
Gen.6 PECVD
-System / Process Development
Gen.7 PECVD
-Concept Design
Gen.2 - 4 PECVD for LTPS
-Process Enhancement
-R&D/Production Support
Gen 5 - 7 EBT (Array Tester)

Continuous Development
-Throughput Enhancement
-Lower Chamber Cleaning Cost
-COO Reduction
-a-Si / LTPS Superior Process
-Particle Reduction
-Low Temperature Deposition
-Future Process Technology

Global Focus
-Start-Up Teams
-Spares Depot
-Productivity Improvement
-Post-Warranty Contracts
-Total Support Package

Envisioning the Future

External Use

Slide 2: AKT CVD Technologies Serving FPD Market

AKT CVD Technologies Serving FPD Market — **AKT**

AMLCD — A-Si TFT, A-Si/LTPS TFT, LTPS TFT → **Large** — TV, Large PC, Public Info Displays

AMOLED — LTPS Driver

PDP — Enhanced Dielectric → **Medium** — Desktop/NB PC, E-Book, Web Pad

FED — Electrode Tip / Enhanced Dielectric → **Small** — Cell Phone, PDA, Automobile, Game

Envisioning the Future

External Use

Slide 3: AKT Customer's Markets

AKT Customer's Markets — **AKT**

- AKT's large area electronics market includes:
  - manufacturing equipment and customer services
- Dominant market segment is
  - TFT-LCD and other Displays

Modern TFT-LCD display ----------->

Prehistoric carvings
from 30,000 years ago ------------>

Human advancement has been
coupled to image representation
and harnessing energy

- Other market segments include:
  - Solar Energy
  - Re-batched packaging of Si IC
  - Architectural Glass

Envisioning the Future

External Use

Slide 4: AKT History

AKT History — **AKT**

Started PECVD Development in AMAT ADT		1991
Joint development program with Sharp/Toshiba		1992 -1993
Shipped the first AKT-1600 CVD to Sharp	Feb.	1993
Formed 50:50 JV Applied Komatsu Technology	Sep.	1993
Established AKT Korea Branch	May	1994
Shipped first AKT-1600 CVD to Korea (Samsung)	Sep.	1994
Shipped the first system to Taiwan (Unipac)	Feb.	1996
AMAT bought 50% share from Komatsu	Oct.	1999
Established AKT Taiwan Branch	Dec.	1999
Shipped the 350th PECVD system	Oct.	2003
Shipped the 400th PECVD system	Sep.	2004
1st AKT office in People's Republic of China	Sep.	2004

Envisioning the Future

External Use

90

Product Line

(deposition equipment only)

	Model Number	Year Launched	Max Substrate Size W (mm)	x	L (mm)
a-Si	1600	1992	370	x	470
PECVD	3500	1995	550	x	650
	4300	1997	600	x	720
	5500	1999	730	x	920
	15K	2002	1200	x	1300
	25K	2003	1500	x	1850
	40K	2004	1950	x	2250
	50K	2006e	2160	x	2460
Low Temp	1600LTPS	2002	370	x	470
Polysilicon	4300LTPS	2002	600	x	720
PECVD	5500LTPS	2002	730	x	920

Also manufacture electron beam array testers (EBT) for pixel testing of completed array structure

External Use

AKT Product Roadmap

AKT-40K Gen.7	1950 x 2250 mm	PECVD 7/04	EBT 8/04
AKT-25K Gen.6	1500 x 1850 mm	PECVD 5/03	EBT 8/04
AKT-15K Gen.5	1200 x 1300 mm	PECVD 6/02	LTPS PECVD TBD
AKT-10K Gen.5	1000 x 1200 mm	PECVD 8/01	EBT 2/03
AKT-5500 Gen.4	730 x 920 mm	PECVD 1/00	EBT 4/01	LTPS PECVD 12/02
AKT-4300 Gen.3.5	610 x 720 mm	PECVD 2/97	LTPS PECVD 12/01
AKT-3500 Gen.3	550 x 670 mm	PECVD 4/95	EBT 11/00
AKT-1600 Gen.2	PECVD 2/93	400x500 mm	LTPS PECVD 6/98	EBT 3/01

> 500 Production/R&D Systems Worldwide (Q205)

1993 1994 1995 1996 1997 1998 1999 2000 2001 2002 2003 2004 2005

External Use

AKT Systems Installation Base

(As of end of Q2/FY 2005)

Taiwan	187		
Japan	160	CVD	453
Korea	147	PVD	16
US & EU	12	Etch	15
China	5	EBT	27
Total	511	Total	511

450th 450th PECVD shipped in May 2005

External Use

AKT Worldwide Locations for Customer Support

United States

Santa Clara
– RD& E
– Manufacturing
– Engineering
– Customer Demo Facility
– Product Marketing
– Strategic Marketing
– Product Support & Training
– Spare Parts

Germany (AKT EBT)

Feldkirchen
– Engineering
– Manufacturing Array Tester

Korea

Seoul
– Sales
– Customer
  Service Center
– Spare Parts
– Product Support

Service Offices
– Kihueng
– Kumi
– Chonan
– Tangjung
– Paju

Japan

Osaka
– Sales and Marketing
– Customer Service Center
  –Spare Parts
  –Process Support
  –Software Development
   and Support

Tokyo
– Customer Service Center

Service Offices
– Tokyo
– Osaka

China

Beijing
– Sales and Service
Spares Depot: Beijing
Service office: Beijing

Taiwan

Hsin-Chu
– Sales and Service
Spares Depot: Taoyuan
Service office: Tainan
           Taichung

External Use

92

LCD Growth Enabled By Price / Cost Reduction

Source: DisplaySearch FPD Conference, April 2005

Area Increases Faster Than Investment

Equipment companies have been extremely successful in maintaining throughput at larger substrate sizes with minimal cost increase

Depreciation Decreases with Larger Substrate Size

Source: DisplaySearch FPD Conference, April 2005

LCD materials (.7mm glass, backlights, color filters, driver ICs polarizers, liquid crystal) dominate cost structure

Substrate Size Expansion

Substrate size increase enables cost reduction to lower panel prices and also permit efficient production of ever larger display sizes to penetrate new markets (such as TV market)

Slide 1

AKT PECVD System Comparison — 🔲 AKT

	Gen 2	Gen 3	Gen 4	Gen 5	Gen 5	Gen 6	Gen 7
System Layout							
Model Substrate Size (mm)	AKT1600 370x470 400x500	AKT4300 600x720 620x750	AKT5500 680x880 730x920	AKT10K 1000x1200	AKT15K 1100x1250 1200x1300	AKT25K (25KA) 1500x1800 (1500x1850)	AKT40K 1870x2200
Substrate Area Scale Up	2,000 cm2 (1.00)	4,650 cm2 (2.33 from 1600)	8,716 cm2 (1.44 from 4300)	12,000 cm2 (1.79 from 5500)	15,600 cm2 (1.30 from 10K)	27,000 cm2 (1.73 from 15 K)	41,140 cm2 (1.52 from 25 K)
System Area Scale Up	6.80 m2 (1.00)	16.37 m2 (2.41 from 1600)	24.84 m2 (1.52 from 4300)	37.47 m2 (1.51 from 5500)	46.54 m2 (1.24 from 10K)	61.43 m2 (1.32 from 15 K)	92.57 m2 (1.51 from 25 K)
Max. Mechanical Throughput	60 sub/hr	60 sub/hr	60 sub/hr	55 sub/hr	55 sub/hr	55 sub/hr	60 sub/hr
Max. P-ch Qty	4	4	5 (w/ H-ch) 6 (w/o H-ch)	5 (w/ H-ch) 6 (w/o H-ch)	5 (w/ H-ch) 6 (w/o H-ch)	4 (w/ H-ch) 5 (w/o H-ch)	4 (w/ H-ch) 5 (w/o H-ch)
Max. WIP	43	40	41 (w/ H-ch) 30 (w/o H-ch)	15 (w/ H-ch) 8 (w/o H-ch)	15 (w/ H-ch) 8 (w/o H-ch)	14 (w/ H-ch) 7 (w/o H-ch)	14 (w/ H-ch) 7 (w/o H-ch)

Scale Up Process & Cluster Tool		
4 Chamber	5 Chamber	4 or 5 Chamber
Batch System	Single Substrate Operation System	

External Use

Slide 2

AKT-40K PECVD System for Gen 7 — 🔲 AKT

Benefits
- **High reliability and productivity – Patented cluster tool architecture**
- **Low risk – Production proven process and hardware**
- **Excellent TFT device performance**
- **Rapid qualification and start-up**
- **Compact and flexible system design**

Process chamber
- Max. 5 process chambers
- Multiple layer deposition
- RPS (Remote Plasma Source) cleaning
- Alternative cleaning gas capability

System work station
- Data logging & substrate tracking
- System diagnosis
- Factory automation compatible

Load lock
- Triple slot load lock
- Cooling function
- Substrate alignment

Transfer chamber
- 4 axis dual arm vacuum robot
- Substrate location sensor
- AKT designed slit valve

External Use

🔲 AKT

Slide 3

Deposition Uniformity — 🔲 AKT

	DR nm/min	R.I.	Stress E9D/cm2	WER (6:1) nm/min	FTIR NH %	FTIR SiH %	FTIR P.P. cm-1	FTIR W cm-1
gate-SiNx	70 ~ 200	1.88 ~ 1.91	C1 ~ C9	30 ~ 70	10 ~ 30	0.2 ~ 15	-	-
a-Si	3 ~ 200	-	C3 ~ C6	-	-	-	1995	95

APX_L Chamber Enables Uniform Deposition for Gen 7+

External Use

Slide 4

AKT LCD Display Equipment Opportunities

Silicon TFT — amorphous or poly **Color Filter**

Array Process — CF Process — Cell Process — Module Process

External Use

Comments on LCD Manufacturing Needs

AKT

- The operation of Gen 6 and Gen 7 factories launches the market ramp of large diagonal LCD-TV. Gen 8 will ship in July 2006.

- Equipment depreciation represents only approximately 10% of the Display manufacturing cost as opposed to Semiconductor IC's where equipment represents 40-60%. (according to Display Search)

- The manufacturing cost of LCD is dominated by variable costs:
  - Materials in particular
  - Half the cost is in module formation

- LCD Manufacturing today is not standardized

- Future progress in LCD Manufacturing requires

  - Investment in equipment and process which will substantially lower manufacturing material cost

  - Improve productivity and yield

  - Promote equipment standardization, particularly substrate size

Envisioning the Future

External Use

Seeing is Believing …

AKT

Gen.6 – AKT-25K in final test

Gen.7 AKT-40K transfer chamber in assembly

Deposited Gen.6 sub under measurement

Deposited Gen.7 sub under measurement

Envisioning the Future

External Use

AKT-40K PECVD (Gen 7)

AKT

AKT-40K PECVD System

Envisioning the Future

External Use

AKT

AKT Inc., an Applied Materials company

**AKT Thin Film
PECVD Deposition**

Robert Bachrach
7 August 2005

Part 2

External Use

Relevance to Solar Panel Manufacturing

External Use

Flat Panel Opportunity

Gen 7: 1870 x 2200 mm

Gen 6: 1500 x 1850 mm

Gen 5: 1200 x 1300 mm
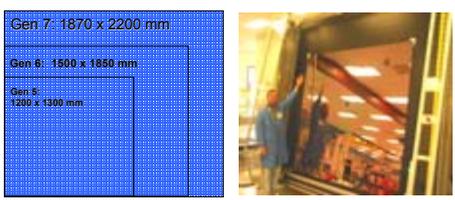
- Producing cost efficient next generation equipment for the rapidly expanding Flat Panel Display (FPD) market

Increasing Substrate Sizes Lower Cost of Production and Drive Flat Panel Proliferation

External Use

TFT LCD Panel Production Capacity (Km2)

Equivalent to 6GW per year Solar

CY	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
		2003				2004				2005		
ROW	0	30	41	49	56	60	60	60	60	78	183	334
Taiwan	690	710	795	1,028	1,228	1,450	1,751	2,055	2,314	2,555	3,076	3,557
Korea	747	864	1,038	1,301	1,461	1,595	1,781	1,927	2,135	2,465	2,921	3,470
Japan	790	847	864	881	897	950	1,053	1,132	1,210	1,280	1,303	1,312

External Use

Slide 1: Area Growth vs. Equipment Spending Growth

Area Growth vs. Equipment Spending Growth

	680 x 880	730 x 920	1100 x 1250	1500 x 1800
Area Growth	100%	112%	230%	451%
Eqpt. Spending Growth	100%	105%	120%	154%

Indexed Growth (y-axis: 0% – 500%)

External Use

Slide 2: AKT Product Model Maximum Substrate Sizes

AKT Product Model Maximum Substrate Sizes

	Model	mm		mm	m sq	inch		inch
Gen 2	AKT 1600	360	x	465	0.17	14.17	x	18.31
	AKT 1600A	370	x	470	0.17	14.57	x	18.50
	AKT 1600B	400	x	500	0.2	15.75	x	19.69
Gen 3	AKT 3500	550	x	670	0.37	21.65	x	26.38
	AKT 3700	590	x	670	0.4	23.23	x	26.38
Gen 4	AKT 4300	610	x	720	0.44	24.02	x	28.35
	AKT 4300A	750	x	750	0.56	29.53	x	29.53
	AKT 5500	730	x	920	0.67	28.74	x	36.22
Gen 5	AKT 10K	1000	x	1200	1.2	39.37	x	47.24
	AKT 15K	1100	x	1250	1.38	43.31	x	49.21
	AKT 15KA	1200	x	1300	1.56	47.24	x	51.18
Gen 6	AKT 25K	1500	x	1800	2.7	59.06	x	70.87
	AKT 25KA	1500	x	1850	2.78	59.06	x	72.83
Gen 7	AKT 40K	1870	x	2200	4.11	73.62	x	86.61
Gen 7.5	AKT 50K	2150	x	2400	5.16	84.65	x	94.49
Gen 8	AKT 60K	2300	x	2600	5.98	90.55	x	102.36

External Use

Slide 3: Silicon PV Manufacturing Process Background

Silicon PV Manufacturing Process Background

- The Silicon PV Manufacturing Process Comprises
- Main manufacturing flows:
  1. Growing, Casting, or Depositing
     - Wafers, Sheets, Ribbon, Thin Films
  2. Solar Cell Formation
  3. Assembly of Cells into Modules
  4. Solar System Assembly
  5. Installation with Balance of Systems
     a. Inverters
     b. Control Electronics
     c. Wiring

External Use

Slide 4: PV Production by Material, 1999-04

PV Production by Material, 1999-04

SILICON FOCUS

	1999	2000	2001	2002	2003	2004
c-Si multi	42.1	48.2	50.2	51.7	57.2	54.6
c-Si mono	40.8	37.4	34.6	36.4	32.2	36.2
c-Si ribbon	4.1	4.3	5.6	4.6	4.4	3.3
a-Si	12.3	9.6	8.9	6.4	4.5	4.4
CdTe	0.5	0.3	0.5	0.7	1.1	1.1
CIS	0.2	0.2	0.2	0.2	0.6	0.4

- Source: Photon International 3/2005

External Use

PV Overview

Wafer/Sheet CELL **Module** **Arrays** **System**

Thin Film **Cell**

Cell Produces
- Voc ~0.5 to 0.65V
- Jsc ~ 30ma/cm2

Cell wiring
- Series - Parallel

DC System **Line Tie or Grid Interface**

DC Interface & Regulation

Batteries

External Use

Envisioning the Future

Crystalline Si PV Value Chain Today

AKT

	%Total		
Si - Basic Material	6%		12%
Wafer/Sheet	20%		40%
Cell	14%	50%	28%
Module	10%		20%
BOS - Inverter	18%		36%
BOS - Other	8%		16%
Installation Mechanical	12%	50%	24%
Installation Electrical	12%		24%
	100%		

- Si - Basic Material
- Wafer/Sheet
- Cell
- Module
- BOS - Inverter
- BOS - Other
- Installation Mechanical
- Installation Electrical

Source: 17th European Photovoltaic Solar Energy and Conference and Exhibition, Munich . 22 . 26 October, 2001
Winfried Hoffmann RWE Solar GmbH   Paper No. PB 2.1

External Use

Envisioning the Future

Solar Module Components

AKT

Figure of Merit

$$=f(s,..)*Cost/(Watt_{peak}/Kg)$$

$$=f(s,r)*Cost*g*t*Area/Watt_{peak}$$

Where
g= panel average density
t= panel thickness
s= structure efficiency
..= others

Rear Protective Cover
Bonding Layer
PV Cells & Interconnection Wiring
Bonding Layer
Front Cover Glass

External Use

Envisioning the Future

Solar Silicon PV Market Segmentation

AKT

Local to Available Energy	Global		Global Manufacturers		Continental Manufacturers	

1 & 2 Materials			Global Equipment Suppliers		6 Panel	7 End Market

1 Raw Materials	2c Metals	3 Silicon Sheet	4 Cell	5 Module
2a Purified Silicon Materials	2d Glass	3a multi-Silicon		
2b xtal Silicon	2e Plastics	3b Thin Film Silicon		
	2f Other			

MW		
#	Company	
1	Sharp Solar	
2	Kyocera	
3	BP Solar	
4	Mitsubishi	
5	Q-Cells	
6	Shell Solar	
7	Sanyo	
8	Isofoton	
9	RWE Schott	
18	Motech	
10	Deutches Cell	
11	GE/Astropower	
12	Kaneka	
13	Evergreen Solar[3]	
14	Uni-Solar Ovonics	
15	First Solar	
16	Photowatt/Matrix	
17	SunPower	
18	SunTech	
19	Yingli	
20	CSG Solar AG	
21	Others ~ 20	

External Use

Envisioning the Future

Cell Process Section Elaboration

A	1 Entrance Stocker	2 Wet Clean & Inspection	3 Damage etch & texture
B	1 Phosphorus diffusion	2 Junction Clean	3 via formation
C	1 SiN Front	2 Optical Front	3 SiN Back	4 Via Fill
D	1 back contact	2 back Reflector & Bus	3 Front Contact	4 Bus Wiring
E	1 Inspection & Test	2 Bin control	3 Exit Stocker

External Use

Cast Si PV Sheet Fabrication

Wafering

Poly-Si ingot

Sawing

wafer

Effective utilization of Si

External Use

Solar Grade Silicon Sheet Growth
Physical Principles

External Use

Solar Power Forecast and Silicon Usage

World-wide Poly -Silicon demand: about 27,000 ton
10,000 ton of Si material produces 1,000 MW of PV cells
Source: Sharp

External Use

99

Non-Sawed Silicon Sheet
ECN and Partners with Bayer AG Process

AKT

External Use

Non-Sawed Silicon Sheet
GE / Astropower Process

AKT

Silicon powder

Zoned
Remelting and Recrystallization

Substrate motion

Re-crystallization process

From: US Patent 5,336,335; Aug 9, 1994
US Patent 6,111,191; Aug 29, 2000
US Patent 6,207,891; Mar 27, 2001

External Use

Non-Sawed Silicon Sheet
Sharp Process

AKT

The Si sheet production technology to make sheet wafer through soaking of the substrate into silicon molten.

The substrate which has special structure, goes on the molten Si, and contacts Si melt.
Molten Si is crystallized on the substrate, and grows to form the Si sheet on substrate.
After sheet formation, the Si sheet is separated from the substrate.
Separated Si sheet which has a structure like Fig.4, is cutting by laser to form a rectangular flat Si wafer

Fig 1

Fig 2

External Use

AKT

External Use

OVERVIEW AND RESULTS OF THE GERMAN RESEARCH NETWORK PROJECT ASIS (<u>A</u>LTERNATIVE <u>SI</u>LICON FOR <u>S</u>OLAR CELLS)

D. Karg[1] and W. Koch[2]

[1] Universität Erlangen-Nürnberg, Lehrstuhl für Angewandte Physik, Staudtstr. 7,
91058 Erlangen, Germany, dieter.karg@physik.uni-erlangen.de
[2] KoSolCo GmbH, Seitz-Berlin-Str. 10, 91550 Dinkelsbühl, Germany

ABSTRACT: The photovoltaic research network project ASiS (<u>A</u>lternative <u>Si</u>licon for <u>S</u>olar Cells) is a joint venture of eleven German research institutes and three German PV-producing companies in the area of crystalline silicon material research. At present, about 40 persons (listed below) are collaborating in the project ASiS. The main topics of ASiS are investigations of the photovoltaic potential of alternative silicon material (e.g. Phosphorus-doped n-type silicon and off-spec silicon), mechanical behaviour of crystalline silicon wafers and development of fast solar cell processes (e.g. Rapid Thermal Processing (RTP)). Examples of experimental results of the research institutes are given. Details can be found in specific contributions of the ASiS partners (see e.g. [3-13]).

1   INTRODUCTION

The photovoltaic network project ASiS (<u>A</u>lternative <u>Si</u>licon for <u>S</u>olar Cells) is a joint venture of eleven German institutes and three German companies in the area of crystalline silicon material research (see also [1]). The project has started in October 2002 and will be finished in September 2005. It is supported by the German Bundesministerium für Umwelt, Naturschutz und Reaktorsicherheit (BMU) under contract number 0329846 (project ASiS), advised by Projektträger Jülich (PTJ), Germany and is coordinated by the authors of this paper. The URL of the project is: http://www.solar-asis.de. At present, the project is mainly investigating n- and p-type multicrystalline silicon grown at Deutsche Solar and RWE Schott Solar. In [1], the main areas of research of the co-operating institutes in the project ASiS are described. The institutes are:

1. Fraunhofer-Institut für Solare Energiesysteme, Freiburg (ISE) (R. Schindler, W. Warta, J. Isenberg, S. Riepe)
2. Universität Kiel, Technische Fakultät, Lehrstuhl Materialwissenschaften (UKI) (J. Carstensen)
3. Institut für Solarenergieforschung Hameln (ISFH) (J. Schmidt, C. Schmiga, K. Bothe)
4. Universität Konstanz, Angewandte Festkörperphysik (UKN) (G. Hahn, M. Käs, J. Libal)
5. Universität Göttingen, IV. Physikalisches Institut (UGÖ) (M. Seibt, R. Khalil, C. Rudolf, O. Voss)
6. Max-Planck-Institut für Mikrostrukturphysik, Halle (MPI) (O. Breitenstein, M. Werner, J.P. Rakotoniaina)
7. IHP GmbH - Innovations for High Performance Microelectronics / Institut für Halbleiterphysik, Frankfurt/Oder (IHP) (M. Kittler, T. Arguirov, W. Seifert)
8. Technische Universität Bergakademie Freiberg, Institut für Experimentelle Physik (TUBA) (H.J. Möller, C. Funke, S. Scholz)
9. Universität Erlangen-Nürnberg, Lehrstuhl für Angewandte Physik (LAP) (G. Pensl, D. Karg, S. Beljakowa)

10. Universität Erlangen-Nürnberg, Institut für Werkstoffwissenschaften, Lehrstuhl für Mikrocharakterisierung (IWW) (H.P. Strunk, M. Becker)
11. Access e.V. Materials and Processes, Aachen (D. Franke, H. Behnken)

The industry partners distribute material and solar cells, participate in the critical discussion of the results and analyze the results with respect to a direct process implementation. The industrial partners are:

1. Deutsche Solar AG (DS)
2. RWE Schott Solar GmbH (RSS)
3. Shell Solar GmbH (SSG)

2   OBJECTIVES OF PROJECT ASIS

The project ASiS is focused on the following three main topics:
   A: Alternative doping, alternative feedstock (all institutes, coordinated by LAP)
   B: Mechanical behaviour of solar-grade silicon (Access, IHP, FhG-ISE, MPI Halle, IWW, TUBA, UKN and UKI, coordinated by Access)
   C: Rapid Thermal Processing (ISE, MPI, LAP, UGÖ, UKI, UKN, coordinated by ISE)

In [1], the main topics of the project ASiS are described in detail.

3   EXPERIMENTAL RESULTS

Due to lack of space, the shown experimental results represent only a small part of the whole research activities of the project ASiS. Additionally, the ASiS partners have presented the following papers at the 20th EC PVSEC in Barcelona [3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13].

3.1 Main topic A: Alternative doping, alternative feedstock
3.1.1 n-type mc-Si
Three types of n-type multicrystalline Si grown at Deutsche Solar [14] are investigated in the project ASiS. The first and the second material are used for preliminary investigations like lifetime measurements, P-gettering and hydrogen passivation. It could be shown that P-gettering and hydrogen passivation works similar to p-type material. Subsequent to P-gettering and hydrogen passivation, average lifetime values of 330 µs and 690 µs are measured for these two materials, respectively (ISFH, C. Schmiga, see [2]). The third material, an n-type multicrystalline HEM material, has been investigated in detail. The resistivity of this material varies from approx. 0.8 Ωcm close to the bottom to approx. 0.15 Ωcm near the top of the block. The strong resistivity decrease is a consequence of the low segregation coefficient of phosphorus in silicon k = 0.35.

Multicrystalline silicon ingots typically show regions of reduced minority carrier lifetimes in the bottom of the blocks. This is true for commercially available p-type material as well as for n-type material. In Fig. 1, lifetime profiles of the as-grown and of the P-Al gettered n-type HEM material are shown and compared with standard p-type mc-Si (S. Riepe, ISE, see also [3]).

Compared to p-type mc-Si, the lifetime values in n-type HEM are approximately one order of magnitude higher. This means that despite the lower minority charge carrier mobility of n-type material (factor 3), the minority charge carrier diffusion length is considerably higher in n-type HEM material.
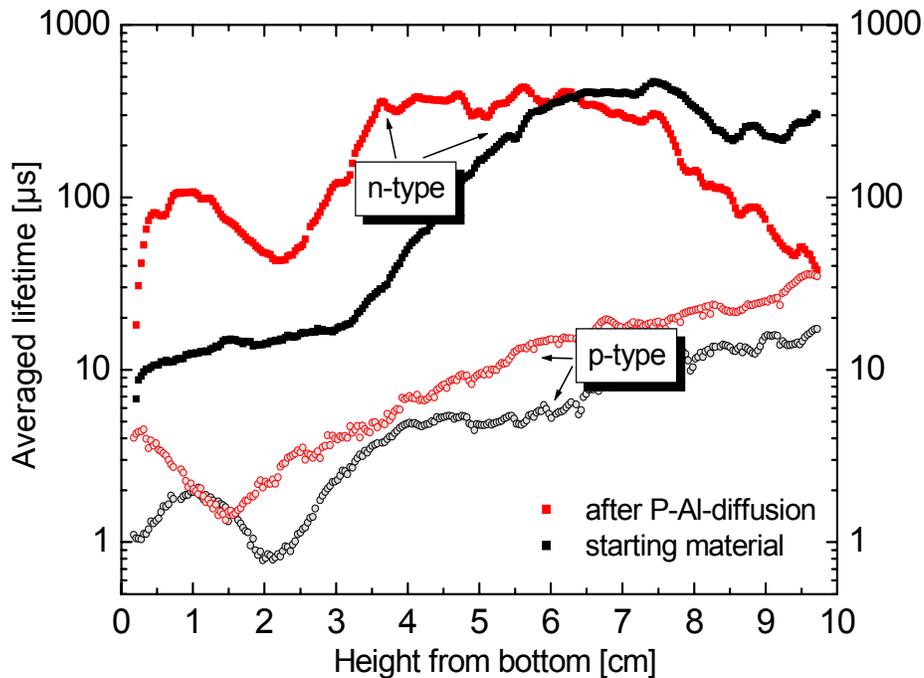
Figure 1: Lifetime profiles of the bottom region and middle part of n-type HEM and standard p-type mc-Si.

By DLTS measurements at 14 to 76 mm distance from block bottom of the as-grown n-type HEM material, different electrically active defects were observed (LAP, S. Beljakowa). However, only one of these defects has a concentration profile, which is consistent with the lifetime profile in Fig. 1. The electrical parameters of this defect are $E_C - E_T = 108$ meV and $\sigma_n = 1.7 \times 10^{-16}$ cm^2. Comparing these values with values from the literature, the most likely candidate for the observed defect would be the acceptor state of the C_iC_S pair [15, 16]. By MCTS measurements, a defect at $E_T = E_V + 360$ meV was observed, which could be the donor state of the C_iC_s pair. To find out, whether the acceptor state or the donor state of the C_iC_s pair is the lifetime limiting defect in the bottom region of n-type HEM material, further measurements are necessary, which will be expanded to p-type HEM material, too.
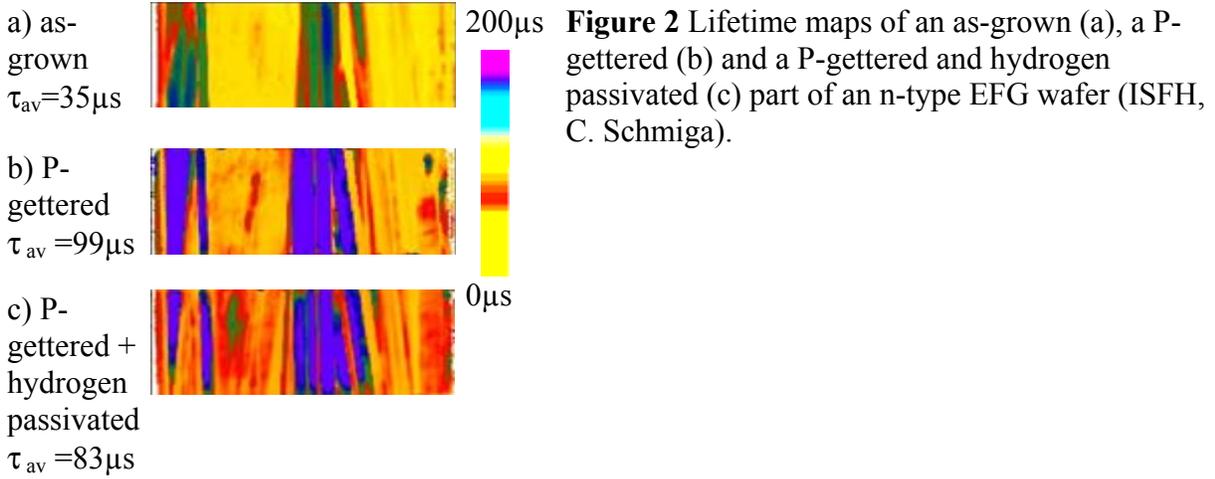
TEM investigations at up to 60 mm distance from block bottom have shown that the dislocation density and the grain structure is not directly correlated with the strong lifetime gradient (IWW, M. Becker). However, dislocations and grain boundaries are more decorated near to the block bottom.

At IHP, EBIC investigations have shown that the recombination properties are strongly dependent on the block height. Near by the block bottom, the recombination properties are homogenous and dominated by point defects like e.g. metal impurities. The recombination activity of dislocations is low in this region. In contrast, close to the top of the block, the recombination activity of dislocations is considerably higher and more inhomogeneous. This could point out the existence of precipitates.

3.1.2 n-type EFG

Multicrystalline n-type EFG silicon ribbons, studied in the ASiS project, have been grown at RWE Schott Solar [17]. The material is phosphorus-doped. The resistivity has a value of approx. 1-3 Ωcm. Lifetime mappings, measured at ISFH (see also [2]), are shown in Fig. 2. Fig. 2a is an

as-grown, Fig. 2b a P-gettered and Fig. 2c a P-gettered and hydrogen passivated part of an n-type EFG wafer. It is noticeable that some grains show high lifetimes of up to 500 μs and some grains show lifetimes in the order of microseconds.

a) as-grown
τ_{av}=35μs

b) P-gettered
τ_{av} =99μs

c) P-gettered + hydrogen passivated
τ_{av} =83μs

200μs

0μs

Figure 2 Lifetime maps of an as-grown (a), a P-gettered (b) and a P-gettered and hydrogen passivated (c) part of an n-type EFG wafer (ISFH, C. Schmiga).

TEM and EBIC investigations have shown that regions with low recombination contrast and high lifetime values have twin boundaries and a low density of dislocations and precipitates. On the other hand, regions with a high density of dislocations and precipitates or regions without any twin boundaries or random grain boundaries typically have low lifetime values and a strong EBIC contrast (MPI, IWW, IHP). In the areas with low and medium lifetime values, dislocations at the twin boundaries, spherical amorphous particles near to the twin boundaries (presumably SiO_2) and particles with a diameter less than 5 nm at the twin boundaries are detected (MPI).

3.1.3 n-type Si solar cells

On n-type silicon material, 2x2 cm^2 solar cells are fabricated at ISFH (C. Schmiga, see [4]) and UKN (J. Libal, see [5]).

At ISFH, rear-junction n^+np^+ solar cells have been fabricated on different n-type materials (Cz-Si, FZ-Si, Solsix and EFG). The processing of the solar cells is described in [4]. The solar cells consist of Al grid fingers, PECVD SiN_x, $POCl_3$ FSF, Al-p$^+$ emitter and Al back side contact. The efficiency values of the best solar cells are shown in Table I.

Table I: Electrical parameters of rear-junction n^+np^+ solar cells (2 x 2 cm^2) fabricated at ISFH (C. Schmiga).

Si	ρ_{base} [Ωcm]	W [μm]	FS	η [%]	V_{oc} [mV]	J_{sc} $\left[\dfrac{mA}{cm^2}\right]$	FF [%]
Cz	4.0	300	pl	17.3	625	35.0	79.2
Cz	4.0	280	tx	18.3*	621	37.0	79.5
mc	1.7	230	pl	14.4	610	31.1	75.8
EFG	3.6	160	pl	14.9	609	32.6	74.9

CELLO investigations at UKI (J. Carstensen, see also [18]) show that compared to FZ-Si and Cz-Si, the relatively low FF in mc-Si (Solsix) and EFG material is caused by point-like shunts in the rear-junction. The reason for the shunts is investigated at present.

Cz-Si and mc-Si based solar cells fabricated at UKN consist of BBr_3 emitter, $POCl_3$ BSF, Ti/Pd/Ag grid fingers and Ti/Pd/Ag back side contact. The solar cells have no surface texture, no anti reflection coating and no emitter passivation. The efficiency values of the best solar cells are shown in Table II.

Table II: Electrical parameters of p^+nn^+ solar cells (2 x 2 cm^2) fabricated at UKN (J. Libal).

	η (%)	J_{SC} (mA)	FF (%)	U_{OC} (mV)
Cz-Si	11.5	24.4	77.9	604
mc-Si	10.4	21.9	77.3	600

The efficiency values achieved at ISFH and UKN show that it is possible to process phosphorus-doped solar cells in a similar electrical quality as boron doped solar cells.

3.2 Main topic B: Mechanical behaviour of solar-grade silicon

Access, TUBA, MPI, DS and UKN have conducted a mechanical proof-test on approx. 1000 as-cut and damage etched mc-Si wafers. Aim of the test is the sorting out of these wafers, which would probably break during solar cell processing. It should be checked, whether a mechanical preload leads also to a damage of the surviving wafers. The sorting out was done by stressing the wafers with ultrasonic or with a 4-line bending test until 5% of the wafers break. It could be shown that in contrast to the 4-line bending test, ultrasonic leads to no damage of the preload surviving wafers. Furthermore, it could be shown that the type of damage etch has a significant influence on the fracture stress distribution (see also [19]). In Fig. 3, the fracture stress distribution of as-sawn and damage etched wafers is shown prior to and subsequent to a preloading.

In many cases, the chemical etching of silicon wafers does not lead to an improvement of the wafer breaking strength. Therefore, a reliable fast method is necessary which is sorting out these wafers, which would probably break during solar cell processing and module manufacturing. At Access an in-line capable roll tester with a cycle time in the order of a second has been developed by support of simulations of the mechanical stress in the wafers during various bending tests (see also [20]). In Fig. 4, a schematic sketch of the roll tester is shown.

### 3.3 Main topic C: Rapid Thermal Processing

The thermal budget (the integral of temperature over time) of solar cell processing can be considerably decreased by RTP processing. Therefore, it may be possible, to enhance cell throughput, improve process control and save floor space by RTP processes.

In the project ASiS, it is investigated, whether the strong illumination intensity (particularly the UV illumination) changes the diffusion and oxidation behaviour. For this reason, a RTP system with adjustable, additional UV-illumination has been acquired (ISE).

Experimental results have shown that diffusion or oxidation by RTP is not significantly accelerated in comparison to conventional furnace processing. Also by additionally using UV illumination during RTP, the diffusion and oxidation is comparable to conventional furnace processing (ISE).
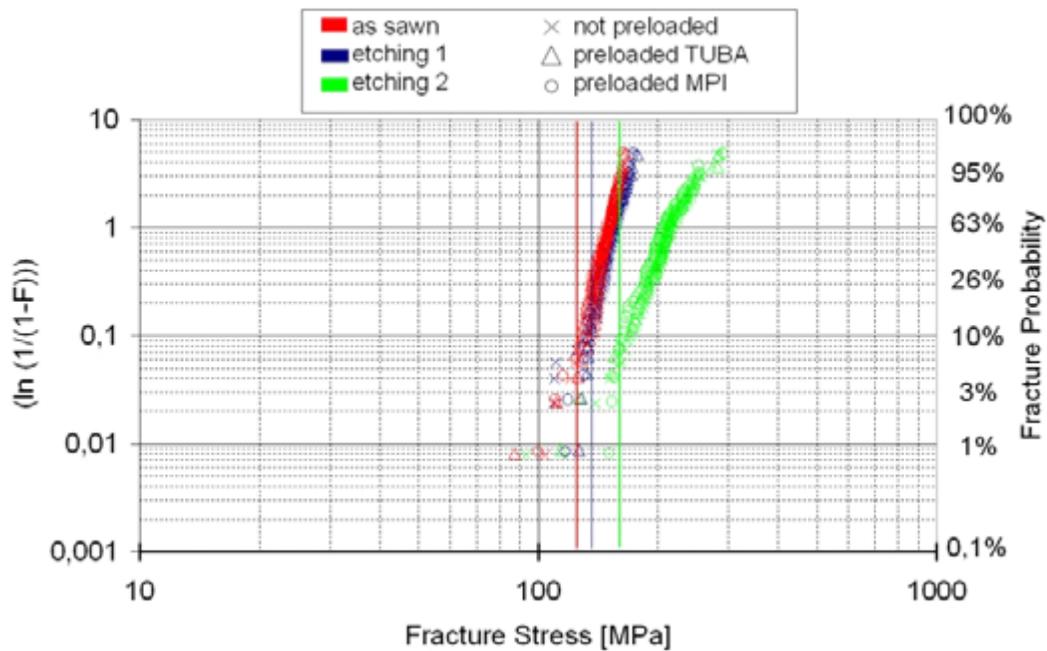
Figure 3: Fracture stress distribution of as cut and damage etched wafers prior to and subsequent to a preloading by ultrasonic or with the 4-line bending test (TUBA).
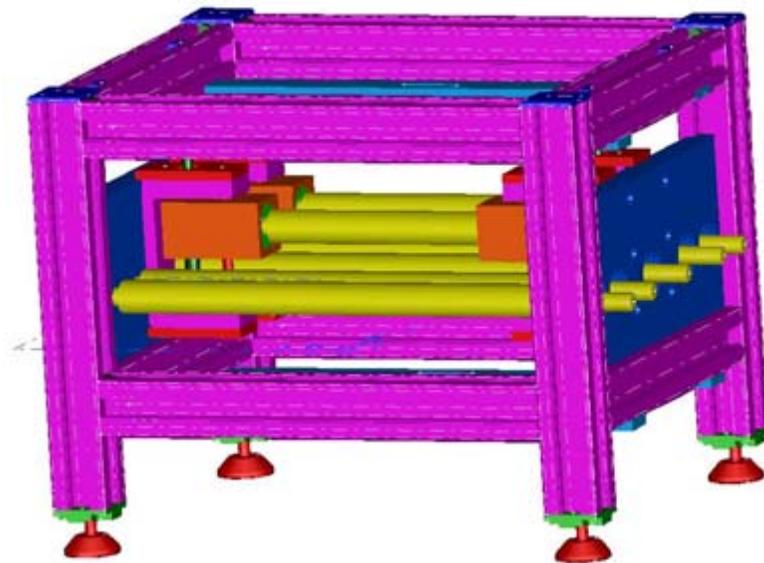
Figure 4: Schematic sketch of an in-line capable roll tester (Access).

3.4 p-type silicon material and solar cells

Material-induced shunts reduce fill factor and open circuit voltage of solar cells and, therefore, these shunts reduce the solar cell efficiency. Investigations have shown (MPI, J.P. Rakotoniaina, see also [6]) that in most cases one of the types of precipitates mentioned below is responsible for material induced shunts in solar cells: (1) multicrystalline SiC filaments with a diameter of some microns, (2) Si_3N_4 fibres with a diameter of < 1 micron, appearing in bundles and (3) straight hexagonal shaped Si_3N_4 rods, surrounded by SiC clusters quite often. The investigations have shown that the columns in the corners and at the edges of the block show the highest concentration of precipitates, whereas the central columns show the lowest. μ-XRF investigations of the precipitates show nanoclusters consisting of $FeSi_2$ and Cu_3Si at the SiC clusters and some $FeSi_2$ at the Si_3N_4 rods. It is suggested that Fe and Cu may play a role in the formation of the precipitates. Furthermore, it is supposed that the horizontal distribution of the precipitates is a result of the convection flow in the melt.

Fe is one of the main contaminations in solar-grade silicon. However, unlike Fe as a point defect, the properties of clustered and precipitated Fe in Si are poorly understood. At UGÖ, the fingerprints of Fe clusters and Fe silicide precipitates were established by DLTS investigations. The DLTS spectra show extended band-like states due to Fe silicide precipitates. Furthermore, at UGÖ, a simulation tool was developed, which calculates solar cell properties as a result of P-diffusion gettering and Al gettering. The so-called "Gettering Simulator" is e.g. able to calculate the remaining Fe_i and Cr_i concentration subsequent to a gettering treatment and the resulting solar cell properties.

At UKN, on p-type Solsix and EFG material, 2×2 cm^2 solar cells were fabricated (M. Käs, see also [10]). The solar cells consist of $POCl_3$ emitter, PECVD SiN_X, Al p$^+$ BSF, Al backside contact, Ti/Pd/Ag grid fingers. The efficiency values of the best solar cells are shown in Table III.

Table III: Electrical parameters of n$^+$pp$^+$ solar cells (2×2 cm^2) fabricated at UKN (M. Käs).

	η (%)	J_{SC} (mA)	FF (%)	U_{OC} (mV)
EFG	17.3%	35.1	79.9	617
mc-Si	18.0%	36.0	79.9	627

4   ACKNOWLEDGEMENT

5   REFERENCES

[1]   D. Karg, K. Roy, W. Koch, 19th EC PVSEC, Paris (2004), 923 and D. Karg, W. Koch, 20th EC PVSEC, Barcelona (2005), to be published

[2]   C. Schmiga, J. Schmidt, R. Hezel, M. Ghosh, A. Metz, 19th EC PVSEC, Paris, France, 439

[3]   S. Riepe, H. Lautenschlager, M. Ghosh, A. Müller, W. Warta, 20th EC PVSEC, Barcelona, Spain, to be published

[4]   C. Schmiga, J. Schmidt, R. Brendel, 20th EC PVSEC, Barcelona, Spain, to be published

[5]   J. Libal, R. Petres, R. Kopecek, G. Hahn, P. Fath, 20th EC PVSEC, Barcelona, Spain, to be published

[6]   J.P. Rakotoniaina, O. Breitenstein, M. Werner, M. Hejjo Al-Rifai, T. Buonassisi, M.D. Pickett, M. Ghosh, A. Müller, Le Quang Nam, 20th EC PVSEC, Barcelona, to be published

[7]   S. Scholz, G. Gärtner, A. Sidelnicov, C. Funke, H.J. Möller, W. Erfurt, A. Seidl, 20th EC PVSEC, Barcelona, to be published

[8]   J. Isenberg, M.C. Schubert, D. Biro, W. Warta, A. Froitzheim, 20th EC PVSEC, Barcelona, to be published

[9]   G. Hahn, A. Schönecker, A.R. Burgers, R. Ginige, K. Cherkaoui, D. Karg, 20th EC PVSEC, Barcelona, to be published

[10]   M. Käs, G. Hahn, T. Pernau, A. Metz, 20th EC PVSEC, Barcelona, to be published

[11]   S. Beljakowa, T. Frank, D. Karg, G. Pensl, 20th EC PVSEC, Barcelona, to be published

[12]   C. Funke, O. Kiriyenko, O. Sciurova, H.J. Möller, 20th EC PVSEC, Barcelona, to be published

[13]   O. Breitenstein, J.P. Rakotoniaina, G. Hahn, M. Käs, T. Pernau, S. Seren, W. Warta, J. Isenberg, 20th EC PVSEC, Barcelona, to be published

[14]   W. Koch, W. Krumbe, I. A. Schwirtlich, Proc. 11th EC PVSEC, Montreux, 518 (1992)

[15]   L. W. Song et al., Phys. Rev. B **60**, 460 (1988)

[16]   J. L. Benton et al., J. Electrochem. Soc. **129**, 2099 (1982)

[17]   J. P. Kalejs in: Silicon Processing for Photovoltaics, Vol. II. Eds. C. P. Khattak and K. V. Ravi (Elsevier Amsterdam 1987) ch. 4

[18]   J. Carstensen, G. Popkirov, J. Bahr, and H. Föll, 16th EC PVSEC, Glasgow, United Kingdom, 1627

[19]   H. Behnken, R. Tiefers, W. Krühler, A. Froitzheim, G. Hahn, D. Franke, Proc. 19th EC PVSEC, Paris, (2004), 640

[20]   H. Behnken, M. Apel, D. Franke, Proc. 3rd WCPEC3, Osaka, Japan (2003), 1308

New Approaches to Solar-Grade Silicon Feedstock and Silane Productions

T.H. Wang, M.R. Page, T.F. Ciszek*
National Renewable Energy Laboratory, Golden, CO 80401, USA
* Now at Siliconsultant, P.O. Box 1453, Evergreen, CO 80437, USA

M.F. Tamendarov, B.N. Mukashev
Institute of Physics and Technology
2 Ibragimov Street, 480082 Almaty, Kazakhstan

The phenomenal growth of the silicon PV industry in the past few years is depleting the world's existing silicon feedstock supply produced by the chlorosilane chemistry. With continued greater demand on silicon feedstock in sight and high initial capital cost of the current feedstock technology, alternative silicon feedstock methods must be investigated even though many have been looked at and discarded. We report two available processes for silicon feedstock and silane production developed at NREL and in collaboration with IPT; atmospheric pressure iodine vapor transport (APIVT) and silane production from phosphorous industry wastes. These new approaches are much simpler either in chemistry (the first) or processing steps (the second), potentially significantly reducing the initial capital investment and production cost in a large-scale production.

Atmospheric Pressure Iodine Vapor Transport Purification of Silicon

Our work on the growth of thin-layer Si at atmospheric pressure by APIVT [1] led us to explore its applicability to MG-Si purification. Iodine reacts with Si to form SiI_4, which reacts further with silicon to form SiI_2. SiI_2 decomposes easily at high temperatures, with a silicon deposition rate >5µm/min when the source Si temperature is >1200°C and the substrate temperature is approximately 1000°C. When MG-Si is used as the source material, impurities can be effectively removed in several ways: (1) During the initial reaction between iodine and MG-Si, the formation of impurity iodides will be advanced or retarded (relative to the formation of SiI_2) depending on their free energies of formation. (2) Purification of SiI_4 by distillation in a cyclic process will cause metal iodides with vapor pressure lower than that of SiI_4 to remain at the bottom of a distillation tower, and those with higher vapor pressure to rise to the top. For example, at one atmosphere, carbon tetra iodide boils at 19°C higher than SiI_4 and phosphorous tri-iodide at 63°C lower.
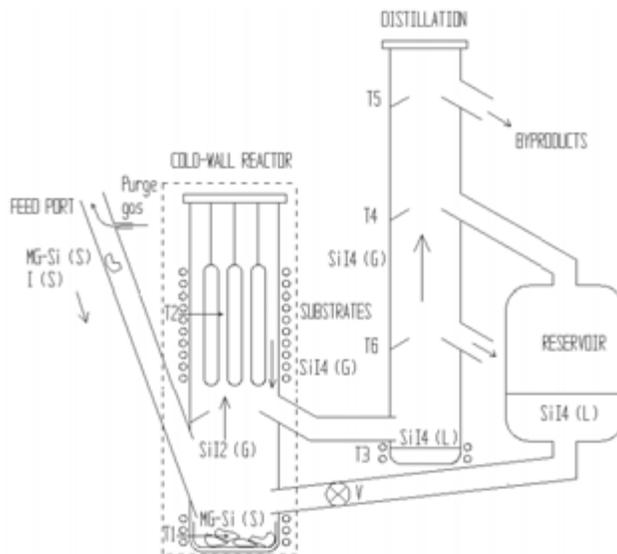

Fig. 1. Schematic of the cyclic APIVT MG-Si purification process incorporating components (1), (2), and (3)

These large differences permit easy separations. (3) During the deposition of silicon from SiI_2, most metal iodides have a large negative value of standard free energy of formation, so they are more stable than SiI_2 and SiI_4. These iodides will form readily in the gas phase, but have only a small tendency to be reduced again in the deposition zone. The cyclic APIVT refinement process incorporating these three components [2] is shown in Fig. 1.

In Fig. 1, MG-Si and I are located in a crucible at the bottom of a cold wall reactor and heated to temperature T1 (T1>1200°C). SiI_4 and then SiI_2 form, and SiI_2 is transported to substrates at a cooler temperature T2. Si is deposited, releasing SiI_4 which is diverted to a distillation column where it is purified before reentering the T1 zone to react again with additional MG-Si. As MG-Si is consumed, it is replenished through a gas-purged feed port. This gas purge is above an equilibrium iodine cloud that forms at a height corresponding to an appropriate temperature region cooler than T2. A similar purge above the cloud in the main reactor can allow removal of deposited purified silicon, thus affording a continuous process.

SiI_4 distillation [step (2) above] has been previously studied [3], so we focused on investigating purification by the initial reaction between iodine and MG-Si and by the final deposition of silicon from SiI_2 [steps (1) and (3) above]. First we grew ~100-μm-thick epitaxial layers of Si by APIVT from a MG-Si source onto high-purity, single-crystal substrates. Impurity levels in these layers are shown in Fig. 2. They were analyzed by secondary ion mass spectroscopy (SIMS) and glow discharge mass spectroscopy (GDMS). Also shown are the MG-Si source material impurity levels determined by GDMS. The vertical lines show the permissible range of impurities in SoG-Si, dependent on growth method, with the upper limit for slow directional solidification and near equilibrium segregation, while the lower limit is for growth with little or no effective segregation such as is the case for some ribbon growth processes. The selective APIVT pick-up, transport, and deposition of silicon reduced the concentration of all major impurities by more than several orders of magnitude except for B (and P, not shown). Addition of the distillation step (2) should reduce B and P to the SoG-Si specification.
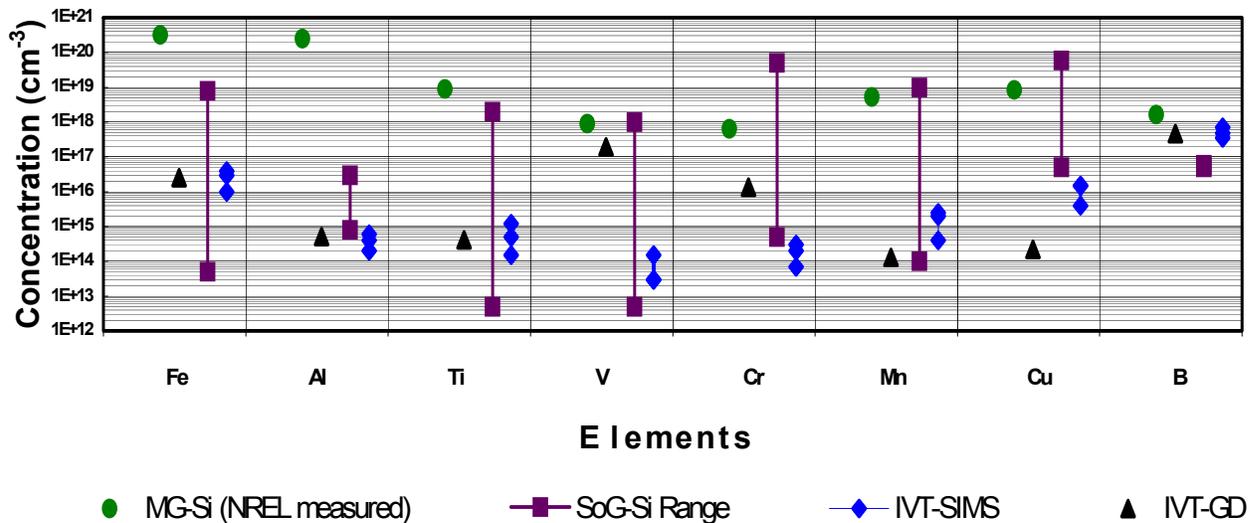

Fig. 2. Impurity contents in the MG-Si source material and in an epitaxial silicon layer grown by APIVT

Multiple large area substrates in the form of concentric quartz cylinders were used for APIVT growth of thick layers from a MG-Si source. These layers were harvested and melted as feedstock for Czochralski (CZ) crystal growth and analysis. The melt was clean and we successfully grew a single crystal from the APIVT purified MG-Si feedstock. GDMS analysis of impurities in the MG-Si source and in the CZ crystal grown from APIVT-purified silicon [4] show that all metallic impurities are below the detection limits of the GDMS technique (values preceded by <) which in the worst case was 0.005 ppma. The predominant non-metallic impurities were O (17.6 ppma), C (14.3ppma), P (6.8 ppma), and B (4.2 ppma). Thus, the crystal was highly compensated and mostly n-type, with $\rho = 0.3$ Ω·cm, n-type, near the tail end. However, a small region of the seed end was p-type with a resistivity of 0.4 Ω·cm. Diagnostic solar cells 2-mm x 2-mm in size were fabricated using a seed end wafer. These had an efficiency of 9.5%, compared to an electronic-grade CZ-grown control cell efficiency of 13.8%. The high degree of compensation and high levels of B and P likely influence the properties of the material. Incorporating the distillation step [step (2)] will probably be necessary to obtain better performance from the APIVT-purified feedstock.

IOSIL has licensed this APIVT technology to further develop the process for large-scale production and commercialization. Interested venture investors may contact the company founder, Dr. John Fallavollita (jfallavollita@iosil-energy.com).

Low-cost and High-yield Production of Silane from Phosphorous Industry Wastes

A significant portion of the cost in the conventional Si feedstock production is the precursor gas, silane or trichlorosilane. Silane is preferred for fluidized bed reactors because of its lower dissociation temperature but more expensive than trichlorosilane, even though Wacker Polysilicon has succeeded in using trichlorosilane with seed particles [5]. There are two well-known techniques to produce silane. One is the simultaneous reduction and oxidation of trichlorosilane with a catalyst. The other is the reaction of a silicon-containing alloy such as magnesium silicide with an aqueous acid solution. The first technique involves a series of complicated steps that leads to high cost. The second technique is much simpler but has the problem of low yield. A third technique is being used by MEMC [6], which involves sodium aluminum hydride ($NaAlH_4$) and silicon tetrafluotide (SiF_4), with SiF_4 production at an added cost.

Using aluminothermic reduction of silica in phosphorous industry wastes, scientists at IPT [7] are able to generate a silicon-containing alloy. This alloy consists of mostly $Ca_xAl_ySi_z$, $CaSi_2$, Mg_2Si and other silicides. In a powder form, this alloy reacts readily with hydrochloric acid to produce silane gas at ambient temperatures with a very high rate. The resultant silane gas is more than 80% of the silicon content in the alloy. The purification of silane may be carried out by known methods such as low temperature condensation and by use of adsorbent. Compared to a conventional silane production technology, even with the improved Bayer process [8] as shown in figure 3, this new process has much fewer process steps.
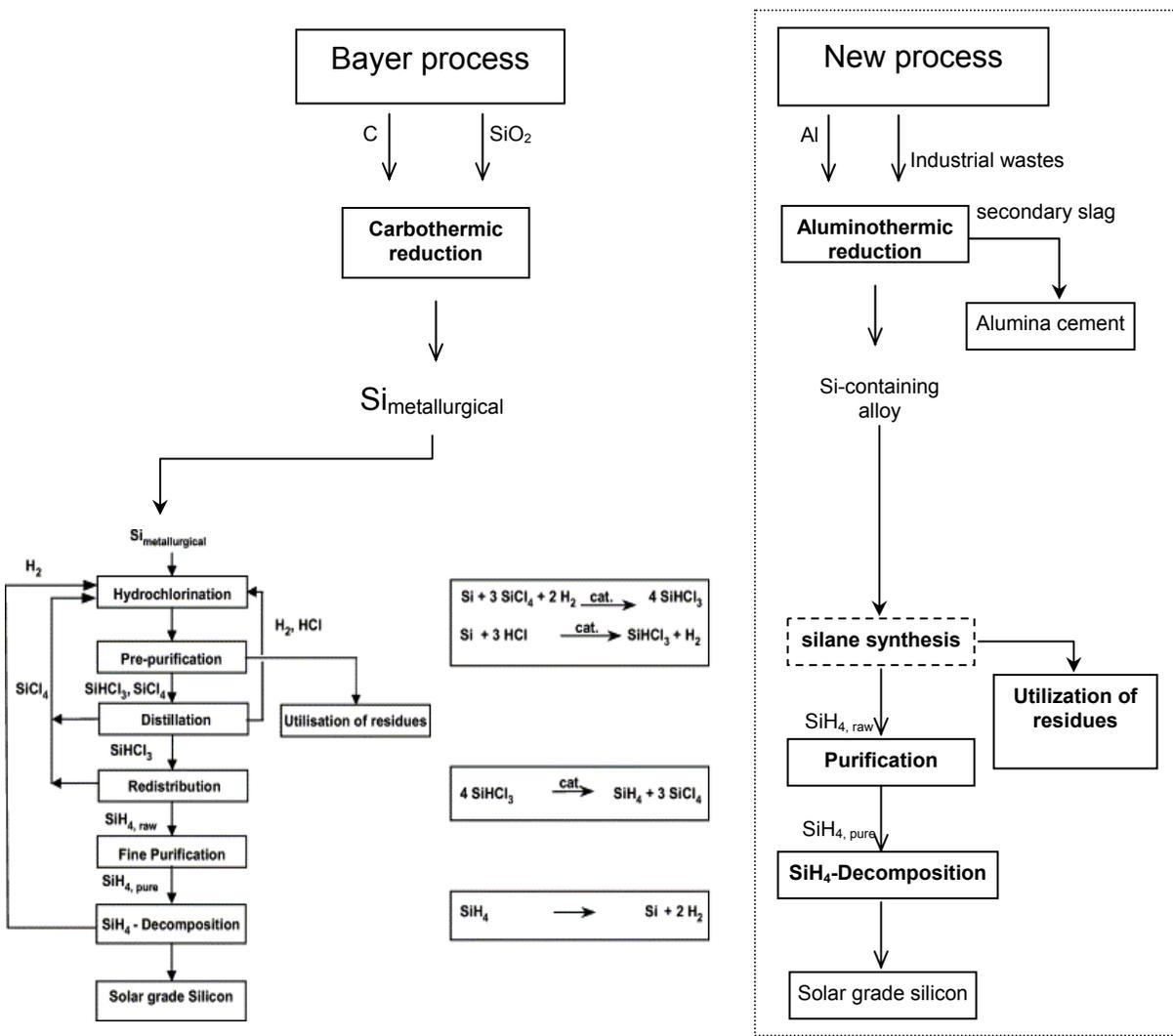
Fig. 3 A comparison of the new silane production process to the Bayer process

[1] T.H. Wang and T.F. Ciszek, *J. Electrochem. Soc.* **147** (2000) 1945-1949.

[2] T.H. Wang and T.F. Ciszek, US Patent#6712908, 2004.

[3] G.H. Moates, et al., US Patent# 3006737, 1961.

[4] T.F. Ciszek, T.H. Wang, M.R. Page, R.E. Bauer, and M.D. Landry, *Proceedings of the 29th IEEE PVSC,* New Orleans, Louisiana, May 2002, 206-209.

[5] Karl Hesse, Ewald Schindlbeck, "Feedstock for the Photovoltaic Industry", *2nd Solar Silicon Conference CD*, Photon Academy, April 11, 2005, Munich, Germany

[6] S. Lahoti, "MEMC Polysilicon Outlook", *2nd Solar Silicon Conference CD,* Photon Academy, April 11, 2005, Munich, Germany

[7] M.F. Tamendarov, B.N. Mukashev, *Proceedings of the 11th Si Workshop*, August 19-22, 2001, Estes Park, Colorado, NREL/BK-520-30838, 189-193

[8] P. Woditsch, W. Koch, *Solar Energy Materials &Solar Cells*, **72**, (2002), 11-26

Production of Solar Grade Silicon by an Ethanol Process

E.P. Belov, N.K. Efimov, E.N. Lebedev, V.V. Zadde, A.B. Pinov, D.S. Strebkov, D. M. Blake,* and K. Touryan*
INTERSOLARCenter, 2, 1-st Veshnaykovsky proezd, 109456, Moscow, Russia. Tel. (+7095) 171-19-20, fax: (+7095) 171-96-70 e-mail: viesh@dol.ru, info2@intersolar.ru.

*National Renewable Energy Laboratory, 1617 Cole Blvd, MS 3322, Golden Co 80401, USA,
Phone: 303-384-7701, Fax: 303-384-6363, email: dan_blake@nrel.gov

Abstract - The status of development of a new process for the production of solar grade silicon from metallurgical grade silicon (MGS) based on the direct reaction with ethanol is presented. Reaction of anhydrous ethanol with MGS produces a mixture of tri- and diethoxysilane that undergo catalytic disproportionation to yield silane and tetraethoxysilicon.   The silane can be converted to solar grade silicon (SGS) by conventional means.

Introduction - The majority of solar panels produced today are made from either crystalline silicon or cast poly-silicon. The silicon used is scrap or off-spec material that is by-products from the semiconductor industry.[1] The growth in demand for solar cells is projected to outpace the available supply from production of semiconductor silicon that will lead to significant increases in the price of silicon for solar cells.[2] A number of approaches to meeting the increased demand for SGS and reducing the cost of the silicon used for solar cells are being considered. In general these approaches are based on conventional chlorine based chemistry[1,2,3,4] but new chemistries are at various stages of development.[5] The goal is to develop these processes and install new production capacity will provide a stable source of solar silicon at a cost below $25/kg.
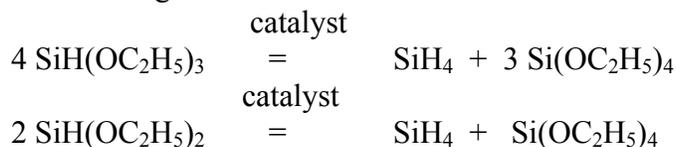
Background - The two dominant process for production of purified silicon are the Siemens process, in which trichlorosilane is reduced with hydrogen,[3] and the Union Carbide process where silane is produced by catalytic disproportionation of trichlorosilane and the silane is thermally decomposed to silicon.[6] In the former USSR, beginning from 1983, the main method of producing of high purity SiH_4, and then SGS, was catalytic disproportionation of triethoxysilane, $SiH(0C_2H_5)_3$.[7] Raw materials for producing $SiH(0C_2H_5)_3$ were $SiHCl_3$ and anhydrous ethanol. The process of synthesis of $SiH(0C_2H_5)_3$ and desorbtion of HC1 was implemented in film type apparatus. This method was realized in the "Kremny polimer" plant in Zaporojie, Ukraine, and production volume of SiH_4 was 12.6 t per year. SGS was produced from silane by pyrolysis, and high quality monocrystals for nuclear particle detectors and IR-receivers were produced by the float zone technique. Disadvantages of this method are: high consumption of ethanol, large waste stream, use of an energy consuming method silane purification at liquid nitrogen temperature, and use of ecologically dangerous Cl-containing materials.

The New Process – Development of a new process based on the ethanol technology was begun in 1999 in a project funded by the US DOE International Proliferation Prevention Program. This project is being done in partnership between NREL and the Intersolarcenter in Moscow, Russia. The block-scheme of the new chlorine-free technology (CFT) of SGS production is presented in Figure1. The new process[8] eliminates the use of chlorine completely. At the first stage raw, powdered metallurgical silicon and anhydrous ethyl alcohol react directly to produce a mixture of that is predominantly triethoxysilane with some diethoxysilane.

$$\text{catalyst}$$
$$\text{Si} + 3\ \text{C}_2\text{H}_5\text{0H} \quad = \quad \text{SiH(OC}_2\text{H}_5)_3 + \text{H}_2$$
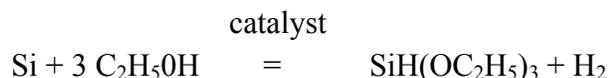
The process is less sensitive to the purity of the MGS than is the synthesis of trichlorosilane, thus less expensive 98% silicon can be used. The reaction is conducted in a high-boiling siloxane liquid with a copper-based catalyst at atmospheric pressure and temperature above 180^0C. At low pressure, unreacted alcohol is removed, which prevents conversion of triethoxysilane to tetraethoxysilane. At optimal conditions 85-90% of $\text{SiH(OC}_2\text{H}_5)_3$ is obtained, and the rest is diethoxysilane.

At the second step in the process the di- and triethoxysilane are converted into silane and tetraethoxysilane according the reactions:
$$\text{catalyst}$$
$$4\ \text{SiH(OC}_2\text{H}_5)_3 \quad = \quad \text{SiH}_4 + 3\ \text{Si(OC}_2\text{H}_5)_4$$
$$\text{catalyst}$$
$$2\ \text{SiH(OC}_2\text{H}_5)_2 \quad = \quad \text{SiH}_4 + \text{Si(OC}_2\text{H}_5)_4$$

Other changes from the "Kremny polimer" plant technology include a better catalyst for disproportionation, an improved process for purifying silane, and recovery and recycle of the ethanol. This allows disproportionation to be done at ambient temperature, increased equipment efficiency, and reduced energy consumption, currently estimated to be below 50 kWh/kg. The new process includes ethanol recycle

A significant advantage is the absence of chlorine in the process, which reduces corrosion, simplifies impurity removal, and eliminates potential release of metal chlorides to the environment. Furthermore, all stages of the silane purification are conducted at ambient temperature or at lower temperatures, down to the temperature of silane liquefaction. These reduce the risk of silane processing. The impurity elements of the III-V groups, and metals which are present in metallurgical grade silicon, are converted to alkoxy compounds without element-hydrogen bonds. Thus there is no possibility for them to be disproportionated with creation of volatile hydride like diborane, phosphine, and arsine. In this case main contaminates in the crude silane are high-boiling ethoxysilanes. Ethoxysilanes and another metalorganic compounds are removed at the next stage by adsorption of contaminants by liquid tetraethoxysilane cooled at -60^0C. Final purity of monosilane 99,999% is reached by adsorption of trace contaminates by activated charcoal and final purifying with a chemisorbent. The removal of boron and other critical impurities occurs at two process stages:

    1. during purification of raw triethoxysilane, due to the linkage of boron in solid or nonvolatile complexes;
    2. During catalytic disproportionation of triethoxysilane, because of the reaction selectivity the boron and some other elements (phosphorus, arsenic etc.) do not form volatile gaseous hydrides (B_2H_6, PH_3, AsH_3 etc.), and their liquid compounds are removed with liquid tetraethoxysilane.

Products that can be obtained from the process - Main products for the new process are production can be:

- SGS for the PV industry - Specific resistance of monocrystalline silicon samples produced by float zone technique is more than 10,000 Ω.cm, and the lifetime of minority carriers is up to 1000 μs
- Silane and silane mixtures with other gases
- Electronic grade silicon

The tetraethoxysilicon can be recycled for silicon production or converted to other products. The technological process allows to change assortment and shares of the products in total amount depending on market situation:

- As result of hydrolysis of tetraethoxysilane, silica sols are produced that can be used for a number of products
- Through organomagnesium reactions of tetraethoxysilane a wide range of silicone polymers can be produced,
- By thermal-oxidation of tetraethoxysilane superfine silicon dioxide (white soot) is obtained which is used as a filler material.

Progress to date - During the period from 2000 till 2003 the scientific and design works on creation of theoretical and experimental basis for chlorine free alkoxysilane technology of solar and electronic grade silicon feedstock production implemented has been made in cooperation and with financial support of NREL. The following works were executed during the period:

- improvements in the reaction of ethanol and MGS were made to maximize the yields of di- and triethoxysilane; effective solvent, catalyst and optimal regimes of the process were selected; design of the reactor was also elaborated.
- methods for recycle of tetraethoxysilane were investigated.
- a new silane pyrolysis apparatus was designed.
- method for tetraethoxysilane hydrolysis and returning of ethanol into the process was developed.
- design work on the small-scale pilot plant for SGPF with productivity 400 kg / year are completed. Works on creation and testing of the small-scale pilot plant can be executed within 25 months. The initial design and cost estimate for a 1000 tonnes per year industrial scale plant will be developed.
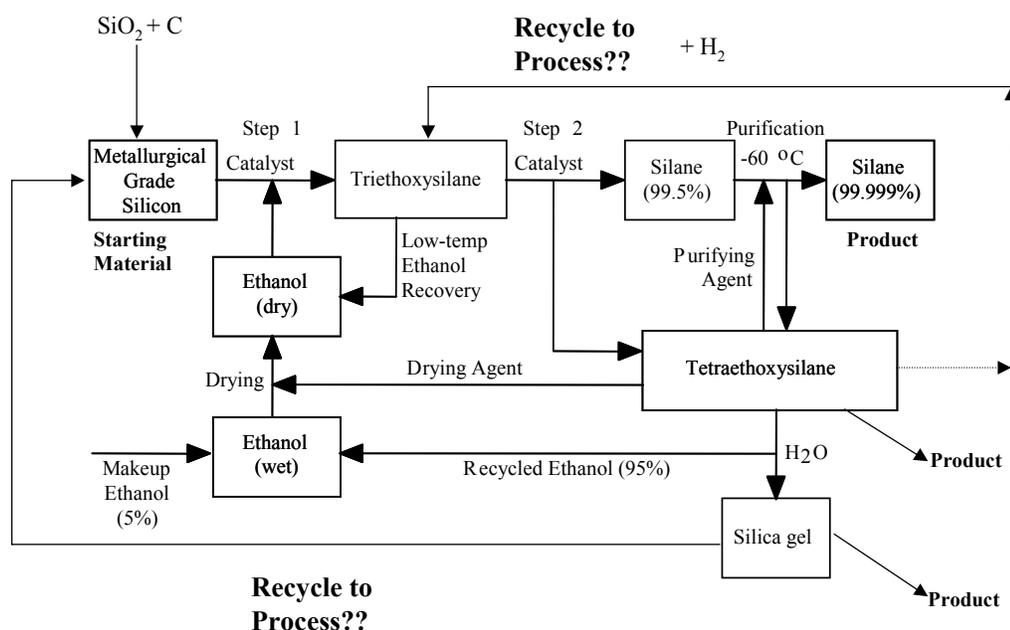
Figure 1. Block process flow diagram for the ethanol process for production of solar grade silicon.

References

[1] M. S. Keshner and R. Arya. Study of Potential Cost Reductions Resulting from Super-Large-Scale Manufacturing of PV Modules. NREL/SR-520-36846, NREL, Golden, CO, October 2004, 50 pp.

[2] H. A. Aulich. Silicon Supply for Solar PV. *Renewable Energy World*, November-December 2002, 49-59.

[3] W. C. O'Mara, R. B. Herring, I. P. Hunt, Handbook of Semiconductor Silicon Technology, Noyes Publications, Park Ridge, NJ 1990, pp.33-77.

[4] W. C. Breneman. Direct Synthesis of Chlorosilanes and Silane. Studies in Organic Chemistry, Catalyzed Direct Reactions of Silicon, K. M. Lewis and D. G. Rethwisch, eds. Elsevier, New York, NY (1993) 441-457.

[5] M.deWild-Scholten, E. Alsema, Towards Cleaner Solar PV, Refocus, September/October, 2004, 46-49.

[6] Union Carbide. Base Gas Condition for use Silane Process. Report DOE/JPL-954343-21, Nat. Tech. Inform. Center, Springfield, VA, 1981.

[7] S. I. Kleschevnikova, G. A. Dubrovskaya, E. I. Rumyantseva, Plastmassy, № 3, 1965, pp. 14-16.

[8] Tsuo, Y. S., et al. Method of High Purity Silane Preparation, US Patent No. 6,103,942, August 15, 2000.

MECHANICAL STRENGTH OF SILICON WAFERS AND ITS MODELLING

G. Coletti, C.J.J. Tool and L. J. Geerligs
ECN Energy research Centre of the Netherlands
Westerduinweg 3, NL 1755 LE Petten, the Netherlands
Tel.: +31 224 564382, coletti@ecn.nl

ABSTRACT: Mechanical strength measurements of multicrystalline Si wafers are carried out with a ring-on-ring test geometry. This geometry is very sensitive to the surface of the wafers rather than the edge. The measurements reveal the great importance of the saw damage on the mechanical stability of as-cut as well as textured wafers. The initial surface defects make a big and unexpected difference in the strength after a standard industrial acid etch. The strength analysis of wafers from different manufacturers shows no influence of bulk defects on strength. This geometry therefore permits to focus on the modification of mechanical stability by adaptations of, e.g., wafering or chemical treatment. The stress at breakage is translated into an apparent critical crack length, which can be used as an intuitive parameter to quantify the surface damage. The relationship between breakage force and wafer thickness from linear plate theory is analysed and verified.

1 INTRODUCTION

In the present photovoltaics industry the reduction of the wafer and cell cost is one of the main targets. This could be achieved by an increase of the wafer size, decrease of the thickness and a lower kerf loss. However, these changes could lead to an increase of the breakage risk reducing yield of wafering, solar cell, and module processes. The mechanical properties of multicrystalline silicon wafers are influenced by several parameters and defects, e.g. surface damage, edge damage, surface structure.

The mechanical properties can be detected in different ways. A bending breakage tester [1] gives the possibility to measure the maximum force necessary to break the wafers. It is one of the most common systems to check the mechanical stability. It is used by several research institutes and universities as well as by several wafer manufacturers. In this paper we use the bending breakage tester in a geometry exclusively sensitive to surface damage (rather than edge damage), and use it to analyse differences between wafers and surface treatments.

2 INSTRUMENT AND MEASUREMENT DESCRIPTION

Wafer strength is measured in a bending breakage tester by applying an increasingly stronger force until the wafer breaks, recording the maximum value of force applied and the maximum wafer displacement.

For the experiments reported here a geometry of the instrument was chosen which is sensitive to the surface damage only and not to the edge damage. The geometry that is most sensitive to the wafer surface is the ring on ring bending tester [1,2]. In our case the instrument consists of a support ring with a diameter of 80 mm, and a ring of half that diameter to apply the load. The loading stress is localised inside the loading ring. The breakage force and its correlations to e.g. sawing defects or a surface etch give important information on the effect of sawing and surface treatment on mechanical stability.

Unless otherwise noted, all wafers in this study are mc-Si 125 mm square size, and 200 μm thick. They were provided by two manufacturers (A and B).

3 THEORY AND MODELLING

In order to quantify the surface damage we propose the critical crack length as a parameter that gives an indication of the maximum size of the cracks present in the wafer surface. We used theory from fracture mechanics [4] to determine this crack length.

Silicon shows elastic behaviour and almost no plastic deformation before breaking at room temperature. Brittle fracture takes place when the applied stress at the tip of one crack (e.g. a micro crack due to saw damage) reaches a critical value. The stress in an element located at (r, θ) close to a crack tip can be written as [4]:

$$\begin{bmatrix} \sigma_x \\ \sigma_y \\ \tau_{xy} \end{bmatrix} = \frac{K}{\sqrt{2\pi r}} \cos\frac{\theta}{2} \begin{bmatrix} 1 + \sin\frac{\theta}{2}\sin\frac{3\theta}{2} \\ 1 - \sin\frac{\theta}{2}\sin\frac{3\theta}{2} \\ \sin\frac{\theta}{2}\cos\frac{3\theta}{2} \end{bmatrix} \quad (1)$$

where r is the distance from the tip, θ is the azimuth and K is the stress intensity factor $K_I = \sigma Y \sqrt{\pi a}$. K is a function of the stress magnitude σ, the crack length a and the configuration factor Y that reflects the geometry and the loading. The index I stands for the tensile mode in which the stress is applied in the normal direction to the faces of the crack. This mode is the overwhelming majority of actual situations involving cracked components.

A crack begins to propagate when the stress intensity factor reaches a critical value. The critical value is a material dependent parameter and is called fracture toughness K_{Ic} (0.93 ± 0.3 MPa·m$^{0.5}$ on {111} plane and 0.89 ± 0.3 on {110} plane for monocrystalline silicon material at low temperature [5]). Knowing the fracture toughness of the material, and the stress resulting in breakage, it is possible to calculate the critical crack length a, for which the stress intensity factor is equal to the fracture toughness K_{Ic}. The critical crack length has an intuitive connection with the surface roughness. It has a quantitative value only if compared under the same geometrical conditions for the samples and the measurement. We call the extracted parameter the *apparent* critical crack length because the geometrical conditions are not precisely known in real experiments.

In the calculation of the stress σ we make use of the linear plate theory [3] in which the deflection of the wafer is small compared to wafer thickness. In practise this condition is not completely satisfied. However, it still allows comparison of wafers with similar thickness.

In order to predict the mechanical stability of thinner wafers the relationship between the breakage force and the thickness of wafer have to be investigated. The relation we want to proof experimentally follow by:

$$\sigma_{max} = \frac{K_{Ic}}{Y\sqrt{\pi a}} \quad (2)$$

and

$$\sigma = C\frac{F}{t^2} \text{ (in linear plate approximation)} \quad (3)$$

The maximum stress tolerable by the sample is proportional to $1/t^2$ when an equivalent crack length a for wafers receiving the same surface treatment is assumed.

This implies the following relationship between breakage force and thickness:

$$F_{max} = c{\cdot}t^2 \quad (4)$$

where $c = K_{Ic}/\left(CY\sqrt{\pi a}\right)$. In the last section this relationship is verified experimentally.

The aim of the following experiments is to detect differences in mechanical stability of wafers cut with different sawing parameters. In order to check the capability of the instrument and the geometry adopted and to verify the values of critical crack length extracted we performed an experiment using different surface treatments.

4 CALCULATION OF THE CRITICAL CRACK LENGTH FOR DIFFERENT SURFACE TREATMENTS

We used 24 neighbouring multicrystalline wafers provided by B. Three out of four groups were treated with different chemical etching as shown in Table I.

All the wafers showed saw marks along the full surface. The saw marks look like straight parallel lines with step height ranging from 10 to 30 μm. However, it is difficult to quantify their number and their density. In Table I the measured average breakage force, the average breakage stress localised inside the loading ring and the extracted critical crack length (using K_{Ic} = 0.9 MPa·m$^{0.5}$) are reported.

Group	As-cut	Saw damage etch	Polish etch	Polished + defect etch
Wafers #	10	2	10	2
Thickness	195 μm	168 μm	147 μm	~150 μm
Average force N	29±(7%)	57±(3%)	72±(31%)	23±(13%)
Average σ_{max} N/m^2	5.6×10^8	1.5×10^9	2.4×10^9	7.4×10^8
Critical crack length	0.8 μm	0.12 μm	0.04 μm	0.5 μm

TABLE I: Surface effects on the breakage force (B wafers). In brackets the standard deviation (%). σ_{max} is the stress (calculated from applied force, with linear plate theory) at which the wafer breaks (the fracture stress).

The as-cut wafers broke with an average force of 29 N and the critical crack length is 0.8 μm. These wafers have more than two times bigger micro cracks than the set of as-cut wafers reported in a previous work [5]. The difference must be due to a different saw damaged surface (including saw marks) and/or different crystal defects in the bulk.

By polishing the saw damaged surface the breaking force is more than doubled (72 N), even though the wafers become 25% thinner due to the polishing etch. The crack length (0.04 μm) is more than an order of magnitude smaller than before the etch. However the standard deviation of the breakage force increases.

Alkaline saw damage etching leads to a smaller but still significant reduction of the maximum crack length (note that stress or crack length should be compared, rather than force, to account for thickness variations).

The defect etch, after polishing, leads to a remarkable increase in the apparent crack length. This treatment exposes the dislocation structure from the polished surface. Apparently, the etched defects are effective nucleation points for fractures.

In conclusion the experiment showed quantitatively the effect of the saw damage on the mechanical stability of the wafers. We have determined that by removing the saw damage from the wafers the mechanical stability is doubled. These observations were made possible by using ring on ring breakage tester, which excludes the wafer edge from the measurement.

4.1 Industrial acid etching

Another set of 20 neighbour wafers provided by the same manufacturer B were compared after processing with ECNs' industrial acid etching and an alkaline saw damage etching. The wafers were divided in 4 groups processed in different ways, as shown in Table II.

Group	As-cut	Saw damage etch	Industrial acid etch T1	Industrial acid etch T2
Wafers #	5	5	5	5
Average force N	30±(9%)	64±(8%)	73±(7%)	54±(18%)
Average σ_{max} N/m^2	5.5×10^8	1.8×10^9	1.6×10^9	1.2×10^9
Critical crack length	0.8 μm	0.08 μm	0.1 μm	0.2 μm

TABLE II: Mechanical stability after industrial acid etching of B wafers. T1 and T2 correspond to the different etching time.

The aim of this experiment is to look at the effect of ECNs' industrial acid etching on the mechanical stability of the wafers. We used two different etching times. T1 is the ECN standard recipe currently used in industry and T2 is the same but with double etching time. For comparison also results of as-cut wafers and alkaline etched wafers are shown.

The results for the as-cut wafers and after saw damage etching are consistent with Table I.

The T1 recipe has a very positive effect on the mechanical stability of the wafers. The stress applied to break the wafers is 3 times greater than for as-cut wafers and the critical crack length is almost ten times smaller. The results

are comparable to the saw-damage etch and approach the strength after polishing etch in Table I.

That the strength after alkaline saw-damage removal and acid etch is comparable is somewhat counterintuitive. One would expect that the more pronounced surface texture after acid etch would weaken the wafer. A detailed analysis on the surface structure should be carried out to resolve this.

We see a weakening of the wafers when the acid etching time is doubled. A dislocation structure appears on the front surface of the wafers. As seen also in the previous experiment (Table I) these areas can be nucleation points for breakage. An important result is that for these wafers the etching time (T1) for best electrical cell properties ($J_{sc}xV_{oc}$) is also good for better mechanical properties.

A similar experiment was performed on wafers of the same size and thickness but from a different manufacturer (A). Each wafer comes from a different position in the ingot and it is neighbouring to the corresponding wafer in each group.

Group	As-cut	Saw damage etch	Industrial acid etch T1
Wafers #	15	15	15
Average force N	43±(18%)	57±(8%)	43±(17%)
Average σ_{max} N/m^2	8.4×10^8	1.5×10^9	9.7×10^8
Critical crack length	0.4 μm	0.1 μm	0.3 μm

TABLE III: Mechanical stability on wafer type A.

The as-cut wafers present a higher mechanical stability than the type B as-cut wafers (Tables I and II). The average stress applied to break them is 40% higher and the critical crack length is half that of the corresponding B wafers.

After the alkaline saw damage etch the fracture stress is about 1.5-1.8×10^9 N/m^2, the same as for the type B wafers in Table I and II. Such an etch is probably not, or only weakly, dependent on the initial condition of the surface. This shows that type A and type B wafers are intrinsically of similar strength. Therefore we can exclude the influence of a bulk defect in comparing results on type A and type B wafers, or at least such an influence is included in the variation we obtain (3×10^8 N/m^2).

The first conclusion is, therefore, that type A wafering has apparently resulted in less surface damage than the type B wafering. A further work would be to correlate the strength of as-cut wafers with the sawing parameters used (e.g. SiC diameter).

When the type A wafers are treated with the T1 industrial acid etch the strength differs strongly from the experiment in Table II. Whereas Table II showed a remarkable increase in σ_{max}, in this case we have only a slight increase (15%). As mentioned above, it is likely that the two kinds of wafers have a different amount and/or type of saw damage. Type B *as-cut* wafers are *weaker*, e.g., due to the presence of deeper defects. After T1 acid etching, the type B wafers are *stronger*.

The difference in the strength after acid etching for the two manufacturers should be addressed to the different defect structure present on the surface because the intrinsic strength of the wafers is the same. Optically they look similar (comparable surface reflectance). The acid etching carried out therefore has the effect to remove the more effective defects better from wafer type B compared to wafer type A (effective from the mechanical stability point of view). We conclude therefore, that the initial defects in the surface make large and unexpected differences in the strength after T1 acid etching.

A remark should be made for the comparison of experiments in Table II and III. The T1 acid etching results in one side of the wafers being rather uniform (what we call front) and the other side with some defects. In Table III the type A wafers were broken with the front side up. Hence the loading ring applies a force on the front and opens the defects present on the backside of the wafers. In Table II, the B wafers were broken with the front side down. An experiment was carried out to quantify this effect, using 10 neighbour A wafers. The wafers received the industrial acid etching T1 and half of them were broken with front side up and half with front side down. Results are shown in Table VII.

Group	Front side up	Front side down
Wafers #	5	5
Average force N	37±(7%)	43±(6%)
Average stress N/m^2	7.8×10^8	9.1×10^8
Critical crack length	0.4 μm	0.3 μm

TABLE VII: Mechanical stability on acid etched type A wafers broken with front side up and front side down.

The force applied to break the same wafers differs by 6 N (15%). This means that the defects on the backside have a limiting impact on the wafer strength, insufficient to explain the difference between type A and B wafers.

5 INFLUENCE OF WAFER THICKNESS ON THE BREAKAGE FORCE

We used 40 wafers from the best quality class of the manufacturer B. The quality class includes the geometric defects of the wafers such as the presence of saw marks and the total thickness variation (TTV). In this case best class means saw marks between 0 and 20 μm and TTV between 0 and 50 μm. Actually no such classification information was available in the previous experiments. The only information there was the qualitative description and height of saw marks.

The B wafers came from a different ingot than the previous experiments, were 270 μm thick and 150x150 mm^2 large. They were divided into two groups and processed with the T1 industrial acid etch and the alkaline saw damage etch with the same process parameters as the previous experiments. The results are shown in Table IV.

Group 270μm	Saw damage etch	Industrial acid etch T1
Wafers #	5	5
Average force N	>215	125±(8%)

TABLE IV: Industrial acid and saw damage etched wafers. The first do not break with the max available load of 215N.

The saw damage etched wafers sustained a load of 215N without breaking. This was the maximum force applicable by the instrument.

It is not possible to correlate the maximum stress for these wafers with the maximum stress of the wafers in the section 4 due to the large differences in the wafer thickness. Comparisons can only be made between wafers with similar thickness due to the approximations in using the linear plate theory.

To see the influence of the thickness on the mechanical stability, Fig. 1 shows the force versus the wafer thickness.
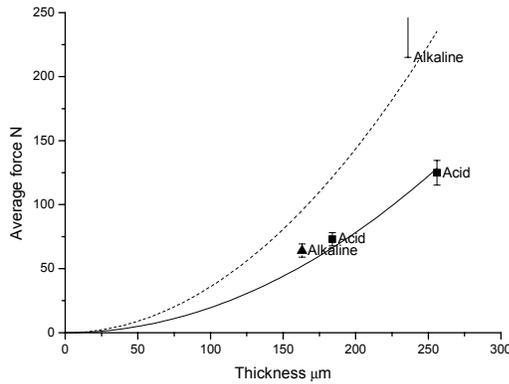
Fig. 1: Force versus thickness for saw damage (alkaline) and acid etched samples. The solid line represents the best fit based on Eq.4 for acid etched samples; the dashed line for saw damage etched.

The unbroken saw damage etched wafers are represented with an error bar starting at the maximum force applicable with our bending breakage tester (215N).

Interesting is the good agreement between the breakage force measured for acid etched wafers and a quadratic dependence on the square of thickness coming from Eq.4.

The quadratic behaviour is not clearly shown by the alkaline etched wafers. The dashed line in Fig. 1 is the best fit to the two available data points. Even though the crack length distribution should be more under control for these samples, the experimental evidence shows that Eq.4 is not fulfilled for a unique value of the constant c as for the case of acid etched samples.

We can analyse this problem by looking in more detail at Eq.3. In the relation between F and σ the geometry of the breakage tester is included. This means beside the rings diameter (support and loading one) also the wafer geometry.

Especially for alkaline samples in which the reduced crack length increases the maximum stress other effects become important. In this particular case the larger wafer size could

have an influence on the stress-force relationship (i.e., $\sigma < CF/t^2$) but also the lower values of TTV and height of saw marks could increase σ_{max} (since the wafers were classified as first class material). That is the reason why the fit does not work well.

In the acid etched samples the larger crack length results in a smaller σ_{max}. This smaller value could somehow hide the effect of TTV and saw marks. Furthermore the maximum wafer deflection is less due to lower force, therefore σ is closer to the result of linear plate theory: CF/t^2 (where it is slightly dependent on wafer size). Those are the reason why acid etched samples fit well the Eq.4.

6   CONCLUSIONS

A ring-on-ring bending tester is very sensitive to surface damages on multicrystalline silicon wafers, and not noticeably to even severe damages in the edge region. This permits to quantify the effect of saw damages as well as etching treatments on the mechanical strength independently of edge damages. To quantify surface damage we propose the apparent critical crack length, which gives an indication of the maximum size of the cracks present in the wafer surface.

There is an inverse correlation between strength as-cut and strength after acid texturisation, which needs to be investigated further. The intrinsic strength of wafers from two different manufacturers was found to be similar, as the alkaline saw damage etch has revealed.

In conclusion we can state that the saw damage has a large effect on the mechanical stability of as-cut wafers but also on the mechanical stability of acid etched wafers. The acid etching time for best electrical cells properties is also good for better mechanical properties.

Essential in further analysis will be the complete analysis of the actual stress force relationship by means of finite element analysis or real stress measurement. Also the breakage of samples with different and known TTV and saw marks has an important role in the understanding of the complete phenomenon. The data presented in the last section shows the importance of the alkaline etch to bring forward these second order effects.

7   ACKNOWLEDGEMENTS

8   REFERENCES

[1] H. Behnken, M. Apel and D. Franke, Simulation of mechancal stress during bending tests for crystalline wafers, WCPEC 3, May 2003, Osaka.

[2] G. Coletti, K. Tool, L. J. Geerligs, Quantifying surface damage by measuring mechanical strength of silicon wafers, 20th EPVSEC, June 2005, Barcelona.

[3] D.K. Shetty, A.R. Rosenfield, P. Mc Guire, G.K. Bansal and W.H. Duckworth, Biaxial flexure tests for ceramics, ACS Bulletin, 1980, vol. 59, n. 12, p. 1193.

[4] Hertzberg R., Deformation and Fracture Mechanics of Engineering Materials, John Wiley & Sons,NY 1996.

[5] R.Hull, Properties of crystalline silicon, 1999, INSPEC, The institution of Electrical Engineers, London, UK.

DEVELOPMENT OF LOW STRESS ALUMINUM BACK SURFACE FIELD PASTES

C. Khadilkar*, S. Kim, and A. Shaikh
Ferro Corporation, Electronic Materials System,
1395 Aspen Way, Vista, CA 92083, USA
Tel: (760)-305-1000, **Fax**: (760)-305-1100
*Ferro Corporation, Posnik Center for Innovative Technology,
7500 East Pleasant Valley Road, Independence, Ohio 44131, USA

Abstract

Aluminum pates are commonly used for an industrial-scale silicon solar cell manufacturing to form an alloyed Back Surface Field (BSF) layer to improve the electrical performance of the cells. The most important variables to control the cell performance under industrial processing conditions are a) paste chemistry, b) deposition weight and c) firing conditions. Also, a wafer bow becomes an issue, as the solar industry is moving towards thinner wafers. Microstructure development, electrical performance, and bow reduction of new pastes developed with an additive have been discussed in this paper. New Aluminum Back Surfaced Field Pastes are developed for use with silicon wafer thicknesses below 200 microns. The bowing of < 1mm of 200 micron wafer was achieved by modifying the paste microstructure. These pastes also show excellent electrical characteristics.

Introduction

There is a need to reduce the Si wafer thickness to improve Si utilization and to reduce solar cell material cost. The wafer warpage or bow becomes an issue when the Si wafer thickness is decreased below 240 μm. Generally, bow tends to decrease with reducing paste deposit amount but there is a practical lower limit below which screen-printed Al paste will result in a non-uniform Back Surface Field (BSF) layer. Understanding the microstructure and stress development during the firing cycle is necessary to address the conflicting requirements of less wafer bowing and an optimum and uniform BSF layer.

The Al back contact paste consists of aluminum powder, glass powder and additives in a suitable organic vehicle system. Recently, more attention has been given to understand effects of paste chemistry and firing conditions on microstructure development [1-3]. In this paper Al-back contact microstructure and stress development during the firing cycle is described. A new low bow Al ink is developed suitable for thin wafers. The effects of temperature and deposition weight on bow and microstructure development are studied. New paste composition has been developed where inter-particle stresses and bonding have been reduced with additives and with modifications to glass chemistry to reduce bowing and to improve electrical performance.

Experimental Procedure

Single and polycrystalline wafers with thicknesses varying between 180 micrometers to 280 micrometers were selected for this study. First an optimum aluminum powder particle size and morphology was selected to produce bead free Al layer. Several lead free glasses were tested. The glass showing the best electrical characteristics and adhesion was selected. The experimental pastes were prepared using the optimum aluminum powder, glass chemistry and carrier organic vehicle. Several inorganic additives were evaluated to study their effect on

bowing behavior. The bowing was measure using by measuring the height between the lowest and the highest point on a silicon wafer. The inorganic additive, which had the most pronounce effect on the bowing was chosen for this study. The effect of amount of inorganic additive on bowing and the electrical performance was studied. The most optimum paste composition was then used to study the effect of processing conditions such as paste deposit weight and firing condition on the BSF formation and on the electrical performance.

The pastes were printed using a 200 mesh screen and varying emulsion thickness to achieve depositions varying between 0.035 grams /inch^2 to 0.055 grams / inch^2. These wafers were then fired in an infrared kiln using varying firing profiles. The infrared furnace used for this study had three firing zone with zone lengths of 7", 15 " and 7 " respectively. The first two zones were set and 780 ^{o}C and 830 ^{o} C and the last zone temperature was varied between 880° C to 990 ^{0} C. A typical furnace profile for the last zone temperature of 930° C is shown in Fig. 1.
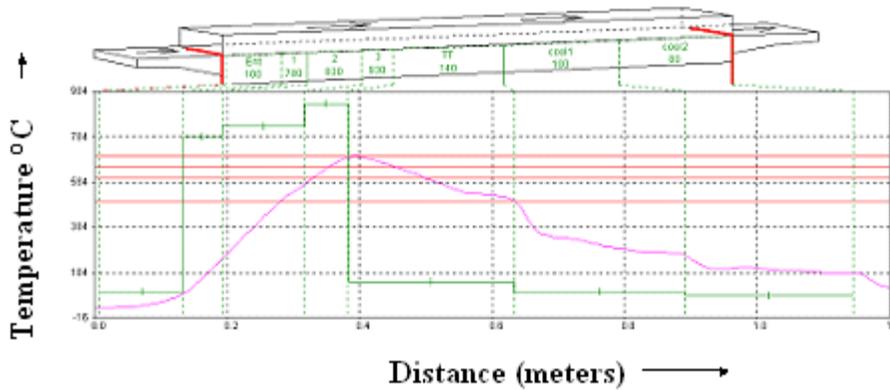
Figure 1 shows a typical temperature profile used for a three-zone belt furnace.

Results

Figure 2A shows effect of inorganic additive amount on the bowing of silicon substrate at various deposition weights and Figure 2B shows the electrical performance as measured by cell efficiency (η) of single-crystal Si cells prepared using these pastes.

The bowing decreased with addition of the additive. Addition of 2 % of the additive gave the optimum electrical performance. The optimum composition was printed on the wafers of different thicknesses. The Table I show the bowing of these wafers. The bowing of 180 micron 125 mm X 125 mm wafer was about 1.4 mm.

Table I: Effect of wafer thickness and the deposit weight on wafer bowing.

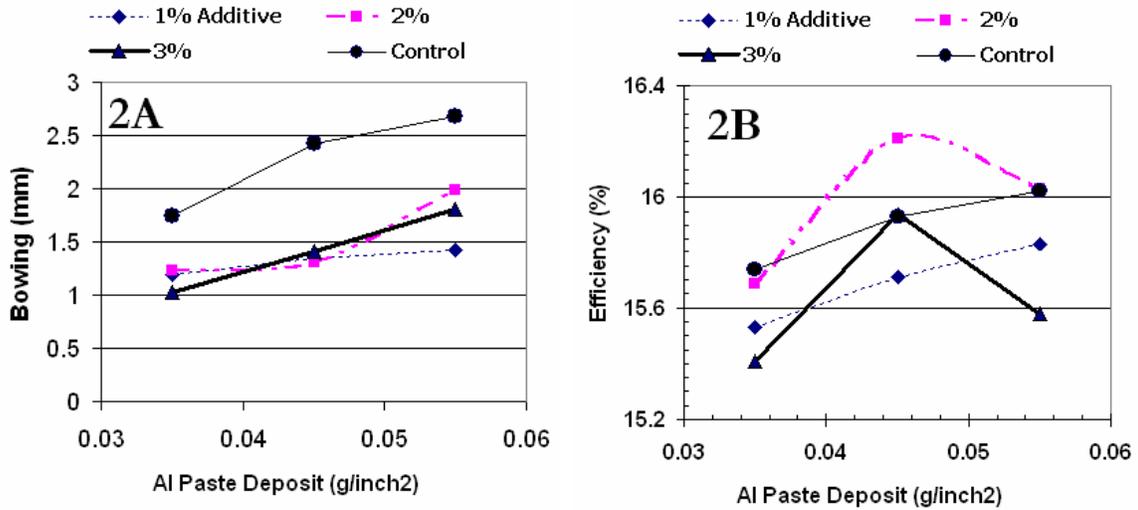| Paste deposit (gr/sq in)	Wafer Thicnkess (µm)		
	260	230	180
	Maximum Bowing (mm)		
0.045	0.50	0.60	1.31
0.055	n/m	0.79	1.99

Figure 2A shows the effect of inorganic additive on bowing and Figure 2B shows the effect of inorganic additive amount and the paste deposit weight (grams/inch^2) on fired cell efficiency.

The BSF formation with the most optimum paste was studied by depositing varying weights of the optimum paste and firing them under different firing peak temperatures. Figure 3 shows a typical cross section of a fired Al-paste Si back contact microstructure consisting of three distinct layers over the Si wafer. The details of paste microstructure development are discussed later.
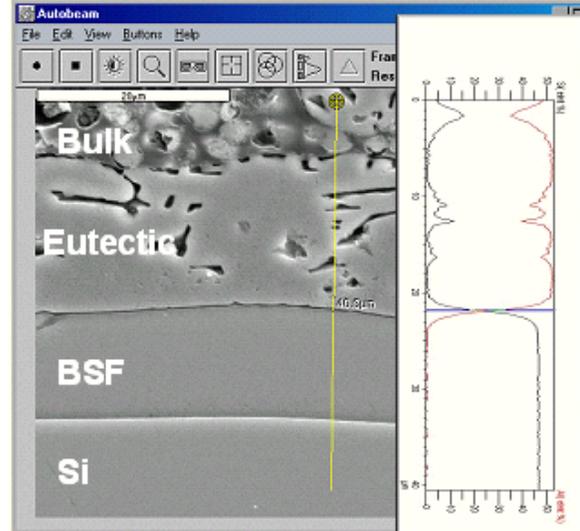
Figure 3 shows a polished SEM cross section of a fired Al paste- Si back contact consisting of a 1) BSF layer 2) an eutectic layer, and 3) bulk particulate Al paste layer. SEM line scan for Al and Si is also shown in the Figure. A sharp change in the Al-Si concentration profiles at the BSF-eutectic interface were observed.

Figure 4 shows plots of BSF and eutectic layer thickness as a function of paste deposit weight for fired samples at a set temperature of 930 °C. Polished and etched SEM cross-section images were used to measure the BSF and eutectic layer thickness. Figure 5 shows plots of BSF and eutectic layer thickness as a function of a set temperature with the paste deposit amount of 0.45g/inch^2. The eutectic layer appears to grow much more rapidly as a function of temperature and amount of paste deposited compared to a BSF layer.
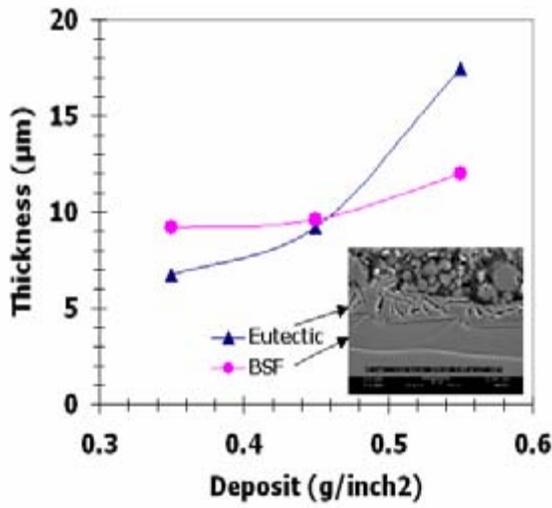
Figure 4 shows influence of the deposit weight and firing temperature on the BSF and eutectic layer thickness for samples fired at the set temperature of 930 °C.
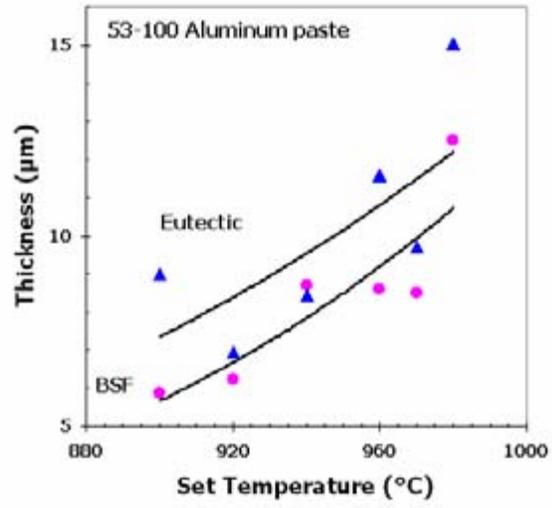
Figure 5 shows effect of furnace set temperature on the eutectic and BSF layer thickness measured from the polished SEM cross sections.

The BSF layer properties such as Al doping level and profile, defects and uniformity have an influence on the electrical performance. Various techniques such as Secondary Ion Mass Spectroscopy (SIMS) [4], Electrochemical Capacitance Voltage (ECV) [5], etc. have been used to study the BSF layer properties. The BSF layer was further analyzed using a Time of Flight (TOF) SIMS technique. Figure 6 shows Al concentration as a function of distance towards the bulk Si as measured by the TOF SIMS analysis.
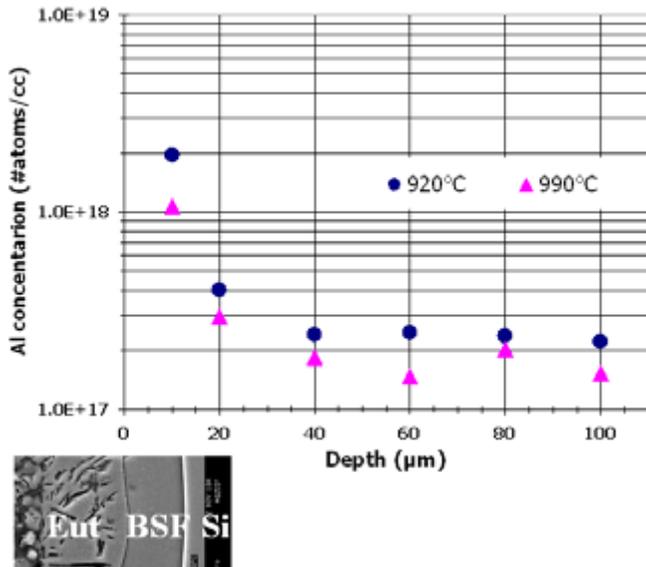

Figure 6 shows a Time of Flight (TOF) SIMS concentration profile of a polished cross section of the Al paste Si interface. The starting depth (zero) represents the BSF-Eutectic layer interface as shown in the Figure. The Al concentration was ~1-2 x 10 [18] atoms/cm^3 similar to reported in literature [4-5]

124

Discussion

The wafer bows and forms a convex body during cooling due to a higher Coefficient of Thermal Expansion (CTE) of a fired paste structure compared to Si (Al CTE of ~ 25 x 10^{-6} 1/°C and Si ~ 3.5x 10^{-6} 1/°C). The amount of bow depends on the fired paste microstructures themo-mechanical response to stresses generated due to differences in CTE's during cooling. For an elastic layer on an elastic substrate the bow can be predicted quantitatively using a bi-metallic strip model. The amount of bow at room temperature depends on a) differences in CTE's b) a ratio of elastic modulii of two materials c) a ratio of relative thicknesses and d) the temperature difference between the temperature at which coating becomes rigid and the room temperature. For a given geometry and firing profile, the elastic modulus of the paste microstructure has the most significant effect on a wafer bow. Bow starts to develop when the paste start to resist the stresses generated due to CTE mismatch. For Al back contact paste, observed bow is significantly less compared to a bow predicted by the elastic model if nominal values for elastic modulii of ~70 GPa for Al and ~110 GPa for Si are used. The observed reduced bow has been explained by plastic deformation of the fired paste layer [6]. It is expected that the Al-Si eutectic structure can plastically deform and can also show a creep flow at temperature as low as 300 °C (0.6T$_M$ where T$_M$ is the melting point of Al in °K) in response to stress due to CTE mismatch to relieve the stress. Also, appropriate temperature needs to be used in the bi-metallic strip model where the paste starts exhibiting elastic behavior and that temperature can be as low as 300 °C instead of an eutectic temperature (Teut) of Al-Si alloy of ~577 °C.

The increased amount of bow with increasing deposit weight as observed in Figure 2A can be related to higher thickness ratio (thickness of Al/thickness of Si) in the elastic model. The decreased bow with additive addition at a given level of deposit as shown in Figure 2A indicates that a) the elastic modulus of the paste microstructure seems to have decreased and or b) temperature at which the Al film has become rigid has decreased with the addition of an additive. The exact role of additives in reducing bow is not well understood but it can be speculated that the inorganic additives tend to reduce the inter-particle interaction hence the elastic modulus of the paste microstructure, which leads to reduced bowing.

Screen-printed and dried paste consists of a porous particulate layer with ~20-40 volume% porosity with an organic binder distributed between the particles. The binder burnout is completed by ~350 °C during the firing cycle. Between the temperature of ~400 °C to the melting point of Al (Tm ~657 °C) several processes are occurring simultaneously. Above ~470 °C (~ 0.8 T$_M$) Al becomes thermally active for a diffusion and sintering. Diffusion and subsequent precipitation of Si into solid Al thin film has been reported for various types of Si substrates well below the eutectic temperature of ~577°C for Al-Si alloy at temperatures as low as ~450 °C [7]. This diffusion bonding of Al particles with Si is expected to take place near ~450 °C, which can prevent lifting of Al particles away from the Si interface. In the same temperature range, glass particles tends to soften and start wetting Al particles and flowing towards Si substrate due to capillarity. A continuous glass layer at Si-Ag paste interface has been observed for a front contact paste but the diffusion bonding of Al particles with Si seems to prevent formation of a continuous glass layer at the Al paste Si back contact interface.

Al particles are oxidized during heating to a higher temperature and oxidation mechanism is described below [8]. Between 300 to 550 °C, an amorphous alumina (Al$_2$O$_3$) layer is formed and its thickness increases with increasing temperature. At about ~550 °C, amorphous layer transforms into γ- Al$_2$O$_3$ when the amorphous layer thickness exceeds ~4 nm. The density of a

newly formed γ- Al_2O_3 is higher than the amorphous Al_2O_3, which leads to a partial coverage of an Al particle. Heating above ~550 °C, there is an initial rapid increase in the oxidation rate till γ- Al_2O_3 layer becomes continuous. It is expected that Al particle-to-particle contact formation will be more favorable when the oxide layer is not continuous. The presence of oxide layer may be responsible for the observed paste microstructure where the fired paste away from the Si interface shows a particulate structure as shown in Figures 3 and 4.

Further heating above T_{eut} of ~577 °C, a substantial interaction and inter-diffusion between Al and Si is expected. Above Tm, Al metal particles will start melting and Si will start dissolving into molten Al liquid more rapidly. During further heat up, flow of Si away from the substrate and Al flow towards the Si substrate is expected. An oxide shell formed on Al particles could play an important role in holding liquid inside the shells. The firing temperature will determine the amount of Si dissolved into molten Al liquid. From the Al-Si phase diagram, an Al-Si alloy with ~30 wt% Si is formed at ~800 °C. The dissolution rate of Si into Al appears to be quite rapid at these temperatures. If the heating rate is too slow then localized Al-Si reactions can take place leading to a non-uniform interface microstructure. It is important to have a complete wetting of Si substrate by Al-Si liquid metal to form a uniform BSF layer [3].

During cooling from a peak firing temperature, the solubility of Si in the Al-Si melt decreases as expected from the Al-Si phase diagram. During cooling from a peak firing temperature to Teut of ~577 °C, liquid-phase epitaxial growth of Si on Si wafer occurs. The concentration of Al dissolved into Si at ~800 °C is ~0.001 wt% leading to a formation of p+ epitaxial layer. During Si solidification form the melt, due to movement of liquid-solid interface away from the Si substrate, impurities are rejected into the melt away from the precipitated Si interface and thus increasing the purity of p+ region enhancing lifetime for minority carriers. The Si concentration in the melt progressively decreases from ~30 wt% to eutectic composition of ~ 12% Si. At or below eutectic temperature of Teut~ 577 °C (with some under cooling) remaining ~80% of the molten liquid with eutectic composition solidifies near the BSF layer and inside the oxide shells. The resulting solidified paste microstructure consists of three layers: 1) BSF layer (5-15 μm thick), 2) Eutectic layer with needle shaped Si crystals (~5-15 μm), and 3) a particulate structure consisting of eutectic composition inside and around Al_2O_3 shells intermixed with glass and additives.

The increased BSF and eutectic layer thickness with a peak firing temperature as shown in Figure 5 can be explained by increased amount of Si dissolution and increased amount of liquid formation with increasing temperature, as expected from the Al-Si phase diagram.

Thus, the thickness of BSF layer, Al concentration in the BSF layer, themo-mechanical properties of the eutectic layer, and a weak particulate structure are important parameters in controlling a bow (Fig 2A) and electrical performance (Fig 2B) of Al back contact paste.

Summary

A new paste with an additive has been developed. The additive decreases the wafer bow for ~180μm wafer to about 1.4mm. The reduced bowing appears to be due to decreased elastic modulus of a fired microstructure with an additive and also lowering of temperature at which the paste becomes more rigid. The peak firing temperature and the deposit weight has a strong influence on the back surface field (BSF) layer thickness. The concentration of Al in the epitaxial BSF layer was ~ 1- 2 x 10 [18] atoms/cm3 as measured by the TOF SIMS measurements. The

electrical performance as measured by cell efficiency was dependent on deposit amount, additive amount and the peak firing temperature.

References:

1) S. Kim et al., "Aluminum Pastes For Thin Wafers", Proceedings, IEEE PVSC, Orlando (2004)

2) A. Schneider et al., Proc. 29th IEEE PVSC, New Orleans (2002) 336

3) F. Huster, "Investigation of the Alloying Process of Screen Printing Aluminum Pastes for the BSF Formation on Silicon Solar Cells", 20th European Photovoltaic Solar Energy Conference, Barcelona (2005)

4) P. Lolgen, "Surface and Volume Recombination in Silicon Solar Cells", Ph.D. Thesis, University of Utretch, 1995

5) F. Huster et al., "ECV Doping Profile Measurements of Aluminum Alloyed Back Surface Fields", 20th European Photovoltaic Solar Energy Conference, Barcelona (2005)

6) F. Huster, "Aluminum-Back Surface Field: Bow Investigation and Elimination", 20th European Photovoltaic Solar Energy Conference, Barcelona (2005)

7) K. Nakamura et al., "Interaction of Al Layers with polycrystalline Si", J. App. Phy. Vol.46, No.11 Nov.1975, 4678-4684

8) M. Trunov et al., "Effect of Polymorphic Phase Transformations in Al2O3 Film on Oxidation Kinetics of Aluminum Powders", Comb. And Flame 140 (2005) 310-318

Fundamental Investigations and Proposed Solutions to Make the Alloyed Al BSF Ready for the Demands of Future Cell Production

Frank Huster

University of Konstanz, Department of Physics, P.O.Box X916, D-78457 Konstanz, Germany
Author for correspondence: Frank.Huster@uni-konstanz.de
Tel.: +49-7531884469, Fax: +49-7531883895

The screen-printed alloyed aluminum back surface field (BSF) is still the standard rear contact and at the same time rear passivation for most of the industrial silicon solar cells, like it was from the beginning of mass production of terrestrial solar cells in the 1970s. The common Al BSF technology within the so-called PECVD-SiN firing through process enables good industrial efficiencies both for multi- and monocrystalline silicon. Alternatives like dielectric passivation are still not competitive in industrial mass production, at least for mc silicon. Therefore it is important to further pursue efforts to optimize the Al BSF and reduce or eliminate the well-known drawbacks. Until the time when a cost-effective dielectric passivation will be available to successfully enter the production lines, we have to make the industrial Al BSF process ready for future larger and thinner wafers with high bulk-lifetimes. The drawbacks that have to be overcome are mainly:

1. Wafer bow caused by the strong contraction of the Al/Si-eutectic rear contact on cooling-down

2. Non-optimal rear surface reflection

3. Generally only moderate surface passivation properties, with S in the range of 500-2000 cm/s (1 .cm) (while calculations predict 200 cm/s or less for optimized doping profiles)

Detailed investigations on these subjects (or, more precisely, on the causes of these drawbacks) are rare in literature so far. But the full potential of the Al BSF can only be exploited if a good understanding of the alloying and doping process and the mechanics is available. The main objective of this work is to provide new insights and from this to give ideas for solving the drawbacks. These investigations comprise, in keywords:

1. Alloying process: Structure during and after firing, inhomogeneities, Al utilization, interface composition

2. Doping profile: high accuracy measurements using advanced ECV profiling and evaluation, role of boron in glass frit, dependence on crystal orientation and firing temperatures, carrier freeze-out due to high concentration effects

3. Internal reflectivity: interpretation of reflectance measurements using a ray-tracing program with different models to include surface roughness and free carrier absorption

4. Wafer bow: investigation of the bow mechanics, leading to a proposal of a process sequence to totally eliminate the bow of finished cells without detrimental effects on the electrical performance. Details will be disclosed later.

Some of the aforementioned issues are covered by three contributions to be presented at the European Photovoltaic Conference in Barcelona, June 2005. The focus and the selected details to be presented within this talk at the workshop can be adjusted according to the workshop program or the organizer´s suggestions if desired.

LEAD-FREE SOLDER ISSUES IN MICROELECTRONICS

J.W. Morris Jr.
Dept. of Materials Science and Engineering, Univ. of California, Berkeley

While lead-free solders have been available and used in microelectronic packaging for decades, high-lead solders have been preferred, both for their generally suitable properties and because the industry is familiar with them and comfortable using them. However, high-lead solders must now be removed from most microelectronic devices for legislative reasons that spring from environmental concerns. The immediate issue concerns the European Union, which is poised to require Pb-free solders as soon as mid-2006. Since similar regulations are likely elsewhere in the world, and since it is often impractical to use different solder materials for different commercial markets, a very significant part of the whole microelectronics industry will soon change to Pb-free solders.

This change in material is technologically threatening since there is no Pb-free solder that offers a simple one-for-one replacement for the high-Pb solders now in use. For example, the most widely used microelectronic solder (the "great white rat" of the industry) is the Sn-Pb eutectic (63Sn-37Pb). This solder has four advantages that are difficult to reproduce. First, because of its eutectic composition it has a low melting point which makes it suitable for the assembly of heat-sensitive electronics. Second, the high Sn content facilitates bonding to Cu or Ni substrates through the formation of Sn-rich intermetallics. Third, it is readily available and relatively inexpensive. Fourth, it has been used for many decades, with the consequence that almost all of the "bugs" have been identified and exorcised. No known Pb-free solder offers all of these advantages.

Two low-melting Pb-free solders that have been used with some frequency are the Bi-Sn and In-Sn eutectics. Both have a number of desirable properties and will find important applications in the future. Unfortunately, neither is a promising universal substitute for Pb-Sn. Bi has chemical incompatibilities that rule it out of many devices, and In is relatively rare and expensive. The Sn-Zn system also provides low-melting solders that are regarded as promising by some users, but these are in the early stages of development and must overcome a tendency to corrode in service.

The solders that are most widely cited as the short-term "standard" replacements for Pb-Sn are Sn-rich solders, based on eutectics from the Sn-Ag (Sn-3.7Ag), Sn-Cu (Sn-0.9Cu) or Sn-Ag-Cu systems (Sn-3.7Ag-0.8Cu)). All of these are predominantly Sn in composition, have microstructures whose volume is dominated by an essentially pure Sn constituent, and have melting points well above that pf eutectic Pb-Sn.. While these solders have given generally satisfactory results in preliminary, short-term tests on microelectronic devices, there are a number of known technological issues which raise concerns about their use.

Among the concerns that are being actively discussed and debated in the relevant metallurgical conferences are the following:

• High melting point

The Sn-rich eutectic solders have melting points that are 20-40ºC above those of eutectic Sn-Pb. Since the soldering and solder reflow processes must be done at temperatures some 20ºC above the melting point, the use of Sn-rich solders will require a re-design of many manufacturing processes and possible materials changes to ensure that the devices are sufficiently robust to survive high-temperature exposure. There is some concern that high-temperature processing may degrade the long-term reliability of sensitive components even if it is nominally successful.

• Sn whiskers

When fine-grained samples of Sn-rich solder are subject to residual stresses and used at moderate temperature, they tend to nucleate long, thin "whiskers" that can grow to considerable length and form catastrophic electrical shorts between adjacent contacts. Whisker formation is suppressed by Pb, but, apparently, not by Cu or Ag. The associated technological problem is serious. Whiskers nucleate after an incubation time that is difficult to predict, and grow at a rate that is maximum at temperatures that are not far above ambient, and near or within the service range. This behavior makes it difficult to design accelerated teats for sensitivity to whisker formation, and no accepted test has yet been developed. Despite on-going research, it is not entirely clear why whiskers form or how they can be suppressed or controlled in Sn-rich solders. The threat of delayed reliability problems with Sn-rich solders is real.

• Uncertain mechanical properties

The dominant constituent of Sn-rich solder is almost pure Sn, a metal with a tetragonal crystal structure and anisotropic mechanical properties that can be complex, particularly during high-temperature deformation. For example, the stress exponents that govern the power law creep of Sn over the temperature range of interest to microelectronic solder are anomalously high and sensitive to temperature, and the measured activation energy that governs creep varies widely. This has the dual consequence that it is difficult to define reliable constitutive equations for mechanical design, and is also difficult to design probative accelerated tests to verify reliability in service.

• Slow stress relaxation

Largely because of their high stress exponents, the rate of stress relaxation in Sn-rich solders is very slow. This has two undesirable consequences. First, internal stresses are believed to provide the driving force for Sn whisker formation and the inability to relax these stresses efficiently may be an important source of susceptibility to whisker formation (stress relaxation is much more rapid in Sn-Pb solders). Second, stress relaxation is accomplished by creep, and, therefore, stress relaxation during service alters

the geometry of the solder joint. This is a particular problem in optoelectronics; geometrical changes in the solder joint may disturb the optical alignment of the device and cause deterioration or failure.

• Sensitivity to chemical contamination from the substrate

Solder joints ordinarily join contacts of Cu or Ni (usually Au-coated), and, sometimes, bond asymmetric contacts that are Cu on one side and Ni|Au on the other. During wetting and reflow, Cu, Ni and Au are dissolved from the substrate into the joint and Sn-rich intermetallics form on the contact surface and penetrate into the joint. Both the mechanical properties of Sn-rich solders and the thickness and morphology of the interfacial intermetallics are sensitive to the nature of the substrate and the degree of solute dissolution from it. The influence of the substrate (or substrate combinations) are only now coming to be understood.

For most microelectronic devices the transition to Pb-free solder contacts is legally inevitable and will happen soon. However, many questions and problems remain. Some serious materials engineering will be needed to smooth this transition the industry must make.

Spectrum Imaging: Fulfilling a Vision in Cathodoluminescence Instrumentation

M.J. Romero, M.M. Al-Jassim, and P. Sheldon

National Renewable Energy Laboratory, 1617 Cole Boulevard, Golden, CO 80401-3393

Email: manuel_romero@nrel.gov, phone: 303-384-6653

In multicrystalline (mc) Si, epi-Si and silicon thin films, carrier lifetimes are very sensitive to the presence of impurities and of lattice disruption represented by extended defects such as dislocations and grain boundaries. Consequently, understanding the carrier recombination processes is of importance from both a fundamental perspective and for further improving cell performance. Scanning electron microscopy and other methods based on scanning probe microscopy provide the resolution needed to investigate single defects. In this contribution, we review the application of cathodoluminescence (CL) to silicon photovoltaics and the development of spectrum imaging. CL is complementary to electron-beam-induced current (EBIC) and can be performed simultaneously. Recent progress in instrumentation will be presented, and future directions in research will be discussed.

The National Renewable Energy Laboratory (NREL) is highly committed to developing instrumentation that meets the increasing demands imposed by our exploratory research in photovoltaics (PV) and other applications of interest to the mission of the Laboratory. Excellent-resolution cathodoluminescence (CL)—which is the photon emission stimulated by an electron beam—is becoming an indispensable tool in characterizing semiconductors. CL has enabled imaging of the electronic and optical properties of semiconducting structures with an ultimate resolution better than 50 nm. *Spectroscopy* and *imaging* modes are accessible in most instruments. In spectroscopy, a spectrum is obtained over a selected area being observed in the electron microscope. In contrast, in imaging, a map of the photon intensity (energy resolved with a spectrograph) is acquired. Because spectroscopy and imaging cannot be operated simultaneously, information is inevitably lost.

We have combined spectroscopy and imaging in one single mode: *spectrum imaging*. In simple terms, spectrum imaging acquires a spectrum for each pixel on the image. This is achieved by synchronizing the scanning of the electron beam with the spectrum acquisition using a multichannel photodetector. In our system, we can select a silicon charge-coupled device (CCD) or an InGaAs photodetector array (PDA), depending on the wavelength of interest. These cryo-cooled detectors offer high sensitivity and superior performance.

Our novel approach to synchronization, based on *linescan control*, allows acquisition times of 10–20 ms by pixel. Therefore, for a 125×125 pixel image, the time to acquire the entire spectrum series—consisting of 15,625 spectra, equivalent to more than ten million data inputs—is about five minutes. This high-speed mode is routinely used in our laboratory. We can increase the pixel density to 250×250 or 500×500, maintaining the acquisition time of 10–20 ms, to further resolve some details on the image. When a very low excitation is used for high resolution, or when the photon emission is very low, we can increase the acquisition time to 500 ms (100×100 pixels) or 2 s (75×75 pixels); however, the measurements will take hours, instead of minutes. We are not restricted to these settings, and additional modes can be implemented to meet the demands of the experiment.
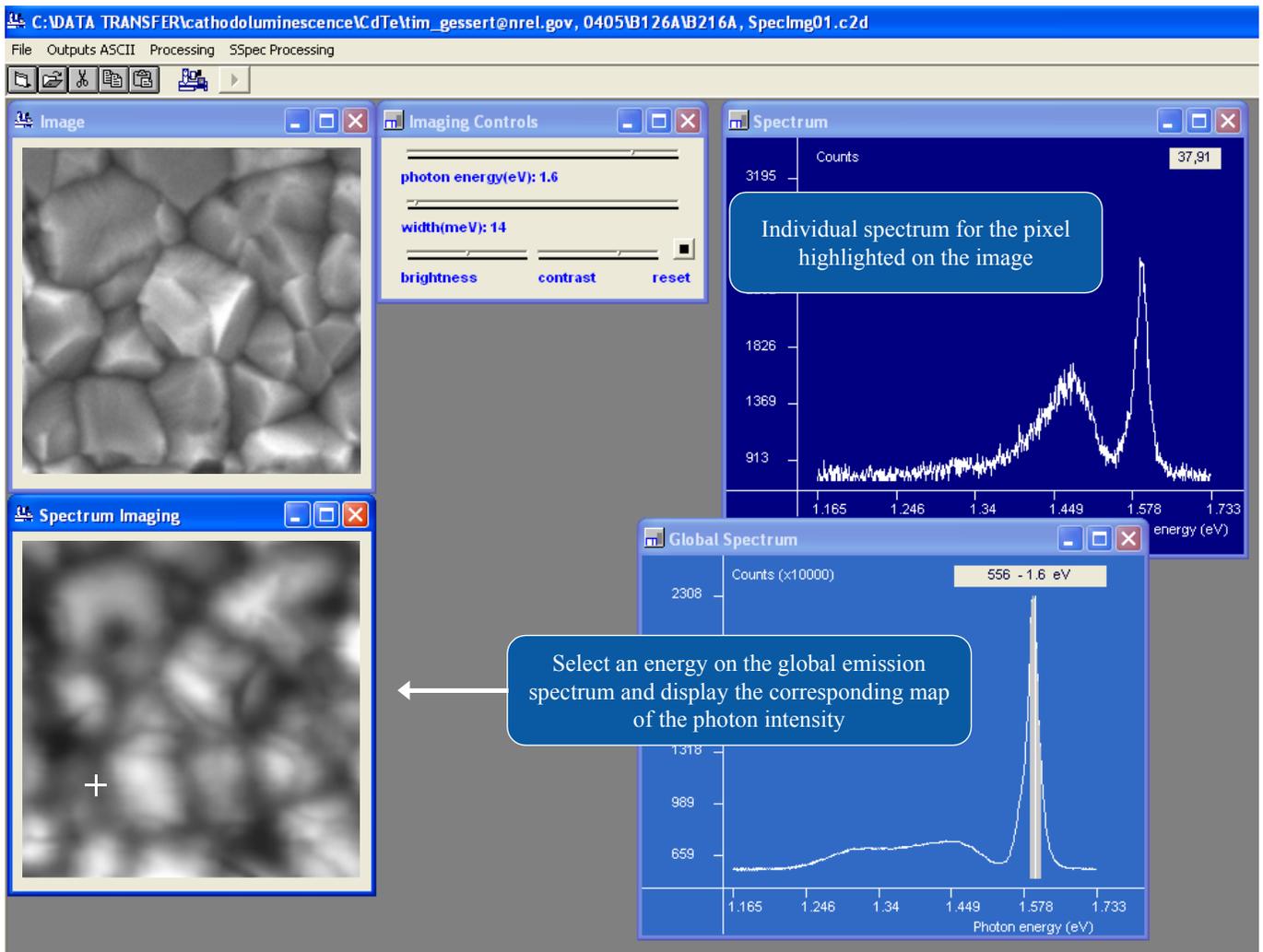
Figure 1. The C2DIMAG software developed at NREL (color).

When the acquisition is completed, a file is generated (the extension of this file is *.c2d). The software developed for spectrum imaging (C2DIMAG), which is shown in Fig. 1, processes the spectrum series to reconstruct images of the photon emission (energy resolved) or to extract the spectrum from a selected area. C2DIMAG provides more advanced processing capabilities such as

- *Mapping of the photon energy and full-width-at-half maximum (FWHM) of selected transitions*
- *ASCII output*
- *Quantitative–imaging mode*
- *Pixel–to–pixel correlation*
- *Spectrum linescan*
- *Spectrum fitting.*

Since its early development, spectrum imaging has been applied in our laboratory to

- *Thin-film solar cells: CdTe and Cu(In,Ga)Se₂*
- *Self-organized quantum dots for solar cells*
- *Semiconductor nanostructures*
- *III-Vs for multijunction solar cells.*

The supremacy of crystalline silicon in photovoltaics should give this technology higher priority in our research. However, silicon represents the *final frontier* for spectrum imaging because of the very low efficiency of radiative transitions in indirect-gap semiconductors. Implementation of a near/mid-infrared InGaAs camera of improved performance and a low-vibration closed-circuit helium cryostat for specimen refrigeration has allowed the application of spectrum imaging to mc- and epi-silicon solar cells for the first time.

For illustrating the process, we have investigated mc-Si wafers prepared by edge-defined film-fed growth (EFG) (provided by Sergei Ostapenko, University of South Florida). This team has identified degraded regions by a combination of scanning photoluminescence, EBIC, and lifetime mapping.[1,2]

Figure 2 shows an emission spectrum obtained at 19.8 K corresponding to one of these defective regions. At helium temperature, the band-to-band recombination is substituted by the TO phonon replica of the boron-bound exciton at 1.093 eV (B+TO). We observe a strong defect-band emission near 0.8 eV (DB), as confirmed previously by scanning photoluminescence. Transitions associated with dislocations, which are commonly referred to as *D*-lines, are shown on the spectrum: *D*1 (0.812 eV), *D*2 (0.875 eV), *D*3 (0.934 eV), and *D*4 (1.000 eV).[3]
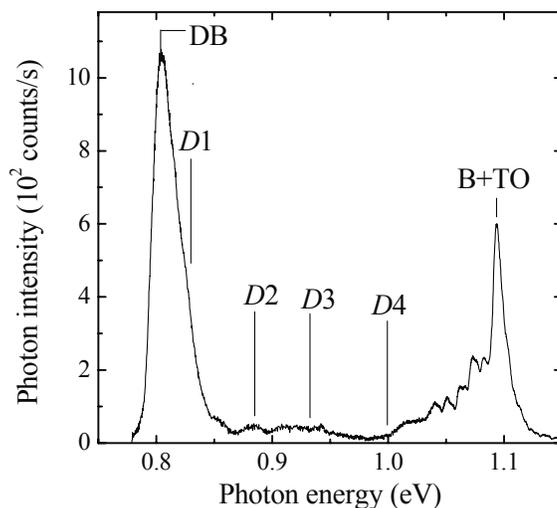
**Figure 2.** Emission spectrum from EFG mc-Si. $E_b = 20$ keV, $I_b = 2$ nA, T = 19.8 K.

Once a region with strong DB recombination is located on the wafer—aided by the live spectrum on display—we trigger the spectrum imaging acquisition. Figure 3 shows the corresponding maps of the photon intensity for the different transitions identified in the emission spectrum.

We have confirmed that these transitions are associated with defect lines (DL). The B+TO emission is largely reduced at the defect line (the photon intensity is reduced 60%), suggesting that non-radiative recombination is bound to the DL. The distribution of the defect band at 0.8 eV can be attributed to the *impurity atmosphere* surrounding the DL. *D*-lines are located at the center of the defect line. Thus, spectrum imaging reveals a high degree of complexity of these defect lines.

B+TO   DB   *D*2   *D*3

50 μm
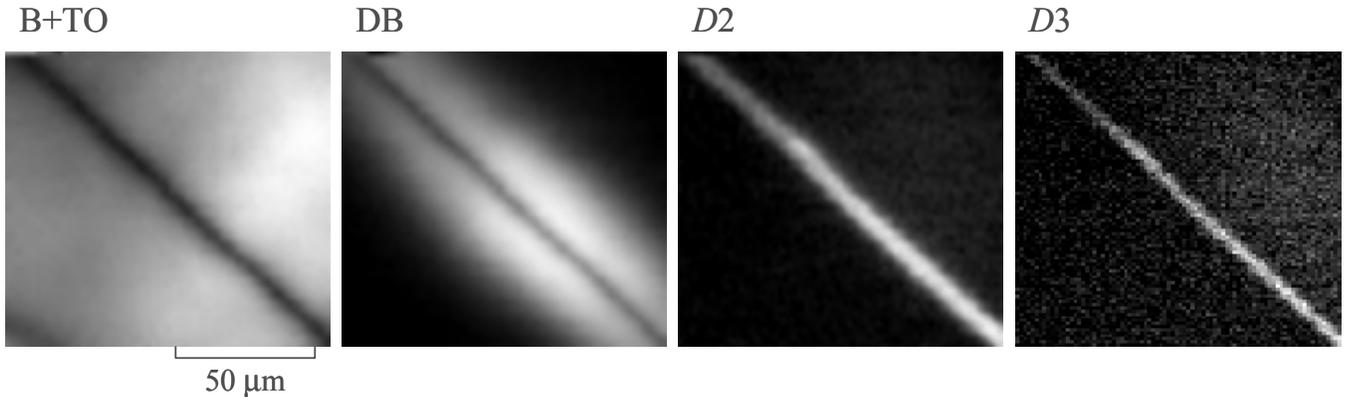
Figure 3. Mapping of the photon intensity for different transitions near a defect line in EFG mc-Si.
E_b = 20 keV, I_b = 2 nA, T = 19.8 K.

Zooming into the DL, as shown in Fig. 4, we can further resolve the *D*-lines. Indeed, *D*2 resembles DB at a finer scale. No structure is revealed for *D*3, though, which lies at the very center of the defect line. A very valuable feature of spectrum imaging is the post-processing capabilities. As seen on the spectrum in Fig.1, *D*1 is obscured by the much stronger defect-band emission. However, with spectrum fitting, we can extract DB from *D*1. The output is shown in Fig. 4 (*D*1), where we observe that this transition is brighter at one side of the DL when compared to the other.

DB   *D*2   *D*3   *D*1

5 μm
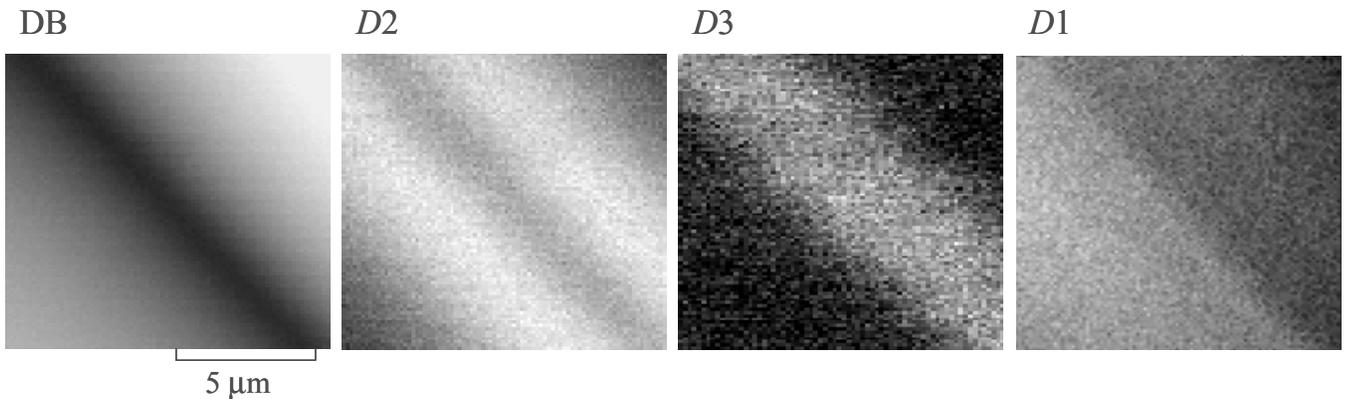
Figure 4. Mapping of the photon intensity for different transitions zooming into the defect line shown in Fig. 3.
E_b = 20 keV, I_b = 2 nA, T = 19.8 K.

Figure 5 illustrates additional features of spectrum imaging. Pixel-to-pixel correlation is very useful to compare linescans crossing the DL for different transitions. Indeed, whereas *D*3 is aligned with DB, *D*1 and *D*2 are displaced with respect to the center of the defect line (see Fig. 5 [left]). To the right, we show the map of the photon energy, considering that the spectral range of the PDA corresponds to the visible spectrum. This provides very intuitive information about the spatial distribution of all these transitions in one single image.
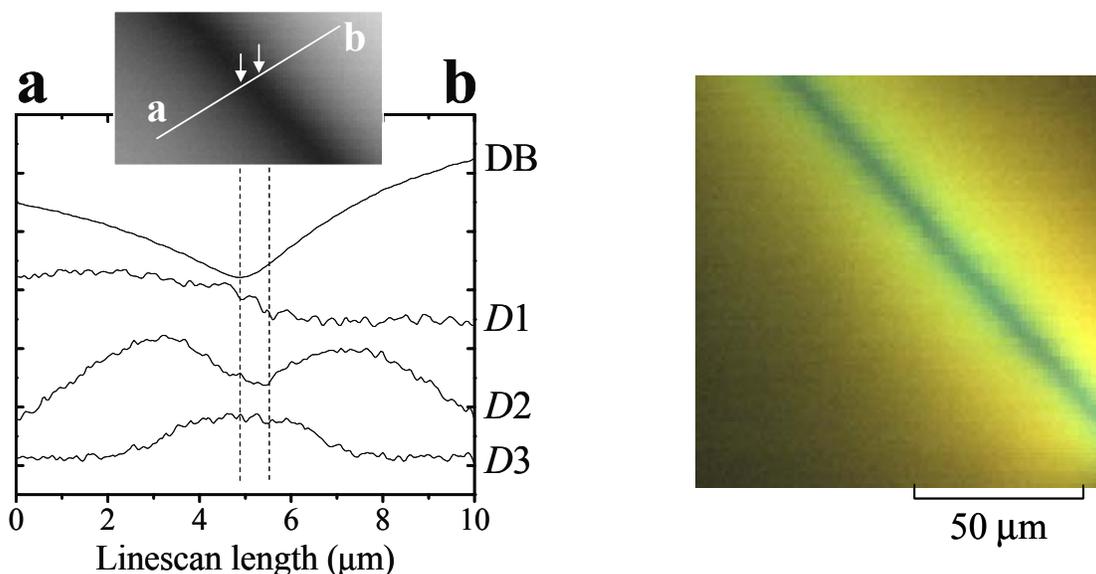
Figure 5. (Left) Linescans crossing the DL for different transitions. (Right) Photon energy mapping (color).

We hope that this contribution will illustrate the potential of spectrum imaging to the silicon PV community. Spectrum imaging is available to researchers involved in collaborative projects with NREL. Additional applications to silicon solar cells will be presented at the Workshop, specially regarding grain boundaries and microprecipitates.

References

1. Y. Koshka, S. Ostapenko, I. Tarasov, S. McHugo, and J.P. Kalejs, *Appl. Phys. Lett.* **74**, 1555 (1999).
2. I. Tarasov, S. Ostapenko, K. Nakayashiki, and A. Rohatgi, *Appl. Phys. Lett.* **85**, 4346 (2004).
3. T. Sekiguchi, K. Sumino, Z.J. Radzimski, and G.A. Rozgonyi, *Mat. Sci. Eng.* B**42**, 141 (1996) and references herein.

Non-radiative carrier recombination at metastable light-induced boron-oxygen complexes in silicon

Mao-Hua Du, Howard M. Branz, Richard S. Crandall, and S. B. Zhang
National Renewable Energy Laboratory, Golden, Colorado 80401

I. Introduction: Solar cells made on boron-doped Czochralski silicon (Cz-Si) wafers lose up to 10% of their initial energy-conversion efficiency due to illumination-induced formation of metastable recombination centers.[1] Since the degradation is found in neither Ga-doped Cz-Si nor oxygen-lean float-zone Si samples (Cz-Si typically has high oxygen concentration, $[O]\sim10^{17}$ to 10^{18} cm^{-3}), the origin of the degradation is attributed to a B-O complex.[2] [3] [4] The linear dependence of the defect complex density upon both [B] and $[O]^2$ suggests that the complex is BO_2.[4] [5]

Schmidt and Bothe proposed that the interstitial oxygen dimers diffuse to B to form the metastable recombination centers [4] [5] and Adey et al. showed that the bistability of the oxygen dimer could lead to light-induced dimer diffusion and trapping at substitutional B.[6] Despite this theoretical progress, at least three fundamental questions remain: 1) how do electrons and holes (e^- and h^+) recombine through the BO_2 complex; 2) why is the BO_2 complex a more effective recombination center than uncomplexed O_2 dimer; and 3) what explains the observed light-induced BO_2 formation kinetics?

Adey et al. suggested that the BO_2-induced defect gap level causes the carrier recombination. But this level (at 0.1 to 0.3 eV below the conduction band edge) is too shallow to act as an effective recombination center. Further, our first-principles calculations show a remarkable similarity between the defect levels introduced by BO_2 and O_2, as shown in Fig. 1.[7] Clearly, it is not a difference in electronic gap levels that explains why BO_2 functions as a strong recombination center but uncomplexed O_2 does not. In this paper, we show that both BO_2 and O_2 are recombination centers in silicon --- in each, recombination is enhanced by carrier self-trapping involving large-scale defect structural relaxation. We propose that the presence of uncomplexed O_2 in silicon does not cause a significant reduction of the carrier lifetime because slow h^+-trapping over a Coulomb barrier limits the carrier recombination rate. However, the formation of the BO_2 changes the net charge at the defect complex and dramatically increases the h^+-capture and recombination rates. Our work thus provides a simple explanation of the enhanced recombination upon the binding of O_2 with B, while improving the understanding of light-induced O_2 diffusion.

II. Method: Our calculations are based on density functional theory (DFT) within the local density approximation (LDA), as implemented in the VASP code.[8] The electron-ion interactions are described by ultra-soft pseudopotentials.[9] The valence wavefunctions are expanded in a plane-wave basis with a cutoff energy of 300 eV. Calculations were performed using both 64- and 216-atom supercells.
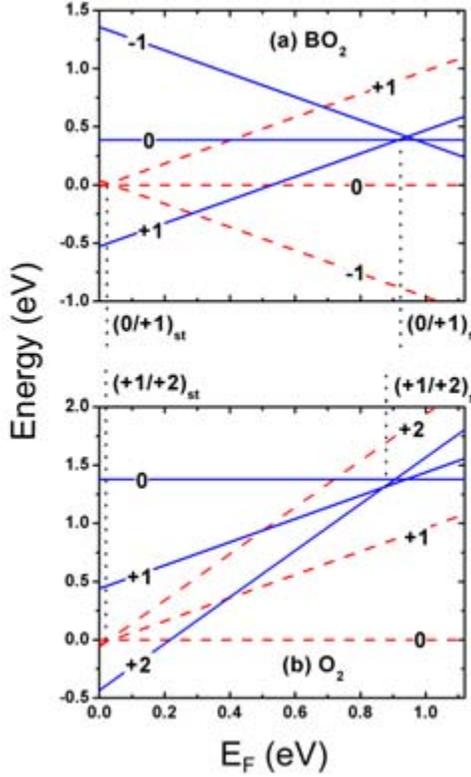
FIG. 1. Energies of (a) BO_2 and (b) uncomplexed O_2 in the square (solid lines) and staggered (dashed lines) configurations as functions of the Fermi level. The B binding sites in both square and staggered BO_2 complex is shown in Fig. 2(c) and (d). We set the energies for the charge-neutral staggered configurations to zero. Dotted vertical lines indicate the primary recombination-active electronic transition energies and emphasize the similarities between the two defects.

III. Results: Figures 2 (a) and (b) show the structures of square (sq) and staggered (st) O_2 complex, with the most stable B binding site indicated. Fig. 1(b) shows that the ground-state structure of the O_2 is square for +2 charge state ($O_2^{sq,++}$) and staggered for the neutral charge state ($O_2^{st,0}$), as in Ref 6. We calculated binding energies of B^- with $O_2^{sq,++}$ and $O_2^{st,0}$ to be 0.55 and 0.41 eV, respectively.

(1) $BO_2^{sq,+} + e^- \rightarrow BO_2^{sq,0}$

(2) $BO_2^{sq,0} \xrightarrow{0.17 eV} BO_2^{st,0}$

(3) $BO_2^{st,0} + h^+ \rightarrow BO_2^{st,+}$

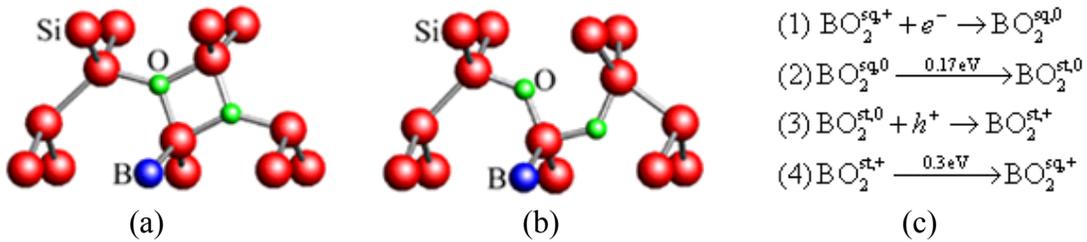(4) $BO_2^{st,+} \xrightarrow{0.3 eV} BO_2^{sq,+}$

(a)   (b)   (c)

FIG. 2. (a) and (b) are the most stable sq and st structures for BO_2 complex, respectively. (c) shows the carrier recombination process at BO_2, which is described in four steps, with energy barriers associated with the $sq \rightarrow st$ and $st \rightarrow sq$ reconfigurations in Step (2) and (4) shown above the arrows.

In p-type Si, $BO_2^{sq,+}$ is the ground state of the BO_2 complex, with B^- bound to $O_2^{sq,++}$. In the dark, $BO_2^{sq,+}$ is separated from $BO_2^{st,+}$ by a high $sq \rightarrow st$ barrier of 0.82 eV. Under light, the recombination occurs by carrier self-trapping, described by four steps in Fig. 2(c). Step (1) is the e^--trapping to a level at $E_c - 0.2$ eV. The reconfiguration Step (2)

is an e^- self-trapping process (over the 0.17-eV barrier), associated with the shallow-to-deep transition of the filled electron level. Step (3) is a fast h^+ trapping, which serves to reduce the $sq \rightarrow st$ barrier from 0.57 eV (for $BO_2^{st,0} \rightarrow BO_2^{sq,0}$) to 0.3 eV (for $BO_2^{st,+} \rightarrow BO_2^{sq,+}$) for the Step (4) reconfiguration. The Step (4) reconfiguration is a hole self-trapping process, associated with a shallow-to-deep transition of the hole-occupied level. The e^-- h^+-pair (bandgap) energy is released to phonons through the $sq \leftrightarrow st$ reconfigurations. It is important that the recombination process is not simply mediated by a fixed energy level. Instead, the defect level sweeps up and down within the bandgap. This self-trapping enhanced recombination process requires a revision of the standard Shockley-Read-Hall analysis[10][11] of carrier lifetimes,[3][12] which is beyond the scope of this paper. Although the BO_2 continually flips back and forth between the sq and st configurations induced by carrier trapping, most O_2 do not easily diffuse away from the B, because of the 0.5-eV binding energy.

The $sq \leftrightarrow st$ reconfigurations of an O_2 have nearly identical barriers as the BO_2 in Fig. 2(c) both in its isolated form and in the complex of Figs. 2(a) and 2(b). In fact, as long as B and O_2 share a common Si neighbor, the B has little effect on the $sq \leftrightarrow st$ barriers. One may therefore naively assume that the same e^--h^+ recombination mechanism should also apply to the uncomplexed O_2. However, without the associated B^-, h^+-trapping to the positively charged O_2^+ must now overcome a repulsive capture barrier. It has been demonstrated that Coulomb repulsion normally decreases the capture probability by orders of magnitude.[13] This results in slow recombination which is not expected to affect the minority carrier lifetime. Nevertheless, the repeated $sq \leftrightarrow st$ reconfigurations associated with the carrier recombination drives the O_2 diffusion.

TABLE I. Rate-limiting process in recombination-driven diffusion of O_2, O_2 hop rate, and the resulting defect generation rate (R_{gen}) at high and low illumination intensity (I). Experimental references are shown in the last column, and agree with our theoretical predictions. τ_{cn} and τ_{cp} are e^- and h^+ capture time constants, and c_n and c_p are e^- and h^+ capture rate coefficients, respectively.

I	Rate-limiting process	$1/\tau$	$R_{gen} \propto [B][O_{2i}]/\tau$	Exp.
High	h^+-trapping	$1/\tau \approx 1/\tau_{cp}$ $= c_p[B]$	$R_{gen} \propto [B]^2$	Ref. 14
			Independent of I	Ref. 4
Low	e^--trapping	$1/\tau \approx 1/\tau_{cn}$ $= c_n[n]$	$R_{gen} \propto [B]$	N/A
			$R_{gen} \propto I$	Ref. 4

The defect generation process is essentially the O_2 diffusion process. Its rate depends on [B], [O_2], and the O_2 hop rate. Because the hop rate is proportional to the e^--h^+ recombination rate, the defect generation rate is $R_{gen} \propto [B][O_{2i}]/\tau$, where τ is the time for O_2 to complete one recombination cycle. By examining which carrier is rate-limiting for recombination under different experimental conditions, the dependences of R_{gen} on [B] and illumination intensity can be predicted. Table I shows the asymptotic forms

predicted at both high and low illumination conditions. All the predictions agree with the experiments, as indicated by the references in Table I, except that $R_{gen} \propto$ [B] at low illumination intensity is not yet tested. The agreement between our theory of the defect generation rate and the experiments supports our findings that the carrier recombination drives O_2 diffusion, and that the slow h^+-trapping limits the recombination-induced O_2 diffusion at solar illumination intensity. It is interesting to note that the rate limiting process is the majority carrier capture rather than the usually expected minority carrier capture. Only in low-illumination intensity regime, which extends to about 1 mW/cm^2, does the minority e^--capture become so slow that it limits the recombination rate.

IV. Summary: We have proposed a self-trapping-enhanced e^--h^+ recombination process for BO_{2i} in Cz-Si, and explain that the change of the defect charge state dramatically increases the recombination rate at oxygen dimers when they form the metastable complex with B. Though the uncomplexed O_2 must act as a weak recombination center in order to diffuse, the Coulomb barrier to h^+-trapping at O_2^+ means the minority carrier lifetime is affected little. In addition, our model predicts the dependence of defect generation rate on [B] and the illumination intensity, in agreement with the experimental observations.

[1] H. Fischer and W. Pschunder, in *Proceedings of the 10th IEEE Photovoltaic Specialists Conference* (IEEE, New York, 1973), p. 405.

[2] J. Schmidt, A. G. Aberle, and R. Hezel, in *Proceedings of the 26th IEEE Photovoltaic Specialists Conference* (IEEE, New York, 1997), p.13.

[3] J. Schmidt and A. Cuevas, J. Appl. Phys. **86**, 3175 (1999).

[4] J. Schmidt and K. Bothe, Phys. Rev. B **69**, 024107 (2004).

[5] K. Bothe, R. Hezel, and J. Schmidt, Solid State Phenom. **95-96**, 223 (2004).

[6] J. Adey, R. Jones, D. W. Palmer, P. R. Briddon, and S. Oberg, Phys. Rev. Lett. **93**, 055504 (2004).

[7] Formation energies calculated according to S. B. Zhang, J. Phys.: Condens. Matter **14**, R881 (2002)

[8] G. Kresse and J. Furthmuller, Phys. Rev. B **54**, 11169 (1996).

[9] D. Vanderbilt, Phys. Rev. B **41**, R7892 (1990).

[10] W. Shockley and W. T. J. Read, Phys. Rev. **87**, 835 (1952).

[11] R. N. Hall, Phys. Rev. **87**, 387 (1952).

[12] Rein and S. W. Glunz, Appl. Phys. Lett. **82**, 1054 (2003).

[13] *Electronic Materials Science: For Integrated Circuits in Si and GaAs*, J. W. Mayer and S. S. Lau, Macmillan Publishing, New York, 1990.

[14] S. Rein, T. Rehrl, W. Warta, S. W. Glunz, and G. Willeke, in *Proceedings of the 17th European Photovoltaic Solar Energy Conference* (WIP-ETA, Munich, 2001), p.1555.

Synchrotron-based spectrally-resolved X-ray beam induced current: a technique to quantify the effect of metal-rich precipitates on minority carrier diffusion length in multicrystalline silicon

T. Buonassisi[1], A.A. Istratov[1], M.D. Pickett[1], M.A. Marcus[2], G. Hahn[3], S. Riepe[4],
J. Isenberg[4], W. Warta[4], G. Willeke[4], T. F. Ciszek[5], and E.R. Weber[1]

(1) Department of Materials Science and Engineering, University of California, Berkeley, and Materials Science Division, Lawrence Berkeley National Laboratory, Berkeley, CA 94720, USA

(2) Advanced Light Source, Lawrence Berkeley National Laboratory, Berkeley, CA 94720, USA

(3) University of Konstanz, Department of Physics, P.O. Box X916, 78457 Konstanz, Germany

(4) Fraunhofer Institute for Solar Energy Systems, Heidenhofstrasse 2, D-79110 Freiburg, Germany

(5) National Renewable Energy Laboratory, Golden, CO; Current address: Siliconsultant, P. O. Box 1453, Evergreen, CO 80437 USA

McHugo, Thompson, et al. [1, 2] were the first to apply a suite of synchrotron-based analytical techniques to study efficiency-limiting, impurity-related defects in solar cell grade multicrystalline silicon (mc-Si). X-ray fluorescence microscopy (μ-XRF), which can be used to locate and characterize the elemental composition of metal-rich nanoprecipitates within mc-Si solar cells, and X-ray absorption microspectroscopy (μ-XAS) which allows one to identify the chemical states of these particles, were subsequently developed, with higher flux and sub-micron spot size, to detect a single iron silicide nanoprecipitate of radius 16±3 nm and to identify its chemical state [3]. However, with only μ-XRF and μ-XAS, no direct correlation between the presence of metals and device performance can be made.

Recently, Hieslmair *et al*. [4] and Vyvenko *et al*. [5] demonstrated the potential of X-ray Beam Induced Current (XBIC) technique to map the recombination activity in-situ at the μ-XRF/XAS beamline. The physical principle of XBIC is similar to light/laser beam induced current (LBIC), in that incident photons generate minority carriers which are collected by a Schottky diode or pn junction, but X-rays are used instead of visible light. XBIC was successfully combined with μ-XRF/μ-XAS to demonstrate the recombination activity of iron and copper [3, 6, 7] related nanodefects in mc-Si. However, XBIC can give only a relative measure of recombination activity of metal clusters, and therefore it is difficult to quantitatively measure the effect of metals on the minority carrier diffusion length using this technique.

This task can be achieved via the technique we propose to call spectrally-resolved X-ray beam induced current (SR-XBIC). The theory behind SR-XBIC is very similar to the spectrally-resolved laser beam induced current (SR-LBIC) technique [8]: a current collection efficiency (CCE, proportional to the fraction of photogenerated carriers collected by the pn-junction or Schottky diode) is measured using X-rays with different penetration depths (energies). X-ray photon flux is determined using a calibrated ion chamber positioned before the sample. Then, a graph is produced comparing CCE^{-1} to α^{-1}, where α is the optical absorption coefficient, and α^{-1} is the attenuation (or absorption) length; for α^{-1} much greater than the depletion width but small enough for back surface recombination not to significantly influence CCE, an effective diffusion length L_{eff} can be extracted, as shown in Fig. 1.

The only major differences between SR-XBIC and SR-LBIC arise from the distinct natures of the excitation sources (hard X-rays vs. visible laser light). A fit to available X-ray absorption data tables[12] indicates that when the incoming X-ray energy E is between 3 and 13 keV, specifically for silicon,

$$\alpha^{-1}(\mu m) \approx 0.1729 \cdot E(keV)^{2.8881}. \qquad (1)$$

Within this energy range, α^{-1} is between 4 and 290 μm, which includes typical values for minority carrier diffusion lengths in mc-Si. Fortuitously, this energy range is available at hard X-ray microprobe beamlines, which are usually designed to scan over the K-edges of the 3d transition elements. Additionally, each x-ray photon can generate multiple electron-hole pairs.
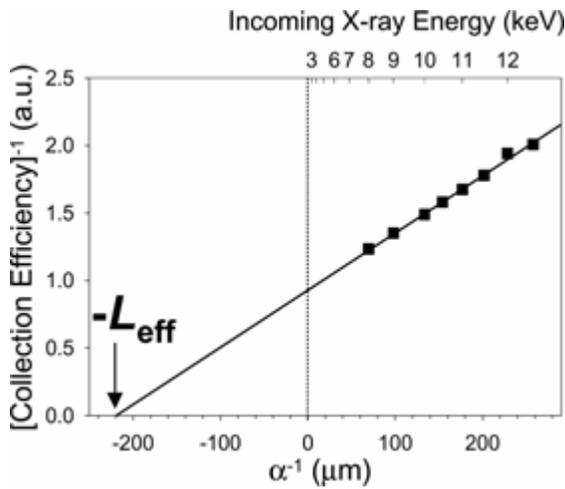

Fig. 1: SR-XBIC determines a diffusion length of 219.9±7 μm at a single point on a FZ-Si sample, which was pre-characterized by the SPV technique and determined to have a diffusion length of 220 m. A monochromator was used to vary the energy of the incoming X-rays for each data point on the graph, thus changing the penetration depth according Eq. 1.

To test the quantitative accuracy of SR-XBIC, comparisons with several other diffusion length measurement techniques were performed. Firstly, a surface photovoltage (SPV, Ref. [9]) calibration standard with 500 μm thickness and 220 μm diffusion length was measured. SR-XBIC consistently revealed diffusion lengths between 215 and 232 μm (e.g. Fig. 1), accurate within experimental error. Since SPV measures the minority carrier diffusion length at low injection levels, this result suggests that SR-XBIC also measures under low injection conditions, i.e. when $\Delta n \ll p_o$. This conclusion is further substantiated by SR-XBIC measurements on samples of n- and p-type silicon with strong injection dependences, generously provided by D. Macdonald at the Australian National University. It must be noted that changes in photon flux and sample doping concentration may alter the condition $\delta n \ll p_o$, and thus, the injection conditions. In particular, the X-ray flux may vary by orders of magnitude, depending on the synchrotron beamline, focusing optics, and aperture settings. All experiments in this paper were performed at Advanced Light Source Beamline 10.3.2 (a bending magnet source).

SR-XBIC was also compared to SR-LBIC, which operates at much higher injection conditions (near 1 Sun), and quantum efficiency measurements averaged over the full wafer area, with variable injection conditions depending on bias lighting, for a solar cell pre-characterized at the Fraunhofer Institute for Solar Energy Systems and the University of Konstanz. Qualitatively, both SR-XBIC and SR-LBIC are very similar, revealing the same recombination-active grain boundaries (Fig. 2). Quantitatively, SR-XBIC and SR-LBIC produce similar peak L_{eff} values (31 and 49 μm, respectively), albeit a shift to lower L_{eff} values is observed for SR-XBIC (Fig. 2). This shift is expected, due to the injection dependence of the minority carrier diffusion length in this particular sample. The average SR-XBIC diffusion length falls within the range of expected

values determined by full-wafer quantum efficiency measurements (dotted lines and arrows in Fig. 2), which reveal average diffusion lengths between 18 and 45 µm for this sample using low (no bias lighting) and medium-high (0.35 Suns bias lighting) injection conditions, respectively.

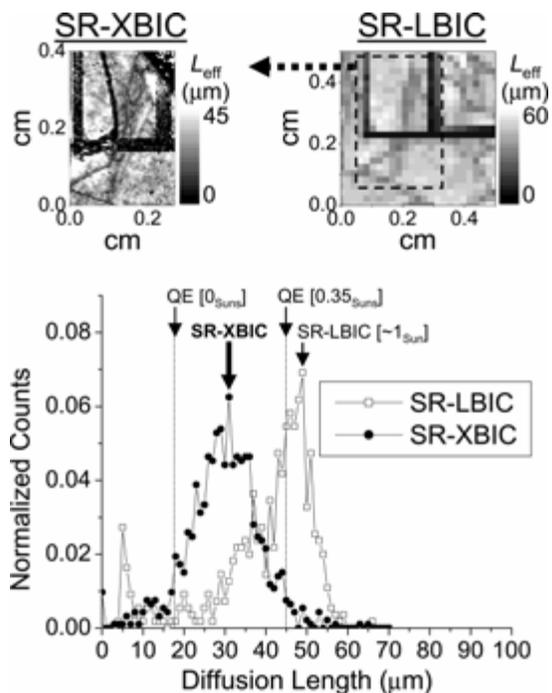When the SR-XBIC technique is combined with the well-established µ-XRF and µ-XAS techniques, one can measure the elemental composition, chemical state, and effect on minority carrier diffusion length of metal-related defects in-situ, with micron- or sub-micron spatial resolution. For example, Fig. 3 shows maps of copper and nickel distributions determined by µ-XRF, and minority carrier diffusion length determined by SR-XBIC, of a metal-contaminated multicrystalline float zone (mc-FZ) sample intentionally contaminated with copper, nickel and iron in order to achieve a very well-defined impurity distribution. µ-XAS analyses determine Cu and Ni to be in the form of Cu_3Si and $NiSi_2$ respectively, in agreement with previous results [7]. Fe did not form precipitates larger than the detection limit of these experiments, and could not be observed in µ-XRF maps.

Fig. 3 demonstrates a clear correlation between local metal concentration and minority carrier diffusion length, and areas with the highest Cu and Ni counts have the lowest diffusion lengths. The recombination strengths of Cu_3Si and $NiSi_2$ appear to be similar, as given by the slopes of the fit by 2D polynomial surface in Fig. 3 (note the different scales of the Cu and Ni axes). By comparing the SR-XBIC value at the points of maximum Cu and Ni (7 µm) versus the points with the least of these metals (25 µm), one deduces that the presence of Cu_3Si and $NiSi_2$ precipitates may locally reduce the minority carrier diffusion length by up to 72% compared to background levels.

Fig. 2: Comparison between spectrally-resolved light/laser beam induced current (SR-LBIC), spectrally-resolved X-ray beam induced current (SR-XBIC), and average diffusion lengths determined from quantum efficiency measurements averaged over the entire wafer with 0 Suns and 0.35 Suns bias illumination. The same features are evident in each map. The slightly lower average minority carrier diffusion length measured in SR-XBIC is believed to be due to the lower minority carrier injection level, as discussed in the text.

When one extrapolates the Cu and Ni concentrations to zero in Fig. 3, one determines a low baseline minority carrier diffusion length of approximately 30 µm. Meanwhile, "clean" mc-FZ samples can obtain local diffusion lengths higher than 100 µm. The likely explanation of this reduction is iron, present in very small clusters or point defects. When comparing "clean" and Fe-contaminated mc-FZ samples, one observes this same effect, while it is not evident in mc-FZ samples contaminated with Cu only. The low solubility and diffusivity of Fe favor the formation of smaller precipitates and point defects, unlike the larger precipitates formed by fast-diffusing and highly soluble Cu and Ni. The small distances separating neighboring Fe defect clusters increases their effect on device performance.

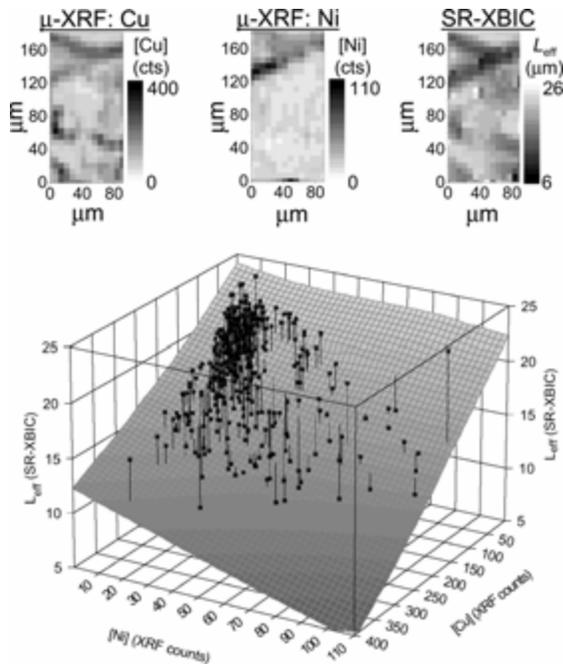Fig. 3: SR-XBIC data (top right) can be obtained in-situ at the μ-XRF beamline, allowing for direct comparisons with metal distributions (top left, middle). The 3D correlation plot demonstrates a strong correlation between increasing metal content and decreasing minority carrier diffusion length.

These results demonstrate that sub-micron-sized metal precipitates, as well as homogeneous distributions of smaller precipitates and point defects, can both significantly reduce the minority carrier diffusion length in mc-Si. In these experiments, the minority carrier diffusion length is observed to decrease when the local concentrations of Cu and Ni found in Cu_3Si and $NiSi_2$ precipitates increase. Furthermore, the effects of these precipitates on minority carrier diffusion length could be decoupled from the background recombination activity. SR-XBIC, in combination with μ-XRF and μ-XAS, is thus demonstrated to be a powerful tool to establish the effects of individual metal species and defect types on the minority carrier diffusion length of mc-Si. In the future, this combination of techniques should make possible the quantitative comparison between different samples, e.g. hydrogen passivated and non-passivated samples.

References

1. S. A. McHugo, *Appl. Phys. Lett.* **71**, 1984 (1997).
2. S. A. McHugo, A. C. Thompson, I. Perichaud, et al., *Appl. Phys. Lett.* **72**, 3482 (1998).
3. T. Buonassisi, A. A. Istratov, M. Heuer, et al., *J. Appl. Phys.* **97**, 74901 (2005).
4. H. Hieslmair, A. A. Istratov, R. Sachdeva, et al., in *10-th workshop on crystalline silicon solar cell materials and processes,* B. L. Sopori, Editor, p. 162, NREL, Golden, CO (2000).
5. O. F. Vyvenko, T. Buonassisi, A. A. Istratov, et al., *J.Appl.Phys.* **91**, 3614 (2002).
6. O. F. Vyvenko, T. Buonassisi, A. A. Istratov, et al., *J. Phys.: Cond. Matter* **14**, 13079 (2002).
7. T. Buonassisi, M. A. Marcus, A. A. Istratov, et al., *J. Appl. Phys.* **97**, 63503 (2005).
8. W. Warta, *Solar Energy Materials & Solar Cells* **72**, 389 (2002).
9. J. Lagowski, P. Edelman, M. Dexter, et al., *Semicond. Sci. Technol.* **7**, A185 (1992).

Metal particle evolution during solar cell processing in multicrystalline silicon

Tonio Buonassisi[a], Matthew D. Pickett[a], Andrei A. Istratov[a], Erik Sauar[b], Timothy Lommasson[c], Roger F. Clark[d], Mohan Narayanan[d], Steven M. Heald[e], and Eicke R. Weber[a]

[a]University of California, Berkeley, CA 94720
[b]Renewable Energy Corporation, Høvik, Norway
[c]ScanCell AS, Narvik, Norway
[d]BP Solar, Frederick, MD 21703
[e]Advanced Photon Source, Argonne National Laboratory, Argonne, IL 60439

Abstract

Synchrotron-based analytical techniques were used to analyze the effects of solar cell processing of metal-rich particles in ingot-cast mc-Si. The response of metal-rich particles is found to depend both on the nature of the processing step (SiN_x deposition, P-diffusion, time–temperature profile) and on the nature of the metal-rich particles (size, chemical state, elemental composition). As a general rule, higher-temperature processing and phosphorus diffusion results in the removal metal silicide nanoprecipitates more efficiently than lower-temperature processing and heat treatments without a gettering layer. Metal silicide nanoprecipitates of high-flux species (e.g. Cu, Ni) are observed to dissolve even during brief low-temperature (e.g. 800°C) gettering steps, and can be re-distributed within the wafer during processing steps without a gettering layer. On the other hand, metal silicide nanoprecipitates containing low-flux species (e.g. Fe) resist dissolution during gettering, although these may also partially or completely dissolve during rigorous, high-temperature gettering. Metal-rich inclusions containing slowly-diffusing species such as Ca, Ti, Zn, and Fe were observed to remain despite commercial solar cell processing.

Materials and Methods:

Ingot-cast mc-Si samples from the most metal-rich (and therefore most problematic for solar cell performance) areas of the ingot (bottom, top, and edges), provided by two commercial vendors, were used in this study. Sets of sister wafers were processed as follows: (1) as-grown, (2) SiN_x-deposited (400-450°C, 20-25 min), (3) phosphorus-diffused (800-850°C, 30-35 min), without a nitride layer, (4) both SiN_x-fired and P-diffused, and (5) fully-processed solar cells (with Al back surface layer).

Synchrotron-based analytical techniques were used to measure the metal distributions and chemical states in samples extracted from nearly-identical regions of these sister wafers. X-ray fluorescence microscopy (μ-XRF) was used to determine the elemental nature and spatial distribution of metal-rich particles, and X-ray absorption microspectroscopy (μ-XAS) was used to determine the chemical state. Complete details of these techniques can be found elsewhere [1, 2]. Microwave photoconductive decay (μ-PCD) and light beam induced current (LBIC) were used to identify under-performing regions in the samples.

(1) As-grown Material:

As expected, two types of metal-rich particle [1] were observed in as-grown ingot-cast mc-Si: metal silicide nanoprecipitates and metal-rich inclusions, often micron-sized and/or in an oxidized chemical state. The metal silicide nanoprecipitates contained some combination of copper, nickel, cobalt and iron, incidentally the four $3d$ transition metal species with highest atomic flux (product of solubility and diffusivity) in silicon. The metal-rich inclusions contained much larger amounts of slowly-diffusing species, such as calcium, titanium, and zinc, occasionally accompanied by high-flux elements.

(2) SiN_x Firing:

We employed μ-XRF to compare metal distributions within the same region of an as-grown wafer and a SiN_x-fired sister wafer. The as-grown wafer contained Cu_3Si nanoprecipitates along a grain boundary, and occasional inclusions of slowly-diffusing species within the grains.

Metals did not appear to be much affected by SiN_x-firing. Inclusions were evident in both wafers. Cu_3Si precipitates were also present in both wafers, only slightly larger and more numerous in the SiN_x-fired wafer than in as-grown wafer (Figure 1). The heat treatment associated with SiN_x firing may have induced the precipitation of additional metal atoms dissolved atomically within the grains, or in smaller precipitates, a similar phenomenon to Ostwald ripening. In the absence of a strong gettering layer, metals appear to have remained largely within the sample.

(3) P-diffusion Results:

Phosphorus diffusion appeared to significantly alter metal distributions within the mc-Si samples analyzed in this study.

Metal silicide nanoprecipitates with the highest fluxes, e.g. copper and nickel, appear to be dissolved below the detection limits (radius < 30 nm) during phosphorus gettering, as shown in Figure 2. Metal silicide nanoprecipitates of lower-flux species (such as iron) are more resistant to dissolution during P-diffusion [3] and may serve as virtual sources of metal point defects within the bulk, as proposed by Plekhanov et al. [4].

On the other hand, large metal-rich inclusions are frequently observed after processing, although complete statistical analyses of their size and spatial distributions before and after processing have not been performed. Despite their composition of low-flux elements and frequently oxidized chemical state [1, 5], some limited dissolution of these particles is likely during high-temperature processing steps. To a certain degree, these particles may serve as virtually inexhaustible sources of metals during solar cell processing.

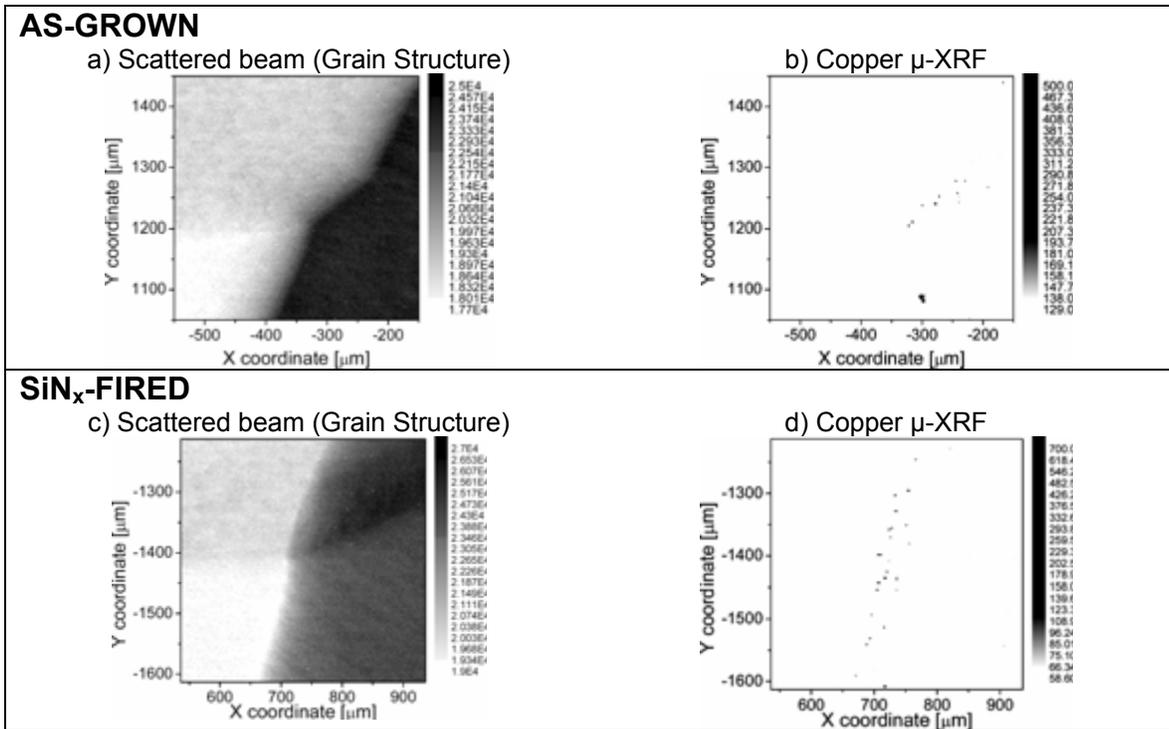**(4+5) P-diffused + SiN_x firing, and Fully-Processed cells:**

The metal distributions in P-diffused+SiN_x-fired and also in fully-processed cells resemble those found in P-diffused cells. Metal silicide nanoprecipitates of high-flux species are seldom observed in these samples, and metal silicide nanoprecipitates of low-flux species are reduced in size. Inclusions of foreign particles can still be observed in fully-processed material.

An interesting effect occurs in material with very high concentrations of metals (e.g. towards the edges of the ingot). Metals present in very high concentrations may re-arrange themselves within the samples as the result of processing, as shown in Figure 3. An as-grown sample is shown above, revealing a distribution of iron oxide and silicide particles within the grains, likely originating from the crucible and/or crucible lining material (see [6] and references therein). The same region in a sister wafers is shown after complete solar cell processing, which reveals a lower density of intragranular particles and a much higher density of iron silicide precipitates agglomerated along a certain grain boundary. Evidently, a considerable fraction of iron atoms dissolved during processing, were unable to be gettered by the P-diffusion layer (perhaps because of the high overall concentration), segregated to an energetically favorable structural defect, and precipitated there. This re-arrangement of metal species during solar cell processing necessitates an intelligent cool-down procedure at the end of processing wafers with high known metal contents that may be slower than usual, in order to promote the formation of larger metal precipitates and a reduction of dilaterious metal point defects.
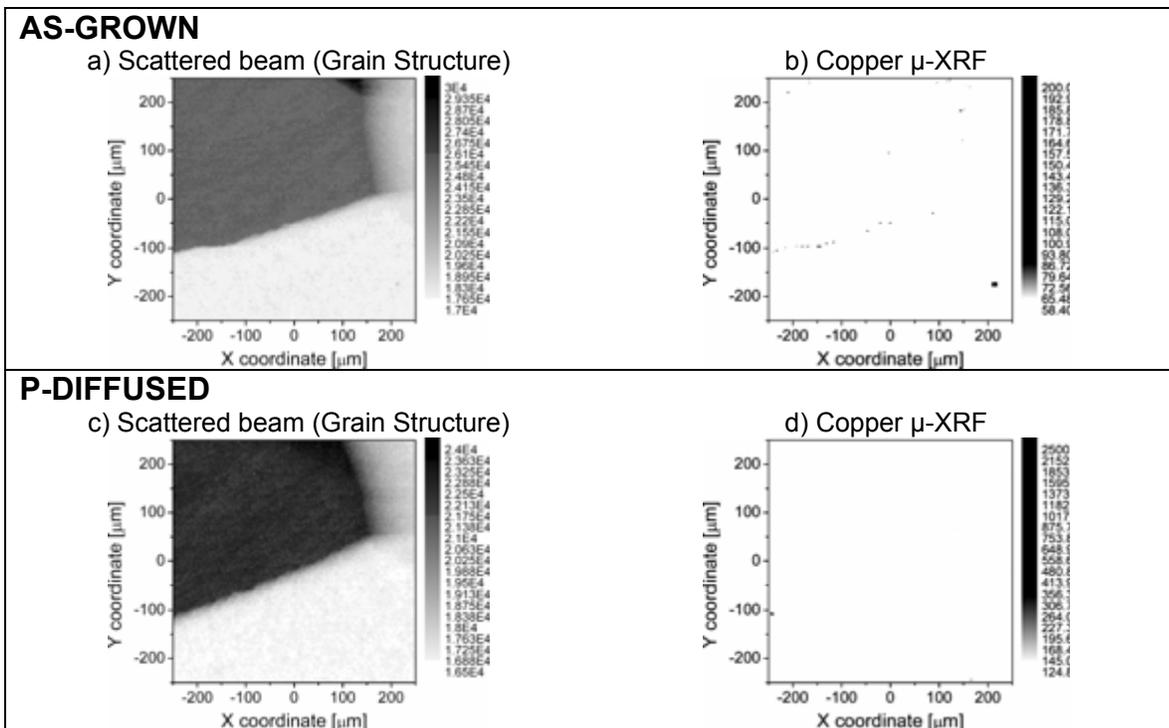
Conclusions:

Of all solar cell processing steps analyzed in this study, phosphorus diffusion appears to be the most effective step to dissolve metal silicide precipitates and alter their distributions. This correlates nicely with previous work, which demonstrated both a significant reduction of total metal concentration [7, 8] and improvement of electrical properties [9] as a result of phosphorus diffusion.

Slightly larger and more numerous metal silicide nanoprecipitates were observed after SiN_x firing, indicating a reduction in the concentration of metal point defects and nanoprecipitates below the detection limits. This could be simply an effect of the annealing, or it could be an effect of metal redistribution promoted by the presence of hydrogen as suggested by Vyvenko et al. [10]. Future work is needed to further investigate these effects, especially during co-firing with p-diffusion or aluminum backside gettering.
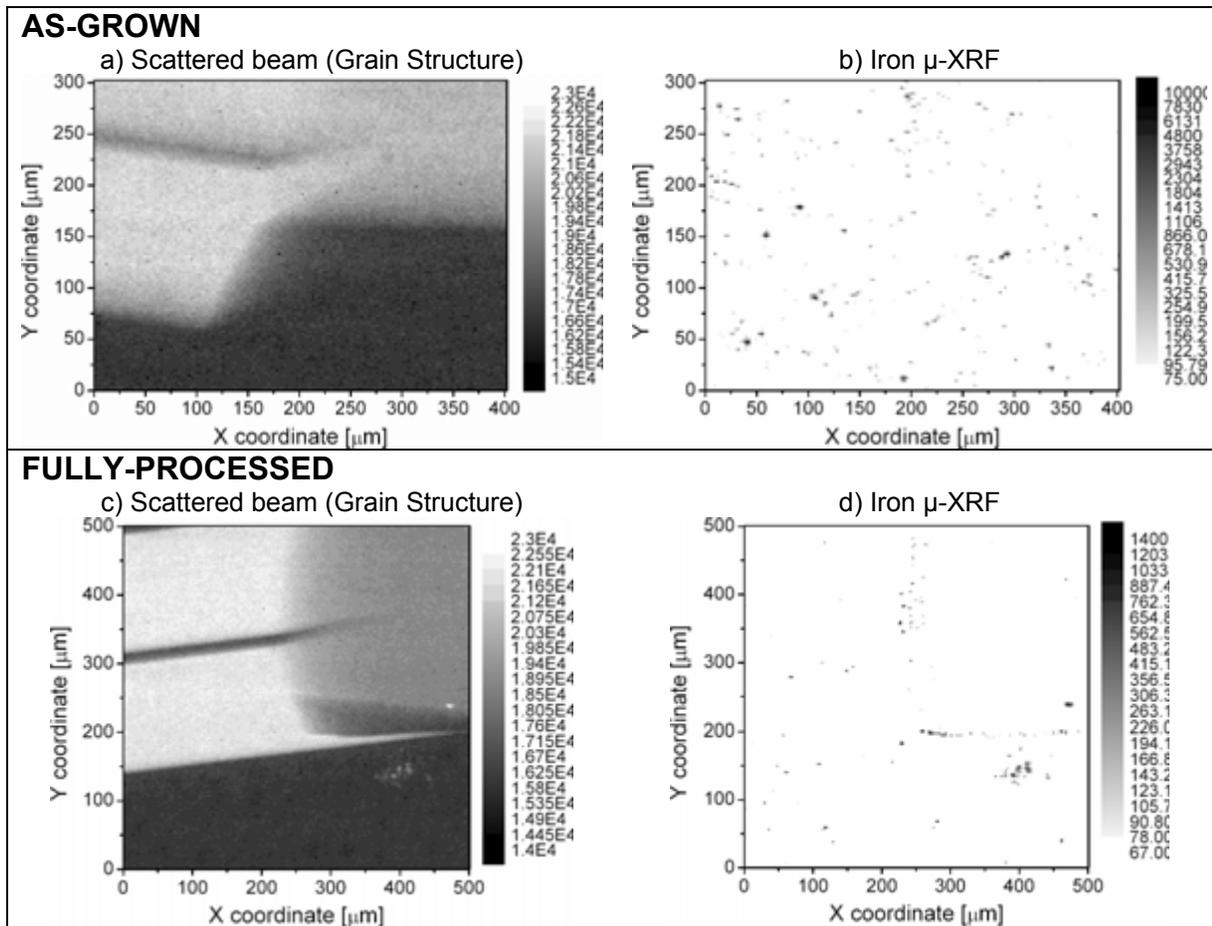
AS-GROWN

a) Scattered beam (Grain Structure)

b) Copper μ-XRF

SiN_x-FIRED

c) Scattered beam (Grain Structure)

d) Copper μ-XRF

Fig. 1: Comparison of Cu distributions in as-grown (b) and SiN$_x$-fired (d) ingot-cast mc-Si from near an ingot top. The elastically-scattered X-ray beam intensity (a and c) provides a map of the grain structure.

AS-GROWN

a) Scattered beam (Grain Structure)

b) Copper μ-XRF

P-DIFFUSED

c) Scattered beam (Grain Structure)

d) Copper μ-XRF

Fig. 2: Comparison of Cu distributions in as-grown (b) and P-diffused (d) ingot-cast mc-Si samples from near an ingot top. While copper-rich precipitates are observed along a GB in as-grown material, few such

particles are observed in the P-diffused sample. The one Cu-rich particle appears in the P-diffused sample also contains Ca, Cr, Fe, and Ni, which indicates an inclusion.

Fig. 3: Comparison of Cu distributions in as-grown (b) and fully-processed (d) ingot-cast mc-Si samples from near an ingot edge. The high density of Fe-rich particles, which evidently cannot all be gettered, is observed to re-distribute itself along certain structural defects during processing.

References:
1. T. Buonassisi, A. A. Istratov, M. Heuer, et al., *J. Appl. Phys.* 97, 074901 (2005).
2. S. A. McHugo, A. C. Thompson, C. Flink, et al., *Journal of Crystal Growth* 210, 395 (2000).
3. T. Buonassisi, A. A. Istratov, S. Peters, et al., *Submitted* (2005).
4. P. S. Plekhanov, R. Gafiteanu, U. M. Gosele, and T. Y. Tan, *J. Appl. Phys.* 86, 2453 (1999).
5. S. A. McHugo, A. C. Thompson, A. Mohammed, et al., *J. Appl. Phys.* 89, 4282 (2001).
6. T. Buonassisi, A. A. Istratov, M. D. Pickett, et al., *submitted to J. Cryst. Growth* (2005).
7. S. Binetti, M. Acciarri, C. Savigni, et al., *Mater. Sci. Eng. B, Solid-State Mater. Adv. Technol. (Switzerland)* 36, 68 (1996).
8. D. Macdonald, A. Cuevas, A. Kinomura, et al., *in* "29th IEEE Photovoltaic Specialists Conference", p. 1707, New Orleans, USA (2002).
9. C. Ballif, S. Peters, C. Borchert, et al., *in* "2001 European Photovoltaics Specialists Conference and Exhibition", Munich, Germany (2001).
10. O. F. Vyvenko, T. Buonassisi, A. A. Istratov, E. R. Weber, M. Kittler, and W. Seifert, *J. Phys.: Condens. Matter* 14, 13079 (2002).

Defects induced by impurity atoms in B-doped cast-grown polycrystalline silicon

Yoshio Ohshita, Koji Arafune, Hitoshi Sai and Masafumi Yamaguchi
Toyota Technological Institute, 2-12-1 Hisakata, Tempaku, Nagoya 468-8511 Japan
Tel: +81-52-809-1876, E-mail: ohshita@toyota-ti.ac.jp

ABSTRACT

The grain size distribution of B-doped cast-grown polycrystalline Si could not explain the minority carrier lifetime map. The lifetime was not mainly determined by the grain boundary recombination, since the grain size of the present cast-grown polycrystalline Si exceeded 1 cm and was large enough as compared with the minority carrier diffusion length ($0.25\,\mu$ m). In the region where the lifetime was relatively short, there were many defects, which appeared as etch-pit by the Secco etching. The relationship between the etch-pit density and the minority carrier lifetime suggested that these defects acted as a recombination center and that they mainly determined the lifetime. There were relatively larger amounts of carbon atoms in the region with short lifetime as compared with in the region with longer lifetime. These impurities might create the defect in the grain during the crystal growth. It was also indicated that Fe atoms were corrected at these defects, and that the defect and/or defect-heavy metal complex deteriorated the minority carrier lifetime.

Introduction

Recently, the solar cell industry has been significantly growing and the total of production of solar cell reached 1GW in 2004. Crystalline silicon (Si) technology has dominated the production of solar cells, which contributed of 95% of the world's PV production. Because of lower cost and relatively better conversion efficiencies, the poly-crystalline Si solar cells are dominant in the crystalline Si solar cell market. Therefore, to improve the conversion efficiency of the polycrystalline Si solar cells and to reduce the cost are more important for the further growth of solar cell market.

So far, since the grain boundary act as recombination centers that determines the solar cell performance, increasing the grain size of polycrystalline Si has improved the conversion efficiency [1-5]. Now, the larger grain size exceeding 1 cm was obtained by cast-grown method, which is large enough as compared with the minority carrier diffusion length (0.25 mm) in B-doped polycrystalline Si. However the expected high conversion efficiency has not been realized. In the cast-grown Si, there are many impurity atoms such as carbon (C) and iron (Fe), and defects that appear as etch-pits. Therefore, now the grain boundary does not mainly determine the conversion efficiency and that the defects and impurities in a grain play important roles in the deterioration of the solar cell performance. Then, to improve the conversion efficiency of polycrystalline Si, they are important to understand the roles of these impurities and defects and

to reduce these amounts. In the present paper, we report the effects of defects and impurities in the grain of the B-doped cast-grown polycrystalline Si on the minority carrier lifetime. The distribution of defects corresponded to that of impurity atoms explained well the minority lifetime map, indicating that the defects and/or defect-heavy metal complex determined the minority carrier lifetime.

1. Experiment

The cast polycrystalline Si grown at JFE Steel Corporation was used in this study. Wafers were boron doped (10^{16} - 10^{17} cm^{-3}) with a resistively of 0.4 - 0.8 Ω cm. The wafer thickness was 350μ m and the size was 50 mm x 50 mm. The cooling rate was slow as compared with that of Czochralski growth. The maximum grain size exceeded 1 cm. The average diffusion length of the electron was 250 μ m, and the conversion efficiency over 18% was obtained by using this wafer as a solar cell material [5]. Before measurements, the saw-induced damaged layer was etched off by the HNO$_3$/HF solution. For lifetime measurements, the Si surface was passivated by iodine (I). The lifetime mapping was obtained by laser microwave photoconductance decay (PCD) measurement. The step size used for generating the lifetime mapping was 1mm and 523 nm He-Ne laser was used as carrier injection source. The wafer surface was Secco etched for 10 minutes and it was studied by the optical microscopy. The numbers of the interstitial oxygen (O) and substitutional carbon (C) in the cast-grown crystal were estimated by Fourier-transform infrared spectroscopy (FTIR) and the total amounts of these impurities were

determined by secondary ion mass spectroscopy (SIMS). Fe distribution and its electric structure were studied by X-ray microprobe fluorescence measurement at BL37XU line of Spring-8 [6]. Exciting energy was 10 keV and the beam size was focused to 5 μ m. The structure of Fe K absorption edge was scanned in the near edge region.

2. Results and discussion

The minority carrier lifetime, which was obtained by PCD measurement, varied from 15 to 360 microseconds in the wafer. However, the distribution of the grain size cannot explain the minority carrier lifetime map. The short minority carrier lifetime region did not correspond to a small grain region. The relationship between the etch-pit density and the minority carrier lifetime is shown in Fig. 1. The lifetime dramatically decreases as the number of the etch-pit increases. The grain size became exceeding 1cm. It is large enough as compared with the diffusion length of the electron and the lifetime is not mainly limited by the recombination at grain
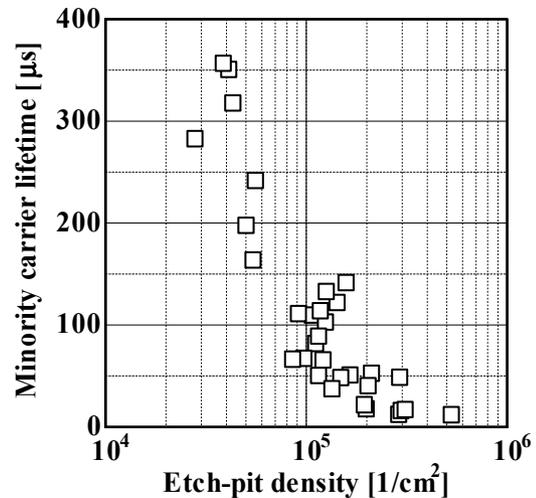

Fig. 1 Effect of etch-pit density on minority carrier lifetime.

boundaries. Then, the defects, which appeared as etch-pit by the etching, acted as recombination centers, and mainly determined the minority carrier (electron) lifetime in the present cast-grown polycrystalline Si.

The numbers of the carbon at substitutional site were 2.9 - 3.5 x 10^{17} cm^{-3} (table 1) and they corresponded to the solubility limit at the growth temperature. The large amount of carbon might be contaminated from the carbon heater during the growth process. The amounts of oxygen were relatively smaller as compared with Cz Si. By the SIMS measurement, the total number of carbon atoms in the shorter minority carrier lifetime region exceeded the solubility limit. SiC particles might form during the crystallization resulting in the formation of defects, which appeared as etch-pit by the Secco etching.

Table 1 C and O concentrations in low- and high-EPD regions [6]

Element	Concentration [atoms/cm^3]	
	low-EPD region	high-EPD region
Oxygen	5.0×10^{16}	8.2×10^{16}
Carbon	2.9×10^{17}	3.2×10^{17}

The distribution of Fe is shown in Fig. 2. Fe concentration was not uniform in the crystal and they were corrected at the particular position. The plan-view optical microscope image of the surface is shown in Fig. 2. There are line-shape defects, which are slip and twin-boundary. As compared with the Fe distribution, little amount of Fe existed at these defects. LBIC results showed that this type defects did not act as a recombination center. On the other hand, large amount of Fe was segregated at the region where there were many etch-pit.

These defects were created by the residual oxygen and/or carbon. The Fe was trapped at the defect of this type.

There is a close relationship between the impurity atoms and defects distributions and minority carrier diffusion length one. Therefore, in order to grow high-quality polycrystalline Si ingots, we need control initial nucleation and crystal-melt interface during the crystal growth. Thus, we are developing new crystal growth furnace, which has four independent heaters and crucible rotation mechanism. The bottom heater, outer carbon crucible and top chamber of the furnace is shown in Fig. 3
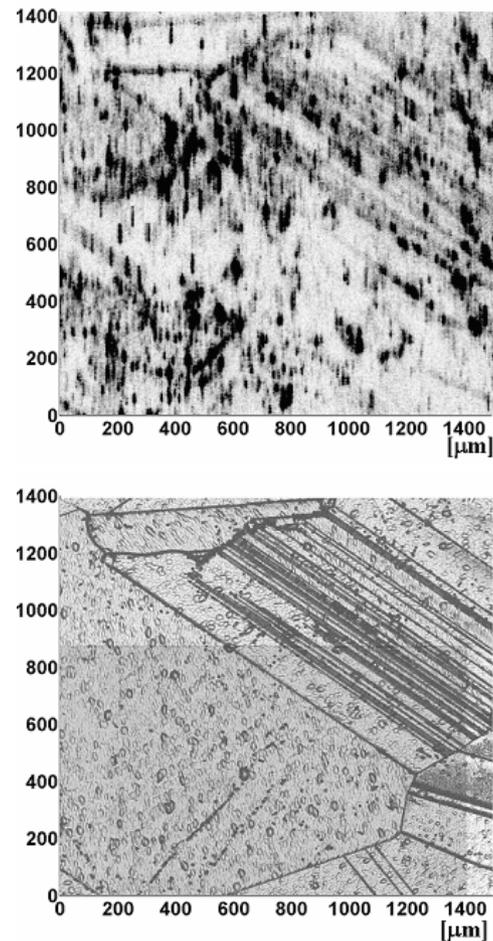

Fig. 2 Iron distribution by μ-XRF measurement (upper) and plan-view optical microscope image (lower); the dark color corresponds to higher iron concentration
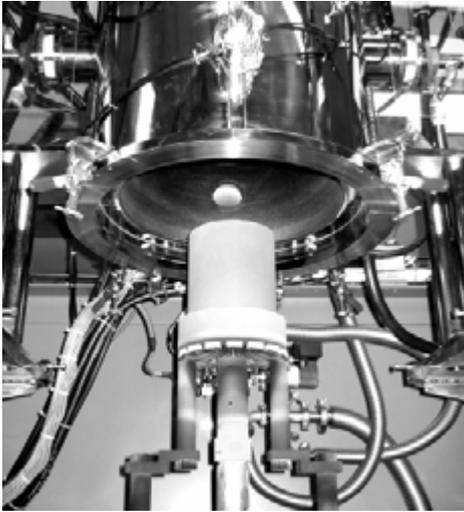
Fig. 3 Polycrystalline Si ingot growth furnace.

Conclusion

The grain size of the present cast-grown polycrystalline Si exceeded the minority carrier diffusion length (0.25 μ m). Therefore, the minority carrier lifetime was not mainly determined by the grain boundary recombination. In the region where the lifetime was relatively short, there were many defects, which appeared as etch-pit by the Secco etching. The relationship between the etch-pit density and the minority carrier lifetime suggested that these defects acted as a recombination center and that they mainly determined the lifetime. There were relatively larger amounts of carbon atoms in the region with short lifetime as compared with in the region with longer lifetime. These impurities might create the defect in the grain during the crystal growth. X-ray microprobe fluorescence measurement results suggested that Fe were corrected at these defects, and that the defect and heavy metal complex deteriorated the minority carrier lifetime. Therefore, in order to realize the high-quality polycrystalline Si, they are important not only to reduce the amounts of these impurity atoms, but also to control the crystal-melt interface during the crystal growth.

REFERENCES

[1] Z.Radzimski, T. Zhou, A. Buczkowski, G. Rozgonyi, D. Finn, L. Hellwig, and J. Ross, Appl. Phys. Lett., 60 (1992) 1096.

[2] M. Kittler, C. Ulhaqbouillet, and V. Higgs, J. Appl. Phys., 78 (1995) 4573.

[3] A. Ihlal, and R. Rizk, J. Phys. D29 (1996) 3096.

[4] J. Lu, M Wagener, and G. Rozgonyi, J. Appl. Phys., 94 (2003) 140.

[5] Y. Komatsu, Y. Takaba, S. Yasukawa, S. Okamoto, and M. Shimizu, Proceedings of 12th Workshop on Crystalline Silicon Solar Cell Materials and Prosesses, (2002) 176.

[6] Y. Ohshita, K. Arafune, T. Sasaki, M. Tachibana, Y. Terada, S. Tanaka, M. Yamaguchi, Proceedings 31st IEEE Photovoltaic Specialists Conference (2005) to be published.

[7] Spring-8 is the largest third -generation synchrotron radiation facility in Japan.

Hydrogen-rich Silicon Nitride Layers: Surface and Bulk Passivation for Solar Cell Applications

Chuan Li[1, 2], Bhushan Sopori[1], P. Rupnowski[1, 3], Anthony T. Fiory[2] and N. M. Ravindra[2]

[1]National Renewable Energy Laboratory, Golden, Colorado, 80401
[2]Department of Physics, New Jersey Institute of Technology, Newark,
New Jersey, 07102
[3]Department of Physics and Astronomy, University of Denver, Denver, Colorado, 80208

Abstract

Hydrogen-rich silicon nitride (SiN:H) layers are used in solar cells to perform many functions — for antireflection (AR) coatings and to passivate bulk and the surfaces. In this study, model calculations of the surface recombination velocities at the Si-SiN interface on wafers coated with nitrides deposited by various techniques are presented. A complete model of H "storage" during nitridation and its subsequent diffusion into the bulk of the Si is established and employed to explain bulk passivation effects after nitridation.

Introduction

SiN:H layers used for antireflection coatings serve several other functions, which include Passivation of impurities and defects at the surface and in the bulk of a solar cell, and acting as a barrier for the fire-through metallization.

The passivation features of SiN:H are very important because:
— High-efficiency Si solar cells must have low surface recombination and high minority carrier diffusion length;
— Commercial Si solar cells fabricated on low-cost substrate usually contain high concentrations of impurities and defects. Gettering itself does not reduce the impurity concentration to desirable levels. A good hydrogenation process can help to improve the cell efficiency range.

Surface Passivation by SiN$_x$

During the last decade, it has become increasingly clear that PECVD SiN$_x$ produces excellent surface passivation in silicon solar cells. Very low surface recombination velocity (SRV) of charge carriers was observed in silicon wafers coated with PECVD nitride layer [1-3]. In 1988, Girisch *et. al.* introduced an extended Shockley-Read-Hall (SRH) formalism [4], which was later adopted by Aberle *et. al.* who successfully explained the measured injection level dependence of SRV at the Si-SiO$_2$ interface [5]. It is well known that the low SRV of SiO$_2$ passivated Si surface is due to the

combination of moderately low density of interface states at midgap [D_{it} = (1-10)×10^{10} $cm^{-2} eV^{-1}$] and a high positive oxide fixed charge density [Q_{ox}=(1-10)×10^{11} cm^{-2}] [6].

Similarly, the deposition of SiN_x layers on silicon substrate leads to the formation of a space charge region at the interface characterized by a fixed positive charge density (Q_f) of the order of 10^{12} cm^{-2}. In p-type Si a depletion/inversion layer is formed, while in n-type Si the positively charged insulator attracts majority carriers and repels minority carriers. Hence, an accumulation layer is formed.

The modeling results of effective surface recombination velocity (S_{eff}) as a function of the injection level Δn for different fixed positive charge densities are shown in Figures 1 (a) and 1(b).
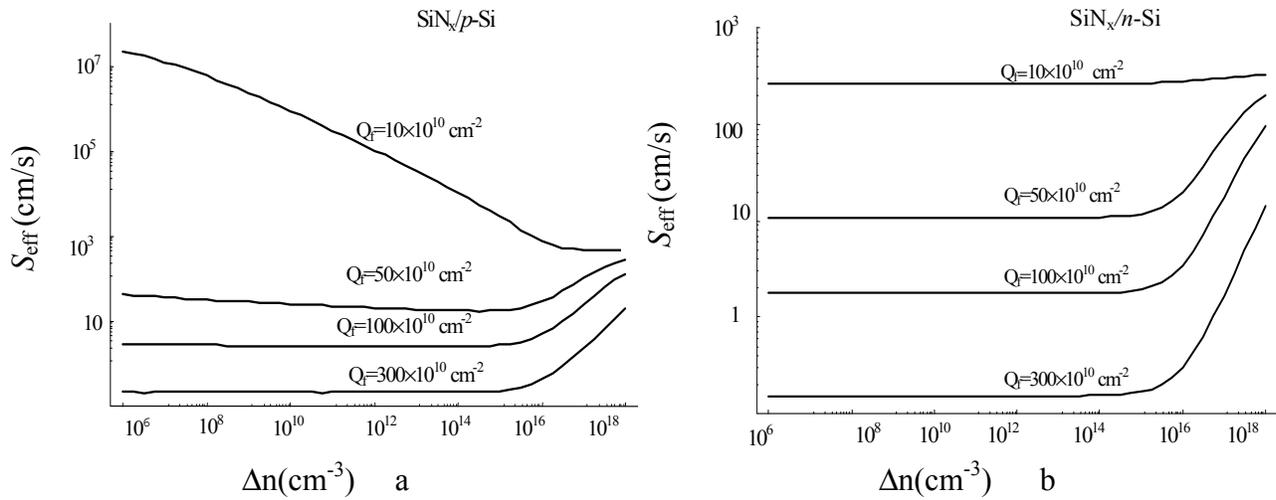

Fig. 1 Calculated dependence of effective surface recombination velocity (S_{eff}) for (a) p-type and (b) n-type surfaces as a function of injection level (Δn) for different fixed positive charge densities.

Good agreement between measured and calculated $S_{eff}(\Delta n)$ dependences at certain Q_f levels has been reported by J. Schmidt et al. [7]. However, according to this model calculation, very high Q_f (1~3 × 10^{12} cm^{-2}) would lead to no injection level dependence of the effective surface recombination velocity for p-type Si wafer, which is in contradiction to experimental results [8]. This discrepancy is assumed to be caused by generation and recombination in the depletion region [9]. It is implied that an improved model of surface recombination at SiN_x/Si interface should also consider the recombination in the space charge region.

Low S_{eff} of the PECVD SiN-passivated Si surface is attributed to the combining of moderately low density of interface states, and a high positive charge density. Both parameters are given in Table 1 for as-deposited and thermally treated silicon nitride films. [10].

Table 1 Positive fixed charge and interface-trap-density of as-deposited and annealed SiN-Si interface

Silicon nitride condition	Q_f (cm^{-2})	D_{it} (cm^{-2}/eV)
As-deposited	3×10^{12}	2×10^{11}
Thermally treated	1×10^{12}	1×10^{11}

According to the SRH formalism, S_{eff} can be also minimized by reducing the interface state density D_{it}.   In Figure 2 the dependence of S_{eff} on D_{it} is shown for 1Ω cm p-Si wafer.

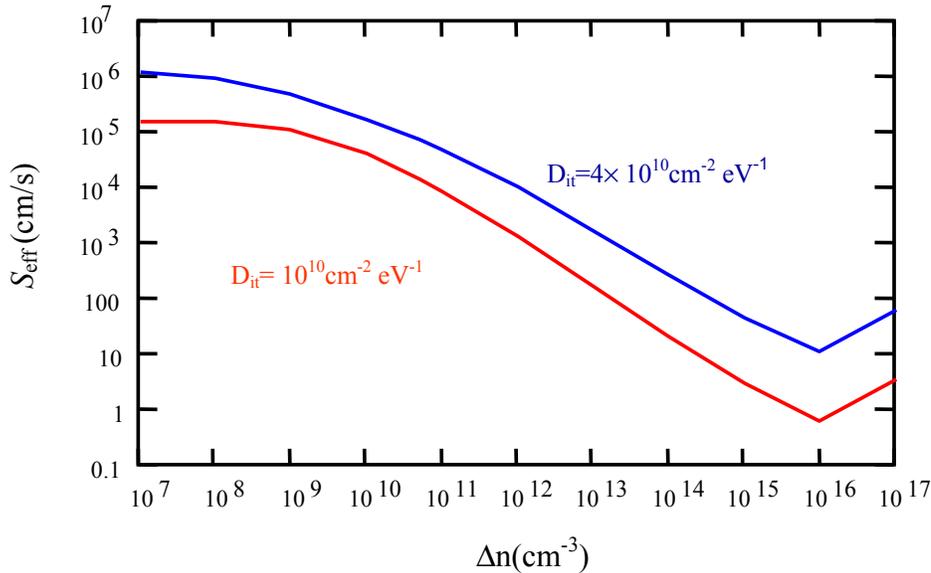Fig.2 Calculated effective surface recombination velocity S_{eff} for p-Si surface as a function of the injection level Δn in the quasi-neutral bulk for different values of interface state density D_{it}. Input parameters: Doping concentration = 1×10^{16} cm^{-3}; σ_n = 1×10^{-14} cm^2, σ_p = 1×10^{-16} cm^2; Q_f = 1.3×10^{11} cm^{-2}.

SiN$_x$ films prepared by remote plasma or direct PECVD at high frequency (HF) provide much better surface passivation than SiN$_x$ films prepared at low frequency (LF). This is achieved by avoiding heavy ion bombardment during the deposition process, and consequently much lower D_{it}.

Bulk Passivation

It is believed that bulk passivation effects are achieved by hydrogen passivating the impurities and defects in bulk silicon and hence increasing the minority carrier lifetime. But the understanding of the mechanism is lacking in the literature.

According to Sopori and Zhang *et al*. [11, 12], PECVD step serves as a pre-deposition step for hydrogen. The majority of the hydrogen atoms are trapped and "stored" in process-induced traps (PITs) in the surface damage produced by the plasma process during the nitride deposition. It should be noted that diffusion of H occurs, but because of the traps, H is primarily confined to the vicinity of the surface. In rapid thermal processing (RTP) anneal step, H is released from the surface and redistributed into the bulk region.

A verification of H "storage" during PECVD process and its subsequent diffusion is seen in Fig. 3. This figure is a secondary ion mass spectrometry (SIMS) plot of H in Si solar cell before and after the standard firing process for solar cell fabrication. The nitride layer was removed prior to SIMS measurements. This figure shows that H has diffused into the Si wafer and that the surface concentration is lower after firing.
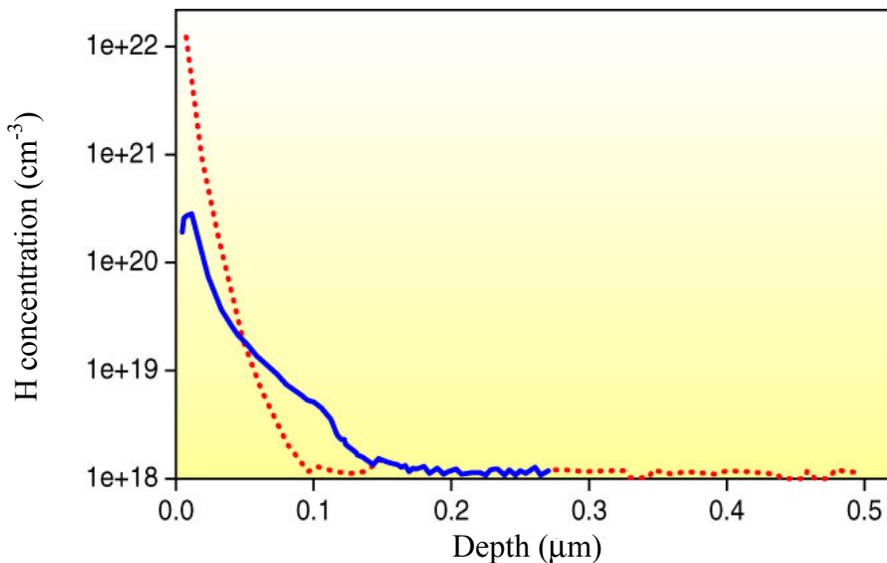

Fig. 3. SIMS profiles of H before (dotted) and after firing (solid) the PECVD nitride-coated wafer [11]

Summary

We have shown that PECVD silicon nitride layers provide both surface and bulk passivation in silicon solar cells. The passivation of a silicon surface can be achieved in two ways: by field-effect passivation or neutralization of the interface defect states. The large positive fixed charge density at the interface is crucial for surface passivation by PECVD SiN_x layer. Silicon nitride films deposited by remote and HF PECVD techniques have demonstrated their capability for improving the surface passivation of silicon solar cells due to much less damage to the silicon surface in comparison to those LF PECVD SiN_x layers. A post-deposition anneal process is important to obtain a low surface

recombination velocity by healing the surface damage caused by ion bombardment during nitridation.

PITs are responsible for the H storage in the vicinity of the Si wafer surface. H is detrapped during subsequent high temperature firing process, diffusing deep into the bulk of Si solar cells.

Acknowledgements

References:

1. H. Mäckel and R. Lüdemann, *J. Appl. Phys*. **92**, 2602 (2002)
2. T. Lauinger, J. Schmidt, A. G. Aberle and R. Hezel, *Appl. Phys. Lett*. **68**, 1232 (1996)
3. A.G. Aberle and Rudolf Hezel, Progress in Photovltaic: Research and Applications, **5**, 29-60 (1997)
4. R.B.M.Girisch, R.P.Mertens, and R.F. de Keersmaeker, *IEEE Trans. Electron Devices* **35**, 203 (1988)
5. A.G. Aberle, S. Glunz, and W. Warta, *J. Appl. Phys*. **71(9)**, 4422 (1992)
6. K. Yasutake, Z. Chen, S.K. Pang, and A. Rphatgi, *J. Appl. Phys., **75**, 2048 (1994)
7. J.Schmidt and Armin G. Aberle, *J. Appl. Phys*. **85**, 3626 (1999)
8. J. Schmidt, J.D. Moschner, J. Henze, S. Dauwe and R. Hezel, *19th European Photovoltaic Solar Energy Conference*, Paris, France, 2004
9. C. Leguijt, P. Lölgen, J.A. Eikelboom, A. W. Weeber, F.M. Schuurmans, W.C. Sinke, P.F.A. Alkemade, P.M. Sarro, C.H.M. Marée, L.A. Verhoef., *Sol. Energy Mater. Sol. Cells* **40**, 297 (1996)
10. F. Duerinckx, J. Szlufcik, *Solar Energy Materials & Solar Cells*, 72, **231** (2002)
11. B.L Sopori, *J. of Electron. Mater*, **32**, 1034, 2003
12. Y. Zhang (Ph.D. thesis, New Jersey Institute of Technology, 2002)

21 % efficient Si solar cell using a low-temperature a-Si:H back contact

P. J. Rostan, U. Rau, V. X. Nguyen, T. Kirchartz, M. B. Schubert, and J. H. Werner

Institut für Physikalische Elektronik, Universität Stuttgart, Pfaffenwaldring 47

70569 Stuttgart, Germany

Abstract

The contribution reports on high-efficiency, p-type crystalline Si solar cells using a low-temperature back contact consisting of a sequence of amorphous (a-Si) and microcrystalline (μc-Si) silicon layers prepared at a maximum temperature of 220°C. Our best solar cells having diffused high-temperature, front-side emitters with random texture and full-area low-temperature a-Si/μc-Si contacts show an independently confirmed efficiency of 21.0 %. An alternative concept uses a simplified a-Si layer sequence combined with Al-point contacts and yields a confirmed efficiency of 19.3 %.

Introduction

High-efficiency silicon solar cells require back contacts that combine low contact resistance with a low recombination velocity for minority carriers as well as with high optical reflectance. Usually, these functions are overtaken by a thermally grown oxide combined with photolithographically defined metallic point contacts and the diffusion of a back surface field underneath these local contacts [1]. Cost reduction in processing high efficiency solar cells would be possible if these complicated back contacts could be replaced by a simpler, but equally efficient scheme, preferentially prepared at low temperature.

This contribution introduces a sequence of amorphous (a-Si) and microcrystalline (μc-Si) silicon layers grown by plasma-enhanced chemical vapor deposition (PECVD) at a maximum temperature of 110°C for the passivation of the back surface of solar cells. We apply these back contacts to solar cells with diffused emitters and random texture at the front surface. These cells, finished with a full-area a-Si/μc-Si contact reach an independently confirmed efficiency of 21.0 %. An alternative concept based on a simplified a-Si layer sequence combined with Al-point contacts yields a confirmed efficiency of 19.3 %.

Solar cell preparation

Our solar cells are based on 250 μm thick p-type FZ Si wafers with a resistivity of 1 Ωcm. The cells have a diffused emitter with a random texture as the front electrode, and a photolithographically defined grid. The different back contact are applied to the cells with the front side being already completely processed. A masking oxide protects the back surface of the wafer during the whole front side processig. After emitter completion, the back side masking oxide is removed by a dip in 5 % HF solution. Then, the samples are mounted into the PECVD system where we deposit a 10 nm thick undoped (i) a-Si layer followed by an approximately 40 nm thick p-type doped a-Si layer using an admixture of B_2H_6. The deposition

of these layers is performed in separate chambers at a substrate temperature $T_S \approx 110\ ^{\circ}C$ and a plasma frequency $\nu_p \approx 13.56$ MHz.

Figure 1 presents the two types of back contacts that we are using: Type A is a full area back contact, consisting of a heavily p-type doped µc-Si layer (obtained at $T_S \approx 110\ ^{\circ}C$ and $\nu_p \approx 80$ MHz) with a thicknesses of about 10 nm is applied to ensure a good ohmic contact to the sputtered ZnO:Al. Type B, the alternative back contact, uses - instead of the µc-Si layer - Al-point contacts that are evaporated through a shadow mask. After annealing at 220 °C, Ohmic contacts form by Al-induced crystallization of the a-Si at the location of the contact points. Note that the contact formation of the present Al-point contacts is similar to that used in Ref. [2]. In our case, both back contacts schemes use a sputtered ZnO layer and evaporated Al as a back surface reflector.
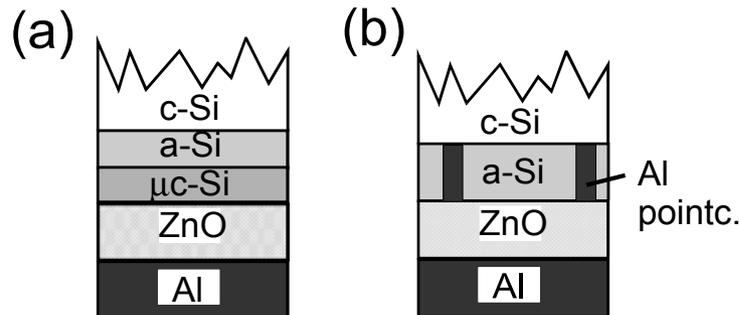

Fig. 1: Sketch of the full area contacts. a) a-Si/ZnO back contact; b) a-Si/Al-point contacts. The a-Si layers consist of 10 nm of un-doped (i) a-Si and a second layer that is p-type doped by adding B_2H_6 into the PECVD chamber.

Results

Figure 2 shows the electrical data of our best cell with full-area a-Si/µc-Si/ZnO back contact (cell area $A = 1\ cm^2$). The cell has an efficiency of 21.0 % as independently confirmed by Fraunhofer Institute (ISE) Freiburg. The photovoltaic output parameters open circuit voltage V_{OC}, short circuit current density J_{SC}, fill factor FF, and power conversion efficiency η of the best solar cells with the full area contact and with Al-point contacts are summarized in Tab. I.
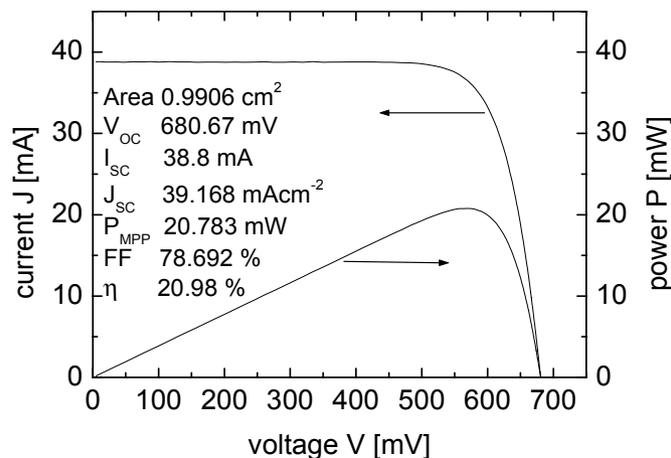

Fig. 2: Current voltage curve of the best of our full area a-Si/ZnO back contact (Type A) under standard test conditions as measured by Fraunhofer Institute (ISE) Freiburg.

Figure 3 presents the analysis of the internal quantum efficiency of cells with our full-area a-Si contacts, type A. The high open circuit voltages $V_{OC} \approx 680$ mV of these cells result

from large effective diffusion lengths $L_{eff} \approx 1000$ µm, thus demonstrating the excellent passivation of the cell's back surface by the PECVD grown (i) a-Si:H. The effective diffusion lengths L_{eff} are derived from a plot of the inverse IQE vs. the absorption length L_α of the radiation [3] as shown in Fig. 4. From the slope s of those plots we obtain the effective diffusion length L_{eff} via $L_{eff} = \cos(\vartheta)/s$, where the refraction angle $\vartheta = 41.8$ ° results from the surface texture and the factor $\cos(\vartheta)$ takes care of the longer effective path length of the refracted light [3].

Table I: Photovoltaic parameters open circuit voltage V_{OC}, short circuit current density J_{SC}, fill factor FF, and power conversion efficiency η under simulated AM1.5G illumination for the best solar cells with a full area a-Si/ZnO back contact (type A) and for a cell with an a-Si back surface passivation and Al-point contacts (type B).

sample	area A (cm^2)	V_{OC} (mV)	J_{SC} (mA/cm²)	FF (%)	η (%)
full area a-Si/ZnO	1	681	39.17	78.69	20.98[*]
full area a-Si/ZnO	4	679	38.74	76.93	20.22[*]
a-Si/Al point/ZnO	2	655	37.14	79.47	19.34[*]

*confirmed by Fraunhofer Institute (ISE) Freiburg

Fig. 3: Internal quantum efficiency IQE of the two types of solar cells from Fig. 1. The low recombination at the surface of the full area a-Si/c-Si back contact (curve a) is reflected in a higher IQE than for cell with the Al-point contacts (curve b) in the wavelength regime 950 nm ≤ λ ≤ 1050 nm.
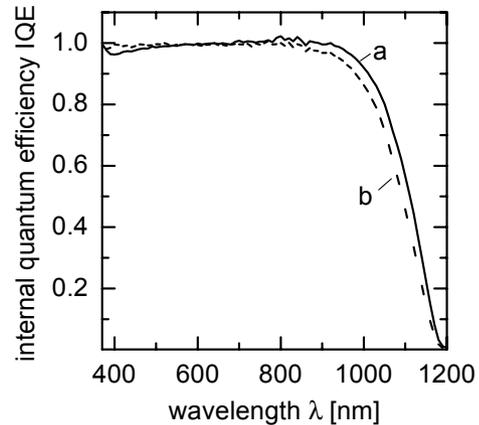
According to Fig. 3 the IQE of the Al-point contact cell (curve b) is somewhat lower than the IQE of the full area contact cell (curve a). Accordingly, the effective quantum efficiency L_{eff} of this type of cell as determined from Fig. 4 is only around 500 µm corresponding to the lower $V_{OC} = 655$ mV. Note that an alternative way to form point contacts on a-Si-passivated surfaces is described in Ref. [4]. This approach uses a layer sequence (i)a-Si/(p$^+$)a-Si/a-SiNX together with Laser Fired Contacts [5] and yields up to now a maximum open circuit voltage $V_{OC} = 667$ mV.

The fill factor FF of the point contact cell is $FF = 79.5$ % and, hence, somewhat higher than the FF of our full area a-Si contacts (cf. Tab. I). In the latter case, the series resistance R_S of typically $R_S \approx 0.8$ Ωcm^2 and the non-ideal diode quality factor $n_{id} \approx 1.6$ lead to a decrease of FF into a typical range of 77 to 78 %. Thus, a major potential for improving the

efficiency of this type of solar cells lies in minimizing the resistance of the various interfaces of this back contact.

Fig. 4: Inverse IQE^{-1} plotted vs. absorption length L_α for the two cell types A and B. From the slope s of the plots we obtain the effective diffusion length L_{eff} via $L_{eff} = \cos(\vartheta)/s$, where the refraction angle $\vartheta = 41.8°$ results from the surface texture.
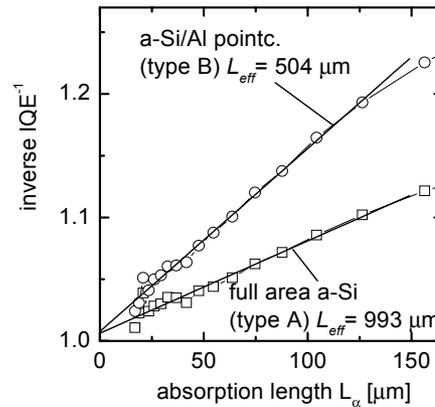
Conclusions

Low temperature ohmic contacts of a-Si to p-type crystalline Si open a new road to lower the preparation cost of high efficiency solar cells. The low thermal budget makes these contacts particularly interesting for the preparation of solar cells from thin Si wafers or from thin crystalline Si films. Moreover, mastering the (p)c-Si/(p)a-Si hetero-contact is a corner-stone for developing a-Si/c-Si/a-Si heterojunction solar cells on p-type c-Si wafers [6] with a similar efficiency as already realized on n-type material [7].

References

[1] J. Zhao, A. Wang, P. Altermatt, and M. A. Green, Appl. Phys. Lett. **66**, 3636 (1995).

[2] H. Plagwitz, M. Schaper, A. Wolf, R. Meyer, J. Schmidt, B. Terheiden, and R. Brendel, in *Proc. of 20th European Photovoltaic Solar Energy Conf.* (2005, in print).

[3] P. A. Basore, in *Proc. 23rd IEEE Photov. Specialists Conf.* (IEEE, New York, 1993) p.. 147.

[4] W. Brendle, V. X. Nguyen, K. Brenner, P. J. Rostan, A. Grohe, E. Schneiderlöchner, R. Preu, U. Rau, G. Palfinger, and J. H. Werner, in *Proc. of 20th European Photovoltaic Solar Energy Conf.* (2005, in print).

[5] E. Schneiderlochner, R. Preu, R. Ludemann, and S. W. Glunz, Progr. Photov.: Res. Appl. **10**, 29 (2002).

[6] U. Rau, V. X. Nguyen, J. Mattheis, M. Rakhlin, and J. H. Werner, in *Proc. 3rd World Conf. Photovolt. Energy Conv.,* K. Kurosawa, L. L. Kazmerski, B. McNellis, M. Yamaguchi, C. Wronski, and W. C. Sinke, Eds., (Arisumi Printing, Japan, 2003) p. 1124.

[7] M. Taguchi, K. Kawamoto, S. Tsuge, T. Baba, H. Sataka, M. Morizane, K. Uchihasi, N. Nakamura, S, Kyiama, and O. Oota, Progr. Photov.: Res. Appl. **8**, 503 (2000).

Structure, electrical activity, and thermal stability of acceptor-oxygen complexes in Si solar cells

M. Sanati, S.K. Estreicher, and D. West
Physics Department, Texas Tech University, Lubbock, TX 79409-1051

Abstract: The carrier lifetime in boron-doped CZ-Si is strongly reduced by illumination, the application of a forward bias, or irradiation. The culprits are believed to be B-O complexes. We use first-principles theory to predict the properties of acceptor-oxygen complexes involving substitutional or interstitial B or Ga and interstitial oxygen or oxygen dimers. Four electrically-active complexes have comparable binding energies at T=0K. When including vibrational free energies and configurational entropies, only two of them remain stable at or above room temperature.

1. Introduction

Substitutional boron (B_s) is the most common p-type dopant in Si and interstitial oxygen (O_i) is the dominant impurity in CZ-Si. Although neither B_s nor O_i diffuse up to rather high temperatures, at least two types of B-O complexes have been observed to form in the 300-400K range following irradiation or exposure to light. These defects reduce the free carrier concentration and are blamed for substantial efficiency reduction (~ 10% relative) in both space and terrestrial solar cells. [1]

The self-interstitials generated [2] by 1MeV electron irradiation interact with B_s and create the fast-diffusing interstitial B_i^+,[3] with an acceptor level [4] at E_c–0.43eV. This level anneals out as the $\{B_i,O_i\}$ complex appears. Its gap level has been reported at E_c–0.27eV by DLTS [3,5], E_c–0.30eV by Hall effect [6] and E_c–0.26 to 0.30eV by photoluminescence (PL). [7] This pair is not seen in Al- or Ga-doped material or in non-irradiated samples in which light-degradation is observed. [7]

In samples exposed to band gap light, a different reaction occurs. Few B_i's are available and almost all of the oxygen in sample consists of isolated O_i, with migration energy 2.5eV. [8] Thus neither of these two impurities diffuses at the temperature which the degradation occurs. However, the samples also contain a small amount of $\{O_i\}_2$ dimers. Minority-carrier lifetime spectroscopy shows that the concentration of the light-induced defects is proportional to the concentration of B and to the square of the concentration of O, [9] suggesting that $\{O_i\}_2$ dimers are involved. The formation of the $\{B_s,O_i,O_i\}$ defect involves an activation energy of 0.37eV and its gap level is at E_c–0.41eV. [10] It anneals out at 200°C with an activation energy of 1.3eV.[9] The degradation also occurs in the dark when a forward bias is applied [11], but it is not observed in Ga-doped material.[12]

The formation of $\{B_s,O_i,O_i\}$ occurs as follows [13]. Upon exposure to light, the $\{O_i\}_2^{++}$ dimer diffuses with the (calculated) activation energy of 0.3eV, close to that observed experimentally. It traps at B_s^- and forms the $\{B_s,O_i,O_i\}$ complex. The (0/+) level associated with this complex is estimated [13] to be in the range E_c–0.5 to 0.7eV, the lower value being close to the observed E_c–0.41eV. The binding energy in the positive charge state (relative to B_s^- and $\{O_i\}_2^{++}$) is estimated [13] at 0.38eV. Since the calculated migration energy of $\{O_i\}_2^{++}$ is 0.86eV, the predicted dissociation energy of the complex is 1.24eV in the dark, consistent with the value reported experimentally [9].

In this work, we calculate the configurations, thermodynamic gap levels, and binding energies and free energies of complexes of substitutional or interstitial B (and Ga) with oxygen and oxygen dimers in Si.

2. Theoretical background

Our results are obtained in 64 Si atoms periodic supercells within local density functional theory as implement in SIESTA [14]. The exchange-correlation potential is that of Ceperley-Alder [15] as parameterized by Perdew-Zunger [16]. Norm-conserving pseudopotentials in the Kleinman-Bylander form [17] are used to remove the core regions from the calculations. For the Si and Ga atoms, we use double-zeta polarized (DZP) basis sets, and doubled-zeta (DZ) for the B and O atoms. The electronic energies are calculated with a 2×2×2 Monkhorst-Pack [18] mesh. The thermodynamic gap levels of the defects were calculated using C_i as a marker [19].

The dynamical matrices are calculated at $k=0$ using linear response theory [20]. Their eigenvalues allow the construction of phonon densities of state and Helmholtz vibrational free energies [21]. The difference in configurational entropy between a complex {A,B} and its dissociation products A and B is $\Delta S_{config} = (k_B/[\{A,B\}]) \ln(\Omega_{pair}/\Omega_{nopair})$, where Ω_{pair} and Ω_{nopair} are the number of configurations when all the possible complexes form and when all dissociated, respectively. Thus, the binding free energies $E_b = \Delta U + \Delta F_{vib} - T\Delta S_{config}$ depend on T and on the concentrations [A] and [B].

3. Properties of the complexes at T=0K

We tested the symmetrically inequivalent configurations in the 0 and +1 charge states involving B_s or B_i and O_i or $\{O_i\}_2$, and found four structures with comparable binding energies. The reaction of B_s^- and $\{O_i\}_2^{++}$ produces the $\{B_s,O_i,O_i\}^+$ complex (Fig. 1, left), with $E_b = 0.54$eV and (0/+) level at $E_c - 0.45$eV. Adey *et al.* [13] find the O_i atoms to be bound to B_s, a structure we get to be barely stable. Recent calculations by Branz and Zhang [22] confirm our finding. The reaction of B_i^+ and $\{O_i\}^0$ produces the $\{B_i,O_i\}^+$ complex (Fig. 1, right), with $E_b = 0.47$eV and a (0/+) level at $E_c - 0.49$eV (Adey *et al.* [23] predict the same complex but with $E_b=0.6$eV). The experimental estimates for this level are in the range $E_c - 0.23$eV to 0.30eV. Our value is within the error bar of the marker method [19].
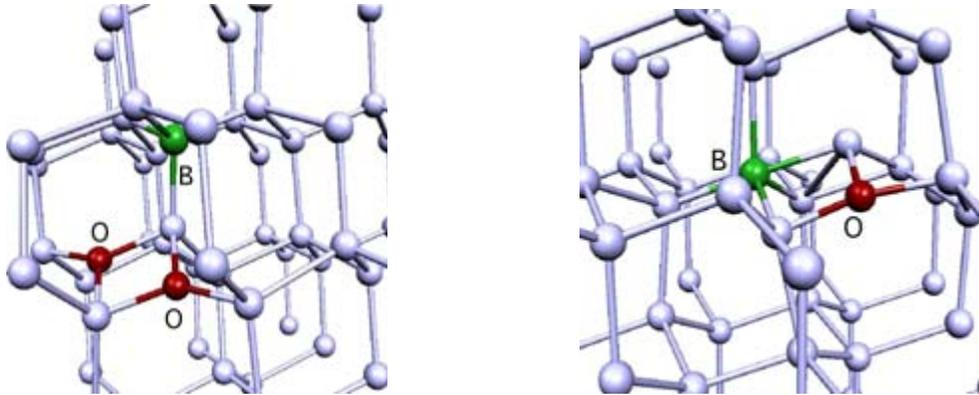

Fig. 1: The {B_s,O_i,O_i}^+ (left) and {B_i,O_i}^+ (right) defects are responsible for the degradation of illuminated (left) and irradiated (right) solar cells.

Finally, the interaction of B_i^+ with $\{O_i\}_2^0$ produces two nearly degenerate $\{B_i,O_i,O_i\}^+$ structures with $E_b=0.55$eV and 0.61eV, and (0/+) levels at $E_c - 0.54$eV and $E_c - 0.48$eV, respectively. Note that the low concentrations of both B_i and $\{O_i\}_2$ in all samples suggest that these two complexes have low formation probability. As will be shown below, both complexes are unstable above room temperature.

4. Stabilities at finite temperature

As discussed in Sec. 2, the total free binding energy of these complexes, consists of the differences of total electronic energy ΔU and Helmholtz vibrational free energy ΔF_{vib} and $T\Delta S_{config}$, where ΔS_{config} is the difference of configurational entropy between the complexes and its dissociation products. The calculation of ΔF_{vib} [21] involves the phonon densities of state which are obtained from the eigenvalues of the dynamical matrices of the cells. The calculation of ΔS_{config} is done analytically from known (or estimated) concentrations of the various defects involved. We start with the following concentrations, in cm^{-3}: $[B_s]=10^{19}$, $[B_i]=10^{14}$, $[O_i]=10^{18}$, $[O_{i2}]=10^{14}$. At low temperatures, we assume that all the possible complexes form, and at high temperatures, all are dissociated, with no dissociation products within a capture radius r_c from each other. When one (or both) component of a complex exist in high concentrations (as is the case for B_s and O_i), there are many configurations for complexes and few configurations for dissociated species. The opposite holds when both components of a complex exist in low concentrations (as is the case of B_i and $\{O_i\}_2$). Because these concentrations vary here from 10^{19} to 10^{14}, the various complexes have vastly different configurational entropies. The numbers for $\{B_s,O_i,O_i\}$, $\{B_i,O_i\}$, and $\{B_i,O_i,O_i\}_{1,2}$ (both of which have the same ΔS_{config}) are 0.515, 0.778, and 1.470 meV/K, respectively. Figure 2 shows $E_b(T)$ for the various complexes. $\{B_i,O_i,O_i\}$ and $\{B_i,O_i\}$ are most stable complexes at room temperature, while both $\{B_i,O_i,O_i\}$ already dissociate.
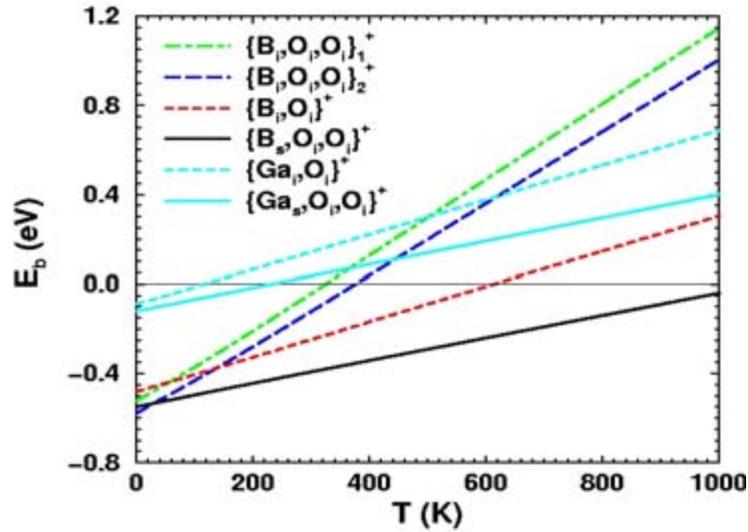
Fig. 2: Binding free energies of the various B-O and Ga-O complexes as a function of T.

We replaced B with Ga in the two most stable structures and obtained very similar structures, but with much smaller binding energies at T=0K: 0.12eV for $\{Ga_s,O_i,O_i\}^+$ and E_b=0.09eV for $\{Ga_i,O_i\}^+$. The Ga-O complexes are marginally stable at very low temperatures but Ga and O repel each other already below 200K. This result is consistent with the experimental observation that none of the O-related lifetime degradation occurs in Ga-doped solar cells.

5. Summary and Discussion

We have calculated from first principles the binding energies and thermodynamic gap levels of B-O and Ga-O complexes in Si. We also calculate their stabilities at finite temperatures. In samples

exposed to light, the $\{B_s, O_i, O_i\}$ complex exhibits all the features expected from the observed lifetime killer. In irradiated samples, where B_i is found, the undesirable defect is $\{B_i, O_i\}$. The calculated binding energies, gap levels, and thermal stabilities are all consistent with the know properties of the lifetime killers. The corresponding Ga-related complexes are all unstable at room temperature. We also find two additional complexes with comparable binding energies (at T=0K), $\{B_i, O_i, O_i\}$, but their binding free energies have a very sharp temperature dependence because they are both made of very low concentration species. They are unstable already at room temperature. Since the defects observed to reduce carrier lifetimes in solar cells form at or above room temperature, we can rule out both $\{B_i, O_i, O_i\}$ complexes as they could only form at much lower temperatures. Finally, we point out that the binding energies of complexes in Si or other crystals vary with the temperature as well as the concentrations of the species involved [24].

References
1. I. Weinberg, S. Mehta, and C. K. Swartz, Appl. Phys. Lett. **44**, 1071 (1984)
2. G.D. Watkins, Phys. Rev. B **12**, 5824 (1975)
3. S. Zhao, A.M. Agrawal, J.L. Benton, G.H. Gilmer, L.C. Kimerling, MRS **442**, 231 (1997)
4. R. D. Harris, J.L. Newton, and G.D. Watkins, Phys. Rev. B **36**, 1094 (1987)
5. P.M. Mooney, L.J. Cheng, M. Süli, J.D. Gerson, and J.W. Corbett, Phys. Rev. B **15**, 3836 (1977).
6. H. Matsura, Y. Uchida, N. Nagai, T. Hisamatsu, T. Aburaya, and S. Matsuda, Appl. Phys. Lett. **76**, 2092 (2000)
7. M. Tajima, M. Warashina, and T. Hisamatsu, Proc. 14th workshop on Crystalline Silicon Solar Cells and Modules, ed. B.L. Sopori (NREL/BK-520-36622, Golden, CO 2004), pp. 27-34.
8. *Oxygen in silicon*, ed. F. Shimura, Semiconductors and Semimetals, vol. **42** (1994)
9. J. Schmidt and K. Bothe, Phys. Rev. B **69**, 024107 (2004)
10. S. Rein and S.W.Glunz, Appl. Phys. Lett. **82**, 1054 (2003)
11. K. Bothe, R. Hezel, and J. Schmidt, Appl. Phys. Lett. **83**, 1125 (2003)
12. S.W. Glunz, S. Rein, and J. Knobloch, Proc. 16th European Photovoltaic Solar Energy Conf. (WIP-ETA, Munich, 2000), p.1.
13. J. Adey, R. Jones, D.W. Palmer, P.R. Briddon, and S. Öberg, Phys. Rev. Lett. **93**, 055504 (2004).
14. D. Sánchez-Portal, P. Ordejón, E. Artacho, and J.M. Soler, Int. J. Quant. Chem. **65**, 453 (1997); E. Artacho, D. Sánchez-Portal, P. Ordejón, A. García, J.M. Soler, Phys. Stat. Sol. (b) **215**, 809 (1999).
15. D.M. Ceperley and B.J. Alder, Phys. Rev. Lett. **45**, 566 (1980)
16. S. Perdew and A. Zunger, Phys. Rev. B **32**, 5048 (1981)
17. L. Kleiman and D.M. Bylander, Phys. Rev. Lett. **48**, 1425 (1982)
18. H.J. Monkhorst and J.D. Pack, Phys. Rev. B **13**, 5188 (1976)
19. J. Coutinho, V.J.B. Torres, R. Jones, and P.R. Briddon, Phys. Rev. B **67**, 035205 (2003)
20. X. Gonze, Phys. Rev. A **52**, 1096 (1995); X. Gonze and C. Lee, Phys. Rev. B **55**, 10355 (1997)
21. S.K. Estreicher, M. Sanati, D. West, and F. Ruymgaart, Phys. Rev. B **70**, 125209 (2004)
22. H. Branz and S. Zhang, private communication.
23. J. Adey, R. Jones, P.R. Briddon, and J.P. Goss, J. Phys.: Condens. Matter **15**, S2851 (2003); J. Adey, R. Jones, and P.R. Briddon, Appl. Phys. Lett. **83**, 665 (2003)
24. M. Sanati and S.K. Estreicher, submitted to Phys. Rev. B.

Photoluminescence: A versatile characterization technique for crystalline silicon

T. Trupke and R.A. Bardos

Centre of Excellence for Advanced Silicon Photovoltaics and Photonics,
The University of New South Wales, Sydney, NSW, 2052, Australia,
Telephone: +61 02 9385 4054, Facsimile: +61 02 9662 4240,
E-mail : thorsten@trupke.de

Introduction

Silicon wafers to be used in photovoltaic applications can generally be expected to be relatively poor light emitters with luminescence quantum efficiencies of typically $<<10^{-4}$. At first sight photoluminescence (PL) experiments on silicon therefore do not appear to be the method of choice, when it comes to sensitive measurements of material properties such as the injection level dependent effective minority carrier lifetime $\tau_{eff}(\Delta n)$. This may be one reason why quantitative analyses of PL measurements have not been too numerous in photovoltaics research in the past[1,2].

Here we review our recent PL related experimental work in which we have shown that: 1.) PL can be a surprisingly sensitive lifetime technique. 2.) PL is insensitive to various experimental artifacts that affect other techniques such as microwave reflection or photoconductance. 3.) The Suns-PL technique is discussed, which is a contactless counterpart to Suns-V_{OC} measurements and which allows the contactless determination of implied IV curves on unfinished cells. 4.) A recently introduced self consistent calibration method is described that can be applied to PL but also to other techniques.

Theory

One important characteristics of PL is that the measured signal I_{PL} is given as the *product* of minority and majority carrier densities

$$I_{PL} = B \cdot n_e \cdot n_h \approx B \cdot \Delta n \cdot (N_D + \Delta n), \quad (1)$$

whereas in other techniques the measured signal is determined by the *sum*. In Eq.1 B is the radiative recombination coefficient, N_D is the doping concentration and n_e and n_h are the electron and hole concentrations, respectively. With $n_e*n_h = n_i^2*\exp(\Delta\eta/kT)$ the PL intensity can also be expressed as a function of the separation of the quasi Fermi energies $\Delta\eta$

$$I_{PL} = B \cdot n_i^2 \cdot \exp(\Delta\eta / kT). \quad (2)$$

The quantitative relation between the PL signal and the excess minority carrier concentration Δn expressed in Eq.1 is the basis of PL lifetime measurements. The relation between the PL signal and $\Delta\eta$ (which is equivalent to an implied voltage) is the basis for reliably determining implied voltages from PL. The direct correlation between the PL signal and an implied voltage, is also the reason why PL is very robust against various experimental artifacts as discussed below.

Sensitivity of PL lifetime measurements

Fig.1 (data taken from Ref.3) shows results from quasi steady state (QSS) injection level dependent PL and photoconductance (PC) lifetime measurements on a 260µm thick 1 Ωcm p-type wafer with a phosphorous diffusion on both sides.
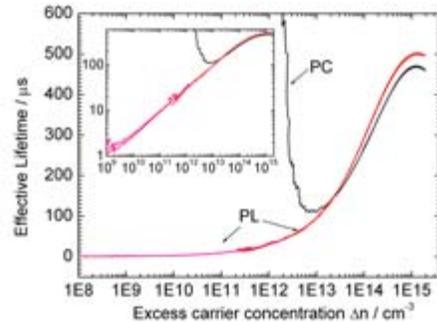

Fig.1 Effective lifetime from PL (red and pink) and from PC (black) for a 1 Ωcm p-type wafer with phosphorous diffusions on both sides.

These measurements were taken with a very sensitive combined PL and PC setup that is described in some detail elsewhere[3]. Good quantitative agreement is observed between PL and PC at injection levels > 10^{13} cm^{-3}, showing that QSS-PL measurements can indeed be used for quantitative injection level dependent lifetime measurements. Fig.1 also shows

that in PL the effective lifetime could be measured down to very small excess carrier concentrations <10^9 cm^{-3}, which is two or three orders of magnitude below the detection limit of typical PC set ups. In our current experimental set up this somewhat unexpected sensitivity is reached in a scan that only takes a few seconds. Reaching such extremely low injection levels may not be of major interest in itself but these measurements clearly show that more relevant injection ranges can be accessed very accurately and quickly with PL. For the Suns-PL technique to be discussed below, the high sensitivity of PL results in a much wider range of implied voltages that can be determined than from any other technique.

Fig.1 also shows that PL lifetime measurements can be used to determine fairly low effective lifetimes. The lowest lifetime detectable with our setup is limited by the light intensity achievable with the LED array that is currently used for illumination and the lowest detectable PL signal. We estimate that in quasi steady state mode lifetimes on the order of τ=1 ns should be detectable with PL.

Reduced sensitivity to experimental artifacts

The effects of excess carriers accumulated in space charge regions (so called DRM effects) have recently been shown to create dramatic artificial effects on the effective lifetime in PC measurements especially at small injection levels[4,5]. Another effect that can cause artificially high apparent lifetimes in PC measurements is minority carrier tapping[6,7]. In both cases additional *free* charge carriers (majorities *and* minorities in the case of the DRM effect and only majorities in the case of trapping) are stored within the sample, which contribute to the measured signal in all experimental techniques which are linear in the *sum* of minority and majority carrier concentrations. Those carriers however, have no direct correlation with the actual free minority carrier concentration to be measured and therefore lead to an erroneous assignment of the effective lifetime. In contrast theoretical modeling[8] reveals that PL measurements should be unaffected by DRM effects, because the separation of the quasi Fermi energies can be almost constant throughout a device even in the presence of space charge regions.

The predicted insensitivity of PL against DRM effects is demonstrated experimentally in Fig.1. The PC lifetime measurement on the phosphorous doped sample (the one for which DRM effects are theoretically predicted) shows a strong and unrealistic increase of the effective lifetime at small injection levels. This increase could clearly be assigned to the

DRM effect as it was not observed on an otherwise identical p-type wafer that had a boron diffusion (hilo junction) on both sides[3]. In contrast to the PC measurement the PL measurement on the phosphorous sample is unaffected by the DRM effect (Fig.1).

The question of the sensitivity of QSS-PL measurements to artifacts resulting from minority carrier trapping is addressed in detail experimentally and theoretically elsewhere[9].

Temperature variations are another potential source of inaccuracies in PC measurements. The problem here is that especially in samples of moderate or poor quality high light intensities are used to create small excess carrier concentrations. Resulting temperature variations, can affect not only the effective lifetime itself, but more importantly the dark conductivity via a temperature dependence of the dark carrier concentrations *and* of the mobilities. The small variation of the conductivity due to the light induced excess carrier concentrations, which is supposed to be measured, can then completely be obscured even by comparatively moderate relative variations in the much larger dark conductivity. Our experimental data indicate that PL is more robust against temperature variations, which is expected since the temperature dependence of the radiative recombination coefficient B(T) becomes very weak around room temperature. An interpolation of recently published data[10] for B(T) indicates that a temperature variation from T=290K to T=300K only results in a relative variation of B(T) of ~3%. Consequently only relatively marginal variations of the PL signal are expected due to temperature variations under typical illumination intensities.

This insensitivity of PL against various experimental artifacts is particularly advantageous at low carrier densities, where the influence on PC measurements is most pronounced. This is a crucial aspect to be considered for experimental work e.g. in advanced lifetime spectroscopy techniques such as temperature and injection level dependent lifetime spectroscopy (TIDLS)[11] which critically depend on the analysis of the lifetime at low carrier densities.

Suns-PL: Contactless measurement of IV curves

According to Eq.2 the PL signal is directly linked to $\Delta\eta$ and can thus be interpreted as an implied voltage. PL measurements in combination with measurements of the incident light intensity can therefore in principle be utilized to predict the IV-characteristics in analogy to Suns-V$_{OC}$ measure-

ments[12] but with the advantage that no electrical contacts, not even a solar cell structure are required.
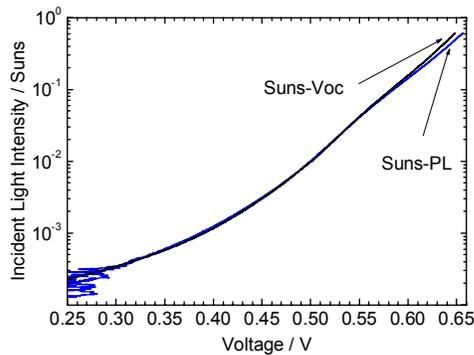

Fig.2 Sun-V_{OC} and Suns-PL curve (see text) of a bifacial double sided buried contact solar cell.

The idea to determine implied IV curves from PL is not new[13] but has only recently been demonstrated experimentally over a wide range of incident light intensities and open circuit voltages[14]. Simultaneous measurements of the open circuit voltage, the PL intensity and the incident light intensity were carried out on bifacial buried contact silicon solar cells. Fig.2 shows the resulting Suns-V_{OC} (incident light intensity as a function of the open circuit voltage) and Suns-PL curves (incident light intensity as a function of the logarithm of the PL signal), which quantitatively agree very well (data from Ref.14). The small deviations of up to 7 mV at large currents are assigned to resistive losses that occur within a solar cell even under open circuit conditions, for instance when carriers flow on a resistive path towards shaded areas under metal fingers[15]. The PL technique is more resistant against such effects, because the voltage is only reduced in the immediate vicinity of the metal contact. The PL signal is thus only affected in proportion of that affected area to the total area of the cell from which PL is collected.

Fig.3 shows the applicability of the Suns-PL technique to non-contactable silicon wafers (data from Ref.14). Here a p-type silicon wafer was measured after various processing steps towards a bifacial buried contact solar cell, i.e. a) after emitter diffusion, b) after laser scribing a contact pattern on the rear surface, c) after cleaving the edges of the cell, d) after scratching the front surface. These measurements which are discussed in more detail elsewhere[14], clearly highlight a major advantage of the Suns-PL technique, i.e. the possibility to measure the implied IV curve over a wide range of voltages after each processing step. This certainly allows the influence of individual processing steps on the material quality to be moni-

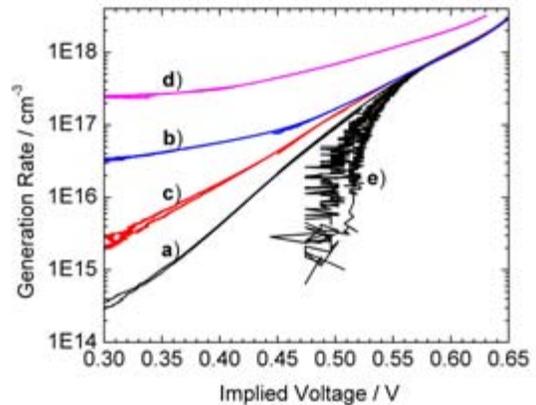tored and consequently these processing steps to be optimized more reliably and effectively.

Fig.3 Suns-PL curves of a silicon wafer after various processing steps (a-d) and implied IV curve from PC data (e) measured after step a).

Implied IV curves can also be determined in contact less mode from PC measurements. However, this method is strictly limited to carrier concentrations at which trapping or DRM effects have only a marginal influence. In many relevant cases this can be a serious restriction. Curve e) in Fig.3 represents the implied IV curve resulting from a QSS-PC measurement (taken after emitter diffusion), which shows that the data below 550mV are strongly affected by DRM effects. Even in the absence of those artifacts the measurement of implied IV curves from PC data becomes very difficult at implied voltages <450 mV because the corresponding excess carrier concentrations are very small. The high sensitivity of PL is a big advantage in this context.

Calibration of PL

The calibration of a relative PL signal is an essential step in PL lifetime measurements and in the Suns-PL technique. In previous work this calibration was carried out by comparison of a PL measurement with a calibrated PC measurement taken under identical illumination conditions and at large injection conditions where the above mentioned experimental artifacts are expected to be insignificant. However, we recently also described a self consistent calibration method[16], which is not only potentially more accurate but also allows PL measurements to be
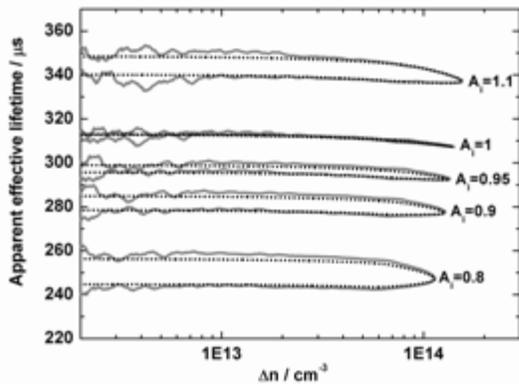
Fig.4: Theoretical (dotted) and experimental (solid) lifetime data with hysteresis effects for inaccurate choice of the calibration factor A_i.

calibrated without any separate technique for calibration. The method is based on the generalized analysis described by Nagel et al.[17] and is very similar to a method for calibrating the generation rate that we have described earlier[18]. Fig.4 shows how the calibration method works (data from Ref.16). A temporal light intensity profile with a rising and a falling branch is used for excitation. Hysteresis effects in the experimental and theoretical injection level dependent lifetime curves result from a wrong calibration of the PL signal. Minimization of such hysteresis effects by variation of a calibration constant A_i (Fig.4) allows PL or PC lifetime measurements to be calibrated.

Conclusions

PL is an unexpectedly sensitive technique that can be used for quantitative characterization of silicon wafers. It allows the contact less measurement of the injection level dependent effective lifetime and of implied IV curves and is unaffected by various experimental artifacts that affect other techniques especially at low excess carrier concentrations. With a recently introduced self consistent calibration method PL can be carried out in a self contained way without the previous need for a separate calibration technique. The advantages of PL measurements over conventional lifetime techniques discussed above also applies to *spatially resolved* PL measurements, giving a significant advantage over other spatially resolved techniques such as Carrier Density Imaging (CDI)[19,20] A

practical problem with PL measurements is the requirement of high intensity monochromatic illumination over a large area. The continuous improvement of solid state light sources such as lasers and light emitting diode arrays will provide solutions to this problem. In summary we believe that given the advantages and possibilities outlined here, PL is a powerful technique, which should be used more widely for silicon characterization in photovoltaics research.

References

[1] G. H. Bauer, R. Brüggemann, I. A. S. Al-Mohtad, et al. , 29th IEEE PVSC, 1278-1281 (2002).

[2] S. Tardon, R. Brüggemann, M. Rösch, et al., 20th EPVSC, Barcelona, Spain, 2005.

[3] T. Trupke and R. Bardos, 31st IEEE PVSC, Orlando, USA (2005).

[4] P.J. Cousins, D.H. Neuhaus, and J.E. Cotter, J. Appl. Phys. **95** (4), 1854-1858 (2004).

[5] M. Bail, M. Schulz, and R. Brendel, Appl. Phys. Lett. **82** (5), 757-759 (2003).

[6] D. Macdonald and A. Cuevas, Appl. Phys. Lett. **74** (12), 1710-1712 (1999).

[7] J. Schmidt, K. Bothe, and R. Hezel, Appl. Phys. Lett. **80** (23), 4395-4397 (2002).

[8] T. Trupke, R.A. Bardos, F. Hudert, et al., 19th EPVSC, Paris, France (2004).

[9] R.A. Bardos, T. Trupke, and D. Macdonald, Manuscript in preparation.

[10] T. Trupke, M. A. Green, P. Würfel et al., J. Appl. Phys. **94** (8), 4930-4937 (2003).

[11] S. Rein, S. Diez, and S.W. Glunz, presented at the 19th EPVSC, Paris, France, 2004.

[12] R.A. Sinton and A. Cuevas, 16th EPVSC, Glasgow, United Kingdom, 1152 (2000).

[13] G. Smestad and H. Ries, Sol. Energy Mater. Sol. Cells **25**, 51-71 (1992).

[14] T. Trupke, R.A. Bardos, M.D Abbott, and J.E. Cotter, Appl. Phys. Lett. (submitted 2005).

[15] N.-P. Harder, A. B. Sproul, T. Brammer, and A. G. Aberle, J. Appl. Phys. **94** (4), 2473-2479 (2003).

[16] T. Trupke, R.A. Bardos, and M.D. Abbott, Applied Physics Letters (submitted) (2005).

[17] H. Nagel, C. Berge, and A.G. Aberle, J. Appl. Phys. **86** (11), 6218-6221 (1999).

[18] T. Trupke and R. A. Bardos, Appl. Phys. Lett. **85** (16), 3611-3613 (2004).

[19] S. Riepe, J. Isenberg, C. Ballif, S.W. Glunz, and W. Warta, 17th EPVSC, Munich, Germany (2001).

[20] M. C. Schubert, J. Isenberg, and W. Warta, J. Appl. Phys. **94** (6), 4139-4143 (2003).

Silicon PV Technology at a Crossroad?

Bolko von Roedern
NREL, Thin Film Partnership
Golden, CO 80401-3393
(303) 384-6480
Bolko_von_Roedern@nrel.gov

All too often, the commercial success and growth of the Si PV industry is taken as an excuse to consider the PV industry a single, monolithic, crystalline Si technology. Looking at the detailed challenges, I believe that Si PV technology is actually at a crossroad. While much investment recently went into scaling up cast-ingot multicrystalline cell manufacture, I argue that in a manufacturing environment high efficiency cell schemes can only be realized using high-quality single crystal wafers, combined with "localized" or "HIT" ("alternative") junction schemes. Conversely, alternative junction schemes will not pay for themselves when used in conjunction with typical multicrystalline Si wafers. With most investment presently made to produce cast-ingot multicrystalline wafers, efficiency expectations (<17% commercial cells, <14.5% efficient commercial modules) have to be tempered. For higher commercial efficiencies (>20% cells, >17% efficient modules), a switch to high-lifetime single-crystal wafers and simultaneously using alternative junction schemes will become a requirement. The latter approach will require substantial new manufacturing capacity for high-lifetime single-crystal ingots and wafers. An argument is made that technological advance is also hampered by inadequate understanding of cell performance and often incorrect identification of factors used to account for "less than ideal" cell behavior.

Introduction

This paper relies heavily on the recently published quantitative analyses by R.M. Swanson et al. [1, 2] who analyzed the losses between theoretical possible efficiencies for Si (31 to 32% range) and the best laboratory and commercial champion cells [1], and in reference 2, reconciles how to increase current "average" commercial cell efficiencies values, presently at 14.7%, to >20% efficient mass-produced cells. The data from Ref. 2 are reproduced in Table 1. It is of great interest to analyze the data in Table 1 to deduce actual manufacturing requirements. As discussed in Ref. 2, Table 1 reveals that the factors enhancing current commercial performance (or, conversely, reducing actual performance below some theoretical or laboratory champion performance) are very *interactive*. This means that traditional methods of analyzing solar cells and attempting to separate losses are introducing fundamental errors by neglecting such interactions. For example, the losses attributable to the emitter and collector in screen-printed cells (line #3,4,5,6) cause approximately 2% efficiency gain, but when combined with high lifetime (line 9 in Table 1) the commercial efficiency will exceed 20% (more than twice the benefit!). Conversely, as is evident from line 2 of Table 1, using a higher-lifetime base (wafer) will barely affect the efficiency of a conventional (diffused full-surface emitter and collector with screen printed contacts) $n^{+}/p^{-}/p^{+}$ cell. I believe that Table 1 provides a meaningful and correct analysis of the real-world situation.

Table 1: Requirements for Higher-Efficiency Commercial Solar Cells.

| Line	Material or Device Enhancement Measure	Commercial cell eff. (%)
1	"Conventional" Silicon Cell	14.7
2	High Lifetime Base	14.8
3	Back Surface Field (BSF)	15.6
4	Rear Local Contacts (RLC)	16.5
5	Passivated Emitter (PE)	16.8
6	Selective Emitter (SE)	17.1
7	BSF + PE	18.3
8	SE + RLC	19.7
9	High Lifetime + SE + RCL	21.2

However, the Si wafer PV community has not yet clearly spelled out the consequences. "Conventional" cells will benefit little from higher-quality wafers and marginally from new contacting schemes. Thus, wafer Si PV is at a crossroad, both high-lifetime single crystal wafers and new contacting schemes are needed to achieve commercial cell efficiency >20%. Without such, efficiency progress can only be expected in slow, incremental steps, with commercial efficiencies saturating well below 20%. As the majority of investment into wafer Si PV is presently made to gear up for increased multicrystalline Si ('cast ingot) manufacturing, this poses the question where the large volumes of high-lifetime, single-crystal Si would come from to allow Si PV technology to transition to higher commercial efficiencies. In a recent assessment, we have concluded that the present "2nd-generation" thin-film PV technologies are capable of competing (in terms of $/W$_p$) with both the "conventional" and the high-efficiency wafer-Si PV schemes [3].

The Lifetime Story Revisited

The quantitative correctness of Table 1 both defines the need for future high efficiency commercial solar cells and at the same time challenges the understanding of the factors controlling cell performance. In the following, I will develop a simple picture explaining the commonly observed correlations of lifetime with solar cell parameters. Such correlations are ubiquitously observed, but certainly a single lifetime parameter is not good enough to predict a solar cell parameter (see Table 1, line 2) unless much more important detail is known about the solar cell, e.g., how emitters and collectors are fabricated, the thickness of the absorber, the wafer material type ("ribbon" versus multicrystalline versus single-crystalline wafers). A simple concept is depicted in Figure 1. I believe that a very good simple approximation of any solar cell is to assume that the splitting of the quasi-Fermi-levels ($E_{fn} - E_{fp}$) is not controlled by the defects within the base of the cell, but rather by the "pressure" p that is exerted from the emitter and collector onto the quasi-Fermi-levels inside the base, forcing a smaller splitting.

Experimentally, very good correlation of lifetime (τ, or the inverse of the recombination rate, 1/R) with the solar cell open-circuit voltage has been reported [4]. Traditionally, it
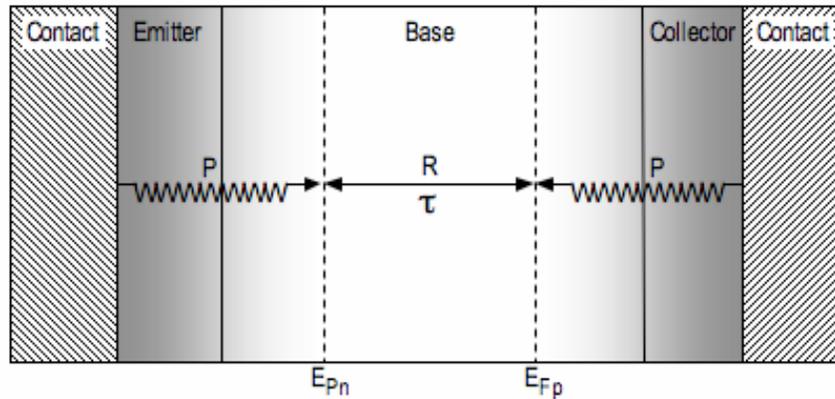
Fig. 1: Schematic of factors determining Solar Cell Voltage and Recombination

has been assumed that defects and impurities in the absorber layer control τ or R. For many years, a major topic of this workshop has been that solar cell processing (i.e., the emitter and collector processing) can increase both wafer lifetime and cell performance. This effect has been dubbed "defect engineering" by the crystalline silicon community.

Accepting Fig. 1 as a working hypothesis not only explains why lifetime and voltage are proportional, but also explains why there is no single lifetime value predicting V_{OC} [5]. The surprising realization is that to prepare cells with high voltage, one has to make the contact less "intimate," so that the "pressure" p from the emitter and collector on the quasi-Fermi-level split is reduced (physically, p accounts for the effects of the contacts reducing the minority-carrier concentration m(x), as described in Ref. 7). Simple fundamental calculations support the conclusion that the less-conductive contacts will separate the contacts as much as possible separated from the cell's base [6,7]. In practice, this is done by lower collector and emitter doping (in Sanyo's HIT cell, the amorphous emitter and collector is many orders of magnitude more resistive than in a "conventional" cell). In recent years, commercial Si has transitioned from mere antireflection coatings to "fire-through" SiN_x:H contacts that increase V_{OC}. It is often postulated that SiN_x:H passivates the Si base, but similar voltage enhancement is observed for all types of Si substrates (ribbon, multicrystalline, and single-crystalline), regardless of any specific defects or impurities, creating suspicion that it may not be a simple passivation mechanism. Localizing the contacts (buried grids, point contacts) is an obvious way to decrease the p. I have previously argued that the strong experimental correlation between V_{OC} and the B-doping level in a "conventional" cell originates from the requirement of forming a high resistivity, compensated buffer layer between the emitter and the base to increase V_{OC} [7,8]. In a "conventional" cell, the free hole concentration cannot be the driver for higher V_{OC}. In other cell schemes (point contact, buried grid, "HIT") lower doping levels of the base are required to nevertheless achieve higher V_{OC} levels than possible in conventional cells. In fact, a recent theoretical analysis predicts highest Si cell performance for thin (90 μm-thick) bases that are intrinsic, as should be expected [9]. In thin film solar cells, "buffers" are commonly employed to enhance V_{OC} and it has been pointed out that their benefit cannot be quantitatively accounted for in terms of bulk lifetimes and surface recombination rates [10].

The Sanyo group has been unable to explain the temperature dependence of V_{OC} in their HIT cells [4]. It may simply be impossible to explain the temperature dependence of a cell in terms of the temperature dependence of bandgap and τ or R, because it could rather be determined by the temperature dependence of p. This explains the results of Fig. 5 in Ref. 4. In higher-voltage cells, p is lower which should generally lower the increase of p with temperature. In the highest voltage HIT cells from Sanyo, the T coefficient is better than -0.25 %/^{o}C. This coefficient is very similar to that of amorphous Si solar cells, and a direct result of the temperature-dependence of the properties of the amorphous p, n, and thin i-layer buffers. Conventional theory has clearly failed to predict correctly the temperature dependence of V_{OC} and its dependence on V_{OC}.

Conclusion

In agreement with Swanson [1], I argue that V_{OC} of solar cells and ultimate efficiencies attainable are dominated by cell "contacting" problems. The low dark recombination rates (characterized in terms of J_o) are usually (but not always) observed in cells with V_{OC} > ~680 mV. While traditional cell theory assumes that such recombination would be controlled by the defects in the base, I instead suggest that the quasi-Fermi-level splitting that is usually dominated by the contacts controls it. As stated in Ref. 6, recombination occurs to the degree that it is allowed to happen; it is not a fundamental factor in control of cell parameters. Defect engineering may not always entail a change in the nature of the defects in the base, but could rather result from lifetime changes due to reduced or enhanced splitting of the quasi-Fermi-levels.

[1] R. M. Swanson, Proc. 31st IEEE PV Specialists Conf. (2005), 889
[2] W.P. Mulligan and R.M. Swanson, Proc. 13th Workshop on Crystalline Silicon Solar Cell Materials and Processes, NREL/BK-520-34443 (2003), 30.
[3] B. von Roedern, Ken Zweibel, and Harin S. Ullal, Proc. 31st IEEE PV Specialists Conf. (2005), 183.
[4] M. Taguchi, H. Sakata, Y. Yoshimine, E. Maruyama, A. Terakawa, M. Tanaka, and S. Kiyama, Proc. 31st IEEE PV Specialists Conf. (2005), 866.
[5] The data of Fig. 7 in Ref. 4 extrapolate to 0.59 V for $\tau=0$, suggesting that low lifetimes could not account for common experimental V_{OC} values <0.59V.
[6] B. von Roedern, Photovoltaic Materials, Physics of, Elsevier Encyclopedia of Energy, Vol. 5 (2004), 47.
[7] B. von Roedern and G.H. Bauer, Proc. 9th Workshop on Crystalline Silicon Solar Cell Materials and Processes, NREL/BK-520-26491 (1999), 219.
[8] B. von Roedern, Proc. 14th Workshop on Crystalline Silicon Solar Cells & Modules: Materials and Processes, NREL/BK-520-36622 (2004), 234.
[9] M.J. Kerr, P. Campbell, and A. Cuevas, Proc. 29th IEEE PV Specialists Conf. (2002), 438.
[10] L.C. Olsen, H. Aguilar, F.W. Addis, W. Lei, and J. Li, Proc. 25th IEEE PV Specialists Conf. (1996), 997.

Progress in the Use of Hot-Wire CVD a-Si:H as Emitters and Collectors in Silicon Heterojunction Solar Cells

T.H. Wang, M.R. Page, E. Iwaniczko, Y. Xu, Q. Wang, Y. Yan, D. Levi,
V. Yelundur*, L. Roybal, R. Bauer, A. Rohatgi*, H.M. Branz
National Renewable Energy Laboratory, 1617 Cole Blvd., Golden, CO 80401
*Georgia Institute of Technology, 777 Atlantic Dr., Atlanta, GA 30332

ABSTRACT: Thin hydrogenated amorphous silicon (a-Si:H) layers deposited by hot-wire chemical vapor deposition (HWCVD) are used as both emitters and collectors in silicon heterojunction solar cells. Low interface recombination velocity and high open-circuit voltage are achieved by a low substrate temperature (<150°C) intrinsic a-Si:H deposition which ensures immediate amorphous silicon deposition. This is followed by deposition of doped a-Si:H at a higher temperature (>200°C) which improves dopant activation and other properties. With an a-Si:H emitter only, we obtain efficiency of 17% and an open-circuit voltage of 652 mV on planar p-type float-zone (FZ) silicon with a screen-printed aluminum back-surface-field (Al-BSF) and contact. Employing a-Si:H as both the front emitter and the back collector, we achieve an open-circuit voltage of 691 mV on planar n-type FZ-Si and 660 mV on textured p-type FZ-Si. These results indicate that a-Si:H provides excellent passivation on the front and an effective back-surface field on the rear.

The silicon heterojunction (SHJ) solar cell is one of the most attractive device structures for fabrication of high-efficiency silicon solar cells at low temperatures (<250ºC) with simple processing. The excellent surface passivation provided by H and extra band bending owing to the larger band gap of a-Si:H compared to c-Si makes a-Si:H (doped oppositely to the base wafer) a superior to the conventional emitters made by dopant diffusion. In contrast to a diffused emitter, no additional surface passivation layer is needed on top of the SHJ. Furthermore, a thin layer of a-Si:H (doped the same as the base wafer) provides a back collector with very effective back-surface field to reduce the recombination velocity. The current conduction through the a-Si:H collector is adequate and no localized current conduction windows are needed, as opposed to the dielectric back-surface passivation layers. These outstanding properties open the path to many hybrid a-Si/c-Si heterojunction silicon solar cell designs, the most successful being the Sanyo HIT cells [1] employing plasma-enhanced chemical vapor deposition (PECVD) to deposit p/i- and n/i-a-Si:H thin layers.

Great care must be taken in using PECVD to make high-efficiency SHJ cells because of the potential plasma damage to the c-Si wafer surfaces. At NREL, hot-wire chemical vapor deposition (HWCVD) is used to eliminate the possibility of such ion damage. Open-circuit voltage (V_{oc}) and the interface-recombination velocity (S) are the key indicators of the a-Si:H/c-Si heterointerface quality. Our work attempts to contribute to both the technological development of high-efficiency silicon heterojunction solar cells and the fundamental understanding of the a-Si:H/c-Si interface; therefore, we study both finished solar cells for complete device characterizations and as-deposited ITO/a-Si:H/c-Si/a-Si:H dot structures for evaluation of V_{oc} and S. High-resolution transmission electron microscopy (HRTEM) and real-time spectroscopic ellipsometry (RTSE) are used to diagnose materials and to monitor layer growth.

Single-heterojunction SHJ solar cells – the a-Si:H emitter

We use the single-heterojunction SHJ solar cell structure shown in figure 1 to optimize the a-Si:H emitter. In a typical a-Si:H/c-Si heterojunction solar cell, a thin (~5 nm) intrinsic hydrogenated a-Si:H layer is interposed between the base wafer and the heavily doped emitter. Though such thin i-layers are difficult to characterize, i-layers likely have a far lower density of defects and possibly a slightly larger energy gap than doped a-Si:H layers; both factors are advantageous for reducing dark current through the junction and increasing V_{oc}. If inadvertent epitaxy occurs during the i-layer deposition, or even extends through the i-layer, the rough c-Si interface will be contacted in places by the doped a-Si:H which is likely a less effective passivant than the i-layer. Any dark-current path through inadequately passivated interface states in a heterojunction solar cell reduces the open-circuit voltage (V_{oc}). Using HWCVD, we vary both the i- and n-layer deposition temperatures to find the optimum conditions. As shown in Figure 2, high V_{oc} values with Czochralski (CZ) silicon are obtained at temperatures below 150°C whereas at temperatures higher than 200°C, V_{oc} is much reduced. The reason for this is that epitaxy usually is favored at i-layer deposition temperature > 200°C while lower temperature (<150°C) ensures abrupt a-Si:H deposition [2].
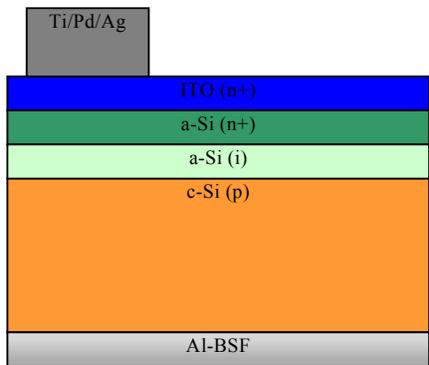

**Fig. 1.** Single-heterojunction solar cell structure
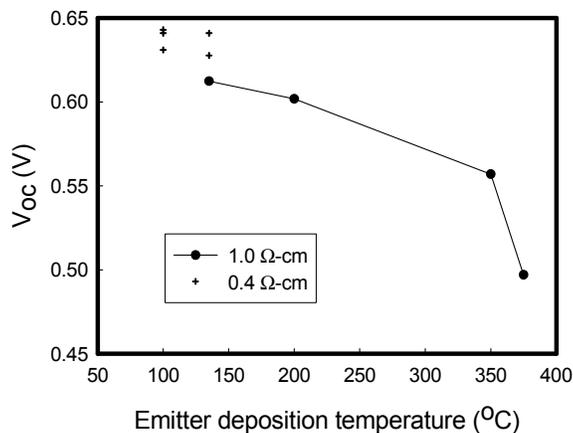
Fig. 2. V_{oc} on CZ-Si vs. i- and n-layer deposition

With an i-layer deposited at a low temperature of 100°C, we find that raising the n-layer deposition temperature to about 200°C provides the highest V_{oc} (see figure 3). This seems to provide effective activation of the phosphorous dopant and a better quality n-layer. Higher doping leads to increased band bending that should contribute to interface passivation by repelling majority holes from the interface and by increasing electron-tunneling rates through any conduction band offset.

The benefit of the abrupt 100°C interface is also shown in interface recombination velocity, *S*. Figure 3 shows *S* as a function of i-layer deposition temperature while the n-layer temperature was fixed at 225°C to activate the n-layer dopants. Not surprisingly, reducing the i-layer temperature lowers *S* as Si epitaxy is suppressed. These optimizations on the a-Si:H emitter lead to 17% efficient single-side SHJ solar cells as shown in Table 1, which includes devices on both FZ- and CZ-Si wafers. Note that all devices shown in Table 1 are non-textured.
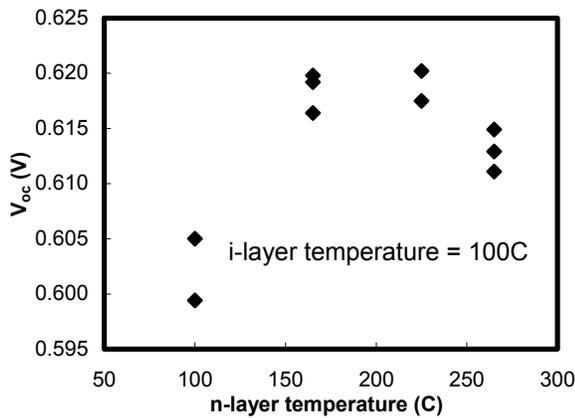
Fig. 3. V_{oc} on CZ-Si vs. n-layer temperature
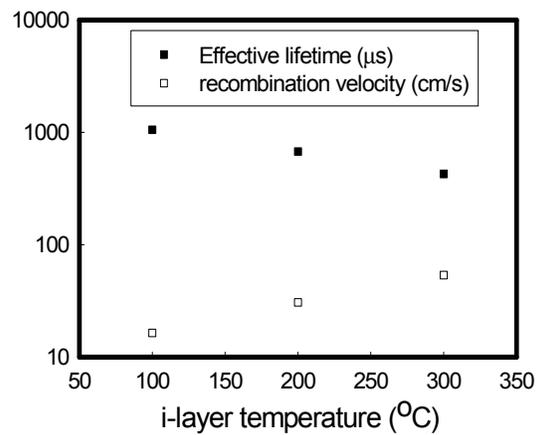
Fig. 4. i-layer temperature effect on passivation

Table 1. 1-cm^2 ITO/a-Si:H/c-Si/Al-BSF single-side SHJ solar cells on planar p-type c-Si substrates

ID	V_{oc}(V)	J_{sc}(mA/cm^2)	F.F.(%)	Eff.(%)	Substrate
16C	0.645	33.11	79.2	16.9	1.0 Ω·cm FZ
16B	0.640	33.55	79.4	17.1	1.0 Ω·cm FZ
65C	0.652	32.16	80.5	16.9	0.5 Ω·cm FZ
08C	0.636	30.15	79.5	15.3	0.4 Ω·cm CZ
06B	0.604	31.66	78.9	15.1	2.0 Ω·cm CZ

Double-heterojunction SHJ – the a-Si:H collector's back-surface field (BSF) effect

Applying the best emitter a-Si:H deposition conditions to the back side collector passivation, we have fabricated the simple double-heterojunction SHJ solar cell depicted in figure 4. Because neither front metal grid nor edge isolation has yet been applied, the J_{sc} and fill factor numbers are approximate, but this preliminary V_{oc} measurement should be quite accurate. Test of solar cell structures with metal contacts on both front and rear will be completed soon.

To illustrate the effectiveness of using a-Si:H as the collector, we completed two devices on n-type silicon substrates with the same front emitter structure of ITO/a-Si(p). On the back side, we then deposited a-Si(n)/a-Si(i)/ITO on one sample but only ITO on the other. The a-Si(n/i) collector enhanced V_{oc} by more than 75 mV compared to the ITO contact.

On textured 1.3 Ω·cm p-type FZ-Si, with an a-Si:H(i/p) collector and a-Si(i/n) emitter, a V_{oc} of 660 mV is obtained (figure 5). Shown also in figure 5 is the I-V curve of a similar device but with Al-
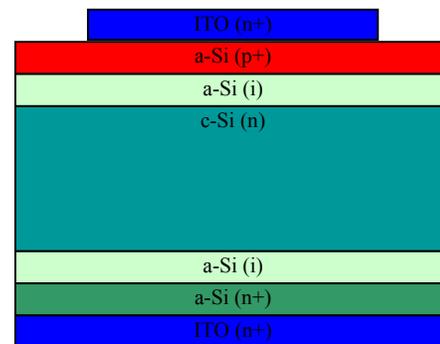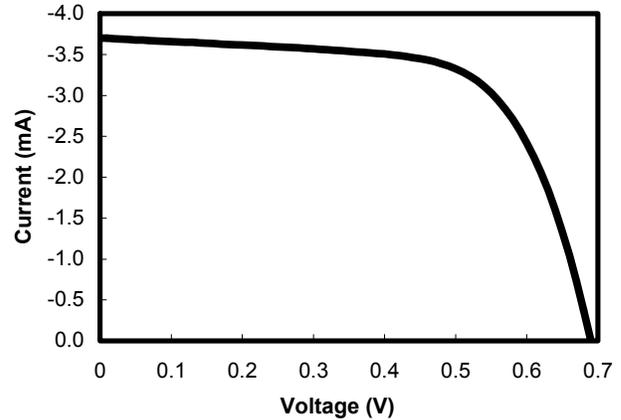

Fig. 4. Double-heterojunction SHJ schematic

BSF as the back contact. Clearly, a-Si:H(i/p) contributes a stronger back-surface field than Al without introducing problems in current collection. On planar 2.0 Ω·cm n-type FZ-Si, we employed an ITO/a-Si(p/i)/c-Si(n)/a-Si(i/n)/ITO structure to obtain an even higher V_{oc} of 691 mV (figure 6, no Si isolation).
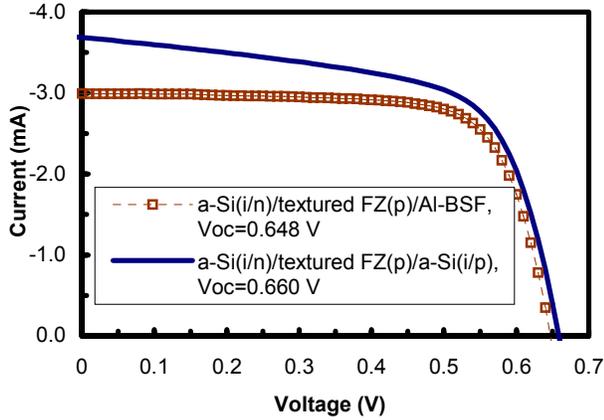
Fig. 5 Comparison of I-V curves of SHJ devices on textured p-FZ silicon with an Al-BSF and an a-Si(i/p) back collector, measured on front surface ITO dots without Si isolation.

Fig. 6. I-V curve of a double-heterojunction SHJ with a V_{oc} = 0.691 V on planar n-FZ silicon, measured on a front-surface ITO dot without Si isolation.

In summary, effective a-Si:H/c-Si heterointerfaces with minimal recombination loss can be obtained using HWCVD. HWCVD growth minimizes wafer damage, and permits abrupt a-Si:H deposition and yields a flat hetero-interface to the c-Si substrate. This ensures that the a-Si:H contacts high quality c-Si with low interface defect density and high band bending while minimizing the a-Si:H/c-Si interface area. Epitaxy on the c-Si surface is avoided by low-temperature deposition (<150°C) of the thin intrinsic layer. A higher temperature (~200°C) deposition of the subsequent doped layer enhances the interface passivation and the built-in voltage, likely by activating dopants and reducing defect density in both the underlying i- and the doped-layer. When HWCVD a-Si:H is used as the back collector, highly effective back-surface field is demonstrated by double-heterojunction SHJ devices with preliminary V_{oc} values of 691 mV and 660 mV on planar n-type FZ-Si and on textured p-type FZ-Si, respectively.

[1] M. Taguchi, K. Kawamoto, S. Tsuge, T. Baba, H. Sakata, M. Morizane, K. Uchihashi, N. Nakamura, S. Kiyama, and O. Oota, *Prog. PV Res. Appl.* **8,** 2000, p. 503.

[2] T.H. Wang, E. Iwaniczko, M.R. Page, D.H. Levi, Y. Yan, V. Yelundur, H.M. Branz, A. Rohatgi, and Q. Wang, *31ˢᵗ IEEE Photovoltaic Specialists Conference*, Orlando, Florida, January 3-7, 2005

Correlation between wafer fracture and saw damage introduced during cast silicon cutting

Y.K. Park[1], M.C. Wagener[1], N.Stoddard[2], M. Bennett[2] and G. A. Rozgonyi[1]

[1]North Carolina State University, Raleigh, NC 27695

[2]BP Solar, 630 Solarex Court, Frederick, MD 21703

Abstract

Four bars, cut from a single brick, having different roughness from saw damage were received from BP solar. Each bar was bevel polished to investigate the depth of the saw damage. The depth of the saw damage extended up to 15 µm. In addition, the beveled sample was etched to determine the distribution of the residual damage under the saw-damaged layer. The damage was found to extend significantly below the cutting surface. The correlation between wafer edge damage and fracture strength will also be reported.

Introduction

The fracture of polycrystalline silicon wafer is an important factor in solar cell yield and cost [1]. The current understanding at BP Solar is that the most mechanical wafer failure is not predominantly due to variations in the intrinsic strength of the wafers, but instead to process-induced damage, *i.e.*, saw damage induced micro- and macro- scale cracks on the edge of the wafer. This paper reports on the relation between the fracture strength of the wafer and the saw-damaged layer on the edge of the wafer.

Experimental

Four bars (labeled A, B, C, and D) with different degrees of roughness from saw damage were investigated. Bar A had the highest roughness, bars B and C had a slightly lower roughness, and bar D the lowest roughness. The band saw characteristics used to cut bars out of bricks define the quality of the wafer edge. Figure 1 shows the cut surface of bar A. The parallel saw-damaged lines are clearly visible along the length of the bar. This plane corresponds to the edge of the wafer in Figure 2.

Figure 1 Optical image of the surface of bar A (21mm × 17mm × 125mm). The saw damage extends from left to right.
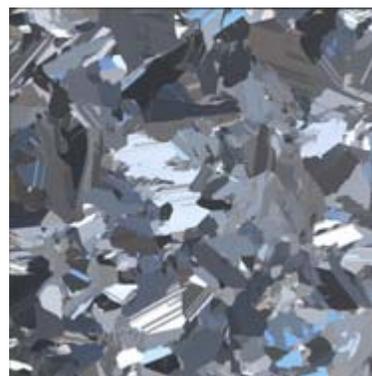
Figure 2 Optical image of a 5×5 in^2 BP solar wafer.

In order to compare the depth and width of the saw damage of each of the four bars, a bevel edge was prepared on each of the surfaces.   A 5-degree bevel angle was used to provide a nominal 10x depth magnification.   The actual post-bevel magnification was confirmed by laser reflection measurements from the beveled surfaces.   The sample bevels were examined by Nomarski optical microscopy.   The extent of near surface induced saw damage was determined by chemical etching the sample for 60 s using a Secco solution.

The correlation between the fracture strength and the saw damage was obtained by preparing samples with one surface containing the saw lines (see Figure 1).   The samples were prepared by cutting the bar into a smaller rectangular block as shown in Figure 3.   A thinner 1 mm thick piece was cross-sectioned and then cut into 6 mm discs using an ultrasonic cutter.   To remove any chips from the edges of the discs, one side was also polished using #1200 silicon carbide abrasive paper.   The mechanical behavior and the fracture strength will be evaluated using the miniaturized disk bend test (MDBT) [2].


Figure 3   Optical image of mechanical test sample preparation performed by low speed diamond sawing and ultrasonic cutting.

Results and Discussion

The Nomarski images of the beveled surfaces (A, B, C, and D) are shown Figure 4.   The black region in each of the figures corresponds to the saw-damaged plane of the block, and the light gray regions correspond to the beveled surfaces.   The depth of the saw damage can be estimated using the depth scale in the figure.   For bar A, the saw damage appears the most extensive, as compared to B, C, and D.   The average depth of the damaged layer for bar A is about 15 μm below the surface.   For bars B, C, and D, there was no appreciable difference in the average saw depth.

The stressed/damaged areas are known to etch preferentially [3].   The beveled surfaces were therefore Secco etched to estimate depth of the residual damage below the cutting surface.   For bar A, which showed the deepest saw damage, defects related to the saw damage extended about 70 μm below the cutting surface.   This implies that the saw damage generates a distortion of the microstructure that extends well beyond the average surface damage.   For bar B, a similar damage is seen, with the depth of the residual damage clearly related to the extent of the saw damage penetration depth.
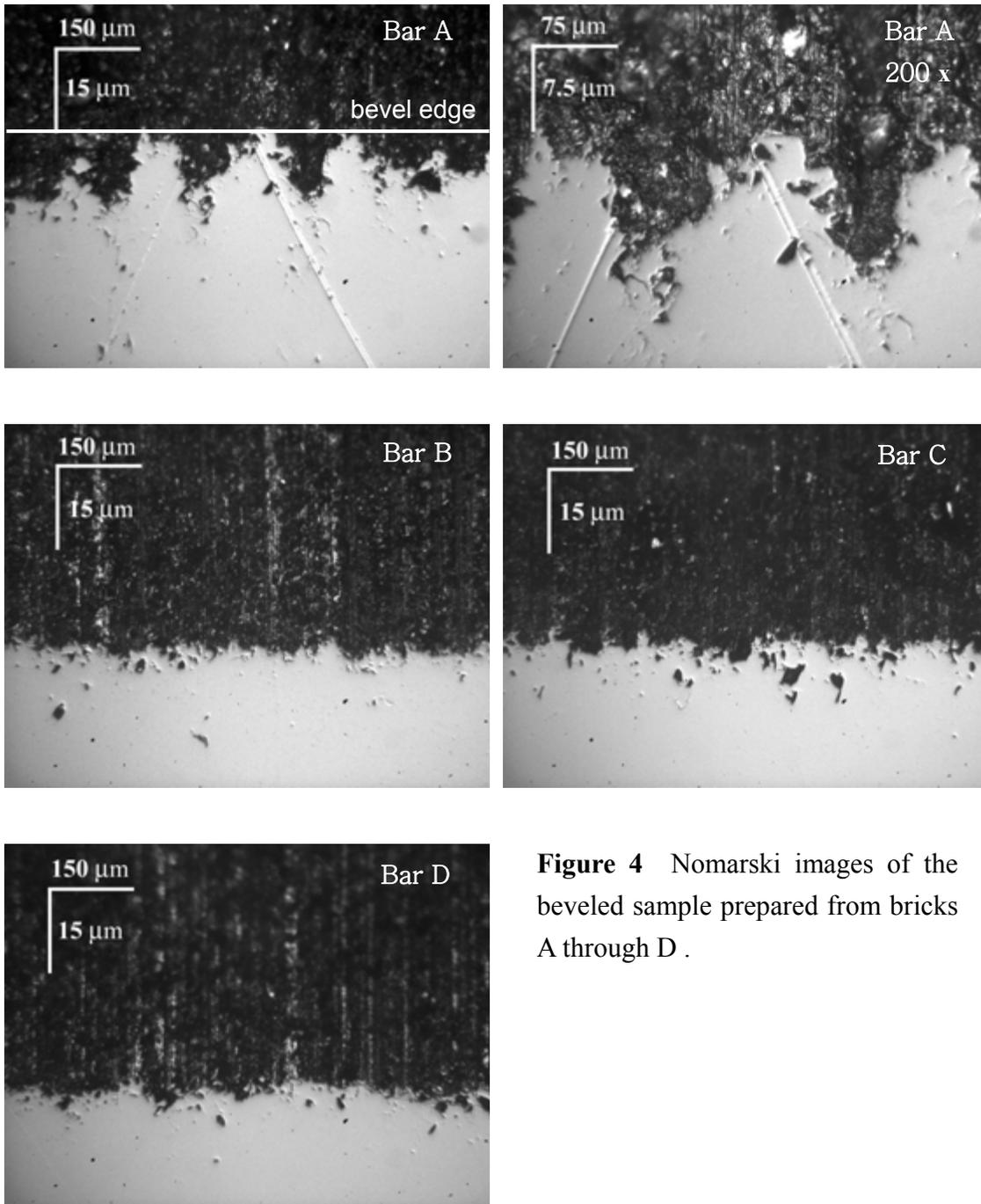
Figure 4 Nomarski images of the beveled sample prepared from bricks A through D .

Conclusions

The depth of the surface damage was found to extend up to 15 μm, with the residual damage penetrating up to 70 μm below the cutting surface. Based on this result, it is anticipated that the saw damage is closely related to the fracture strength of the wafer edge, and we are required to explore potential solutions for limiting the influence of edge damage.
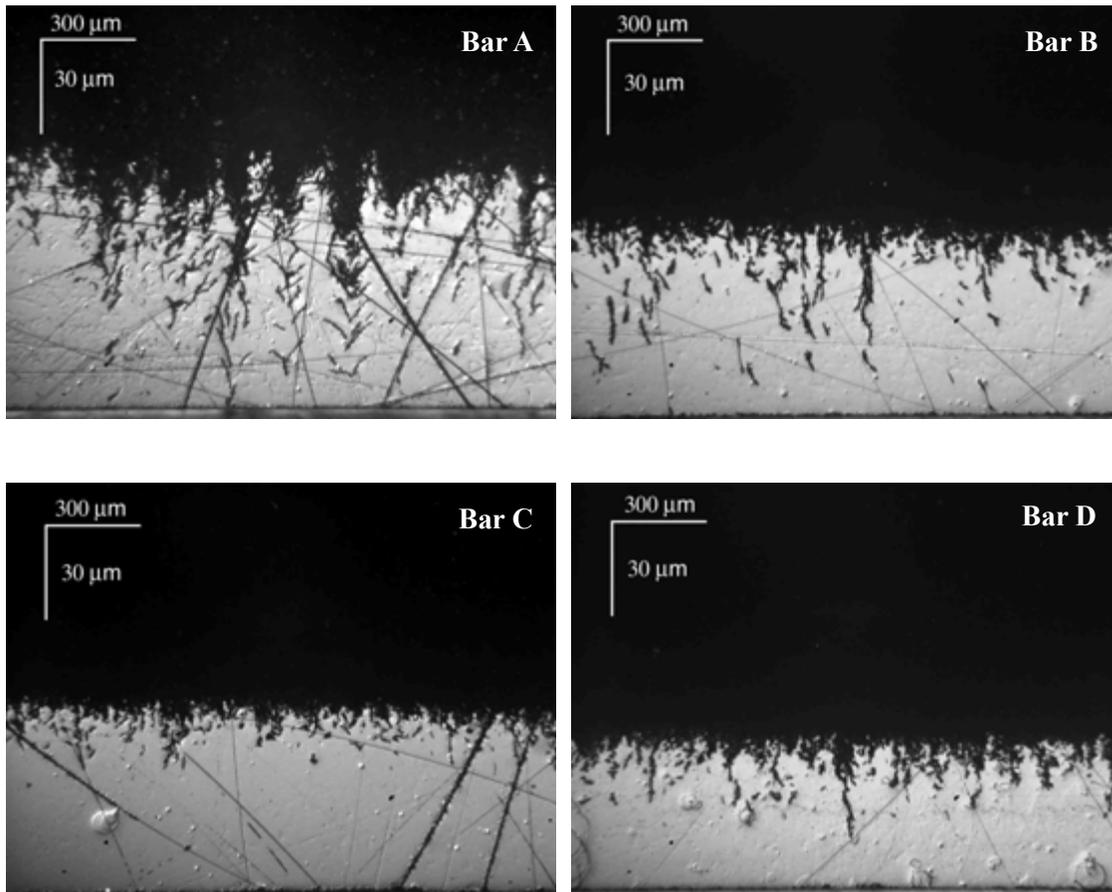
Figure 5   The Nomarski image of the beveled sample from bars A through D after Secco etching for 60s.

References

[1] L.W. Mittelstadt, A. Metz and R. Hezel, "Mechanical and Electrical Properties of Surface Grooved Thin Crystalline Silicon Solar Cells", 16th European photovoltaic solar energy conference and exhibition, Glasgow, United Kingdom, May 2000.

[2] K.M. Youssef, R.O. Scattergood, K.L. Murty, and C.C. Koch, Appl. Phys. Lett. **85** (2004) 929.

[3] J.M. Kim and Y.K. Kim, J. Electrochem. Soc., **152** (2005) G189.

Investigation of Intragrain Lifetime Dependence in Cast Polycrystalline Silicon

J.K.L. Peters[1], M.C. Wagener[1], G.A. Rozgonyi[1] and M. Narayanan[2]

[1]North Carolina State University, Raleigh, NC 27695
[2]BP Solar, 630 Solarex Court, Frederick, MD 21703

Abstract

The role of intragrain defects as recombination centers in BP Solar cast polycrystalline silicon wafers is studied using laser microwave photoconductive decay (µPCD), electron beam induced current (EBIC), and preferential etching/Nomarski optical microscopy. Photoconductive decay measurements show carrier lifetime variations from 0.5 µs to 20 µs. Comparison of Nomarski images in the high and low lifetime regions show that the low lifetime areas correspond to high dislocation densities formed by thermal stress during ingot cooling. EBIC measurements confirm the electrical activity of the dislocations in the intragrain regions. Although passivation appeared to be efficient at reducing recombination at large angle grain boundaries, the low angle intragrain boundaries significantly reduced the effective grain size. Further investigation of the passivation and recombination behavior of the intragrain defects by near-field scanning optical microscopy (NSOM) is pursued.

Introduction

The presence of stress related intragrain defects due to thermal gradients is a well known phenomenon in cast polycrystalline silicon. Such gradients form from the lateral heat flux of the furnace sidewalls, which control the planarity of the liquid-solid interface, and the vertical heat flux, which controls the solidification front velocity. Convex transverse gradients, although favorable during growth to prevent sidewall nucleation, generate high dislocation densities during cool down near the sidewall edges. Such dislocations either pile up along grain boundaries, or form shallow grain boundaries, thereby acting as recombination centers and degrading the minority carrier lifetime. Prior DLTS and EBIC studies [1,2] on Solarex material confirmed the existence of grain boundary related electron and hole traps, and electrically active dislocation formation at grain boundaries.

Experimental

Carrier lifetime mapping of a 5×5 in, SiN passivated cast silicon wafer was done using an AMECON JANUS 300 microwave photoconductive decay (µPCD) system. A grain boundary map was obtained by optical scanning of the sample surface and using image processing software. The grain boundary outline was then overlaid onto the µPCD map to correlate the microstructure with the lifetime map. Regions A and B, (shown in Figure 1) where both high and low lifetimes are present, were cut, polished, and Secco etched for 60 seconds to delineate the dislocations, and were observed using Nomarski microscopy.

Results and Discussion

As a precursor to the present study, deep level transient spectroscopy (DLTS) on unpassivated, high resistivity BP wafers was performed. The results indicated less than 10^{10} cm^{-3} impurities, and that the measured hole traps were solely related to underlying intragrain defects. The μPCD map and grain boundary overlay for the SiN coated and passivated wafer is shown in Figure 1.
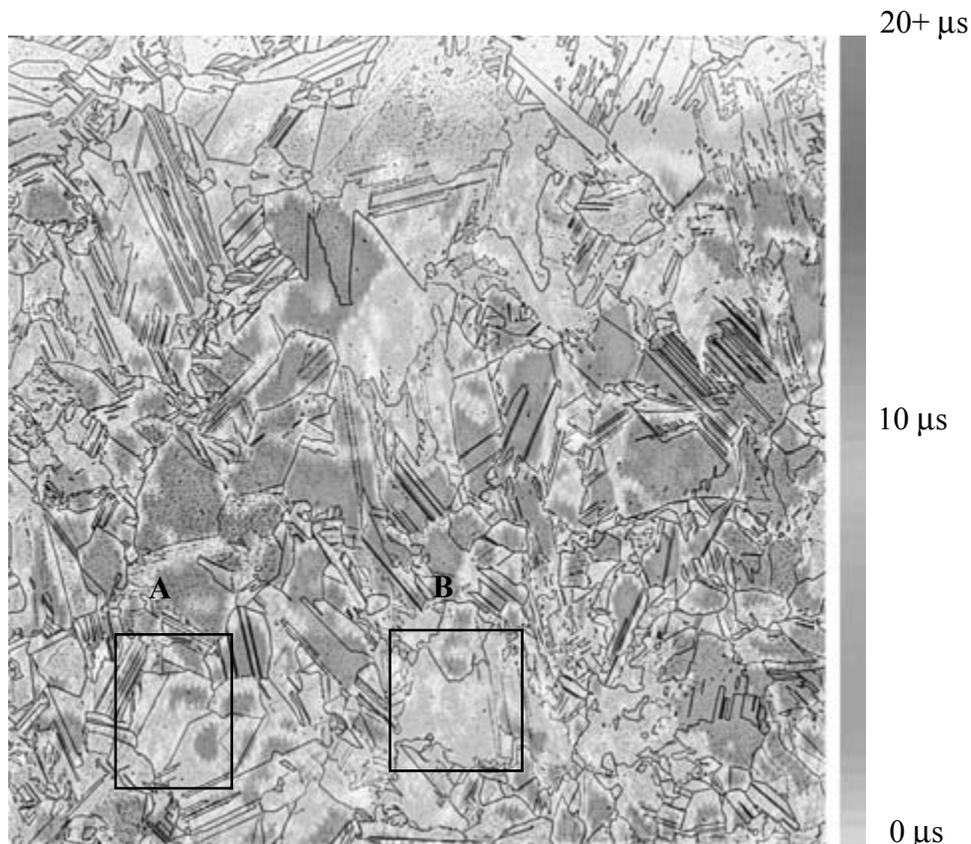

Figure 1 μPCD map of SiN passivated wafer. Areas A and B were cut and Secco etched to examine the intragrain structure.

High lifetimes (dark areas correspond to lifetimes exceeding 10 μs) correspond to areas of effective bulk passivation. From the overlaid grain boundary map, many areas with large structural features, such as high angle grain boundaries and twin boundaries have high lifetimes. The low lifetime areas therefore appear to be limited by a different mechanism. The low lifetime band at the top of the map corresponds to impurity diffusion from the crucible, and no significant increase in intragrain defect density was noticed in this region. The other low lifetime areas of the wafer are believed to be purely attribute to intragrain defects. Regions A and B were cut for Nomarski microscopy to identify the intragrain fine structure. The Nomarski images these regions are shown in Figure 2. The areas of low lifetime (as indicated by the μPCD maps) show the presence of dislocations networks, as well as the formation of shallow angle grain boundaries due to dislocation pileup. The effective recombination behavior of the intragrain dislocation is depicted by the EBIC image in Figure 3. The formation of the intragrain fine structure would therefore clearly reduce the effective grain size to only a few microns.
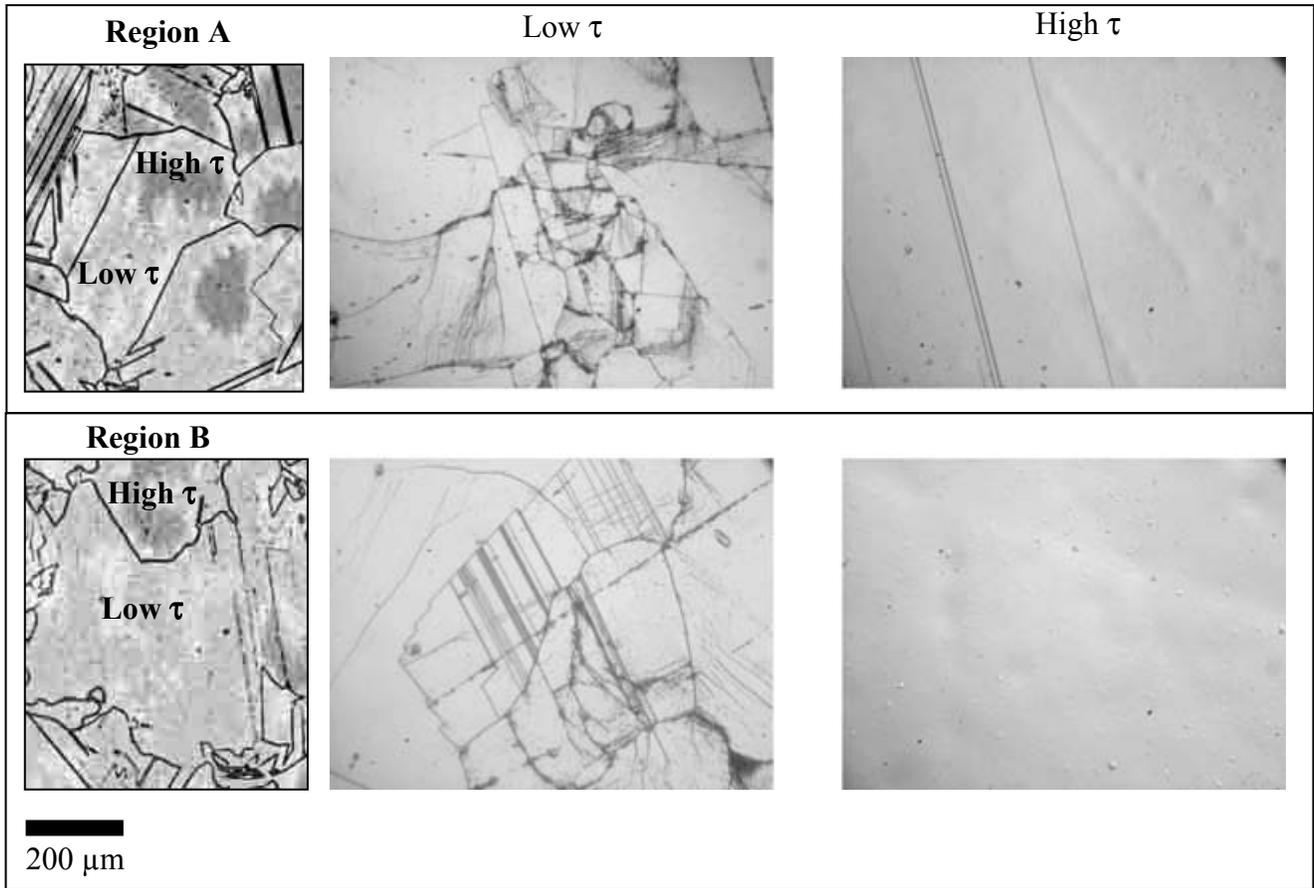
Figure 2 Nomarski optical microscope images of high and low lifetime areas of Regions A and B. The low lifetime areas clearly correspond to regions of high dislocation density, while the high lifetime regions show little intragrain structure.
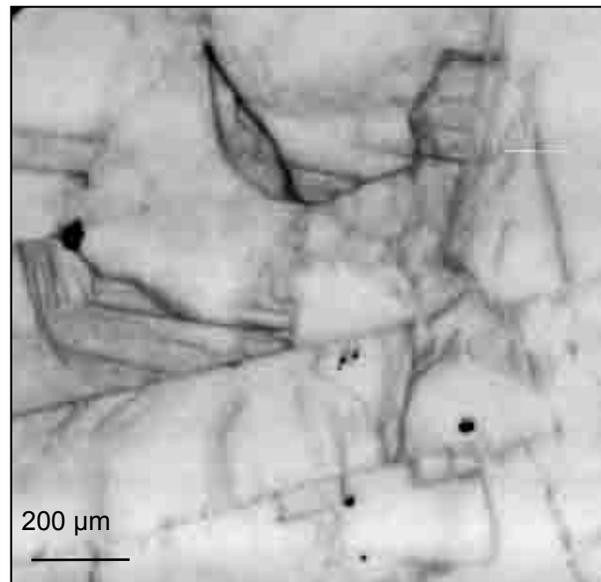
Figure 3 EBIC image of the low lifetime region observed in Figure 2. Shallow angle grain boundaries and dislocation networks produce strong recombination behavior.

Conclusions

Comparing the µPCD and Nomarski results, the low lifetime regions in this wafer are attributed to intragrain dislocations. Furthermore, passivation does not seem to be effective at reducing the recombination at low angle grain boundaries. In order to better understand the observed lifetime behavior of individual intragrain defects, a detailed imaging technique would be necessary. With the advances in scanning probe microscopy enabling quantitative lifetime imaging beyond the optical diffraction limit, the investigation of the dislocation passivation/recombination behavior on the scale of the grain boundary would be possible. NSOM provides the nanometer scale probing of optical and opto-electronic properties [3]. NSOM, which uses a sub-wavelength (<100 nm) aperture at the end of a tapered, aluminum-coated optical fiber as a probe, enables the illumination and detection of "near-field" light. The resolution of the NSOM images is well beyond the diffraction limit, typically better than 100 nm. We have configured our NSOM to measure carrier lifetime (τ-NSOM). Time resolved infrared transmission [4] will be used as the contrast mechanism, using a "pump-probe" approach, in which a modulated visible laser creates a localized carrier population in the sample, while a continuous wavelength infrared laser measures the change in transmission through the wafer. Using NSOM, we therefore hope to generate images of the carrier lifetime distribution near the shallow angle grain boundaries.

References

[1] P. K. McLarty, D. E. Ioannou, and S. P. Shea, J. Appl. Phys., **61,** 2672 (1986)
[2] K. C. Yoo, S. M. Johnson and W. F. Regnault, J. Appl. Phys., **57,** 2258 (1985)
[3] E Betzig and J.K. Trautman, Science, **257**, 189-195, (1992)
[4] A. H. LaRosa, B. I. Yakobsen, and H. D. Hallen, App. Phys. Lett., **70**, (13), 1656 (1997)

PV Manufacturing Initiative

S. Danyluk, S. Melkote, A. Dugenske, S. He, F. Li, X. Brun, D. Furbush

Georgia Institute of Technology
Manufacturing Research Center and the
George W. Woodruff School of Mechanical Engineering

Abstract

The Manufacturing Research Center at Georgia Tech is addressing the handling, transport and inspection of thin polycrystalline silicon sheet. Polariscopy is being used as a prototypical inspection station around which the handling and transport of wafers will be done. In addition, the research program also includes the development of software tools for the exchange of information between the manufacturing steps.

1 Introduction

The Manufacturing Research Center (MARC) at Georgia Tech is currently addressing photovoltaics manufacturing as a part of an NREL grant. Part of the Initiative deals with the creation of a laboratory that will address the handling and transport of thin wafers, residual stress inspection and the development of software tools for the exchange of information. The purpose of the lab will be to research and develop new manufacturing techniques in order to both improve the quality and yield, and lower the cost of photovoltaic devices. A focal point of the laboratory will be an industrial scale manufacturing pilot line which will be used to investigate the handling and fracture of thin polycrystalline silicon wafers such as those produced by RWE Schott Solar, BP Solar, and Evergreen Solar. This work was initiated in May 2005 and this paper describes the layout of the laboratory and the software and instrumentation design.

2 Pilot Line Description

The pilot line will contain several manufacturing cells that are connected by conveyors or other material transfer mechanisms, as shown in Figure 1, "Laboratory Equipment Layout and Process Flow".

The first cell will be used to study forces exerted by pick-and-place grippers on thin silicon wafers and their resulting deformation, and residual stresses present in wafers. A 4-axis SCARA robot equipped with either Bernoulli, vacuum or mechanical grippers will pick up wafers using precisely-controlled grip forces and position them in a near-Infrared Polariscope (a stress measuring system based on near Infrared Photoelasticity technique) so that residual stresses can be measured. After a wafer has been inspected, it will then be moved to a conveyor by the robot and transferred to the back metallization station.

Upon arriving at the back metallization station, a material handling mechanism will place the wafer on a platform, and a stencil will be placed on top of the wafer. Solder paste will be applied to the wafer through the stencil either by using a squeegee or a sponge. Upon completion of the printing process, the stencil will be removed and the wafer will be moved to a second conveyor for transfer to the third station. This cell will be used to study the printing process and recommend material handling improvements.

Monitoring and control of the pilot line cells will be accomplished though a CAM XML-based (CAMX) factory information system. CAMX makes use of a virtual message broker which exchanges XML messages amongst assets in an enterprise across the internet. An application

server will be used to collect, store, and present manufacturing data through a web interface such as stress histories, wafer yield, work-in-process, and sensor output. Figure 2, "Software and Instrumentation Design", provides an overview of the proposed instrumentation design for the first manufacturing cell.

3 Conclusions

This research program addresses the handling, transport and inspection of polycrystalline silicon wafers used in PV manufacturing. The program also addresses the development of software tools for exchange of information between the various hardware tools and the manufacturing line manager. Ultimately, the program aims to improve the yield of thin wafers. The research results will be made available to the PV manufacturers.
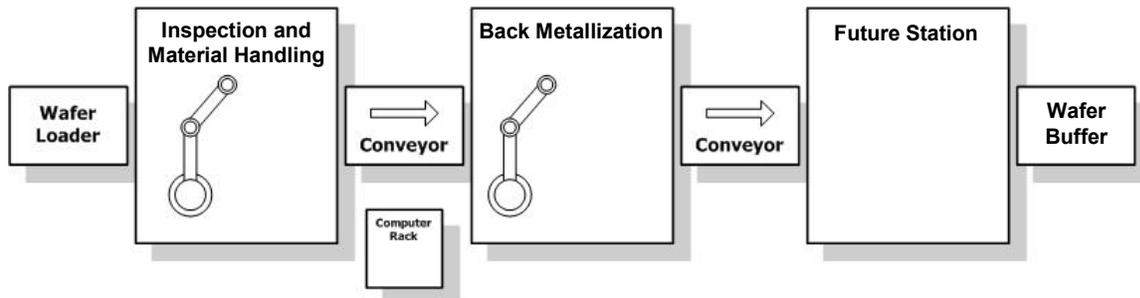
4 Acknowledgements

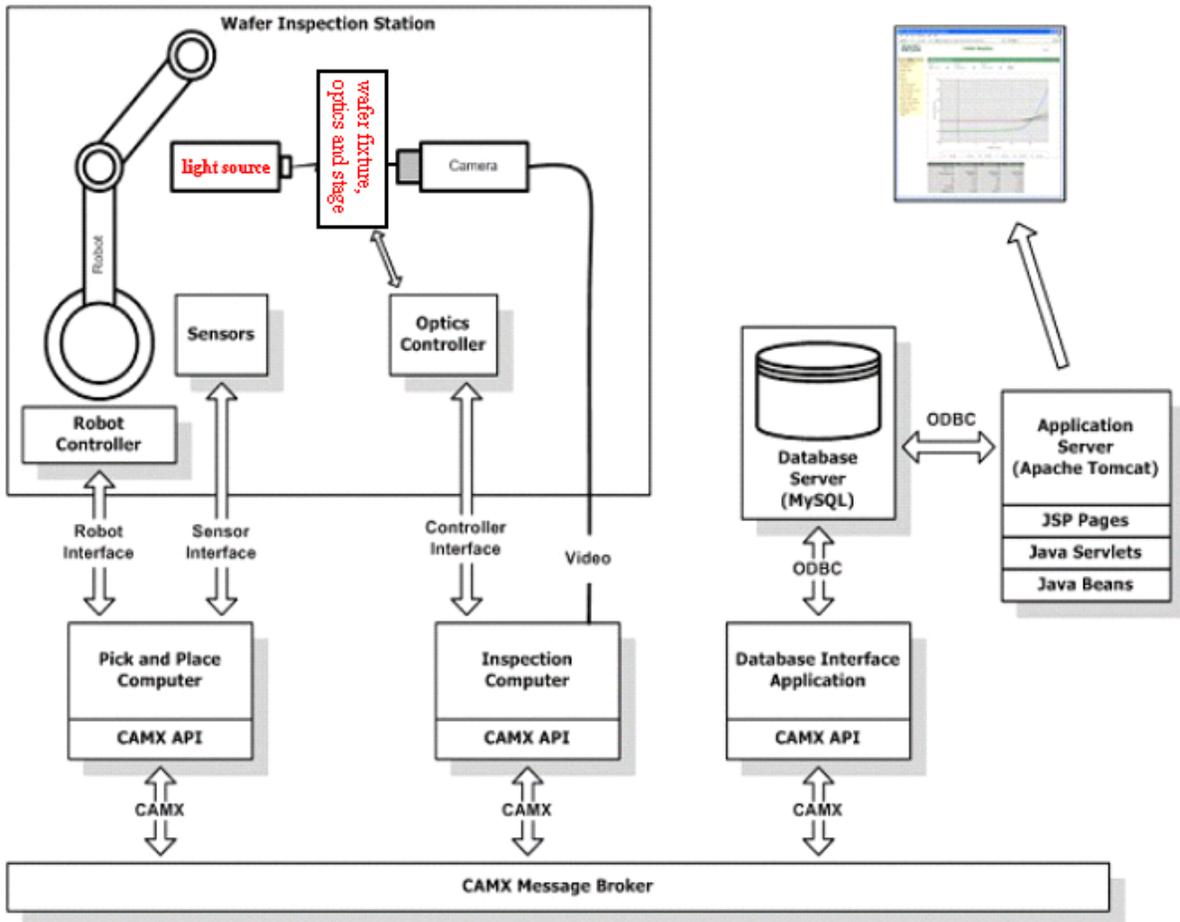Figure 1. Laboratory Equipment Layout and Process Flow

Figure 2. Software and Instrumentation Design

Analysis and Determination of the Stress-optic Coefficients of EFG silicon

S. He, F. Li, S. Danyluk
Georgia Institute of Technology
I. Tarasov, S. Ostapenko
University of South Florida

Abstract
This paper reports on the anisotropic stress-optic coefficient of EFG silicon, which was determined using a four-point bending technique. The stress-optic tensor components $\pi_{11} - \pi_{12}$ and π_{44} were then determined.

1 Introduction

Photoelasticity has been applied to semiconductor materials since the 1950's. Bond and Andrus [1] reported the first fringe pattern of residual stresses in silicon in 1955 with infrared illumination. The quantitative measurement of residual stress in silicon was made possible after the piezo-birefringence constants was first measured by Giardini(1958) [2]. Later Lederhandler [3], Denicola and Tauber [4], Kotake and Takasu [5], Wong et al [6] used this technique to characterize the residual stress for the purpose of process control. Zheng [7] used a six-step phase-stepping and fringe multiplier techniques to extract residual stresses in thin samples.

The extraction of the residual stresses in crystalline silicon samples from the photoelastic parameters also requires a knowledge of the influence of crystal anisotropy on the stress-optic coefficients. Quantitative residual stresses were first obtained by Kotake et al [8] in as-grown GaP. Yamada [9] studied analytically the anisotropy of the strain-optic coefficient in a (001) GaA. Liang and Pan [10] presented an analysis of the stress-optic relationship of the (001) and (111) silicon, but both the illumination and the observation were in-plane only. He et al [11] analyzed and calibrated the anisotropy in (001) silicon. This paper reports on the stress-optic laws for (011) silicon observed along the normal direction. These were than calibrated using four-point bending of "plates" sectioned from the silicon wafers.

2 Anisotropy in the Stressoptic Coefficient

The anisotropic stress-optic coefficient can be derived from the general relation between the stress tensor and the dielectric impermeability tensor [12].

$$\Delta\boldsymbol{\beta} = \boldsymbol{\pi}\boldsymbol{\sigma} \tag{1}$$

where $\boldsymbol{\pi}$ is a fourth-rank piezo-optical coefficient tensor, $\boldsymbol{\sigma}$ is the stress tensor, and $\Delta\beta$ is the increment of the impermeability tensor caused by stress. This equation can be expressed in matrix form as:

$$\begin{bmatrix} \Delta\beta_1 \\ \Delta\beta_2 \\ \Delta\beta_3 \\ \Delta\beta_4 \\ \Delta\beta_5 \\ \Delta\beta_6 \end{bmatrix} = \begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{12} & & & \\ \pi_{12} & \pi_{11} & \pi_{12} & & & \\ \pi_{12} & \pi_{12} & \pi_{11} & & & \\ & & & \pi_{44} & & \\ & & & & \pi_{44} & \\ & & & & & \pi_{44} \end{bmatrix} \begin{bmatrix} \sigma_x \\ \sigma_y \\ \sigma_z \\ \tau_{yz} \\ \tau_{zx} \\ \tau_{xy} \end{bmatrix} \tag{2}$$

Also as a result of cubic symmetry, there are only three independent components π_{11}, π_{12} and π_{44} in the piezo-optical tensor.

EFG silicon has a preponderance toward (110) irrespective of the seed crystal orientation [13]. The effective stress-optical coefficient can be obtained by two consecutive coordinate transformations. The piezo-optical tensor is first transformed to the local coordinate, $(001, 1\bar{1}0, 110)$, and then to the principal coordinate of the impermeability tensor. For a thin silicon sample, the shear stresses τ_{xz}, τ_{yz} and the normal stress σ_z can be considered zero, and the non-zero components σ_x, σ_y and τ_{xy}, can be considered uniform through the thickness. Therefore, the state of stress in a thin silicon sample can be

considered in a state of plane stress. The orientation of the principal axes of the impermeability is determined by the isoclinic angle, μ, the principal direction of the impermeability tensor obtained from experiment by the phase stepping. This relation in Equation 1 can also be transformed to the principal axes, where $\Delta\beta'_6 = 0$,

$$\begin{bmatrix} \Delta\beta'_1 \\ \Delta\beta'_2 \\ \Delta\beta'_3 \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} \pi'_{11} & \pi'_{12} & \pi_{12} & 0 & 0 & \pi'_{16} \\ \pi'_{12} & \pi'_{11} & \pi_{12} & 0 & 0 & -\pi'_{16} \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ \dfrac{\pi'_{16}}{2} & -\dfrac{\pi'_{16}}{2} & 0 & 0 & 0 & \pi'_{66} \end{bmatrix} \begin{bmatrix} \sigma'_x \\ \sigma'_y \\ 0 \\ 0 \\ 0 \\ \tau'_{xy} \end{bmatrix} \quad (3)$$

The piezo-optical matrix is no longer symmetric. Generally, the coefficients in these principal axes are functions of θ.

$$\pi'_{11} = \pi_{11} - \frac{1}{2}(\pi_{11} - \pi_{12} - \pi_{44})\cos^2 2\theta$$

$$\pi'_{12} = \pi_{12} + \frac{1}{2}(\pi_{11} - \pi_{12} - \pi_{44})\cos^2 2\theta \quad (4)$$

$$\pi'_{16} = \frac{1}{2}(\pi_{11} - \pi_{12} - \pi_{44})\sin 4\theta$$

$$\pi'_{66} = \pi_{44} + (\pi_{11} - \pi_{12} - \pi_{44})\cos^2 2\theta$$

In these principal axes, the relation between τ'_{xy} and $\sigma'_x - \sigma'_y$ can be derived from $\beta'_6 = 0$.

$$\tau'_{xy} = \frac{\pi'_{16}}{2\pi'_{66}}(\sigma'_x - \sigma'_y) \quad (5)$$

The phase retardation is related to the impermeability by [14]

$$\delta = \frac{\pi n_0^3}{\lambda}(\Delta\beta'_1 - \Delta\beta'_2) \quad (6)$$

where n_0 is the refractive index when the silicon is stress free. The stress-optic coefficient $C(\theta)$ for the (001) orientation observed along the normal direction can be obtained as,

$$C(\theta) = \frac{n_0^3}{2} \frac{1}{\sqrt{\dfrac{\sin^2 2\theta}{\pi_{44}^2} + \dfrac{\cos^2 2\theta}{(\pi_{11} - \pi_{12})^2}}} \quad (7)$$

After the values of $\pi_{11} - \pi_{12}$ and π_{44} are determined, the anisotropy of $C(\theta)$ can be determined. For the (011), the stress-optic coefficient has a maximum of $n_0^3 \pi_{44}/2$ and a minimum $n_0^3(\pi_{11} - \pi_{12})/2$.
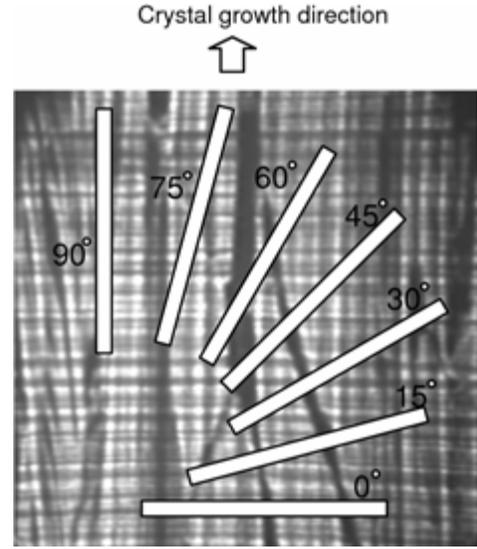

Figure 1: The sample for the calibration of EFG wafer

3 Experimental Results and Discussion

Four-point bending was used for calibration. As shown in Figure 1, seven silicon 'beam', with size of 120×12×0.32 mm were removed from 4×4 inche EFG wafers at various orientations. The beams were loaded into a fixture and the load was applied by two weights. Compared with single crystal silicon, EFG wafers have notably higher residual stresses. The average shear stress is approximately 5 MPa. To minimize the effect of the residual stresses, a significantly larger load with a maximum stress of 32 MPa was applied, and the average residual stress is reduced to 15% of the applied stress. The effect of the residual stress on the stress-optic coefficient is expected to be smaller than 15% because the least-square fit, which is an average along the transverse direction, was used to extract the data.

The retardation of the four-point bending of an EFG sample is shown in Figure 2(a). The maximum retardation is around 1.5 rad. The

retardation of the residual stress is shown in Figure 2(b). The maximum magnitude of the residual stress is around 0.3 rad, which is substantially lower than the applied stress.
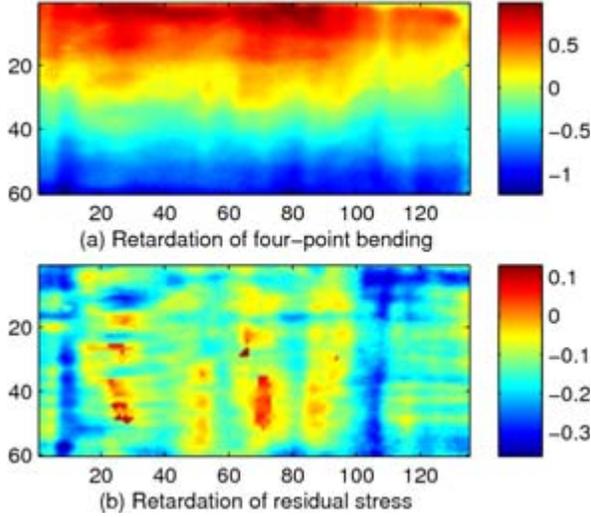

(a) Retardation of four-point bending

(b) Retardation of residual stress

Figure 2: The calibration result of four-point bending of an EFG silicon beam cut at 0°, the retardation of the stressed (above) and free (below) sample of EFG wafer

The least-square fit is used to extract the slope of the retardation along the transverse direction. It not only reduces the effect of the error, but also can minimize the influence of the residual stress because the residual stress is self-balanced along any section. A linear least-square fit of a randomly selected cross sec tion is shown in Figure 3. The correlation of this fit is R2 = 0.988. The stress-optic coefficient can be obtain from this slope [11]

$$C = \frac{d\delta}{dy} \bigg/ \left(\frac{2\pi t}{\lambda} \frac{M}{I} \right)$$ (8)

where $I = h^3 t / 12$ is the moment of inertia of the beam, M is the applied moment, and y is the vertical location from the center. No obvious correlation between the stress-optic coefficient and residual stress was found.

Table 1 shows the value of the coefficients and variances. The anisotropy can be clearly observed in Figure 4. The components of the piezo-stress tensor, $\pi_{11} - \pi_{12}$ and π_{44}, can be

determined with higher accuracy through the nonlinear least-square fit of the anisotropic stress coefficient,

$$\begin{cases} \dfrac{\partial}{\partial(\pi_{11} - \pi_{12})} \sum_{i=1}^{7} [C(\theta_i) - C_i]^2 = 0 \\[4mm] \dfrac{\partial}{\partial \pi_{44}} \sum_{i=1}^{7} [C(\theta_i) - C_i]^2 = 0 \end{cases}$$ (9)
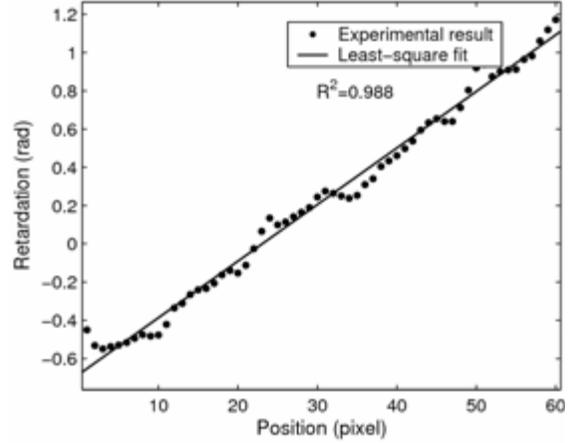

Figure 3: Least-squares fit of retardation along transverse direction of an EFG sample with an orientation of 0°

The tensor can be obtained as,

$$\pi_{11} - \pi_{12} = 16.8 \times 10^{-13} \, Pa^{-1}$$
$$\pi_{44} = 11.1 \times 10^{-13} \, Pa^{-1}$$ (10)

These values are considerably larger than single crystal silicon, $\pi_{11} - \pi_{12} = 9.88 \times 10^{-13} \, Pa^{-1}$, $\pi_{44} = 6.50 \times 10^{-13} \, Pa^{-1}$. The results are shown in Figure 4. The dash line shows the least-square fit of the experimental results of the EFG silicon, and the solid line is for the coefficient of (001) CZ silicon. The difference demonstrates that substantial error will be introduced to the residual stresses when the coefficient of single crystal is used for EFG samples. The maximum and minimum of the stress-optic coefficient are:

$$C_{max} = 2.127 \times 10^{-11} \, Pa^{-1}$$
$$C_{min} = 1.435 \times 10^{-11} \, Pa^{-1}$$ (11)

and the anisotropy in the coefficient is

$$\frac{C_{max} - C_{min}}{(C_{max} + C_{min})/2} \times 100\% = 39\%$$ (12)

Table 1: The stress-optic coefficients of EFG silicon Orientation

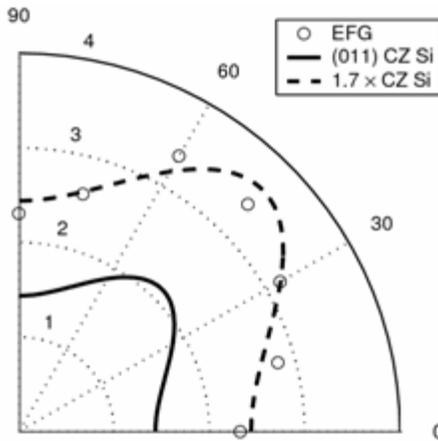| Orientation (°)	C ($\times 10^{-11} Pa^{-1}$)	Standard deviation ($\times 10^{-11} Pa^{-1}$)
0°	2.312	0.372
15°	2.848	0.578
30°	3.188	0.224
45°	3.433	0.249
60°	3.013	0.410
75°	2.463	0.377
90°	2.297	0.259

(°)

Figure 4: Experimental results of the effective stress optic coefficient of the EFG sample compared with that of single crystal silicon

4 Conclusions

The stress-optic coefficients of EFG silicon were derived analytically and calibrated experimentally. The components of the stress-optic tensor were measured to be: $\pi_{11} - \pi_{12} = 16.8 \times 10^{-13} Pa^{-1}$, $\pi_{44} = 11.1 \times 10^{-13} Pa^{-1}$. The coefficient of EFG has the anisotropic profile same with that of (001) silicon with a magnitude of 1.7 times bigger.

References

[1] W.J. Bond and J. Andrus. Photographs of the stress field around edge dislocations. Physical Review, 101(3):1211–1212, 1956.

[2] A. A. Giardini. Piezobirefringence in silicon. The American mineralogist, 43:249–263, 1958.

[3] S.R. Lederhandler. Infrared studies of birefringence in silicon. Journal of applied physics, 30(11):1631–38, 1959.

[4] R. O. Denicola and R. N. Tauber. Effect of growth parameters on residual stress and dislocation density of czochralski-grown silicon crystals. Journal of Applied Physics, 42(11):4262, 1971.

[5] H. Kotake and Shin. Takasu. Quantitative measurement of stress in silicon by photoelasticity and its application. J. Electrochem. Soc., 127(1):179–184, 1980.

[6] S. P. Wong, W.Y. Cheung, M.R.Sajan N.Ke, W.S.Guo, L.Huang, and Shounan Zhao. IR photoelasticity study of stress distribution in silicon under thin film structures. Materials Chemistry and Physics, 51:157–162, 1997.

[7] Tieyu Zheng and Steven Danyluk. Study of stresses in thin silicon wafers with near-infrared phase stepping photoelasticity. J. Mater. Res, 17(1):36–42, 2002.

[8] H. Kotake, K. Hirahara, and M. Watanabe. Quantitative photoelastic measurement of residual stress in lec grown gap crystals. Journal of crystal growth, 50:743–751, 1980.

[9] M. Yamada. Quantitative photoelastic measurement of residual strains in undoped semiinsulating gallium arsenide. Appl. Phys. Lett., 47(4):365–367, 1985.

[10] H. C. Liang, Y. X. Pan, S. N. Zhao, G. M. Qin, and K. K. Chin. Two-dimensional state of stress in a silicon wafer. Journal of Applied Physics, 71(6):2863–2870, 1992.

[11] S. He, T. Zheng, and S. Danyluk. Analysis and determination of the stress-optic coefficients of thin single crystal silicon samples. Journal of Applied Physics, 96(6):3103–3109, 2004.

[12] J. F. Nye. Physical properties of crystals. Oxford, 1957.

[13] T. Surek, C. B. H. Rao, J. C. Swartz, and L. C. Garone. Surface morphology and shape stability in silicon ribbons grown by edge-defined, film-fed growth process. Journal of the Electrochemical Society, 124(1):112–123, 1977.

[14] Tieyu Zheng. A Study of Residual Stresses in Thin Anisotropic (silicon) Plates. Ph.D thesis, Georgia Institute of Technology, 2000.

Effect of oxygen on the quality of Al-BSF in Si cells

V. Meemongkolkiat, K. Nakayashiki, B.C. Rounsaville, and A. Rohatgi
School of Electrical and Computer Engineering
Georgia Institute of Technology, Atlanta, GA 30332-0250

Abstract

It has been reported by the authors that the surface passivation quality of screen-printed Al-back surface field is inferior in Czochralski (Cz) Si compared to float zone (FZ) Si. The purpose of this paper is to investigate the source of this discrepancy. It is found that not only the effective back surface recombination velocity (BSRV) is inferior, but also the front p-n junction leakage current is generally higher in Cz Si solar cells. In addition, the Magnetic Cz cells, with lower initial interstitial oxygen, did not show these adverse effects and exhibited equally good junction and BSRV as FZ Si cells. The inferior junction and back passivation quality is attributed to the presence of oxygen precipitates in both the depletion regions of Cz Si cells. Further analysis is needed to establish the exact role of high oxygen concentration in enhancing the junction recombination.

1. Introduction

Screen-printed (SP) Al-back surface field (BSF) for back surface passivation is one of the most widely used processes in the photovoltaic industry because of its simplicity and effectiveness. The studies in the past report that effective back surface recombination velocity (BSRV) as low as 200 cm/s on 2-4 Ω-cm can be achieved by using optimized process scheme [1,2]. However, it has also been shown by the authors that the BSRV can vary significantly depending on the substrate being used [3]. The BSRV in high quality float zone (FZ) Si was best described by hi-lo junction theory [4]. However, it was found that Czochralski (Cz) Si, despite being single crystalline Si, gave significantly higher BSRV compared to the same resistivity FZ Si. The reason for this discrepancy is not very well understood. This paper provides more extensive data analysis to understand and explain the difference between the BSRV of FZ and Cz cells.

2. Experimentals

Four different single crystalline Si were used in the study including single crystalline FZ Si, B-doped Cz, Ga-doped Cz and low-interstitial oxygen Magnetic Cz (MCz). Description of materials used in the study is summarized in Table I.

SP Al-BSF cells were fabricated and analyzed. First, all the samples were POCl$_3$ diffused to obtain ~45 Ω/sq n-type emitter. Subsequently, SiN$_x$ antireflection coating was deposited on the front. All the samples were then subjected to full-area Al screen-printing on the backside followed by Ag gridline printing on the front. The samples were then co-fired using rapid thermal processing.

Table I Summary of samples used in the study.

	FZ			MCz	B-doped Cz		Ga-doped Cz	
Resistivity (Ω –cm)	0.7	1.4	2.5	1.2	0.8	1.1	1.2	2.1
Initial Interstitial oxygen (ppma)	-	-	-	1.26 (GT)	13.6 (GT)	16 (NREL)	18 (NREL)	19 (NREL)

3. Results and discussions

3.1 Open circuit voltage (V_{oc}) difference in FZ and Cz single crystalline Si cells

The illuminated IV characteristic was obtained after a 200°C anneal for B-doped Cz Si to obtain the cell parameter without any LID effect. The V_{oc} is plotted as a function of resistivity for various single crystal Si materials in Fig. 1. It can be seen that the single crystalline cells with high oxygen concentration (e.g. B- and Ga-doped Cz Si) produce significantly lower V_{oc} compared to the ones with low oxygen concentration (e.g. FZ and MCz Si). This data suggests that the presence of oxygen in the silicon material significantly enhances the recombination in the solar cells.
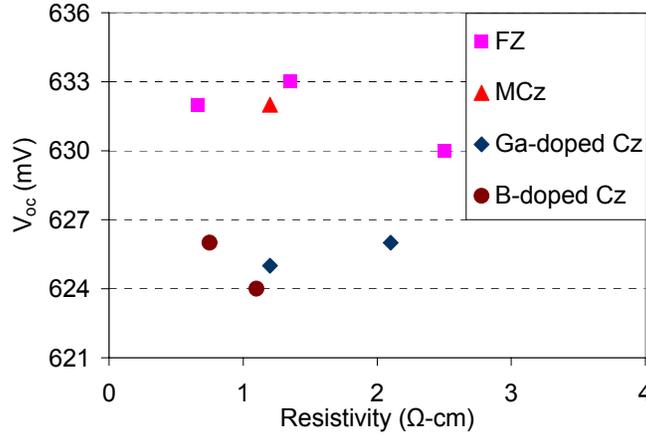
Fig 1. V_{oc} of solar cells as a function of resistivity for different single crystalline Si.

3.2 Investigation of ideality factor (n_2) and reverse dark saturation current (J_{02})

For comparison purposes, only the solar cells within 1.1-1.4 Ω-cm resistivity range were chosen for the analysis. The dark IV curves were measured and analyzed on the cells made on all four materials. These curves were fitted to the following double exponential model.

$$J = J_{01}e^{\frac{q(V+J\cdot R_s)}{kT}} + J_{02}e^{\frac{q(V+J\cdot R_s)}{n_2 kT}} + \frac{V+J\cdot R_s}{R_{Sh}} \qquad (1)$$

The best-fit values for J_{01}, n_2 and J_{02}, averaged over three cells, for each material are summarized in table II. It is clear that the recombination in the high-oxygen materials was not only enhanced in the diffusion component (indicated by higher J_{01}), but also increased in the depletion region recombination (indicated by higher J_{02}). In fact, many research groups have shown that oxygen precipitation in Si can enhance the recombination in the depletion region [5-7]. In [7], a relationship has been shown between the size of the oxygen precipitates and the recombination in the p-n junction.

Table II. J_{02} and n_2 for different single crystalline Si with resistivity of 1.1-1.4 Ω-cm.

Material	J_{01} (fA/cm^2)	J_{02} (nA/cm^2)	n_2
FZ	510	18	2.00
MCz	580	19	2.05
B-doped Cz	670	36	2.11
Ga-doped Cz	640	35	2.07

3.3 Internal Quantum efficiency (IQE) analysis

The IQE was measured on all the four samples with resistivity in the range of 1.1-1.4 Ω-cm, Fig. 2. Again, B-doped Cz cell was measured right after the 200°C anneal to remove any LID effect. B- and Ga-doped Cz cells showed lower long wavelength IQE, while the short wavelength IQE was identical for all four cells. This indicates that oxygen influences either the bulk lifetime or BSRV, both of which influence long wavelength IQE response. Next step was to separate the BSRV and bulk lifetime in these cells.
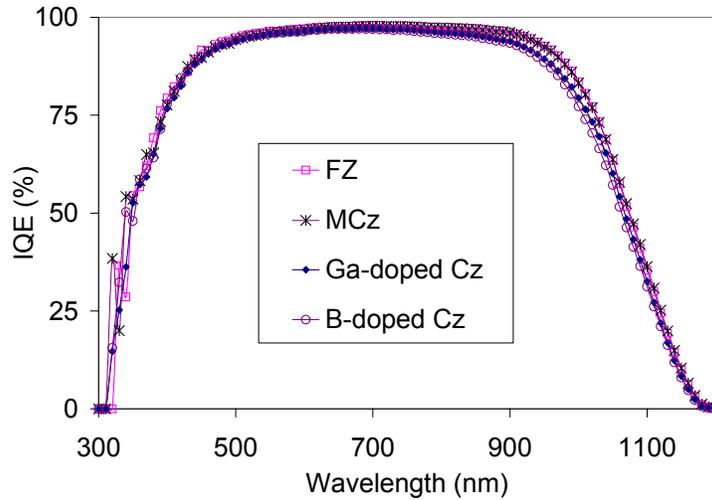
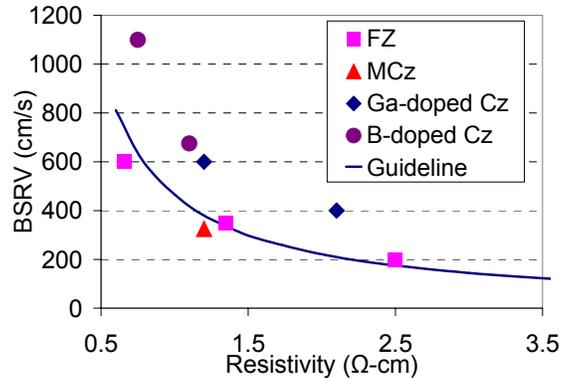**Fig. 2.** IQE for different types of single crystalline Si with resistivity of 1.1-1.4 Ω-cm.

3.4 Extraction of bulk lifetime and BSRV

The bulk lifetime in the finished cells was measured by the contactless photoconductance decay measurement after etching the cells down to the Si bulk. Subsequently, the BSRV was obtained by matching the measured long wavelength IQE with the simulated IQE using PC1D with measured bulk lifetime as one of the inputs to PC1D. The lifetime and BSRV values are summarized in Table III. Additionally, the BSRV values are plotted as a function of resistivity as shown in Fig. 3.

It is clear that the high oxygen content in single crystalline silicon repeatedly gave higher BSRV than the lower oxygen materials. In addition, the lifetime in all the material is reasonably high indicating that the long wavelength IQE, or recombination in the base is, in fact, dominated by the back surface recombination. As a result, it can be concluded that the BSRV is enhanced by the presence of high oxygen in Si.

Table III. Lifetime and BSRV summary for different types of single crystalline Si.

Resistivity range (Ω-cm)	Material	Lifetime (μs)	BSRV (cm/s)
0.65-0.75	FZ	245	600
	B-doped Cz	275	1100
1.1-1.4	FZ	1400	350
	MCz	2100	325
	B-doped Cz	410	675
	Ga-doped Cz	630	600
2.0-2.5	FZ	3070	200
	Ga-doped Cz	1470	400

Fig. 3. BSRV as a function of resistivity for different types of single crystalline Si.

The higher BSRV due to oxygen cannot be explained by the simplified hi-lo junction theory, which predicts that BSRV should be the same for the same doping profile and base doping. Since the recombination within the BSF itself is mainly dominated by the Auger recombination, the presence of any oxygen precipitation should not affect the BSF lifetime appreciably. Thus, the higher back surface recombination is most likely attributed to the recombination in the depletion region at the p-p+ interface. This could result from the presence of the oxygen precipitates. This is in good agreement with the higher recombination in the p-n junction at the front side, which showed higher J_{02} values (section 3.2). Further analysis is needed to understand the exact role of high oxygen concentration in enhancing the junction recombination.

4. Conclusion

It was found that the Cz Si solar cells with SP Al-BSF consistently gave higher BSRV compared to FZ cells. The J_{02} was also found to be higher in the Cz Si cells. On the other hand, the FZ and MCz cells with low oxygen content did not show this enhanced recombination in front and back junction. In addition, oxygen precipitation is known to give rise to recombination centers, which in turn can contribute to higher junction leakage current. Therefore, the observed effect of higher recombination in both the front and back junctions can be attributed to the presence of oxygen precipitates or higher oxygen in Cz. More work is needed to validate this hypothesis.

REFERENCES
[1] P. Lolgen, C. Leguijt, J.A. Eikelboom, R.A. Steeman, W.C. Sinke, L.A. Verhoef, P.F.A. Alkemade and E. Algra, *Proc. 23rd PVSC*, (IEEE, Louisville, 1993) p.236.
[2] S. Narasimha, A. Rohatgi, and A.W. Weeber, *IEEE Trans. on Electron Devices*, **ED-46**, 1363 (1999).
[3] V. Meemongkolkiat, M. Hilali, K. Nakayashiki, and A. Rohatgi, *Proc. 14th PVSEC*, (Bangkok, 2004) p. 401.
[4] A. Rohatgi, P.Rai-Choudhury, *IEEE Trans. on Electron Devices*, **ED-31**, 596 (1984).
[5] V.V. Batavin, *Sov. Phys. Semicond.,* **4**, 641 (1970).
[6] Y. Murakami, Y. Satoh, H. Furuya, and T. Shingyouji, *J. Appl. Phys.*, **84**, 3175 (1998).
[7] H. Uchiyama, K. Matsumoto, T. Mchedlidze, M. Nisimura, and K. Yamabe, *J. Electrochem. Soc.*, **146**, 2322 (1999).

Resonance Ultrasonic Vibration (RUV) for Crack Detection
in PV Crystalline Silicon Wafers
A. Belyaev, W. Dallas, O. Polupan, L. Zhukov, S. Ostapenko
University of South Florida, Tampa, FL 33620

The photovoltaic industry, with crystalline silicon as a dominant segment, is expanding rapidly to meet growing renewable energy demands all over the world. One of the current technological problems is to identify and eliminate sources of mechanical defects such as thermo-elastic stress and cracks leading to the loss of wafer integrity and ultimate breakage of as-grown and processed Si wafers and cells. The problem is of increased concern as a result of the current strategy of reducing wafer thickness down to 100 microns. Cracks generated during wafer sawing or laser cutting can propagate due to wafer handling and solar cell processing such as, phosphorous diffusion, anti-reflecting coating, front and back contact firing, and soldering of contact ribbons. It is recognized that development of a methodology for fast in-line crack detection and control is required to match the throughput of typical production lines.

In the resonance ultrasonic vibration (RUV) method, ultrasonic vibrations of a tunable frequency and adjustable amplitude are applied to the silicon wafer. Ultrasonic vibrations are generated in the wafer using an external piezoelectric transducer. They propagate into the wafer from the transducer and form standing acoustic waves at resonance frequencies, which can be analyzed with a broadband ultrasonic probe. Using a frequency sweep (f-scan) through a particular resonance mode, the RUV system provides accurate measurements of the resonance frequency, the maximum vibration amplitude, and the bandwidth (BW) of the resonance curve.

In the present design, the ultrasonic probe measures the longitudinal vibration mode characteristics by contacting the edge of the wafer with a controlled contact force. The importance of measuring longitudinal vibrations is that according to vibration theory and our own experiments, the resonance frequencies of the longitudinal vibration modes are independent of the wafer thickness (h), in contrast to the flexural vibrations, which are proportional to $h^{3/2}$. This is especially beneficial in the multicrystalline ribbon silicon wafers, which may have significant (up to 20%) thickness variations across the wafer, as well as from wafer to wafer. A typical full range acoustic spectrum obtained on a representative 125mm x 125mm Cz-Si wafer is shown in Figure 1. In the frequency spectrum, we observed a set of distinctive resonance modes, which are consistently reproduced from wafer to wafer in terms of the maximum amplitude, frequency position and BW. A single mode of vibration is selected to concentrate on from both the physical measurements as well as Finite Element Analysis data. Modeling of the wafers with and without cracks allows us to find relevant modes of longitudinal vibration.

The *HS1000 HiSPEED*™ Scanning Acoustic Microscope (SAM) by *Sonix Inc* was used for surface morphology and structural (bulk) integrity evaluation of the wafers further validating our data. Sets of similar wafers were acoustically analyzed to determine a signature frequency spectrum. In the frequency spectrum we were able to concentrate on certain modes of vibration and look for frequency shifts between similar

wafers indicating physical differences. An example using 100mm x 100mm pseudo-square Cz-Si wafers is presented in Figure 2. The wafer #39 with the shifted peaks were then taken to the SAM for crack length and orientation analysis. In Figure 3 we show a location and length of the crack on the wafer #39 identified previously by the RUV technique. We estimated a cub-millimeter range of crack length as a sensitivity limit of the RUV method for the crack detection in Cz-Si wafers. Multi-crystalline silicon wafers (ribbon and cast) are currently under investigation.

This work presented an experimental methodology using resonance ultrasonic vibration technique to detect cracks in crystalline silicon substrates for solar cells. A shift of the resonant frequency and line broadening of the longitudinal vibration mode versus crack length has been shown through experimentation as in Figure 4. The probable mechanism of the observed effect is a decrease in wafer stiffness affecting the vibration mode frequency with the mm-length peripheral crack. These dependences clearly demonstrate a direct relation of the extracted parameters on crack length. The RUV system allows fast data acquisition and analyses matching the throughput of solar cell production lines

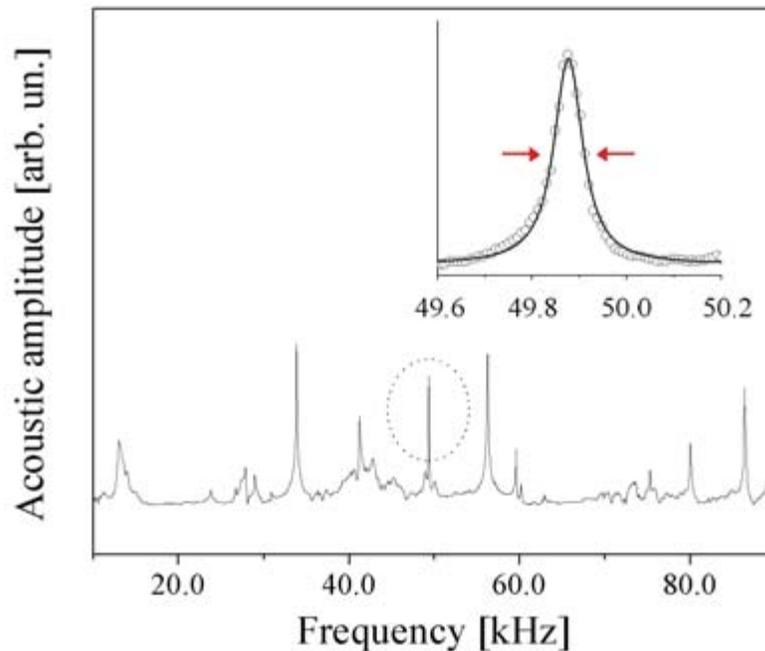Figure 1: Full range f-scan on 125mm x1 25mm Cz-Si wafer

Figure 2: Frequency peaks for a resonant mode with cracked wafer indicated by the peak shift
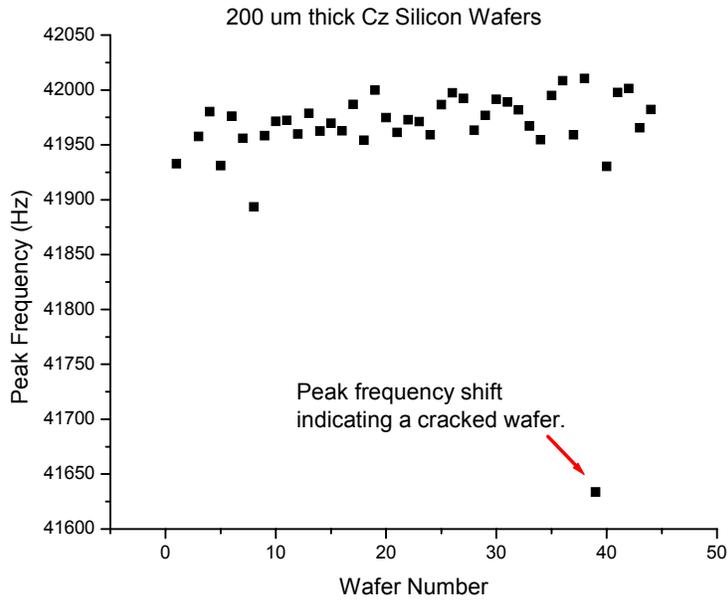

Figure 3: SAM image indicating crack length and crystallographic orientation
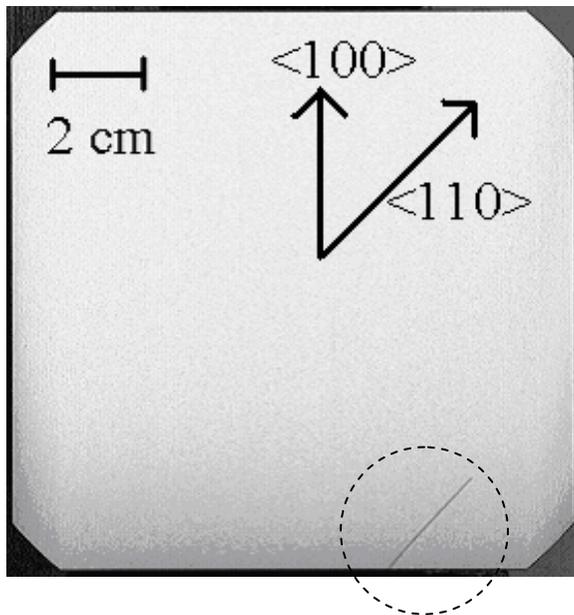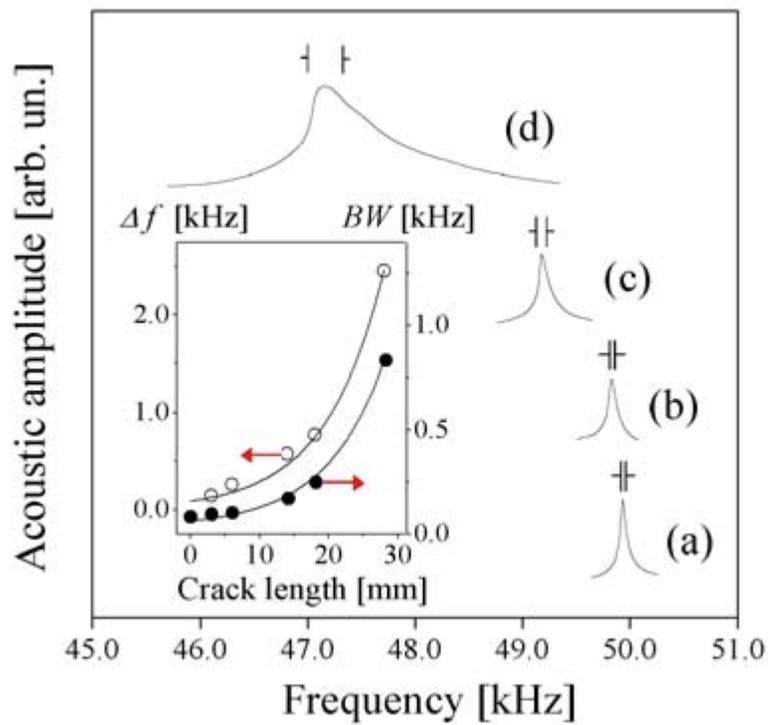
Figure 4: The A-mode spectra of (a) non cracked wafer, and wafers with different crack

lengths: (b) 3.0 mm, (c) 18 mm and (d) 28 mm. . The insert shows the dependence of

resonant frequency shift and also *BW* of the longitudinal mode spectra versus crack

length.

High Efficiency Thin Multicrystalline Silicon Solar Cells

Manav Sheoran[1, 2], Ajay Upadhyaya[1],Ajeet Rohatgi[1],
David E. Carlson[3], Mohan Narayanan[3]
[1]University Center of Excellence for Photovoltaics Research and Education
School of Electrical and Computer Engineering
Georgia Institute of Technology, Atlanta, GA 30332-0250
[2]School of Physics, Georgia Institute of Technology, Atlanta, GA-30332
[3]BP Solar, 630 Solarex Court, Frederick, MD 21703

Abstract

The influence of reducing the thickness of multicrystalline (mc-Si) wafer on the performance of a solar cell has been investigated. In this study we obtained 15.7% and 15.6% efficient un-textured 4 cm^2 solar cells, with single layer antireflection (AR) coating and full area Aluminum back surface field (Al-BSF) on a 115 μm and 150 μm thick cast mc-Si wafers. These are among the highest efficiency cells reported on such thin mc-Si wafers. There was about 5 mm bowing due to full Al back contact. Identical processing on 280 μm thick wafers gave cell efficiencies of ~16.6%. The ~1% difference in the efficiency of thick and thin cells was analyzed and back and front surface recombination velocities were identified as the main factor limiting the performance of thin cells compared to their thicker counterpart. Bulk lifetime was in excess of 100 μs, which made the thin cells quiet sensitive to BSRV and less dependent on lifetime. Device modeling was performed using PC1D in order to quantify and identify the factors that contributed to the observed loss in V_{oc} and J_{sc} and efficiency in the thin mc-Si cells.

1. Introduction

Cast multicrystalline Silicon is a cost effective alternative to single crystal Silicon for solar cells. One of the ways to drive down the cost is to use thin wafers without the loss in performance. However the use of thin wafers causes yield and bowing problems when using the conventional cell designs with full area Al-BSF. Yield enhancement can be achieved by going down on the learning curve over time while wafer bowing, which becomes serious for cells <200 μm [1], can be mitigated by the use of special low bow Aluminum paste or alternate device structures involving dielectric passivated rear surface. Finckenstein et. al. reported 15.2 % mc-Si cells on 180 μm thick wafer with full area Aluminum coverage on rear surface [2]. Tool et. al. reported an efficiency of 12.4% on 150 μm thick wafer with full area Al coverage [3]. Mittlestädt et. al reported 13.9% efficiency with full area Al coverage and 14.9 % SiN rear passivated 100 μm thick solar cells [4]. In this paper we report 15.7% and 15.6% efficient solar cells on 115 and 150 μm thick mc-Si wafers, respectively. These cells were fabricated by standard industrial process with full area Al coverage and single layer AR coating and no texturing. We analyzed the performance of solar cells made on thin Silicon (115 μm and 150 μm) and compared it to the performance of conventional 280 μm thick solar cells.

2. Experimental

Wafers with a good as-grown lifetime (25-50 μs) were chosen for this study. Three different thicknesses were used: 115 μm, 150 μm and 280 μm. These wafers were sourced from different ingots. All wafers had identical resistivity of ~1.5 Ω.cm, boron

doped and p-type. After chemical etching and RCA cleaning, lifetime measurements were performed using the Quasi-Steady-State Photo-conductance (QSSPC) technique, with the surface passivated with an iodine-methanol solution. Wafers were then diffused using liquid $POCl_3$ as the dopant source, resulting in a sheet resistivity of ~45 Ω/□. After the deposition of SiN via PECVD, solar cells were fabricated by screen printing Al on the back and silver grid on the front. These cells were then co-fired using an optimized process in a lamp-heated IR belt furnace, resulting in simultaneous formation of an Al Back Surface Field (BSF) and the Ag grid contact on the front. Finally, cells were annealed at 400 °C for 15 min in forming gas. There was appreciable bowing of both the 115 μm and 150 μm wafers (~5mm) due to the full area Aluminum coverage on the back.

3. Results and discussions

3.1 I-V results

It was found that the optimum firing conditions were different for thick and thin cells. The best condition for thin cells was attained by lowering both the temperature and belt speed as also suggested in ref [3]. I-V results of solar cells made on 115, 150 and 280 μm thick Si with new optimum firing conditions for thin cells are shown in Table 1. Cell data shows that 280 μm thick mc-Si gave 16.6% efficient cell while the 115 μm thick cells were ~15.7%. While this represents the highest efficiency cell reported on un-textured thin (115 μm) mc-Si, there was about 1% difference in efficiency of thick and thin cells.

Table 1: Summary of the I-V results and other parameters of 4 cm^2 solar cells made on 115, 150 and 280 μm thick p-type base

	Voc	Jsc	FF	Eff	n-factor	Rs	R-shunt	Number cells
	mV	mA/cm^2	%	%		ohm.cm^2	ohm.cm^2	
115 um								
Best	617	32.7	77.67	15.7	1.15	0.7	4645	
Average	613	32.6	76.34	15.3	1.21	0.8	11125	30
150 um								
Best	615	32.7	77.46	15.6	1.16	0.8	9296	
Average	612	32.6	76.43	15.3	1.15	0.9	15073	17
280 um								
Best	625	34.1	77.72	16.6	1.09	0.9	17911	
Average	624	34.0	76.45	16.2	1.11	1.0	20122	8

Table 1 shows a decrease in both V_{oc} and J_{sc} for the thin cells, which is partly attributed to lower back surface recombination velocity (BSRV). An efficiency difference of ~ 1% between the 280 μm and 115 μm Silicon wafers is consistent with results of Mittelstädt et.al. who obtained an efficiency of 15.1% on 300 μm and 13.9% on 100 μm substrates [4].

3.2 Device Modeling

The experimentally obtained internal quantum efficiency (IQE) for these cells was modeled in PC1D the device simulation program, using the R_s and R_{sh} along with the I-V parameters enlisted in Table 1 to understand the source of efficiency loss in thin devices. Experimentally determined values of bulk lifetime and reflectance were used. The internal reflectance parameters were found to be 92% at front surface and 67% for the rear surface (BSR), for first and subsequent bounces. Front and back surface recombination velocities were varied in the model calculations to match the cell data. These matched parameters are summarized in Table 2. As expected, BSRV was high (750 cm/s) but same for the 115 and 150 μm cells but decreased to 550 cm/s for the 280 μm cell. This indicated a better Al-BSF formation for the 280 μm cell. This is partly because the thinner cells cool down faster so that the, BSF formation and crystallization is not as good as compared to the thick cells. This is consistent with the findings of ref. [3].

Table 2: BSRV and FSRV derived from the fitting of IQE in PC1D for the three cells with varied thickness.

Device Thickness (μm)	Bulk Lifetime(μs)	Avg. Weighted Reflectance(%)	BSRV (cm/s)	FSRV (cm/s)
115	130	11.4	750	120000
150	100	11.4	750	70000
280	150	12.4	550	30000

A more detailed loss analysis was performed in PC1D to account for all the sources that contributed to the observed ~1% efficiency difference between the 280 μm and 115 μm solar cells. To accomplish that, first we modeled the performance of 280 μm thick device in PC1D. Then we changed the thickness from 280 μm to 115 μm to see the impact of thickness reduction alone. After that we increased the FSRV from 30000 cm/s to 120000 cm/s to obtain the performance loss due to higher FSRV in the thin cells. Next we changed the bulk lifetime from 150 μs to 130 μs, keeping the thickness at 115 μm, FSRV at 120000 cm/s and BSRV at 550 cm/s to account for the impact of lower lifetime in thin cell. Finally we changed the BSRV from 550 cm/s to 750 cm/s, keeping thickness at 115 μm, FSRV at 120000 cm/s and bulk lifetime at 130 μs to quantify the loss in performance due to higher BSRV alone. These results are summarized in the pie charts in Fig. 2 to show the effect of thickness, FSRV, BSRV and bulk lifetime on J_{sc}, V_{oc}, and cell efficiency. It is clear that FSRV and BSRV had significant impact but bulk lifetime difference did not contribute to appreciable loss in performance. This is because the diffusion length is greater than three times the thickness so that the performance becomes limited by the BSRV. It should be reiterated that these values of losses are only for the cells fabricated and analyzed in this study with the lifetime, FSRV, BSRV and thickness listed in table 2. These distribution of losses can be significantly different if one or more of the parameters are different in the finished cell, especially the BSRV.
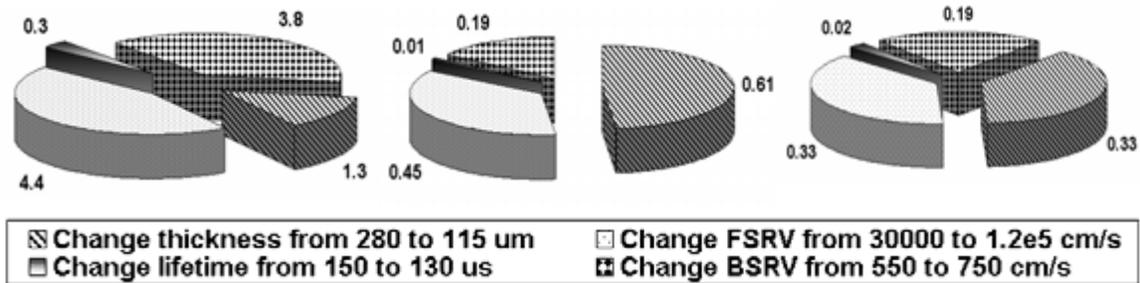
(a) Voc changes   (b) Jsc changes   (c) Efficiency changes

Figures 2: Pie chart showing the breakup in losses due to various factors on going from a 280 μm to a 115 μm solar cell fabricated in this study.

4. Conclusions

In conclusion, 15.7% and 15.6% efficient 4 cm^2 planar solar cells were fabricated on 115 μm and 150 μm thick mc-Si using conventional screen printed technology. These are some of the highest efficiency cells on ~100 μm thick mc-Si wafers. These cells had a single layer SiN AR coating with full area Aluminum coverage on the rear side. An efficiency reduction of ~1% was observed compared to 280 μm thick mc-Si cells processed simultaneously. A detailed and systematic analysis showed that efficiency gap is largely due to an inferior FSRV and BSRV for the thin cells. Somewhat lower BSRV of thin cells could be related to faster cooling of the sample as suggested in ref. [3]. Exact reason for lower FSRV is not fully understood at this time. The IQE analysis and matching in PC1D gave a BSRV value of 750 cm/s and a BSR of 67% for the 115 μm solar cell. Thicker cell (280 μm) had a BSRV of 550 cm/s and a BSR of 67%. Further understanding of loss mechanisms and process optimization can eliminate the efficiency gap between the thin and thick cells.

Acknowledgments

References

[1] F. Duerinckx , P. choulat, G. Beaucarne, R.J.S Young, M. Rose, J.A. Raby, *Proc. 19th EPVSEC, Paris*, 2004, pp 443 .
[2] B. F. Finckenstein, H. Horst, M. Spiegel, P. Fath, E. Bucher, *Proc. 28th IEEE PVSC, Anchorage, Alaska,* 2000, pp 198.
[3] C.J.J Tool, P. manshanden, A.R Burgers, A.W Weeber, *Proc. 29th IEEE PVSC, New Orleans*, 2002, pp 304.
[4] L. Mittelsätdt, A. Metz and R. Hezel, *Proc. 29th IEEE PVSC, New Orleans*, 2002, pp 166.
[5] A.Rohatgi, A.Upadhyaya, M.Sheoran, *Appl. Phys. Lett.* **86**, 054103, 2005.
[6] M. Schaper, J. Schmidt, H. Plagwitz and R. Brendel, "*Progress in Photovoltaics*, **13**, pp 381, 2005.

Approach towards 20% efficient screen-printed crystalline silicon solar cells

A. Ebong, M. Hilali, B. Rounsaville and A. Rohatgi

University Center of Excellence for Photovoltaics Research and Education, School of Electrical and Computer Engineering, Georgia Institute of Technology, 777 Atlantic Drive, Atlanta, GA 30332-0250

Abstract

In this paper we report on the fabrication, characterization and analysis of high-efficiency textured screen-printed and photolithography solar cells with high sheet resistance emitters ~100 Ω/sq. These cells were fabricated on 4.75 Ω-cm magnetically confined Czochralski (MCZ) silicon. The screen-printed and photolithography cells gave energy conversion efficiencies of 18.2% and 19.7%, respectively. There is about a 2% gap in the efficiency of planar screen-printed cells on 45 -Ω/ emitter with single layer AR coating and photolithography cells on 100-Ω/ emitter with double layer AR coating [1]. This indicates that using the textured and high sheet resistance emitters can reduce the efficiency gap between the two technologies from 2% to 1.5%. The 0.5% gain in efficiency can be attributed to improved surface passivation and blue response due to lightly doped emitters. The IQE data in conjunction with the PC1D computer modeling revealed a diffusion length of 1273 μm for these cells. After matching the performance of the 18.2% screen-printed cell by modeling, device modeling is extended to provide guidelines for achieving 20% screen-printed MCZ silicon solar cell.

1. Introduction

The majority of the commercial silicon solar cells today are made by screen-printed contacts on 30-55 Ω/sq emitters, rather than on 90-100 Ω/sq. shallow emitters to avoid high contact resistance and junction shunting. Heavy doping in the emitter results in reduced short-wavelength response and higher emitter saturation current density (J_{oe}), which reduces the cell performance. In order to improve the efficiency of screen-printed solar cell, high efficiency attributes such as surface texturing and high sheet-resistance emitters should be incorporated. In our previous work we demonstrated efficiency of >17% on planar FZ silicon by implementing the high sheet resistance emitter [2,3] and >18% when both high sheet resistance emitters and surface texturing were incorporated [4]. However, the commercial solar cells generally uses boron doped Czochralski (CZ) silicon, which suffers from the light induced degradation [5].

To circumvent the light induced degradation observed in the boron-doped CZ, the gallium doped CZ has been introduced and efficiency in excess of 22% [6] with photolithography contacts has been demonstrated. Also, magnetically confined CZ (MCZ) grown substrate has given efficiency of >24% [7] with photolithography contacts. By using a belt emitter in conjunction with the photolithography contact (one mask only) we have demonstrated an efficiency of >18% without surface texturing on MCZ substrate [8]. Screen-printed contacts on gallium-doped CZ with high sheet-resistance emitters has produced >16% efficiency without texturing and >17% with texturing [9].

In this work we applied the high sheet resistance emitters and surface texturing to improve the efficiency of screen-printed cells fabricated on MCZ silicon wafers. In order to

assess loss due to the screen-printed contacts, selected cells with photolithography contacts were fabricated for comparison. After evaluating the loss mechanisms through detailed characterization and modeling, we have developed a roadmap through computer modeling on how to achieve 20% efficient screen-printed solar cells on MCZ silicon.

2. Device fabrication

Planar MCZ silicon wafers of 4.75 Ω-cm resistivity were textured, both sides, cleaned in 1:1:2 H_2SO_4:H_2O_2:H_2O for 5 minutes, followed by a 3 min rinse in de-ionized (DI) water. This was followed by a clean in 1:1:2 HCl:H_2O_2:H_2O for 5 minutes and a 3 min rinse in DI water. Next the wafers were dipped in 10% HF for 2 minutes, followed by a 30 second rinse in DI water. The wafers were loaded in the diffusion furnace for the n^+ emitter formation. A diffusion temperature of 843°C was used to achieve the 100-Ω/ emitters. After the phosphorus glass removal and another clean, the wafers were divided into two groups; A and B, respectively, for screen-printed and photolithography front contacts. A thin (100 Å) rapid thermal oxide (RTO) was grown on group B samples at 900°C for 2 minutes in RTP. A 50 kHz PECVD SiNx AR coating was then deposited on the emitters in the groups A and B samples. Next, an Al paste was screen-printed on the backside and dried at 200°C. The Ag grid was then screen-printed on top of the SiNx film, for group-A wafers, dried at 200°C and then the Ag and Al contacts were co-fired in a lamp-heated three-zone infrared belt furnace. The Group-A samples were edge isolated before forming gas anneal for 18 minutes and characterized by light I-V as well as the internal quantum efficiency (IQE) measurements. The group-B samples were fired in RTP to form Al BSF before the samples were coated with photo-resist and baked to open the contacts. After the evaporation of Ti/Pd/Ag followed by the lift-off step, the cells were electroplated in Ag plating solution. The Group-B cells were characterized by light I-V and spectral response measurements after edge isolation and forming gas anneal for 18 minutes.

3. Results and Discussion

3.1 Light I-V characterization

Table 1: Electrical output parameters of MCZ screen-printed and photolithography cells.

Cell ID	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Efficiency (%)	R_s (Ω-cm^2)
SP MCZ (4.75)-2-4	**628**	**38.2**	**75.7**	**18.2**	**0.926**
SP MCZ (4.75)-2-5	627	38.2	75.9	18.2	0.830
SP MCZ (4.75)-2-6	628	38.2	75.6	18.1	0.942
SP MCZ (4.75)-2-8	627	38.4	75.5	18.2	0.910
PL MCZ (4.75)-1	**627**	**39.9**	**78.8**	**19.7**	**0.398**
PL MCZ (4.75)-4	627	39.8	78.7	19.7	0.425
PL MCZ (4.75)-7	623	39.8	78.3	19.4	0.491

SP – screen-printed; PL – photolithography

Table 1 shows the light I-V characteristics of the textured screen-printed MCZ cells, with photolithography contacts and high sheet resistance emitters. The open circuit voltage (V_{oc}) of the SP and PL cells was the same and commensurate with the high resistivity material. The fill factor on the SP cell is lower by ~0.031 than that obtained on the photolithography cells. This can be attributed to the series resistance which is ~0.526 Ω-cm^2 higher. Model calculation showed that the measured difference of 0.526 Ω-cm^2 in series resistance could fully account for

the loss in FF. A further characterization by the Suns-V_{oc}, to ascertain the impact of the series resistance on the fill factor, is shown in Table 2. The Suns-V_{oc} results showed an 80% fill factor for the SP as well as the PL cells in the absence of series resistance. This loss in FF accounts for ~0.7% loss in cell efficiency. The remaining 0.8% loss in efficiency is due to the loss in J_{sc}, which is analyzed below.
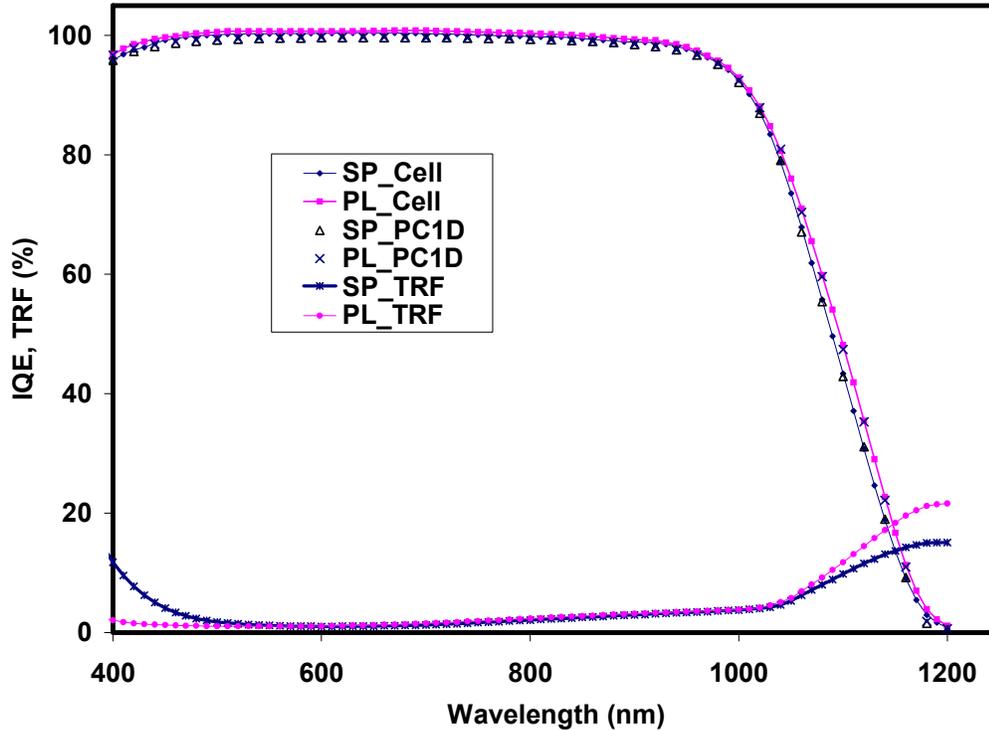

Figure 1: Internal quantum efficiency of SP and PL cells fabricated on high sheet resistance emitter and textured surface.

The short circuit current density showed a difference of 1.7 mA/cm^2 between the SP and PL cells. The IQE measurements on SP and PL cells were only slightly different from each other in the short wavelength as shown in Figure 1, therefore the difference in the J_{sc} may be explained by front surface recombination velocity (FSRV), grid shading and front reflectance due to AR coating and back surface reflectance. This is shown pictorially in Figure 2. The PC1D calculation (Table 3) gave an FSRV value of 60,000 cm/s for the SP and 50,000 cm/s for the PL cell. Model calculations showed that the ΔFSRV of 10,000 cm/s is responsible for only 0.1-mA/cm^2 loss in J_{sc}. There was no appreciable difference in the long wavelength IQE up to 1 μm. This is consistent with the high lifetime in both the cells and identical BSRV. This lifetime and BSRV did not contribute to any loss in J_{sc}. There was a slight difference in the very long wavelength response (> 1μm), which indicated a difference in BSR. The back surface reflector (BSR) value of 72% matched the long wavelength response of the PL cell while 66% BSR matched the SP cell. Model calculations showed that the ΔBSR of 6% accounts for ~0.2-mA/cm^2 loss in J_{sc}. The difference in the BSR can be attributed to the difference in the Al BSF formation temperature. This can be recovered by setting the peak temperature in the belt furnace to be identical to the RTP system.

Most of the current loss is due to the difference in grid shading factor, which in this case is about 6% for SP cells and 3% for PL cells. Currently, our SP grid contains finger widths of ~135 μm compared with only ~25 μm for the PL grid. Grid shading in the SP cell therefore accounts for about 1.1 mA/cm^2 (3% of 39.9) of the J_{sc} difference indicating that substantial improvement can be realized if fine-line ($\leq$75 μm) printing can be implemented at low cost. The reflectance due to the difference between SiNx AR coating (n~2.03) for SP and RTO/SiNx AR coating for PL cells accounts for 0.3 mA/cm^2 (0.75% of the 39.9). AR coating model calculation revealed that reflectance loss can be restored by using SiNx with higher index of refraction (n = 2.1).

Table 2: Suns-V_{oc} output parameters for the SP and PL MCZ cells

Cell ID	V_{oc} (mV)	FF (%)	Eff. (%)	J_{o1} (FA/cm^2)	J_{o2} (nA/cm^2)
PL MCZ (4.75)-1	622	80.2	19.9	780	59
PL MCZ (4.75)-4	623	80.3	19.9	810	58
SP MCZ (4.75)-2-4	627	80.7	19.3	880	45
SP MCZ (4.75)-2-8	625	80.3	19.2	930	53

Table 3: Modeling parameters for the 18.2% and 19.7% SP and PL cells

Cell Parameters	**SP Textured MCZ Cell**	**PL Textured MCZ cell**
Base Resistivity (Ω-cm)	4.75	4.75
R_s (Ω-cm^2)	0.926	0.398
R_{sh} (Ω-cm^2)	68299	5688
n_2	2.0	2.0
J_{o2} (nA/cm^2)	45	29
Emitter sheet resistance (Ω/sq)	100	100
Surface concentration (cm^3)	1.5x10^{20}	1.5x10^{20}
Texture angle (degrees)	54.7	54.7
Texture depth (μm)	3	3
τ_{bulk} (μs)	506	506
BSRV (cm/s)	200	200
R_{back} (%)	66	72
FSRV	60,000	50,000
Grid shading	6%	3%
Modeled V_{oc} (mV)	625.4	627.5
Modeled J_{sc} (mA/cm^2)	38.6	39.9
Modeled FF (%)	75.8	78.7
Modeled Efficiency (%)	18.3	19.7

Table 3 shows the modeling parameters for the SP and PL on textured 100 Ω/sq cells. The saturation current density J_{o1} and junction leakage current J_{o2} were measured using Suns-V_{oc} for the SP and PL cells and these values are shown in Table 2. These values were used in modeling the cells along with other parameters that are listed in Table 3. According to these PC1D calculations, the parameters required for achieving 20% on 4.75 Ω-cm MCZ screen-printed efficiency include: FSRV of 40,000 cm/s, BSRV of 180 cm/s, J_{o2} of 1.5x10^{-8} A, R_s of 0.4 Ω-cm^2, R_{sh} of 68299 Ω-cm^2, grid shading of 4%, fill factor of 79.6%, J_{sc} of 39.7 mA/cm^2 and

Voc of 633.2 mV. However, if the BSRV can be reduced to 100 cm/s for this 4.75 Ω-cm MCZ it will relax the requirement on R_s, FF and AR coating, in this case 20% cell can be achieved with an R_s = 0.6 and single layer AR, resulting in a J_{sc} of 39.7mA/cm^2 and V_{oc} of 639.4 mV.
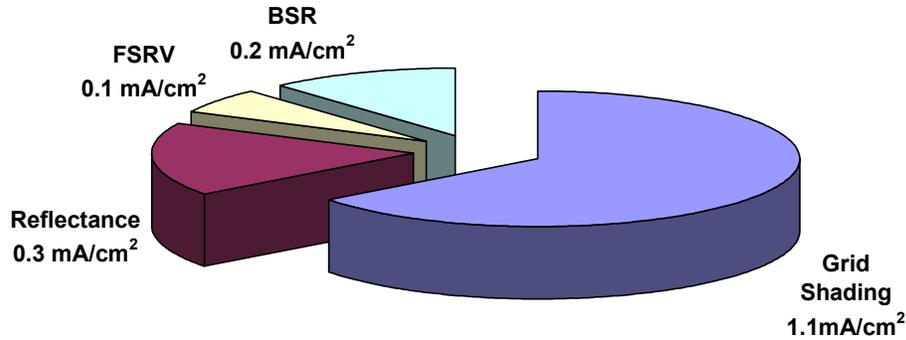

Figure 2: Components of the 1.7 mA/cm^2 ΔJsc between SP and PL cells.

4. Conclusion

We have modeled, fabricated, characterized and analyzed textured screen-printed and photolithography solar cells on MCZ silicon material. A simple cell process sequence involving emitter formation using POCl$_3$, Al BSF, PECVD SiNx AR coating, and belt furnace co-firing of front and back screen-printed contacts was used for commercial type cells. The photolithography sequence involved a two-minute RTO growth after the POCl$_3$ diffusion before the PECVD SiNx deposition, RTP Al BSF formation, finger openings, evaporation and electroplating of silver. Both the processes resulted in very high post process lifetimes (>500 μs at 1E15 cm^3 injection level). The screen-printed and photolithography cells exhibited efficiencies of 18.2% and 19.7%, respectively. Detailed analysis was performed to explain the difference in this performance and provide guidelines for achieving ~20% SP cells.

The open circuit voltages on both screen-printed and photolithography cells were the same. However the ΔJ_{sc} of 1.7 mA/cm^2 and ΔFF of 0.031 led to 1.5% efficiency loss for the screen-printed cells. Model calculation showed that the measured difference of 0.526 Ω-cm^2 in series resistance could fully account for the loss in FF. This loss in FF accounts for 0.7% loss in cell efficiency. The remaining 0.8% loss in efficiency is due to the loss in J_{sc}, which is analyzed below.

The IQE measurements on SP and PL cells were only slightly different from each other in the short wavelength. The PC1D calculation gave an FSRV value of 60,000 cm/s for the SP and 50,000 cm/s for the PL cell. Model calculations showed that the ΔFSRV of 10,000 cm/s is responsible for only 0.1-mA/cm^2 loss in J_{sc}. There was no appreciable difference in the long wavelength IQE up to 1 μm. This is consistent with the high lifetime in both the cells and identical BSRV. This lifetime and BSRV did not contribute to any loss in J_{sc}. There was a slight difference in the very long wavelength response (> 1μm), which indicated a difference in BSR. The back surface reflector (BSR) value of 72% matched the long wavelength response of the PL cell while 66% BSR matched the SP cell. Model calculations showed that the ΔBSR of 6% accounts for ~0.2-mA/cm^2 loss in J_{sc}. AR coating difference accounted for 0.3 mA/cm^2 loss in

J_{sc}. The grid shading difference of 3% accounted for the remaining 1.1-mA/cm^2 loss in J_{sc} of the SP cell.

Through Suns-V_{oc} characterization, it was noted that pseudo FF is ~0.80 for both the cells so efficiencies of 19.3% screen-printed and 19.9% photolithography cells could be achieved, if the series resistance is completely eliminated. This will reduce the efficiency gap between the two technologies to ~0.6%, which is accounted for by higher shading from the grid. If the shading is reduced to less than 5% through the use of hot melt paste, with <75 μm finger width, the SP and PL cells can become nearly equal. Thus a 20% screen-printed, 4.75 Ω-cm MCZ, solar cell can be achieved with the grid shading of ~4.5%, BSRV of 100 cm/s, J_{sc} of 39.7 mA/cm^2, V_{oc} of 639.4 mV, FF of 78.8%, $R_s = 0.6$ Ω-cm^2, FSRV of 40,000 cm/s and a BSR of 66%.

5. References

1. P. Doshi, J. Mejia, K. Tate and A. Rohatgi "Modeling and characterization of high efficiency silicon solar cells fabricated by rapid thermal processing, screen printing, and plasma-enhanced chemical vapor deposition", IEEE Trans. Electron Dev. 44 (9) 1997, 1417-1424.
2. M. M. Hilali, A. Rohatgi and S. Asher, "Development of screen-printed silicon solar cells with high fill factors on 100 Ω/sq emitters", IEEE Trans. on Elect. Dev., 51, no.6, 2004, pp948-955.
3. A. Ebong, M. Hilali, V. Upadhyaya, B. Rounsaville, I. Ebong and A. Rohatgi 'High efficiency screen-printed planar solar cells on single crystalline silicon materials", Proc. 31st IEEE Photovoltaics Specialist Conference, Orlando, Florida, 2005, pp.1173-1176.
4. M. Hilali, K. Nakayashiki, A. Ebong and A. Rohatgi, "Investigation of high-efficiency screen-printed textured Si solar cells with high sheet-resistance emitters", Proc. 31st IEEE Photovoltaics Specialist Conference, Orlando, Florida, 2005, pp.1185-1188.
5. R. L. Crab, Photon induced degradation of electron irradiated silicon solar cells. Proc. 9th IEEE PV Specialist Conference, Silver Springs, 1972, pp.329-330.
6. S. Glunz, J. Lee and S. Rein "Strategies for improving the efficiency of CZ-Silicon solar cells" Proc. 28th IEEE Photovoltaics Specialist Conference, 2000, pp.57-60.
7. J. Zhao, A. Wang and M. Green "24.5% Efficiency silicon PERT Cells on MCZ substrates and 24.7% efficiency PERL cells on FZ substrates" Progress in Photovoltaics: Research and Applications; 7, (1999), 471-474.
8. A. Ebong, Y. H. Cho, M. Hilali, A. Rohatgi and D. Ruby, "Rapid thermal technologies for high-efficiency silicon solar cells", Solar Energy Materials and Solar Cells, 74 (2002) pp.51-55.
9. A. Ebong, V. Meemongkolkiat, M. Hilali, V. Upadhyaya, B. Rounsaville, I. Ebong, A. Rohatgi, G. Crabtree, J. Nickerson and T. L. Jester, "Variation of screen-printed solar cell performance along commercially grown Ga- and B-doped Czochralski ingots" 14th Workshop on crystalline silicon solar cells and modules materials and processes, 2004, pp.254-258.

WAFERING RESEARCH AT FRAUNHOFER ISE

D. Kray, S. Baumann, K. Mayer, F. Haas, M. Schumann, M. Bando, A. Eyer and G. P. Willeke

Fraunhofer Institute for Solar Energy Systems ISE, Heidenhofstr. 2, D-79110 Freiburg,
Phone: ++49 761 4588 5355, Fax: ++49 761 4588 9250, email: daniel.kray@ise.fraunhofer.de

INTRODUCTION

The crystalline silicon wafer technology has today's largest market share in terrestrial photovoltaics. After the crystallisation of very pure blocks, these have to be sliced into thin wafers that are processed into solar cells afterwards. Today, this step makes up about 20% of the total solar module cost [1] which clearly justifies research efforts in this area. Thus Fraunhofer ISE has started a new market area "wafer technology" to optimize the existing multi-wire slurry saw (MWSS) and to develop mid-term alternatives as the stream etching [2] and laser-chemical etching LCE [3].

In this paper, the new market area is presented concerning its experimental capabilities as well as current research results in the area of MWSS.

MULTI-WIRE SLURRY SAW

Currently, practically all silicon wafers for photovoltaics and microelectronics are cut from large mono- or multicrystalline blocks by the MWSS technique. The principle is depicted in fig. 1: A thin steel wire (of about 180-160 μm diameter and several hundreds of km long) is wrapped many times around two or four wire guides thus producing a wire web. The wire is accelerated to more than 10 m/s in the cutting process and wetted with a slurry (composed of mineral oil or polyethylene glycol with small SiC particles). When the silicon is pressed against this moving wire, a mechanical cutting process is produced by the interaction of wire, SiC, carrier liquid and silicon. Even though the method is used since many years already, the
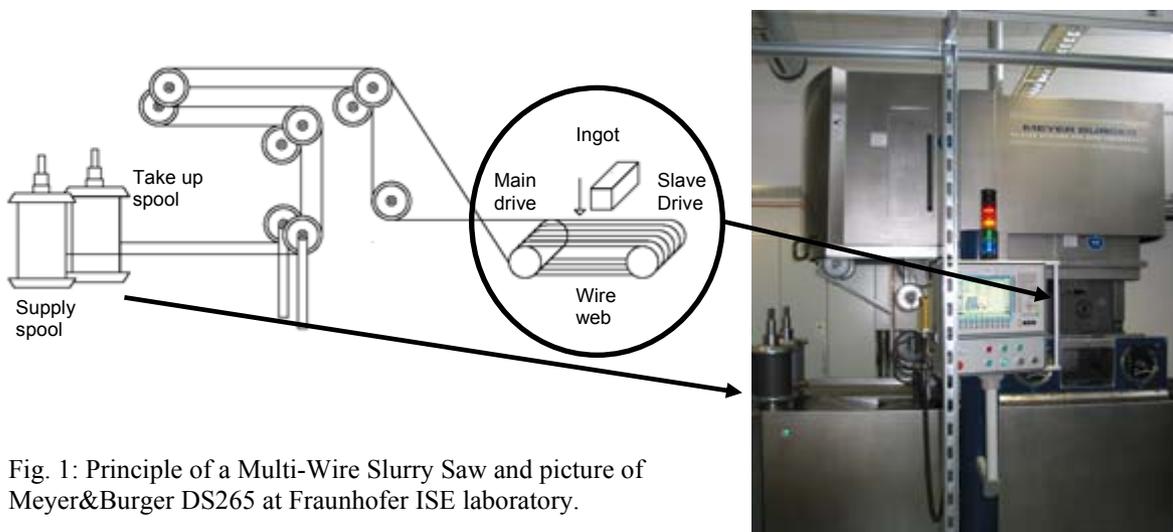

Fig. 1: Principle of a Multi-Wire Slurry Saw and picture of Meyer&Burger DS265 at Fraunhofer ISE laboratory.

Tab. 1: Power usage and energy consumption of cutting processes with different loading with 100x100x25 mm³ silicon blocks. The calculated net energy consumption per wafer does not represent the complete energy consumption for wafer cutting since it does not take into account the idle power consumption.

Exp. no.	No. Blocks	Cutting direction	Idle Power [kW]	Mean cutting power [kW]	Net mean cutting power [kW]	Net mean cutting power [W/wafer]	Cutting time [min]	Net Energy consumption [kWh/wafer]
2	1	One way	0.84	2.88	2.04	39.2	245	0.160
3	3	One way	0.88	4.64	3.76	24.1	245	0.098
6	5	One way	0.86	6.47	5.61	21.5	245	0.088
5	11	One way	0.92	11.23	10.31	18.0	245	0.074
7	3	Back and forth	0.79	3.71	2.92	18.7	261	0.081

exact process mechanisms are still unclear [4] and wafer producers are guided mostly by empirical studies.

To enable industrial-scale optimisation and research in this field, a small production wire-saw (Meyer&Burger DS265) was installed at Fraunhofer ISE labs. This machine is capable of cutting blocks of up to 200x200x300 mm³ or two ingots of 125x125x300 mm³ with a maximum wire length of 220 km and wire thickness down to 100 μm. The small slurry tank of only 120l enables us to conduct industrial-scale cutting experiments with a minimum of consumables. The operating software is very versatile and can automatically log data from measurement devices every four seconds. This includes also the viscosimeter that determines the viscosity of the slurry in the tank. Further measurement systems for wire deflection or oscillation as well as video cameras can easily be added into the architecture to give a clear view of what happens during multi-wire slurry cutting.

CUTTING EXPERIMENT EVALUATION

After cutting some silicon blocks with defined saw parameters, all wafers are thoroughly analysed: First, a breakage statistics is made about how many wafers break in the saw, in the precleaning under hot water, in the manual singularization, in the cleaning process or in handling steps. Afterwards, the geometry of all cleaned wafers is measured using an Eichhorn+Hausmann MX203-6-37 system which works via capacitance measurements of 37 sensors on an area of 125x125 mm². The thickness, the total thickness variation as well as the

Tab. 2: Statistics of geometric parameters of wafers from cutting processes with different loading. For each block the first and last two wafers have not been taken into account for the statistics.

Exp. no.	No. Blocks	Cutting direction	Number of wafers	TTV [μm]	Standard deviation TTV [μm]	Total warp [μm]	Standard deviation Total warp [μm]
2	1	One way	33	22.1	3.1	16.6	3.5
3	3	One way	117	23.4	5.0	30.8	22.4
6	5	One way	223	12.9	3.9	33.4	24.9
5	11	One way	462	19.2	4.0	20.7	16.0
7	3	Back and forth	133	6.3	1.9	12.9	7.8

total warp are recorded as a basis for the geometry statistics. Then, some wafers are selected to measure high resolution surface maps using an FRT MicroProf optical surface profiler that uses the effect of chromatic aberration for the measurement of height differences with a lateral resolution of 1-2 μm. From the surface profiles parallel and perpendicular to the wire movement, a complete reconstruction of the local kerf shape can be realised and also local values for roughness and waviness can be extracted.

In the following steps, breakage tests and lifetime measurements after subsequent etch steps can help to determine the mechanical properties as well as the depth of the surface damage layer. Concerning the fundamental mechanical assessment of wire-sawn wafers, we have a strong partnership with the Fraunhofer Institute for Mechanics of Materials IWM in Freiburg and Halle, Germany.

INFLUENCE OF BLOCK LENGTH

In the following we shortly present MWSS cutting experiments with different loading of silicon blocks. We used multicrystalline blocks of 100x100x25 mm^3 size and repeated the cutting process with identical machine parameters and a varying number of these small blocks, cf. tab. 1 and 2. However it is to note that the slurry composition changed over the experiments since the original slurry mixture has been continuously used for all cuts. Additionally, the wire has been used several times so that every cut has been done with different wire conditions. This shows clearly the difficulty of wire sawing experiments: There is a pronounced wear of all consumables which is quite hard to quantify. An optimum scientific approach would require only one parameter to be changed from one experiment to another so this would mean to discard the costly wire and slurry after each single cut. This can not be realised due to the high cost so one has to cope with this suboptimal situation.

In fig. 2 on the left side the net main power of the wire-saw is shown for the experiments in tab. 1 and 2. The larger energy consumption with higher loading can clearly be seen.

From the recorded machine data we see also that the loading of the saw has a strong influence on the specific energy necessary for cutting one kerf (some kind of *sawing*
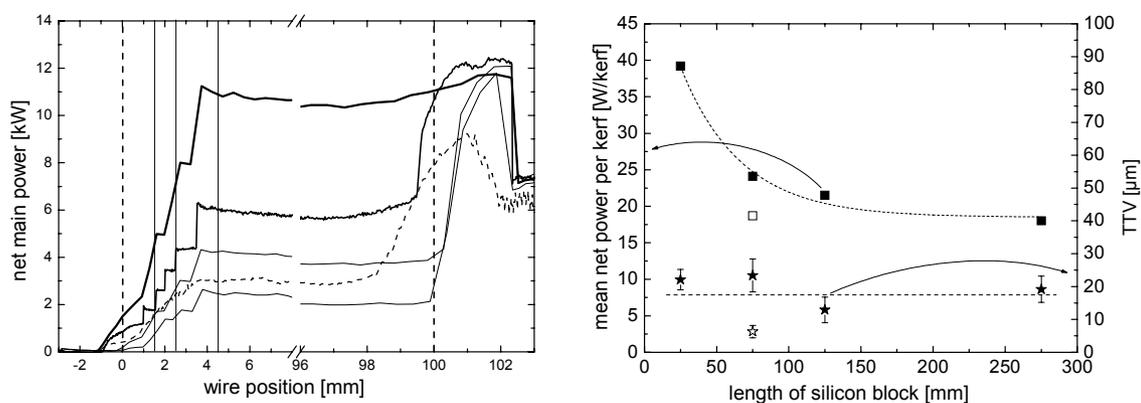

Fig. 2: Left graph: Net main power of wire saw with different loading depending on wire position (note the broken x-axis). The solid lines with different thicknesses represent monodirectional cutting of 1, 3, 5 and 11 mc-Si blocks (100x100x25 mm^3). The dashed line shows the 2-minutes-mean value of back-and-forth cutting of 3 blocks. On the x-axis, the wire position is shown, the vertical dashed lines represent the block edges. Up to a depth of 4.5 mm, a ramp-up of the cutting parameters is realized (with parameter changes indicated by the solid vertical lines) to smoothly cut into the block. The strong raise in power at the end of the cut comes from the cutting of the wire into the glass plate.
Right graph: Specific energy consumption / TTV dependent on block length. Solid symbols represent monodirectional cutting, open symbols back-and-forth cutting. The upper dashed line is a monoexponential fit to the data.

efficiency). As shown in fig. 2 on the right side, the net energy consumption in kWh per wafer (left y-axis) decreases exponentially (cf. exponential fit in the graph) with the length of the cut silicon block. One would expect that when one doubles the silicon length to be cut, the net power would also double but this is obviously not the case. From the right y-axis in fig. 2 we see that the TTV does not reflect the different energy consumption nor does the kerf loss change over the experiments so the question remains open where this extra energy is dissipated.

An interesting fact is that the scheme of cutting with back and forth oscillating wire seems to have advantages over the standard mono-directional cutting. The net energy consumption is 17% lower with only 7% longer cutting time compared to the standard process. Additionally, the wafer geometry is much better with mean TTV of 6.3 ± 1.9 μm and total warp of 12.9 ± 7.8 μm compared to TTV > 12 μm and total warp > 16 μm. This cutting scheme seems very promising since also the wire consumption is much lower than for the mono-directional cutting.

DISCUSSION, CONCLUSIONS AND OUTLOOK

With the new installations at Fraunhofer ISE, applied and fundamental research concerning the industrial wire-sawing process become possible. Experimental testing of consumable as SiC, liquid carrier and wires can be offered to the industry. A thorough assessment concerning the mechanical and electrical quality for solar cell production gives optimum feedback for optimising consumables and processes in modern wire-sawing. Together with PV-TEC, a complete Photovoltaic Technology Evaluation Center, which is currently built up at Fraunhofer ISE, we can even offer the evaluation of the effects of optimised wire-sawing on the industrial solar cell production.

As an example, we have shown the influence of silicon block length and the wire movement scheme on the wafer geometry and the energy consumption. Neglecting the wear of wire and slurry, we see a strong influence of silicon loading on the energy necessary to cut one kerf. Higher loadings give more efficient cutting processes for monodirectional cutting. Back-and-forth cutting seems to have strong advantages since the energy and wire consumption decreases considerably together with clearly improved wafer geometry.

Possible future alternatives to the MWSS are also investigated, especially the laser-chemical etching (LCE). Current research results are published elsewhere [5].

Acknowledgements

REFERENCES

[1]   T. L. Jester, "Crystalline silicon manufacturing progress", Progr. Photovolt., 99-106(2002)
[2]   D. Kray and G. P. Willeke, "50 μm wafering techniques - first experimental results", *12th NREL workshop on crystalline silicon solar cell materials and processes*, (2002)
[3]   D. Kray, S. Baumann, K. Mayer, A. Eyer et al., "Novel Techniques for Low-Damage Microstructuring of Silicon", *Proceedings of the 20th European Photovoltaic Solar Energy Conference*, (2005) in press
[4]   C. Funke, O. Sciurova, O. Kiriyenko, and H. J. Möller, "Surface Damage from Multi Wire Sawing and Mechanical Properties of Silicon Wafers", *Proceedings of the 20th European Photovoltaic Solar Energy Conference*, (2005) in press
[5]   D. Kray, S. Baumann, K. Mayer, A. Eyer et al., submitted to Progress in Photovoltaics: Research and Applications

Determination of Impurities Introduced During Solid Phase Crystallization of Amorphous Silicon Thin Films

Robert C. Reedy, Eugene Iwaniczko, Qi. Wang, Yueqin Xu, and David Young

National Renewable Energy Laboratory
1617 Cole Blvd., Golden, CO 80401

Thin-film silicon solar cells are produced on a variety of low-cost substrates by a variety of methods. Polycrystalline silicon has better material properties than hydrogenated amorphous silicon (a-Si:H) [1], and solar cells produced from these films are not subject to light-induced degradation effects. Crystallized films grown by plasma-enhanced chemical vapor deposition (PECVD) have been shown capable of producing adequate 8-9% solar cell modules [2]. Deposition of electronic-grade a-Si thin films by PECVD is typically done at a low rate, between $1 - 10$ Å/s. Higher deposition rates (greater that 100 Å/s) of good quality a-Si:H films can be achieved by hot wire chemical vapor deposition (HWCVD) [3]. Recrystallization of these films shows potential for solar cell applications.

Films of hydrogenated amorphous silicon (a-Si:H) were deposited by HWCVD and PECVD onto low-cost substrates. Solid phase crystallization (SPC) was achieved by annealing the films over a wide temperature range using a variety of systems. Substrate materials, e.g., glass, stainless steel, and ceramic, all have constituents that can be detrimental to material quality if incorporated into the recrystallized silicon. SIMS was used to study the incorporation of impurities from substrate relative to process conditions, and substrate selection. The influence of metallic substrate coatings and diffusion barriers, e.g., SiO_2 and SiN_x, is addressed.

[1]   K. Pangal, J. C. Sturm, and S. Wagner, Integrated amorphous and polycrystalline silicon thin-film transistors in a single silicon layer. IEEE Transactions on Electron Devices 48, 707 (2001).
[2]   M. A. Green, P. A. Basore, N. Chang, D. Clugston, R. Egan, R. Evans, D. Hogg, S. Jarnason, M. Keevers, P. Lasswell, J. O'Sullivan, U. Schubert, A. Turner, S. R. Wenham, and T. Young, Crystalline silicon on glass (CSG) thin-film solar cell modules. Solar Energy Materials and Solar Cells 77, 857 (2004).
[3]   A. H. Mahan, Y. Xu, D. L. Williamson, W. Beyer, J. D. Perkins, M. Vanecek, L. M. Gedvilas, and B. P. Nelson, Structural properties of hot wire a-Si:H films deposited at rates in excess of 100 Å/s. Journal of Applied Physics 90, 5038 (2001).

Dislocation Generation by Thermal Stresses in Silicon

Bhushan Sopori,[1] Przemyslaw Rupnowski,[1,2] Davor Balzar,[2] and Pete Sheldon[1]

[1] National Renewable Energy Laboratory, Golden, CO
[2] University of Denver, Denver, CO

ABSTRACT

In this study, the mechanical behavior of silicon wafers during optical thermal processing was analyzed experimentally and numerically. The experimental study included wafer processing and defect etching, followed by examination of the plastic region of the wafer. Laser scanning and optical microscopy were employed to count and visualize dislocation etch pits in the plastic region. By comparing the experimental and simulation results, it was found that the numerical model could successfully predict the location of the plastic zone in a silicon wafer during thermal processing.

INTRODUCTION

The photovoltaic (PV) industry uses low-cost single- and multicrystalline silicon (mc-Si) for commercial fabrication of solar cells. These materials are grown at high speeds using lower-grade Si feedstock. High crystal growth rates generate excessive thermal stresses with concomitant high dislocation densities. Because defects interact with impurities, defects strongly control the performance of Si solar cells fabricated on both the single- and mc-Si substrates. To improve material quality for higher-efficiency solar cells, it is important to both understand the generation of defects and to develop methods to ameliorate their influence on solar cell performance. Considerable work has been done—and continues to be done—on the role of thermal stresses in generating defects, buckling, and residual stresses during crystal growth [1-3]. However, severely lacking is a quantitative description of defect formation in rapidly grown materials, particularly in (cast and ribbon) mc-Si. One basic issue in predicting the dislocation distribution in an ingot or ribbon is relating dislocation generation to stress/strain distributions. Dillon, Sumino, and Hassen (DSH) [1,2] established a commonly used relationship between dislocation generation and shear stress. This relation is based on stress-strain curves obtained by applying tensile deformation at a constant strain rate. Other authors have performed calculations using the DSH model, but little or no data exist on the experimental verification.

We are performing both experimental and theoretical studies to establish a relationship between the thermal stresses and resultant dislocation distributions for single- and mc-Si wafers. Experiments involve subjecting single- and mc-Si wafers (typically 4.5 in. x 4.5 in.) to predetermined thermal stresses by exposing them to known temperature distributions. The resultant dislocation distributions are measured by a commercial instrument, GT-PVSCAN [4,5], which rapidly maps dislocation distribution over the entire wafer. These distributions are correlated with the theoretical stress distributions calculated by finite-element (FE) modeling, which includes appropriate boundary conditions for mc-Si. The physical mechanism associated with this effect is that when thermal stress exceeds the critical shear stress in grains of a particular preferred orientation (those with slip directions along the shear), they locally yield and relieve stress by local generation of dislocations. This mechanism, which leads to "clustering" of

defects, causes regions of high dislocation density to be surrounded by regions of low dislocation density, has a profound effect on the solar cell performance. We will compare the experimental results of dislocation distributions in some commercial PV Si wafers/ribbons with our theory, which includes plastic behavior, and discuss recommendations for improving material quality.

EXPERIMENTAL APPROACH

Circular monocrystaline Si wafers of 3-in diameter and polished on one side were used in this study. Since only prime-grade wafers were tested, it can be assumed that before a heat treatment, the material was dislocation free. The wafers were processed in an optical furnaces equipped with a linear light heater (see Figure 1). The rough, unpolished side of the wafer was illuminated. The energy flux distribution on the surface of the wafer generated by the heater was almost constant along the heater axis and highly non-uniform in the direction perpendicular to that axis. This non-uniform profile of the energy is shown in Figure 2. During thermal processing, the wafer was placed on a belt furnace that could move the wafer in the direction perpendicular to the heater axis. Therefore, both static and dynamic processing could be performed. In the dynamic case, the wafer moved below the heat source with a constant speed in the range of 3 to 20 inches/minute, whereas in the static case, the belt did not move and the light was concentrated along a line passing through the center of the wafer. The temperature of the wafer was measured using K-type thermocouples that were cemented to the bottom, polished surface of the wafer. The amplitude of the heat flux was adjusted so that the maximum temperature in the wafer was below 1000°C.

During processing the wafers were subjected to high-temperature gradients, which consequently gave rise to high residual stresses, dislocation generation, and plastic deformation. After thermal processing, the wafers were defect-etched using the Sopori etch [6] and examined using an optical microscope and a commercial GT-PVSCAN laser scanner. These techniques allowed, respectively, for the qualitative and quantitative evaluation of dislocation distributions generated in the Si specimens during the thermal processing.
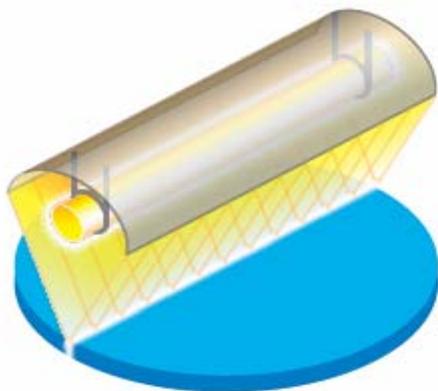

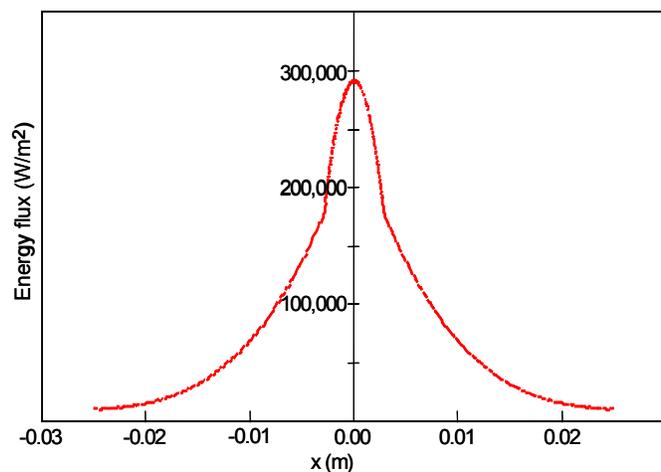Figure 1. Wafer processing using a linear infrared heater

Figure 2. Distribution of energy on the wafer surface along the line perpendicular to the heater axis

NUMERICAL APPROACH

Both thermal and mechanical simulations were conducted to examine the behavior of the wafer illuminated by the light heater. In both cases a 3-dimensional finite element model of a silicon wafer was employed. The radius and the thickness of the wafer equaled 38.1 mm (1.5 in) and 300 μm, respectively. In this study only the computations for the static case are presented.

In the thermal modeling, the following phenomena were taken into account: the surface radiation, the surface convection, and the conduction within the wafer. Following the experimental setup, it was assumed that the illuminated surface of the wafer was unpolished. The emissivity of that surface was taken as 0.90. The other side was polished, and the emissivity was assumed to be 0.65. The wafer edge in the model had the same thermal properties as the unpolished surface. The convection coefficient equaled 9 W/(°K m^2), which was the same for all surfaces in the model. The line heater was modeled by applying energy flux to the unpolished surface. The distributions of that flux followed a specification obtained from the manufacturer of the light heater (see Figure 2). The magnitude of the flux was adjusted so that the maximum temperature in the wafer could reach approximately 960°C.

After the temperature distribution in the wafer was established, nonlinear mechanical computations were performed. In that simulation, the silicon was modeled as an elasto-perfectly-plastic material, with the Young's moduli and the elastic limits being a function of temperature. The yield stress values for the model were taken from the Dillon-Sumino-Hassen (DSH) equations [1,2]. The effective stress strain curves from the DSH model and from the simplified mechanical model employed in this study are shown in Figure 3 using continuous and dashed lines, respectively. It can be observed in Figure 3 that the simplified elasto-perfectly-plastic curves neglect the drop of stress after the maximum stress peak. Consequently, one should expect the simplified material to be accurate only for small plastic strains. However, for high plastic strains, it can be anticipated a resultant plastic zone will be smaller in the simplified model than the zone in the DSH model. It should also be noted that the material was assumed to be isotropic.

The thermal and mechanical simulations were conducted using CalculiX open-source finite element code (version 1.3). Due to the symmetries of the mathematical representation of the system, only one-quarter of the entire wafer was actually simulated.

RESULTS

A typical temperature profile obtained from the thermocouples attached to processed wafers for both static and dynamic modes is shown in Figure 4. It can be observed for the static case that an initial rapid increase of the temperature is followed by a region of stable, almost constant temperature. This flat region represents the system in the steady-state mode. In the dynamic case, the wafer heats up and cools down as it is moving under the heat source. Consequently, a peak-type temperature history was recorded (Figure 4). By comparing all available results, it was observed that the peaks are not symmetric and that their width and height depend on the light intensity and the speed of the moving belt.
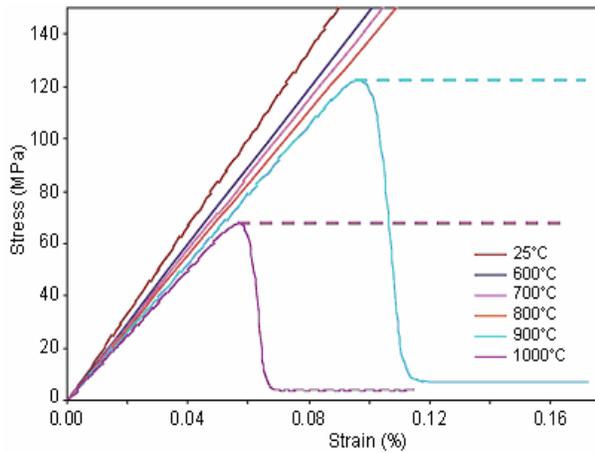
Figure 3. Silicon stress-strain curves from DSH model (continuous lines) and from a simplified elasto-plastic model (dashed lines) that was used in this study.
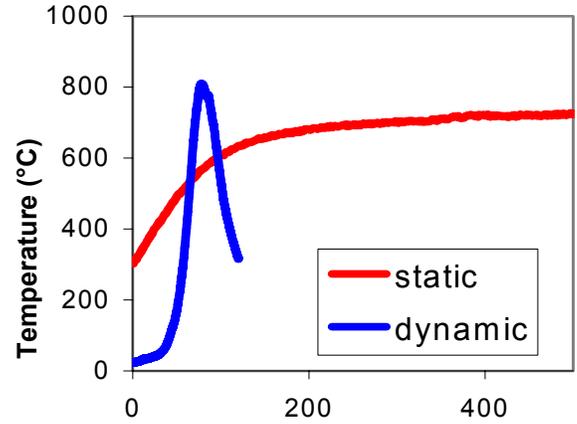
Figure 4. Temperature as a function of time during the static and dynamic thermal processing

Dislocations were generated on single-crystal wafers of two orientations, (100) and (111). Figure 5 shows a dislocation map of a (100) sample produced by illuminating the wafer with a flux corresponding to that shown in Figure 2. The dislocation map was generated by a GT-PVSCAN. Based on these results, it can be found that the maxim density of dislocations equaled approximately $4.10^6/cm^2$. We examined the directions of dislocation propagations. Figure 5 also shows photographs of the defect-etched sample, showing dislocation formation along the slip directions. One can also see dislocation network formation caused by slip on different (111) planes.
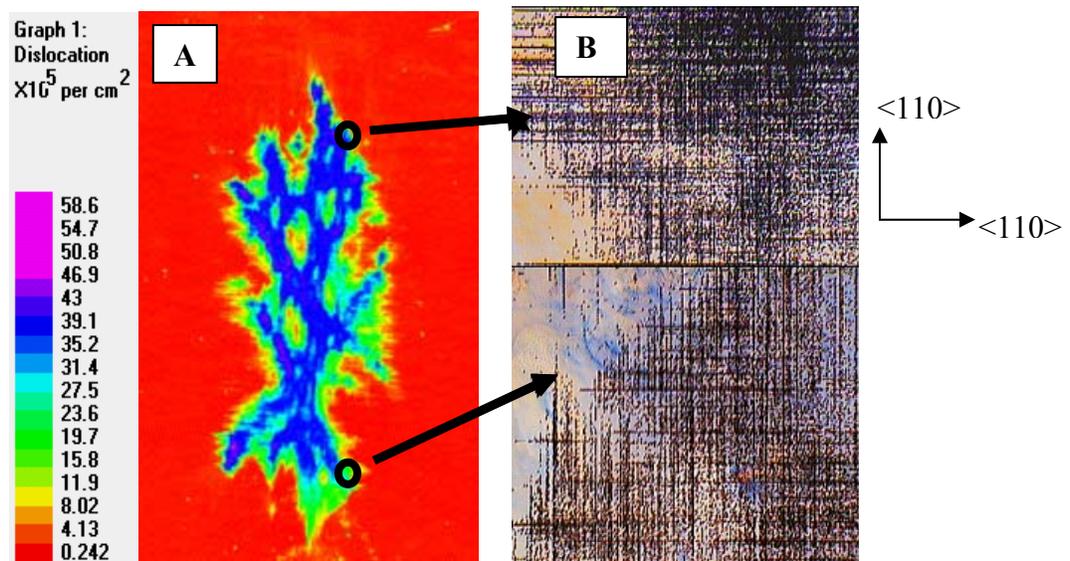
Figure 5. Dislocation density map (A) and optical microscope images (B) of a (100) wafer after thermal processing

Figures 6 and 7 depict the results of the numerical computations from both thermal and mechanical models. Figure 6(a) shows very high temperature gradients between the center (962ºC) and the cold edge (386ºC) of the wafer. It should be noted that the temperature distribution observed in Figure 6(a) was generated by only one linear heater that focuses energy along the line going through the center of the wafer (x=0). For the temperature profile illustrated in Figure 6(a), stress distributions were also computed for purely elastic (Figure 6(b)) and elasto-plastic models. It was observed that the stresses concentrate along the central line (x=0) and that the highest value is located in the proximity of the wafer edge. It is important to note that both the highest stresses and highest temperatures were found to be in the same region of the wafer. Since the yield stress is inversely proportional to the temperature, one would expect the material to deform plastically in this region. The results from the elasto-plastic model clearly indicate that the magnitude of stress in the hottest parts of the wafer decreased significantly when compared to the elastic case. Obviously, this effect was attributed to plastic yielding. The regions where the material yielded are illustrated in Figure 7, which depicts the distribution of the plastic strain on the wafer surface. Clearly, there is a strong correlation between the location of the nonzero plastic stain in the numerical results and the location of the plastic zone in the experimental images.
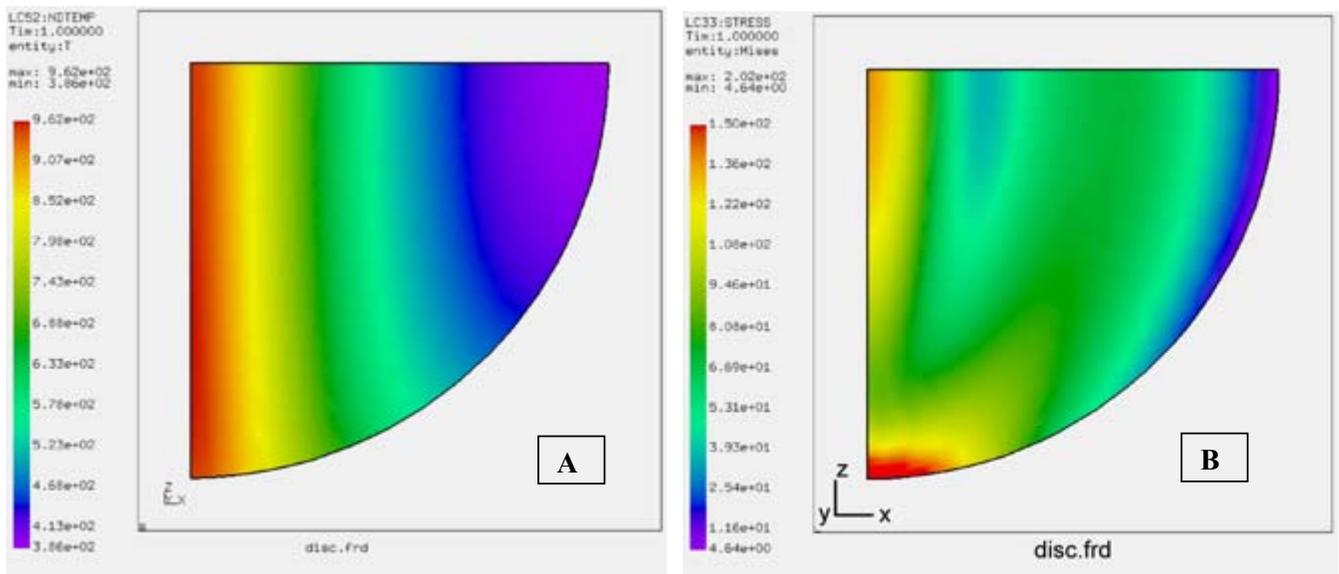

Figure 6. Numerically predicted distribution of (a) temperature and (b) von Misses stress.

Although we have not completed our model to predict dislocation distribution, it is fruitful to compare the predicted plastic deformation with the observed dislocation distribution. Figure 8 compares observed dislocation distribution (as a photograph of the defect etched wafer after thermal treatment) and the calculated plastic deformation corresponding to the same flux profile. One can notice an excellent qualitative agreement between the two.
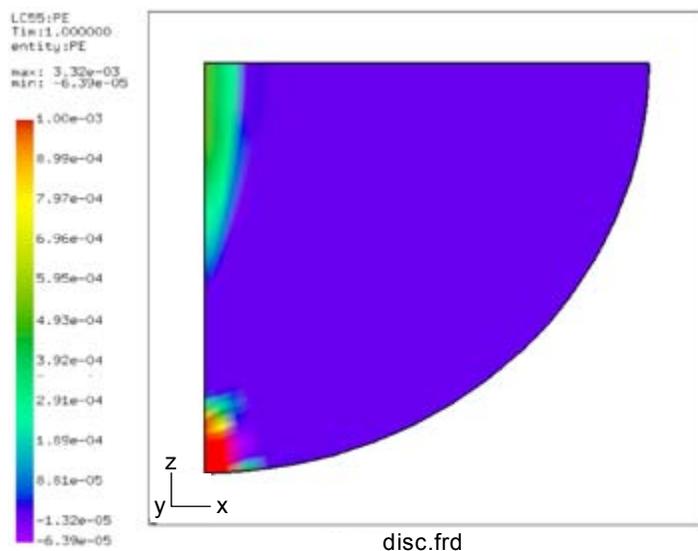
Figure 7. Numerically predicted distribution of plastic strain

Figure 8. Digital image of a (100) wafer after thermal processing

CONCLUSIONS

In this project single crystal silicon wafers were processed using an optical furnace operating in both static and dynamic mode. Due to the non-uniform distribution of the temperature during the processing, a plastic deformation in the central part of the wafer was generated and examined using a laser scanner and an optical microscope. Furthermore, mechanical behavior of the system was numerically simulated using an elasto-plastic finite element model of the wafer. Thermal and mechanical computations were performed to find the distribution of the temperature and plastic strains in the wafer. It was shown that the location of the plastic zones obtained form the experiment and simulation was almost the same. Consequently, it was concluded that the proposed model simulates the mechanical behavior of the wafer subjected to rapid thermal processing very well.

ACKNOWLEDGMENTS

REFERENCES

[1] K. Sumino, Dislocations and Mechanical Properties of Silicon, Materials Science and Engineering, B4, 335 (1989).
[2] O. W. Dillon, C.T. Tsai, and R.J. DeAngelis, Dislocation Dynamics of Web Type Silicon Ribbon, J. Crystal Growth, 82, 50 (1987).
[3] R. W. Gurtler, Nature of Thermal Stresses and Potential for Reduced Thermal Buckling of Thin Silicon Ribbon Growth at High Speeds, J. Crystal Growth, 50, 69 (1980).
[4] B. L. Sopori, R. Murphy, C. Marshall, Scanning defect-mapping system for large-area silicon substrates, Conference Record of the IEEE Photovoltaic Specialists Conference, 1993, p 190-196
[5] Products: GT-PVSCAN 6000, http://www.gtsolar.com/products/pvscan.php.
[6] B. L. Sopori, A New Defect Etch for Polycrystalline Silicon, Journal of The Electrochemical Society, 1984, vol. 131, no. 03, pp. 667-672.

Polishing Multicrystalline Silicon Wafers for Defect Etching

Bhushan Sopori, Peter Rupnowski, Bryan Taliaferro, Doug Gagnon, and Chuan Li
National Renewable Energy Laboratory
1617 Cole Boulevard
Golden, CO 80401

ABSTRACT

The effect of pressure on the chemical-mechanical polishing characteristics of multicrystalline silicon wafers is evaluated. Higher pressure during polishing minimizes grain-to-grain height variations but produces surface damage. On the other hand, lower pressure produces enhanced grain-to-grain height variations and leads to formation of "hillocks" in deeper grains. The mechanism of hillock formation is described.

INTRODUCTION

Chemical-mechanical polishing (CMP) is used extensively in the microelectronic industry for a variety of applications, such as polishing single-crystal wafers and planarization of microcircuit devices. The microelectronics industry has developed CMP techniques to control very precisely polishing characteristics of large-area, single-crystal Si wafers. Although Si wafers are also used in very large quantities in the photovoltaic (PV) industry, polishing PV-Si is a rare process because solar cells do not use polished wafers. However critical polishing is needed for a variety of applications involving characterization of wafers and devices. Because multicrystalline Si (mc-Si) constitutes a large part of wafers used in the PV industry, polishing mc-Si wafers is also needed for defect analysis, spectroscopic analyses of impurities, optoelectronic analyses of grain boundaries, and intragrain defect characterization. CMP for mc-Si can produce many artifacts that can interfere with defect delineation. Good polishing requires control of polishing parameters.

Polishing mc-Si Wafers

Because of the extensive use of mc-Si in the PV industry, defect characterization of mc-Si wafers is very important. Defect delineation by chemical etchants is the most common procedure for characterizing defects in silicon. A good delineation of defects must avoid extraneous pitting, which often occurs if there is surface damage. Hence, surface preparation for defect etching requires a well-polished, damage-free surface. Damage-free surface preparation, using a CMP procedure, is well established for single-crystal wafers to produce starting wafers and for other processes such as planarization. Although this procedure works very well for a single-crystal wafer, CMP can produce many artifacts in mc-Si wafers [1]. These include grain-to-grain (GTG) polishing rate variations, which cause GTG height variations in the surface profile of the polished wafer. The grain-to-grain variation can be minimized by suitable control of pressure,

during polishing, rotational speed, choice of pad material, and slurry flow rate [1].   For a given pad, the increased pressure also increases surface damage, causing extraneous pitting during defect etching. In most cases, the main controlling parameter is the pressure applied to the wafer during polishing.   Previous work has shown that an increase in the pressure increases the polishing rate and reduces the GTG height variations. However, increased pressure can result in surface damage, which degrades the delineation characteristics. One might believe that one can balance the surface damage and the GTG height variations by a judicious choice of pressure. In an attempt to arrive at such an optimum pressure range, we found that if mc-Si wafers are polished at a very low pressure, some regions of the wafer can develop "hillocks."   The generation of such hillocks is quite intriguing. This paper describes some characteristics of hillock formation.

Experimental Procedure

The main objective of this study was to characterize the quality of the surfaces of the mc-Si wafers after CMP. To achieve this, mc-Si wafers were polished with different pressures and subsequently analyzed using profilometer and optical microscopy techniques.   A typical polishing process consists of mounting the wafer on a stainless steel chuck using a low-temperature wax, with a melting point of about 150°C. The sample is mounted to have the polishing surface as planar as possible to minimize the polishing time. The mounted wafer is placed on a polishing machine with a rotating wheel and a rocker arm. The wheel is covered with a pad that has specifically designed features for removal of semiconducting materials such as Si, GaAs, and Ge. A commonly used pad material is Suba IV 2 II 16, manufactured by Eminess Technologies. Adequate flow of a suitable slurry provides the medium for material removal. In our laboratory, we use Nalcog (manufactured by ONDEO Nalco Company). Nalco 2350 slurry is a mild alkaline (NH_4OH-based) solution, and is typically diluted with water at a 1:7 ratio.
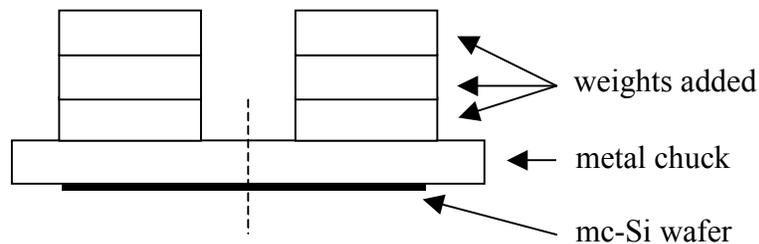
Figure 1. A wafer chuck with additional weights

During polishing, the pressure on the wafer depends primarily on the weight of the wafer chuck itself. In order to control the pressure, we devised a procedure to add weights on the chuck itself. Figure 1 is an illustration of how weights were added to the chuck. In the case with no additional weight, the pressure on the wafer surface equaled 0.28 psi. By adding 1, 2, and 3 additional sets of weights, the pressure could be increased up to 0.35, 0.42, and 0.49 psi, respectively.   To examine the changes in the polishing quality, we used adjacent "sister wafers" wire-sawn from the same cast Si brick. Consequently, the same grains could be identified on the surface of all polished wafers.

Wafers were polished until the whole surface was smooth and shiny. Because wafers have significant surface roughness and some degree of saw marks and concomitant thickness variation within the wafer, polishing times to obtain the same degree of polish varied significantly. Following polishing, wafers were demounted, cleaned, and profile measurements using DEKTAK3 profilometer were performed to show the height variations on the wafer surface. To further examine quality and morphology of the polished wafers, optical microscope images were acquired and analyzed.

Results and Discussion

Effect of pressure on polishing rate
The pressure during polishing plays an important role in the quality of the polish and also controls the polishing rate. Figure 2 shows the average polishing rate as a function of pressure during polishing (with same pad, slurry flow rate, rotational speed, and rocker arm speed).
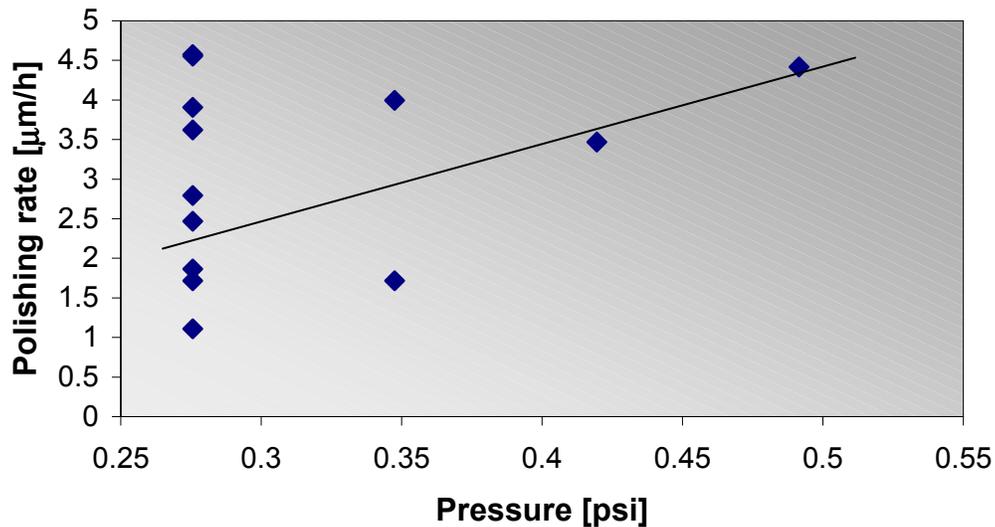
**Figure 2. Polishing rate as a function of pressure**

Effect of pressure on grain-to-grain height variation
We determined that the average GTG height variation over the entire wafer increases as the pressure is lowered. Because the grain structure of the entire wafer can be quite complex, it is valuable to study changes in the height of the same grains in sister wafers produced by polishing at different pressures. Figure 3 shows plots of GTG height variations resulting from polishing three wafers at different pressures. The data correspond to the same eight grains on each wafer, which are identified by the same symbol.
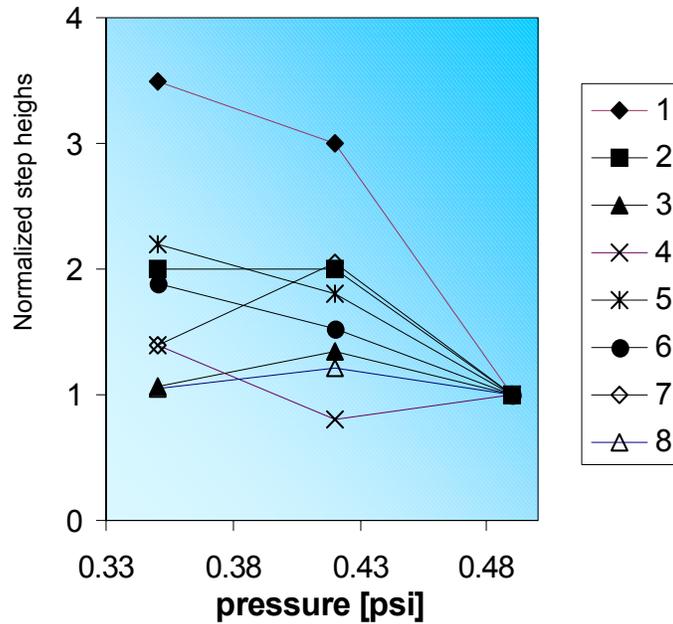
Figure 3. Normalized step height vs. pressure at eight boundaries

It is thus clear that higher pressure reduces not only the average GTG height variation, but also the step height of each grain (i.e., reduces the effect of preferential polishing-rate for different orientations). However, it known that higher pressure causes extraneous pitting. Thus, for good defect delineation, it is necessary to reduce the pressure during polishing. But one of the very interesting (and technically very important) phenomenon that we have observed is that polishing at low pressures causes generation of intragrain morphology that we called hillocks. Hillocks are formed only in a few grains of the whole wafer. Figure 4 shows a Nomarski photograph of hillocks in one grain.
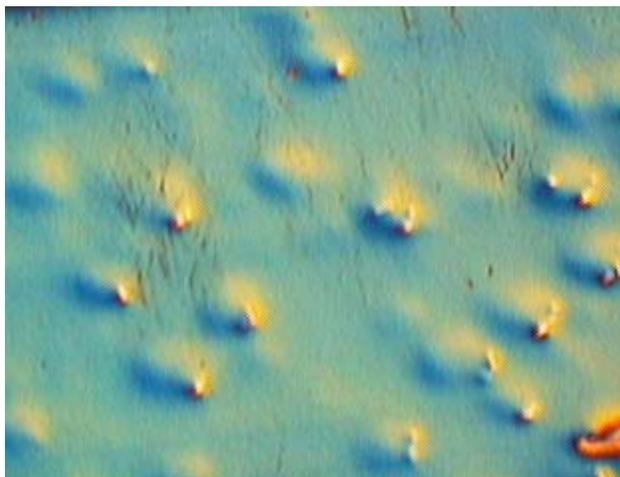
Figure 4. A Nomarski photograph of a polished wafer showing formation of "hillocks" in some grains

50 μm

The formation of hillocks is a very intriguing phenomenon. Detailed characterization of the polishing led to the following observations:

1. Hillocks appear only on specific (preferred) grains of the wafers and on the same grains of all wafers (under suitable polishing conditions).
2. Formation of the hillocks is a dynamic process, in which the size of the hillock can change with the height of the grain during polishing.
3. Certain grain orientations have a propensity for higher polishing rate and, hence, formation of hillocks.

Effect of pressure on hillock formation

Figure 5 shows photographs of the same grain of sister wafers polished with different pressures. Hillocks do not appear until pressure is reduced below 0.35 psi. Figure 6(a) shows Dektak traces across several grains, one of which has hillocks. The depth of the grain with hillocks is about 10 μm, whereas the height of hillocks is about 1 μm. Figure 6(b) is another Dektak trace showing height variations of hillocks (note: some of the apparent height variations are simply because the stylus of the profilometer does not go through the highest point of the hillock).

(a)   (b)   (c)
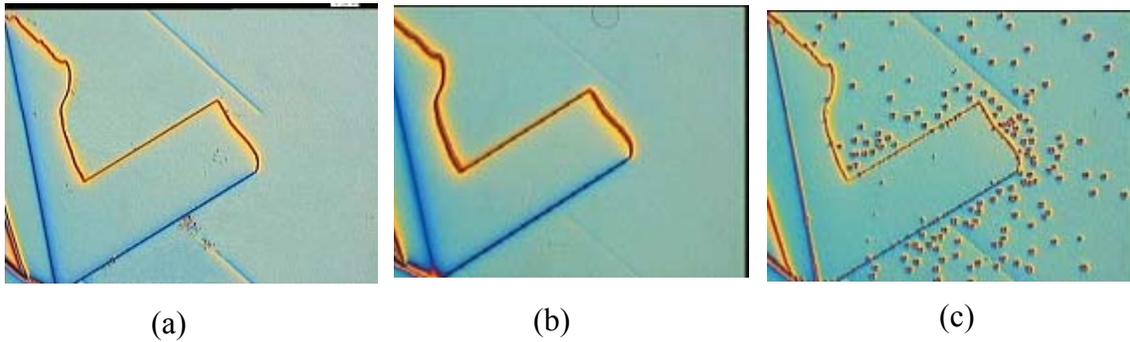
Figure 5. Nomarski photographs the same grain in three samples polished at different pressures: (a) P = 0.49 psi, polishing time =9.5 h, (b) P = 0.42 psi, polishing time = 16.5 h, and (c) P = 0.28 psi, polishing time = 15 h.

(a)   (b)
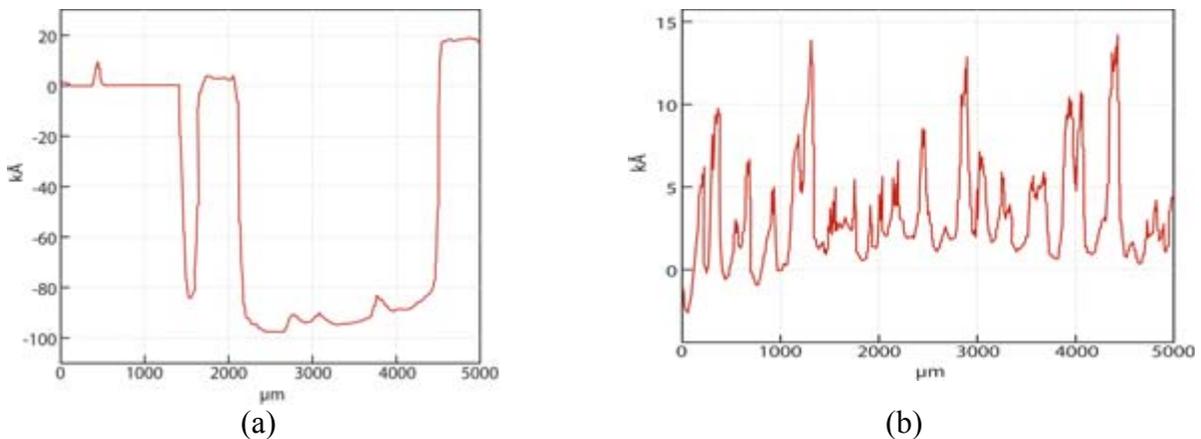
Figure 6. Profiles along (a) a path crossing a few grain boundaries and (b) inside a deep grain.

226
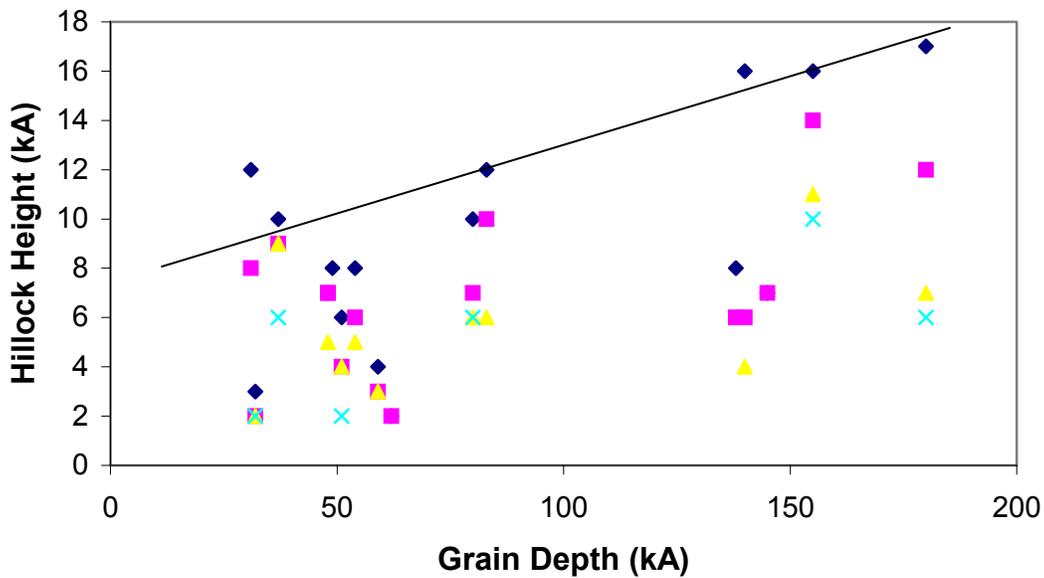
Figure 7. Relationship between the height of hillocks and the grain depth. A line is drawn over the tallest hillocks only as guide for visualization.

Figure 7 shows the relationship between hillock height and grain depth as determined by Dektak profiles. Although there is a large scatter (as expected) in these data, there is also a trend of increasing hillock height with grain depth. This is particularly evident by selecting the largest peak heights, as illustrated by the line drawn in the figure.

It was determined that hillocks are formed in the same grains, but not in the same locations; thus they are not related to crystal defects within the grain. Furthermore, the density of the hillocks (under the same polishing pressure of 0.28 psi) increases with the polishing time. This is illustrated in Figure 8, which shows photographs of the same grain in two different samples polished for 9 hours and 17.5 hours. A higher density and larger size of hillocks appear on the sample polished for a longer time.

(a)
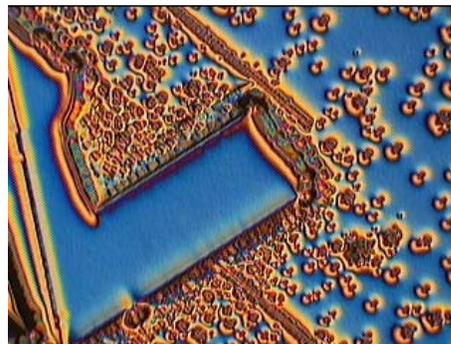
(b)

Figure 8. Photographs of the same grain of two wafers polished under low pressure for different times; longer polishing causes denser hillocks. Polishing times:(a) 9 h, and (b) 17.5 h.

Conclusions

One of the unusual observed features in CMP of mc-Si is the formation of "hillocks." Hillock formation takes place under low-pressure conditions when the differential polishing rate of various grains is high. The above results suggest that:

- Hillocks are formed in grains of preferred orientation(s), which have high chemical-mechanical polishing rates.
- Hillocks appear only after a certain depth of grains is reached and then hillock height increases with the grain depth.
- The density of hillocks is largest near the deepest edges of the grains.

These results suggest that the mechanism of hillock formation is related to trapping of slurry in deep grains. We have tried to investigate two mechanisms that can cause hillock formation in deep grains: (i) trapping of fine particles of wax carried by the slurry, which act as masks and reduce the Si dissolution directly underneath them; and (ii) formation of flow pattern or a standing-wave type of mechanism of the liquid slurry, which can reduce the Si dissolution at the nodes of such a pattern. We have found that reducing the exposure of wax to slurry greatly reduced the hillock formation and, in many cases, completely prevented hillock formation. However, further studies are needed in which the wax used for wafer mounting can be eliminated.

References

1. B.L. Sopori, T. Nilson, and M. McClure, *Damage-Free Polishing of Polycrystalline Silicon,* J. Electrochem. Soc., **128**, 215 (1981).

Characterizing Thin Films on Absorbing Substrates

Bhushan Sopori, Juana Amieva, and Peter Rupnowski

National Renewable Energy Laboratory

ABSTRACT

Thin films are used in many applications such as reflection/antireflection, material strengthening, and protection, as well as for active devices including those used in solar cell fabrication. There are many techniques used in the industry and in research laboratories to characterize such films. Most of these apply only to nonabsorbent thin films with planar interfaces. Some ellipsometery-based techniques can measure n, the refractive index, and k, the extinction coefficient, of weakly absorbing films. However, these techniques are difficult to use on films for photovoltaic applications, which feature large-area devices, have significant roughness, and are highly absorbing. These films include absorbing semiconductor films, absorbing films on metallic substrates, and multilayer films. Furthermore, these composite films have rough or textured surfaces in order to promote optimal light-trapping. A suitable technique for characterizing photovoltaic films must be rapid, low cost, capable of measuring very large areas, and easy to use. In addition, it must be capable of measuring a number of thin-film parameters such as thickness and interface quality.

We have developed a capability to characterize thin films on any type of substrate (including highly absorbing) to measure the film thickness and the interface roughness. This technique can also be extended to measure absorption coefficient of the film. This technique uses spectral reflectance measurements corresponding to different angular illumination to separate specular and diffuse (scattered) components of the reflectance spectra. The angular illumination capability is inherently present in the GT-FabScan 6000 reflectometer. The results are fitted to calculated reflectance plots. The best-fit data yield the thin-film parameters.

REPORT DOCUMENTATION PAGE

1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED *(From - To)*
November 2005	Workshop Proceedings	August 7–10, 2005

4. TITLE AND SUBTITLE
15th Workshop on Crystalline Silicon Solar Cells and Modules: Materials and Processes; Extended Abstracts and Papers

5a. CONTRACT NUMBER
DE-AC36-99-GO10337

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
B.L. Sopori

5d. PROJECT NUMBER
NREL/BK-520-38573

5e. TASK NUMBER
WO97G400

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
National Renewable Energy Laboratory
1617 Cole Blvd.
Golden, CO 80401-3393

8. PERFORMING ORGANIZATION REPORT NUMBER
NREL/BK-520-38573

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
National Renewable Energy Laboratory
1617 Cole Blvd.
Golden, CO 80401-3393

10. SPONSOR/MONITOR'S ACRONYM(S)
NREL

11. SPONSORING/MONITORING AGENCY REPORT NUMBER

12. DISTRIBUTION AVAILABILITY STATEMENT
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road
Springfield, VA 22161

13. SUPPLEMENTARY NOTES

14. ABSTRACT *(Maximum 200 Words):* The National Center for Photovoltaics sponsored the 15th Workshop on Crystalline Silicon Solar Cells & Modules: Materials and Processes, held in Vail, CO, August 7-10, 2005. This meeting provided a forum for an informal exchange of technical and scientific information between international researchers in the photovoltaic and relevant non-photovoltaic fields. The workshop addressed the fundamental properties of PV silicon, new solar cell designs, and advanced solar cell processing techniques. A combination of oral presentations by invited speakers, poster sessions, and discussion sessions reviewed recent advances in crystal growth, new cell designs, new processes and process characterization techniques, and cell fabrication approaches suitable for future manufacturing demands. The theme of this year's meeting was "Providing the Scientific Basis for Industrial Success." Specific sessions during the workshop included: Advances in crystal growth and material issues; Impurities and defects in Si; Advanced processing; High-efficiency Si solar cells; Thin Si solar cells; and Cell design for efficiency and reliability module operation. The topic for the Rump Session was "Si Feedstock: The Show Stopper?" and featured a panel discussion by representatives from various PV companies.

15. SUBJECT TERMS
photovoltaics; crystalline silicon; solar cells; module; materials and processes; manufacturing; cell fabrication; impurities; thin films;

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	**b. ABSTRACT**	**c. THIS PAGE**	UL		
Unclassified	Unclassified	Unclassified			19b. TELEPHONE NUMBER *(Include area code)*