Affordable Multi-Layer Ceramic (MLC) Manufacturing for Power Systems (AMPS)

Final Report - Phases I and II

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ABSTRACT

McDermott Technology, Inc. (MTI) is attempting to develop high-performance, cost-competitive solid oxide fuel cell (SOFC) power systems. Recognizing the challenges and limitations facing the development of SOFC stacks comprised of electrode-supported cells and metallic interconnects, McDermott Technology, Inc. (MTI) has chosen to pursue an alternate path to commercialization. MTI is developing a multi-layer, co-fired, planar SOFC stack that will provide superior performance and reliability at reduced costs relative to competing designs.

The MTI approach combines state-of-the-art SOFC materials with the manufacturing technology and infrastructure established for multi-layer ceramic (MLC) packages for the microelectronics industry. The rationale for using MLC packaging technology is that high quality, low-cost manufacturing has been demonstrated at high volumes. With the proper selection of SOFC materials, implementation of MLC fabrication methods offers unique designs for stacks (cells and interconnects) that are not possible through traditional fabrication methods. The MTI approach eliminates use of metal interconnects and ceramic-metal seals, which are primary sources of stack performance degradation. Co-fired cells are less susceptible to thermal cycling stresses by using material compositions that have closely matched coefficients of thermal expansion between the cell and the interconnect.

The development of this SOFC stack technology was initiated in October 1999 under the DOE co-sponsored program entitled "Affordable Multi-layer Ceramic Manufacturing for Power Systems (AMPS)". The AMPS Program was conducted as a two-phase program: Phase I – Feasibility Assessment (10/99 – 9/00); and Phase II – Process Development for Co-fired Stacks (10/00-3/02). This report provides a summary of the results from Phase I and a more detailed review of the results for Phase II.

Phase I demonstrated the feasibility for fabricating multi-layer, co-fired cells and interconnects and resulted in selection of the most promising configuration for high-performance, low-cost SOFC stacks. During Phase II, the MTI Team successfully refined the fabrication processes and achieved low-rate production of cells and interconnects (about 100 per month). Short stacks (3-10 cells) using co-fired cells and interconnects were assembled and tested to validate the MTI multi-layer SOFC design. The team successfully demonstrated co-fired repeat units, comprised of a cell and the interconnect layers. Development of co-fired cells and multi-layer interconnects based on the new stack design was completed; all component fabrication and stack testing efforts were redirected to the new design toward the end of Phase II. Finally, low-cost alternate materials for the interconnect body and conductors within the interconnect were identified. At the end of Phase II, the MTI Team successfully transitioned the multi-layer SOFC stack development effort to the Solid State Energy Conversion Alliance (SECA) program.

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EXECUTIVE SUMMARY

McDermott Technology, Inc. (MTI) is attempting to develop high-performance, cost-competitive solid oxide fuel cell (SOFC) power systems. Recognizing the challenges and limitations facing the development of SOFC stacks comprised of electrode-supported cells and metallic interconnects, MTI has chosen to pursue an alternate path to commercialization. MTI is developing a multi-layer, co-fired, planar SOFC stack that will provide superior performance and reliability at reduced costs relative to competing designs. The development of this SOFC stack technology was initiated in October 1999 under the DOE co-sponsored program entitled "Affordable Multi-layer Ceramic Manufacturing for Power Systems (AMPS)". The AMPS Program was proposed as a three-phase program: Phase I – Feasibility Assessment (10/99 – 9/00); Phase II – Process Development for Co-fired Stacks (10/00-3/02); and Phase III – SOFC Testing and Preparation of Business Plan (4/02-12/02). This report provides a summary of the results from Phase I and a more detailed review of the results for Phase II. Phase III of the research program was not authorized.

The SOFCo approach combines state of the art SOFC materials with the manufacturing technology and infrastructure established for multi-layer ceramic (MLC) packages for the microelectronics industry. The rationale for using MLC packaging technology is that high quality, low-cost manufacturing has been demonstrated at high volumes. With the proper selection of SOFC materials, implementation of MLC fabrication methods offers unique designs for stacks (cells and interconnects) that are not possible through traditional fabrication methods.

The overall objective for Phase I was to demonstrate the feasibility for fabrication of co-fired cells and multi-layer interconnects, and then to select the most promising configuration for high-performance, low-cost SOFC stacks. The MTI Team achieved almost all of the Phase I milestones. The preliminary design and materials characterization activities for the multi-layer cells and interconnects were completed. The team also made significant progress in the development of fabrication processes. The design/modeling team completed development of 2-D and 3-D electrochemical/thermal models and performed analyses for a number of alternative stack designs. Structural analyses were performed for many of the design options. This work led to the discovery of a new stack design that should provide for superior performance and reliability. Concurrently, a preliminary manufacturing cost model for the multi-layer SOFC stack was completed. Initial results suggested that the current cost target can be achieved, but only if low-cost raw materials for the interconnect are used.

The goal for Phase II was to complete implementation of MLC manufacturing processes for cell and interconnect fabrication and to demonstrate co-firing of cells and interconnect layers to form integral repeat units and short stacks. During Phase II, the MTI Team successfully refined the materials compositions and processes to achieve repeatable fabrication of cells and interconnects at a low production rate of 100 per month. In support of the manufacturing process development efforts, numerical models were developed for tape casting, lamination of interconnects and co-fired repeat units, binder removal, and stresses generated during co-firing. Intermediate cell performance targets (e.g., area specific resistance less than 0.8 ohm-cm^2) were achieved for 2.5cm button cells. However, the desired level of performance was not obtained for full-size 10cm cells. Materials and process refinements to improve performance for full-size cells will be

continued on the Solid-State Energy Conversion Alliance (SECA) program. One key outcome from this effort was the definition of a path forward for development of co-fired cells that will achieve commercial performance targets.

Short stacks (3-10 cells) using co-fired cells and interconnects were assembled and tested to validate the MTI multi-layer SOFC design and to provide feedback to the cell and interconnect fabrication efforts. In support of stack assembly and testing, 3-D finite element models were developed to define stresses associated with stack assembly processes and stack operation. A 3-D finite element current distribution model was also developed to better understand the relationship between interconnect design and stack resistance.

A key accomplishment during Phase II was the successful demonstration of co-fired repeat units comprising a cell, the air-flow interconnects layers (laminated to the cathode side of the cell) and the fuel-flow interconnect layers (laminated to the anode side of the cell). While more work is required to achieve the desired level of performance, no major hurdles were identified. The MTI Team elected to not pursue the development of co-fired short stacks during Phase II due to the perceived challenges and the lack of clear benefits.

Another major accomplishment for the MTI Team was the successful development of co-fired cells and multi-layer interconnects using a new stack design. This design should offer improved performance and reliability relative to the initial stack design. Toward the end of Phase II, all component fabrication and stack assembly/testing activities were redirected to the new stack design. This design will be used for future development activities within the SECA program.

Significant progress was made in the development of alternate materials for the interconnect. Low-cost commercial powders for the multi-layer interconnect body were identified. In addition, promising candidate conductor materials for the interconnect were developed. These materials will be further refined and then implemented into interconnect production development efforts in the SECA program.

Finally, the MTI Team evaluated many non-destructive examination methods to assess their suitability for in-process quality control and final cell/interconnect inspection. A number of commercial-ready inspection methods, including microfocus X-ray radiography, C-scan ultrasonics, IR thermal imaging, and Shadow Moiré imaging, were shown to provide valuable quality information.

MULTI-LAYER, CO-FIRED SOFC STACK CONCEPT

The basic design for the MTI multi-layer, co-fired SOFC stack repeat unit is illustrated in ***Figure 1.*** For the cell, a thin electrolyte layer (50-75 μm green thickness) is fabricated by tape casting. Anode ink is screen-printed onto one side of the electrolyte tape and cathode ink is printed onto the other side. The printed cell can be excised and then co-fired to form a self-supported cell or combined with the interconnect layers and then co-fired to form a single repeat unit (as illustrated in the figure).

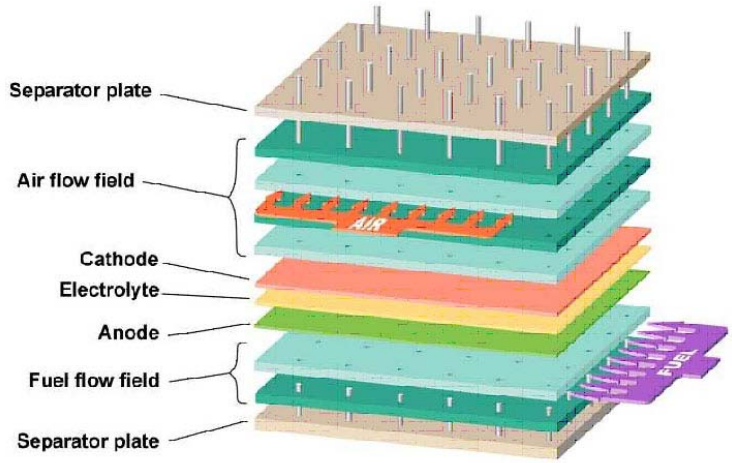


Figure 1. Schematic of multi-layer, co-fired repeat unit. A single cell is surrounded by the fuel and air-flow layers of the interconnect.

The interconnect consists of multiple dense ceramic layers which provide for the essential functions of gas separation, reactant gas flow and electrical conduction. Air and gas separation is accomplished using one or more dense layers. Current flow through the interconnect is accomplished by imbedding conducting materials within each layer. ***Figure 1*** illustrates one such approach being explored by MTI, in which conductive vias permit current flow through the ceramic layers. The use of conductive vias is well established in the microelectronics industry. The conductor material must have sufficient conductivity so that the electric current can flow from one cell to the next with minimal resistive losses. Reactant gas flow is facilitated by punching holes or other structures in the gas flow layers within the interconnect (not illustrated in the figure). The size of the holes (or other features) and the thickness of the layers are driven by SOFC operating considerations, such as fuel distribution and utilization, air-side pressure drop, and temperature gradients. The interconnect is fabricated using standard multi-layer ceramic production operations: tape casting, punching, screen-printing, lamination, excising and co-firing.

In developing the multi-layer, co-fired SOFC stack components, a critical issue is the selection and engineering of materials for the cell and interconnect that have compatible processing characteristics. For the cell, defining a co-firing temperature that yields a dense electrolyte while avoiding deleterious reactions between the cathode and the electrolyte is a significant challenge. In addition, the materials have to be engineered so that shrinkage matching is achieved between the electrolyte and the electrodes, while maintaining the desired porosity in the electrodes. For the interconnect, selection of the composition of the ceramic body is driven by a number of factors. A key objective is to match the thermal expansion behavior of the cell. A second objective is to avoid materials that will adversely contaminate the cells, either during manufacturing or during SOFC stack operation. The conductor materials used in the interconnect have to provide sufficient conductivity to carry the current, but also require close matching of the coefficient of thermal expansion (CTE) and sintering shrinkage with the interconnect body.

The MTI multi-layer, co-fired SOFC approach offers a number of key advantages over competing approaches:

- Eliminates the use of metal interconnects and ceramic-metal seals, which are major sources for stack performance degradation.
- Less susceptible to thermal cycling problems (through close matching of the coefficient of thermal expansion (CTE) between the cell and interconnect).
- Reduced contact resistance between the electrodes and interconnect (for co-fired repeat units).
- Requires fewer sintering steps.
- Low-cost, high-volume manufacturing, which has been established in the microelectronics industry.

PHASE I – FEASIBILITY ASSESSMENT

Phase I Summary

Phase I of the AMPS Program began in October 1999 and was completed in September 2000 (12 month duration). The objectives for the Phase I effort were:

- Develop the materials and fabrication processes for multi-layer, co-fired cells and interconnects;
- Establish analytical performance and structural models for planar SOFC stacks; and
- Develop a manufacturing cost model for multi-layer SOFC stacks and demonstrate the viability of achieving low-cost manufacturing.

In accomplishing these objectives, the key outputs from Phase I were demonstrating the feasibility for the fabrication of multi-layer, co-fired cells and interconnects, and selecting the most promising configurations for high-performance, low-cost SOFC stacks.

The MTI Team substantially achieved the Phase I objectives. The preliminary design and materials characterization activities for the multi-layer cells and interconnects were completed. The team also made significant progress in the development of fabrication processes. The design/ modeling team completed development of 2-D and 3-D electrochemical/thermal models and performed analyses for a number of alternative stack designs. Structural analyses were performed for many of the design options. Concurrently, a preliminary manufacturing cost model for the multi-layer SOFC stack was completed. Initial results suggest that the current cost target can be achieved, but only if low-cost raw materials are used for the interconnect.

Phase I Task Structure and Organization

Phase I of the AMPS Program was subdivided into six (6) tasks:

- Task 1 – NEPA Reporting and Development of Co-fired Cells (10/99-9/00)
- Task 2 – Development of Filled-Via Interconnects (10/99-9/00)
- Task 3 – Cell and Stack Modeling and Design (12/99-9/00)
- Task 4 – Manufacturing Cost Evaluation (3/00-9/00)
- Task 5 – Multi-layer, Co-fired Oxide Configuration and Manufacturing Process Selection (7/00-9/00)
- Task 6 – Project Management and Reporting (10/99-9/00)

The Phase I effort was led by McDermott Technology, Inc (MTI), and was supported by two key subcontractors: Ceramatec, Inc. and Advanced Refractory Technology (now M/A-COM). The primary responsibilities for each entity follow:

- McDermott Technology, Inc (MTI) – Prime Contractor
  - Materials development and characterization
  - Multi-layer SOFC design and modeling
  - Inspection/test methods development (e.g., NDE methods)
- Ceramatec, Inc. – Subcontractor
  - SOFC materials technology
  - Co-fired cell development
  - Cell testing
- Advanced Refractory Technologies (now M/A-COM) – Subcontractor
  - Multi-layer interconnect development
  - MLC manufacturing process development

The Phase I project organization is shown in ***Figure 2***. The responsibility for planning and executing the work within each task was assigned to key individuals within the MTI Team. These Task Leaders worked with the MTI Program Manager, Dr. Eric Barringer, to insure that the project objectives were achieved on time and within budget.

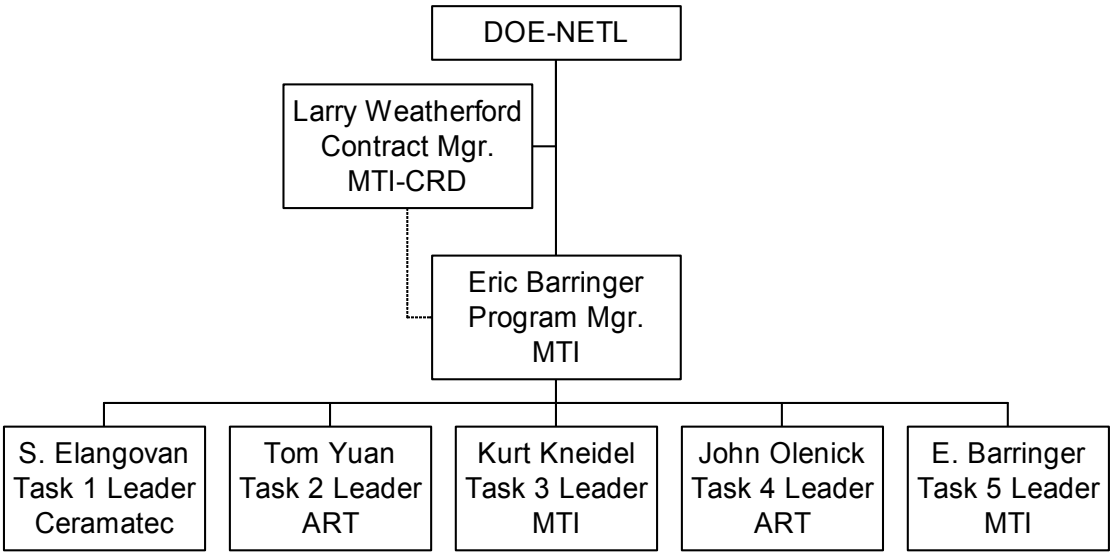


Figure 2. Phase I project organization.

Additional information regarding the Phase I activities and key accomplishments is provided in the following sections.

Task 1 – NEPA Reporting & Development of Co-fired Cells

MTI completed a report providing environmental information described in "Required Information for the National Environmental Policy Act (NEPA)". The report was reviewed by DOE; the MTI Team was granted a Categorical Exclusion status for the Phase I activities. In addition, Hazardous Waste Substance Plans were prepared for each participant of the MTI Team. At the conclusion of Phase I, Hazardous Waste Reports were prepared and submitted to DOE.

A preliminary design of the co-fired cell was established. The design utilized current SOFC materials and is consistent with MLC fabrication methods. This cell is expected to have good electrochemical performance; area specific resistance (ASR) should be ≤ 0.5 ohm-cm^2 at 850°C.

The team determined that the present anode, cathode and electrolyte materials are compatible with co-firing in air at 1300-1400°C. Matching of sintering behavior (shrinkage) and achieving the desired level of residual porosity in the electrodes were achieved by adjusting the physical properties (particle size and surface area) of the starting powders and adding fugitive material to the electrode compositions.

Substantial progress was made in the development of the cell fabrication processes. Development of the YSZ tape formulation was completed. Tape casting, punching and lamination operations were demonstrated. Furthermore, tape-casting operations were successfully transitioned to a new 30-foot Carsten caster at Ceramatec. Substantial progress was also achieved in the formulation and screen-printing of electrode inks. However, achieving shrinkage matching between the electrolyte tape and the electrodes during co-firing, while at the same time obtaining the required electrode adhesion and desired level of porosity, was a significant challenge. The MTI Team defined a number of potential approaches toward achieving the desired electrode properties with the goal that acceptable electrodes would be developed during Phase II of the program.

Initial co-fired button cells (~2.5 cm diameter) achieved open circuit voltages > 1 Volt and area specific resistance (ASR) values in the range of 0.9-1.2 ohm-cm^2 at 850°C; the electrolyte thickness for these cells was approximately 180 microns. The performance of a button cell is shown in ***Figure 3*** (ASR ~ 1.0 ohm-cm^2 at 850°C). Although testing of cells was limited during Phase I, preliminary endurance test data, shown in ***Figure 4***, indicate that cell performance is relatively stable after an initial "burn-in" period (first 100 hours).

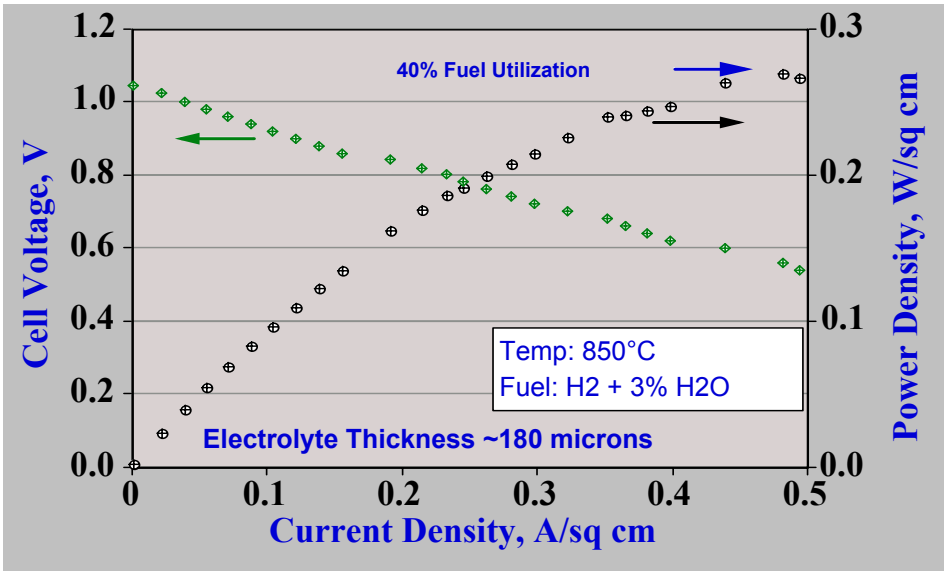


Figure 3. Electrochemical performance for an initial 2.5 cm "button" cell. The ASR for this cell is approximately 1.0 ohm-cm^2 at 850°C.

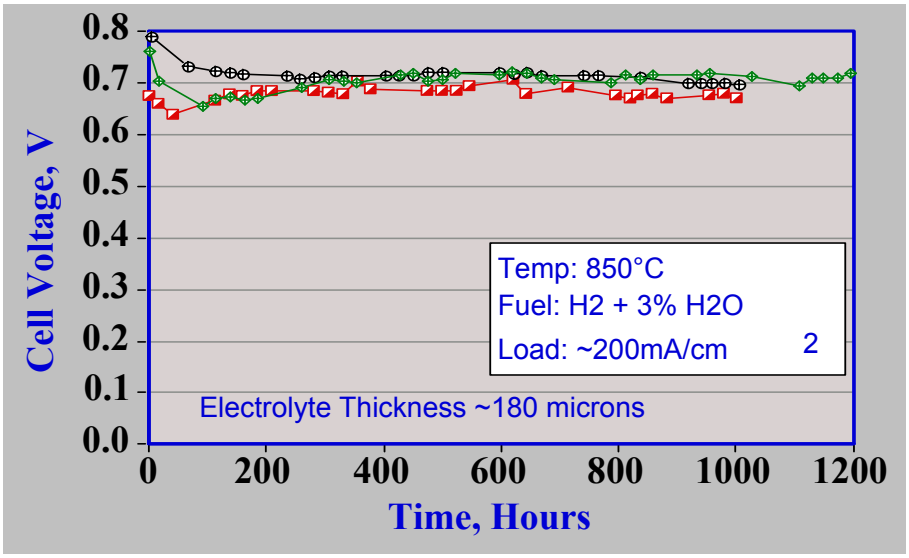


Figure 4. Long-term test results for initial 2.5 cm "button" cells. Performance is relatively stable after an initial "burn-in" period.

Based on these results, performance of full-size (10cm x 10cm) co-fired cells using our proprietary electrolyte design (effective thickness of ~100 microns) should meet the Phase I target of ≤ 0.8 ohm-cm^2 at 850°C. Further reduction of the ASR to < 0.5 ohm-cm^2 at 850°C will require improved electrolyte and anode materials (planned for Phase II). The team demonstrated fabrication of 10cm x 10cm co-fired cells in August 1999 (using 250 micron thick electrolyte tape). Initial efforts to fabricate cells using thin electrolyte tape yielded mixed results. It is believed that the improvements in ink formulation discussed above will be necessary to successfully fabricate large co-fired cells (MTI proprietary design). Based on the results to date, though, the MTI Team believes that the Phase I objective of demonstrating the feasibility for fabrication of co-fired, multi-layer cells has been met.

Task 2 – Development of Filled-Via Interconnects

A preliminary design for the co-fired filled-via interconnect was established. The design utilized materials having thermal coefficients of expansion that were well matched to those for the electrolyte. Materials usage, pressure drop in the air and fuel gas flow passageways, and through-thickness resistance were key factors considered in the design. The MTI Team was successful in developing a design that appears to be consistent with the design guidelines and manufacturing practices (tape casting, punching, screen printing, lamination and excising) for MLC packages. This fact was demonstrated through the successful fabrication of "mock" filled-via interconnects by an outside vendor using two different tape/ink systems (low temperature co-fired ceramic/gold and alumina/platinum).

A set of materials for co-firing filled-via interconnects in air at 1300-1400°C was defined. The interconnect material was selected based on compatibility with the materials comprising the cell in terms of chemical interactions, physical properties (e.g., thermal coefficient of expansion), and sintering behavior. Materials to be used for conductive pathways through the interconnect were

selected based on compatibility with the interconnect material and electrical conductivity. Although the selected materials are suitable for demonstrating the feasibility of fabricating co-fired, multi-layer SOFCs, their cost may be too high to achieve commercial cost targets for SOFC stacks. As a result, the MTI Team will need to explore lower cost materials for the interconnect body and the electrical conductors during Phase II.

Development of the fabrication processes for the filled-via interconnect represented the most difficult challenge for the MTI Team. Significant progress was made during Phase I. First, construction of an 8000 square foot clean room facility at M/A-COM (formerly ART) was completed and all equipment required for MLC component fabrication was installed. Second, preliminary interconnect tape and conductor ink formulations were defined. Third, all of the basic MLC operations (tape casting, blanking, punching, screen printing, lamination and firing) were demonstrated in the MLC facility at M/A-COM. During September 1999, fabrication of the first co-fired, filled-via interconnect was performed. While much work remains to enable the fabrication of functional interconnects, the MTI Team believes that feasibility for the multi-layer, co-fired interconnect design was successfully demonstrated.

Task 3 – Cell and Stack Modeling and Design

The objective of this task was to develop analytical models that can be used to guide the design of a high-performance, reliable multi-layer SOFC stack. Significant accomplishments toward this objective were made during Phase I. A combined thermal/electrochemical model for planar SOFC stacks was developed. The basic concept behind this iterative model is illustrated in ***Figure 5***.

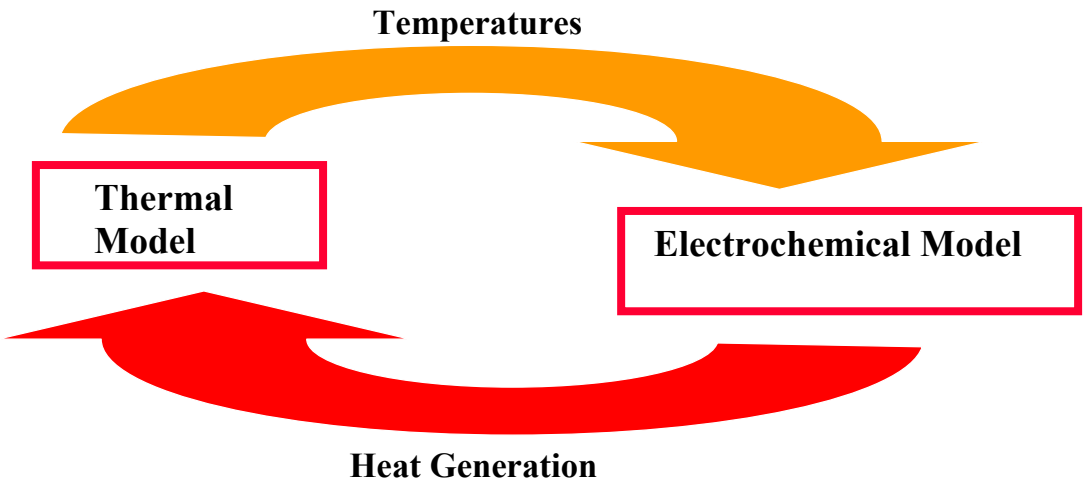


Figure 5. The combined thermal/electrochemical model for stack performance requires an iterative process to reach solutions.

The model was used to predict 2-D distributions of temperature, resistance, current density and fuel gas composition (electrochemical potential) for a number of stack designs. ***Figure 6*** provides an example of the model results for a cross-flow stack at a specific set of operating conditions. ***Figure 6a*** shows the hydrogen concentration over the surface of a cell, while ***Figures 6b and 6c*** show the resulting power density and temperatures, respectively.

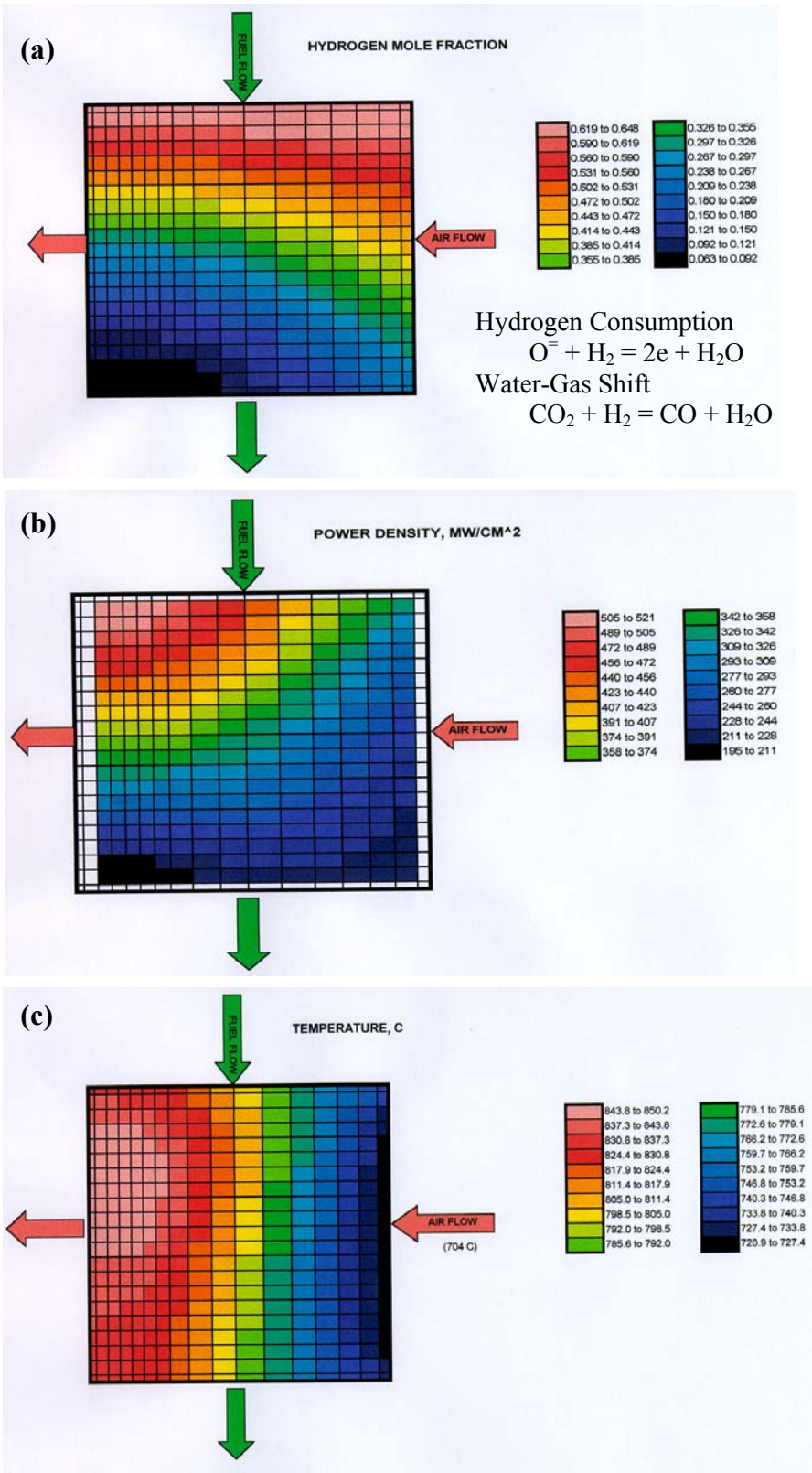


Figure 6. Thermal/electrochemical model results for a cross-flow stack: a) hydrogen concentration; b) power density; and c) temperatures.

Initial structural mechanics models were generated to calculate stress distributions resulting from temperature gradients across cells. As an example, the stress distribution predicted for a typical temperature profile exhibited by a cross-flow stack is shown in ***Figure 7***. Since limited mechanical property data were available for the cell and interconnect materials, the modeling was only performed at the macro-scale level. Detailed models incorporating properties for each layer and specific geometric features are being prepared as material properties become available. A number of design options were analyzed, such as optimization of air and fuel gas flow. Although many options showed little difference in apparent electrochemical performance, substantial differences in temperature distribution and peak stresses were observed.

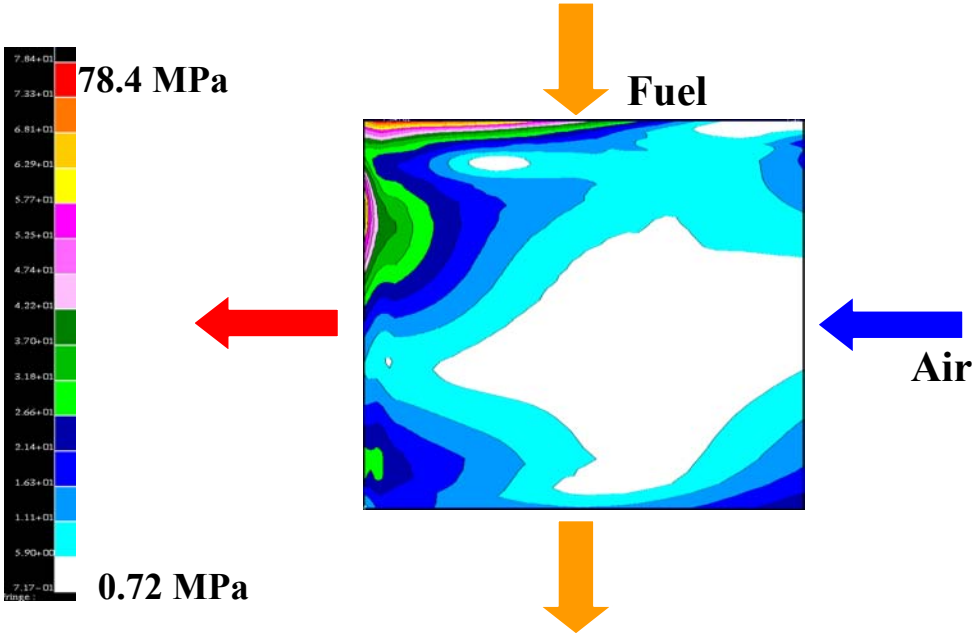


Figure 7. Stress distribution for a typical temperature profile exhibited by a cross-flow stack (stress values in MPa).

To address issues regarding the flow of air and fuel gas through the multi-layer stack additional modeling was performed. Computational Fluid Dynamics (CFD) codes were used to evaluate pressure drop through the air and fuel gas flow channels within the filled-via interconnect. In addition, micro-analyses were conducted to assess mass transfer through the porous electrodes. Micro-analyses of current flow through the stack were performed to insure that the selected materials and design features would provide for low stack resistance during operation at 800-900°C.

The most promising outcome of the modeling effort was the development of a novel modular stack design. Performing analyses for this design, however, required that the 2-D thermal/electrochemical model be extended to 3-D. The MTI design includes unique approaches for air and fuel gas manifolds, current collection and integration with air preheating and fuel

reformation. Significant improvements in electrochemical performance and stack reliability (temperature uniformity) appear possible. Equally important, the design represents a standardized stack configuration that appears to be amenable to high-volume production. The MTI Team pursued this new stack design during Phase II.

Task 4 – Manufacturing Cost Evaluation

A critical factor in selecting SOFC stack designs and fabrication methods will be manufacturing costs. As such, the MTI Team is developing cost models for MLC production operations, with specific focus on the multi-layer, co-fired SOFC. Initial production models providing high-level cost estimates have been established and include raw material inputs and all factors (labor, equipment through-put and capacity, yields, etc.) associated with each manufacturing operation. Estimates of capital cost for a 110-120 MW/year production facility were included. Although more work is required to refine the production model, results to date indicate that raw material costs and process yields will have a major impact on stack cost. In particular, raw material costs may represent 30-50% of the total manufacturing costs for planar SOFC stacks, thus emphasizing the critical need to develop low-cost sources of raw materials.

Task 5 – Multi-layer, Co-fired Oxide Configuration and Manufacturing Process Selection

The purpose of this task was to select the most promising stack design and approach to stack manufacturing. This task was initiated during August 2000 (month 11 of Phase I). Based on the work performed to date, the MTI Team developed a unique multi-layer SOFC stack design that can be readily configured into a standardized module that includes manifolds and current collectors. This design provides for superior electrochemical performance and reliability and appears to be compatible with MLC manufacturing methods. Preliminary cost analyses indicate that this stack can be manufactured at a cost of less than $300/kW. During Phase II, the MTI Team further refined the fabrication processes established during Phase I and developed the new stack design. Cost modeling efforts were expanded to include process simulations in preparation for design of a pilot-scale manufacturing facility.

Task 6 – Project Management and Reporting

All project management activities necessary to organize task activities, ensure adherence to project schedules and control costs were performed on a routine basis. A key accomplishment during Phase I was the creation of a unified team comprised of three different organizations in four geographic locations (MTI-Alliance, MTI-Lynchburg, Ceramatec-Salt Lake City, and M/A-COM-Buffalo). Open, direct communication between team members and technical assistance/collaboration between team members was accomplished. We also initiated activities involving external resources, such as Sandia National Laboratory, the Idaho National Engineering and Environmental Laboratory, Oak Ridge National Laboratory and Virginia Tech.

PHASE II – PROCESS DEVELOPMENT FOR CO-FIRED STACKS

Phase II Objectives

Phase II of the AMPS Program begin in October 2000 and was completed in March 2002 (18 month duration). As proposed, the goal for Phase II was to complete implementation of MLC manufacturing processes for cell and interconnect fabrication and to demonstrate co-firing of active cell components to form integral short stacks (with 3-10 cells). This goal was subsequently modified to include demonstration of 3-10 cell stacks using separately co-fired cells and interconnects.

To achieve the Phase II goal, the following specific objectives were defined:

- Refine the materials and processes for fabrication of co-fired cells and multi-layer interconnects. Demonstrate the ability to achieve repeatable fabrication of cells and interconnects.
- Develop models to support manufacturing process development for cells and interconnects and to support stack assembly and performance testing.
- Establish the materials and methods for assembly of short stacks (3-10 cells) using co-fired cells and interconnects.
- Demonstrate cell ASR < 0.8 ohm-cm^2 and stack ASR < 1.0 ohm-cm^2 at 850°C (for electrolyte supported cells). Define a pathway to reduce cell and stack ASR to commercial targets.
- Demonstrate the fabrication of co-fired repeat units and assess the feasibility for the fabrication of co-fired short stacks.
- Develop an improved SOFC stack design that overcomes the limitations created by the initial stack design and takes advantage of the strengths associated with multi-layer ceramic manufacturing methods.
- Assess the feasibility for replacing the high-cost raw materials used for multi-layer interconnects with low-cost alternatives.
- Develop destructive, non-destructive and electrochemical characterization methods that can be used for in-process quality control and final component inspection.
- Update the preliminary manufacturing cost model and reaffirm the potential for low-cost, high-volume production of co-fired, multi-layer SOFC stacks.

Phase II Task Structure

The Phase II effort was subdivided into six (6) primary tasks and additional subtasks, as follows:

- Task 7 – Information Required for the National Environmental Policy Act
- Task 8 – Preliminary Design of Short Stack (Active Area Component)
    - Subtask 8.1 – Design and Modeling
    - Subtask 8.2 – Stack Assembly and Testing
- Task 9 – Co-fired Short Stack Development and Characterization
    - Subtask 9.1 – Refinement of Co-fired Cell Fabrication
    - Subtask 9.2 – Refinement of Multi-layer Interconnect Fabrication

- Subtask 9.3 – Development of Co-fired Short Stacks
- Optional Subtask 9A – Design and Fabrication Development for Improved SOFC Stack
- Optional Subtask 9B – Alternate SOFC Materials

- Task 10 – Test Methodology and Plan
- Task 11 – Short Stack Fabrication and Cost Verification
- Task 12 – Project Management and Reporting

The schedule for the Phase II activities is shown in Table 1.

Table 1. Phase II Schedule and Key Milestones

TASK	YEAR 1				YEAR 2				YEAR 3				YEAR 4		MILESTONE/DECISION POINT DESCRIPTION
	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	
PHASE I															
PHASE II															
TASK 7															NEPA reporting requirements completed
TASK 8															Models validated and pSOFC short stack design established
TASK 9.1															Fabrication of high quality co-fired cells (100/mo)
TASK 9.2															Fabrication of high quality interconnects (100/mo)
TASK 9.3															Co-fired pSOFC short stack demonstrated
TASK 10															Inspection methods defined & test plan completed
TASK 11															Decision on short stack design/assembly
															Short stacks successfully fabricated
TASK 12															
Optional Work															
TASK 9A															Design and development of improved stack (10cmxn)
															Demonstration of 10cmxn cells and interconnects
															10 cm x n pSOFC stack demonstrated
															Preliminary validation of models & 10 cm x n design
TASK 9B															Improved cell and interconnect materials identified

▼ Milestone ◆ Decision Point

The Phase II project organization is shown in ***Figure 8***. The responsibility for planning and executing the work within each task was assigned to key individuals within the MTI Team. These Task Leaders worked with the MTI Program Manager, Dr. Eric Barringer, to insure that the project objectives were achieved on time and within budget.

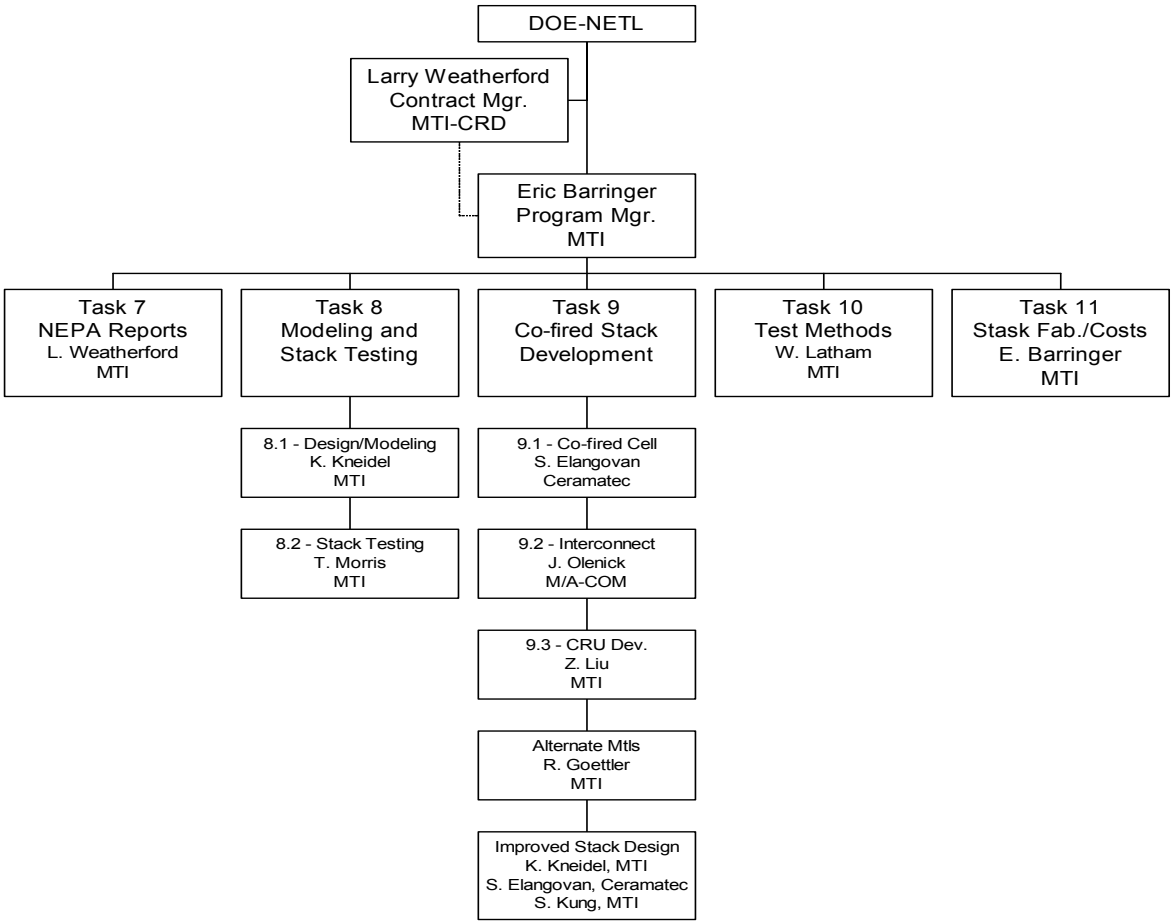


Figure 8. Phase II project organization

Additional information regarding the Phase II activities and key accomplishments is provided in the following sections.

Task 7 – Information Required for the National Environmental Policy Act

MTI provided to DOE all of the information required for the National Environmental Policy Act (NEPA). In particular, Environmental Questionnaires and Hazardous Waste Substance Plans were prepared for each entity participating in the Phase II effort. At the conclusion of Phase II, Hazardous Waste Reports were prepared for each entity and submitted to DOE.

Task 8 – Preliminary Design of Short Stack (Active Area Component)

The Task 8 effort, as originally proposed, consisted of updating the planar SOFC performance and structural models developing during Phase I, and then establishing a preliminary design for a 3-10 cell co-fired short stack. Prior to initiating Phase II, the work plan was modified to incorporate the following additional activities:

- Fabrication Process Modeling – Fabrication of co-fired cells, multi-layer interconnects and co-fired short stacks involve a number of sequential steps. Fabrication of high-quality components that achieve expected performance requires substantial knowledge of the key processing steps and the ability to control the processes. As such, the MTI Team recognized that numerical modeling of specific processes might be required to support the manufacturing process development work being performed under Task 9.

- Stack Performance and Structural Modeling – In addition to performing design/modeling activities for co-fired short stacks, the MTI Team defined the need to perform parallel design/modeling efforts for post-fired assembled stacks comprised of co-fired cells and multi-layer interconnects. The models were to be used to evaluate alternate designs, assess the impact of new materials, and to evaluate the structural reliability of individual components and assembled stacks.

- Short Stack Testing – Testing of short stacks (3-10 cells) comprised of co-fired cells and interconnects was determined to be a critical activity for validating the MTI multi-layer SOFC stack design and also for providing feedback to the cell and interconnect fabrication development tasks. Thus, the Team proposed to fabricate and test a limited number of short stacks. Performance data from these tests were to be used to validate the thermal/electrochemical and structural models and to update them, as appropriate. It was estimated that post-fired short stacks would be available for testing in the first quarter of 2001, while co-fired short stacks would not be available until early 2002. The results from this work produced improvements in the cells and interconnect design about one year earlier than originally scheduled.

The Task 8 activities and key results are summarized in the following sections.

Fabrication Process Modeling

Numerical modeling was performed to support the manufacturing process development efforts for co-fired cells, multi-layer interconnects and co-fired repeat units. Modeling activities are summarized below for the following areas: tape casting, lamination of interconnects and co-fired repeat units, binder removal, and stresses generated during co-firing.

- Tape Casting – Two modeling activities were conducted to support tape casting of electrolyte and interconnect tape. First, modeling of the slip drying process during tape casting was performed to improve the quality of tape used for cell and interconnect fabrication. Casting of the electrolyte and interconnect tape proved to be quite difficult

due to the use of fine-grained ceramic powders that are necessary for the co-fired repeat unit approach (to minimize the co-firing temperature). Tape fabricated with these powders often showed excessive defects (cracks, curling) and poor thickness uniformity. After considerable study, it became evident that controlled removal of solvent from the slip in the drying section of the tape caster was the key to improving tape quality. To optimize the slip drying process, illustrated in ***Figure 9***, a gas-phase mass transfer model was developed. The model was used to calculate the required air flow rate and temperature profile within the drying section of the caster to insure that almost all of the solvent was removed, but that the drying rate would not exceed the internal diffusion rate of solvent from the slip (to prevent "skinning"). Calculations were performed for both electrolyte and interconnect tapes; recommended drying profiles were successfully implemented on the tape casting machines at Ceramatec and M/A-COM. Significant improvements in tape quality resulted at both locations.

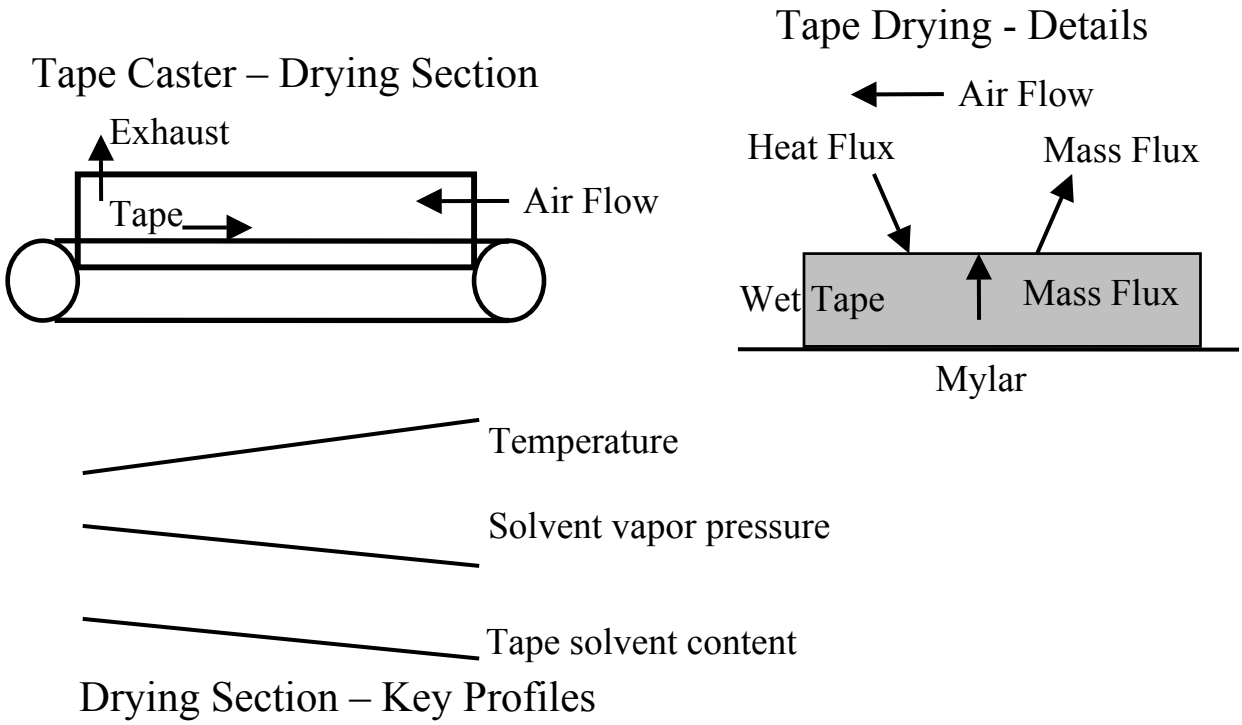


Figure 9. Illustration showing key processes addressed in modeling the slip drying step with the tape caster.

Second, modeling of slip flow in the doctor blade assembly was performed to support the design of an improved doctor blade that would achieve more uniform flow distribution for the slip and allow for casting of wider tape. Based on the modeling results, a new doctor blade assembly was fabricated and successfully demonstrated. After a few minor modifications, the new doctor blade assembly was implemented in the manufacturing development operations at Ceramatec and M/A-COM.

- Lamination of Interconnects and Co-fired Repeat Units – In the fabrication of the multi-layer interconnects and co-fired repeat units, laminating individual tape layers together to form a coherent body is required. Lamination is achieved by applying pressure to the tape layers at an appropriate elevated temperature to cause the "green" (unfired) tape layers to bond together. Insufficient pressure or too low in temperatures leads to non-bonded areas (delaminations) within the laminated part. Excessive pressure generally leads to deformation of the tape and/or the formation of cracks. Because of the fine ceramic powder used in fabricating the multi-layer interconnects, lamination of the interconnect tape proved to be very difficult.

  To identify appropriate temperature and pressure conditions for achieving acceptable lamination, numerical modeling of the lamination process was performed. Finite element models were developed for simplified versions of the multi-layer interconnect and the co-fired repeat units; these "mock" structures retained the key features of the components, but eliminate details that would overly complicate the models. In order to run the models, mechanical properties for the interconnect tape were required. A substantial number of tape specimens were tested under tension and compression to obtain the necessary data. An example of the finite element model output for a mock co-fired repeat unit is shown in ***Figure 10***. For the case shown, the lamination conditions were such that the model predicted that substantial deformation of the cell would occur. Upon examination of mock repeat units fabricated using such conditions, the predicted level of deformation was observed (see ***Figure 10***).

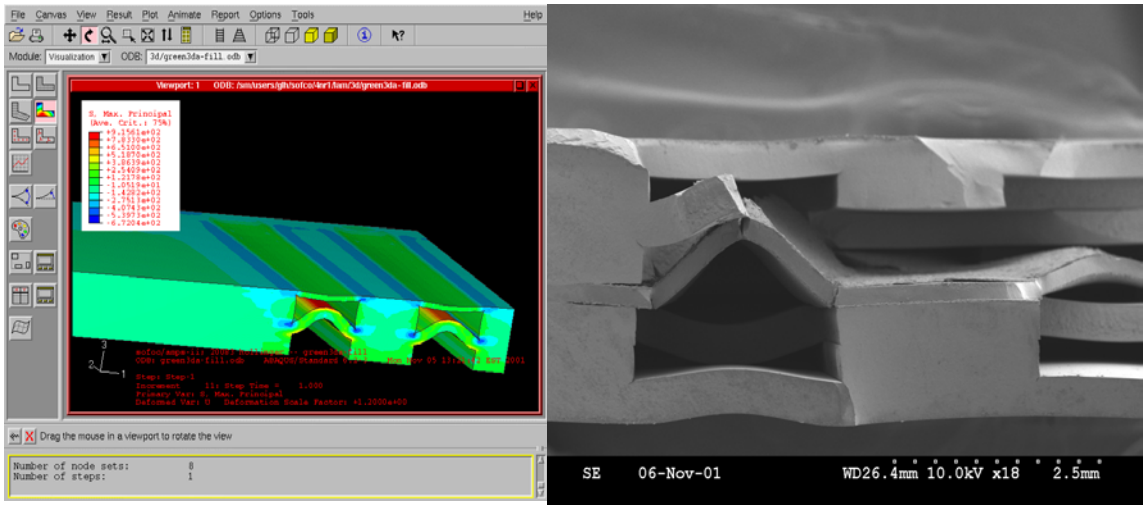


Figure 10. Finite element model prediction showing the expected level of cell deformation within a mock co-fired repeat unit (prior to firing) and the observed deformation of a cell within a mock repeat unit due to excessive lamination pressure.

After validation using mock components, the finite element models were used to evaluate design modifications for the interconnect and co-fired repeat units and changes to the lamination process in order to achieve more uniform stress distributions during lamination, and thereby substantially reduce the occurrence of deformation and cracks.

- Binder Removal – Removal of organic tape constituents from laminated multi-layer ceramic bodies is a critical step within the co-firing process. Improper removal of the binder phase (organics) during co-firing can result in defects, such as minor delaminations between layers or slight warpage of the component. In the extreme case, excessive binder removal rates can cause severe deformation and cracking of the part.

  During the development of the fabrication processes for multi-layer interconnects and co-fired repeat units, the MTI Team experienced significant difficulties in the co-firing operations. Significant delamination and cracking was observed; improper binder burnout was identified as a primary cause. Initial investigations showed that binder removal from the interconnect tape was made more difficult as a result of two factors: a) the fine ceramic powder used for the interconnect requires a high binder content in the tape to enable lamination; and b) the fine ceramic powder creates very small pathways for the diffusion of gasses out of the components during the burnout process. Rather than rely on empirical approaches to finding a solution to the binder removal problem, the MTI Team used numerical modeling to define an optimal binder burnout process.

  Modeling of the binder removal process involved a multi-step approach. First, thermogravimetric analysis (TGA) runs were performed in flowing air for the interconnect tape using a range of heating rates. The TGA data were then used to generate rate equations for the various kinetic processes (volatilization of solvent and low molecular weight species, oxidation of binder constituents, diffusion of gasses out of the part). Calculated values of weight loss versus time/temperature for the interconnect tape agreed well with the measured values (from TGA runs). Second, the rate expressions were used to define an "ideal" binder burnout heating schedule. The "ideal" heating schedule was then converted into a practical heating schedule that might be implemented in a commercially available co-firing furnace. Third, a numerical thermal transient model was developed for the current sintering furnace. The furnace was instrumented with numerous thermocouples and then run to obtain data for model validation. Fourth, final calculations were performed and a refined binder burnout heating schedule was defined. In addition, recommendations were made regarding the furnace capabilities and settering method that would achieve the desired binder removal process.

  As a result of the modeling effort, a binder burnout step was added to the co-firing process for both interconnects and co-fired repeat units. This process change dramatically improved the quality of the co-fired parts, eliminating many of the delaminations and cracks, and improving flatness.

- Stresses Generated During Co-firing – A key area of concern for the MTI Team was the stresses generated during co-firing of cells and interconnects. It was recognized that high stresses would lead to warpage of components and the formation of cracks. Excessive stresses could lead to component failure. Preliminary analysis indicated that the primary sources for stresses were: a) shrinkage mismatch during co-firing between the materials comprising the cells and interconnects, and b) coefficient of thermal expansion (CTE) mismatch between the materials.

  Shrinkage mismatch during co-firing was examined for both the cells and interconnects. For the cells, the primary concern was shrinkage behavior of the electrodes that were in contact with the electrolyte layer. Finite element modeling, primarily performed by Sandia National Laboratory, and experimental work revealed that shrinkage mismatch between cell constituents would strongly affect the flatness of the co-fired cells. Cell failure due to cracks or other defects was not an issue unless the shrinkage mismatch was excessive. For interconnects, shrinkage mismatch between the ceramic body and the electrical conductors was investigated through modeling and experimentation. Cracking of the ceramic body surrounding the conductors was the key concern. Through careful engineering of the starting raw materials, good shrinkage match was readily achieved for the interconnect; no cracks or other defects have been observed.

  Mismatch of coefficients of thermal expansion (CTE) between the cell and interconnect constituent materials is a major source for stresses, particularly during cool down of components from the sintering temperature and subsequently during thermal cycling. For the interconnects, the CTE mismatch between the ceramic body and the conductor material used during Phase II was very small. As a result, high stresses and crack formation were not an issue. However, the conductor material utilized a noble metal, making it prohibitively expensive for practical use. To support development of new, low-cost conductor materials for the interconnect; finite element modeling was performed using a simplified conductor geometry, as illustrated in ***Figure 11***. The modeling results were used to define the allowable range of CTE mismatch to minimize stresses and achieve an acceptable probability of failure.

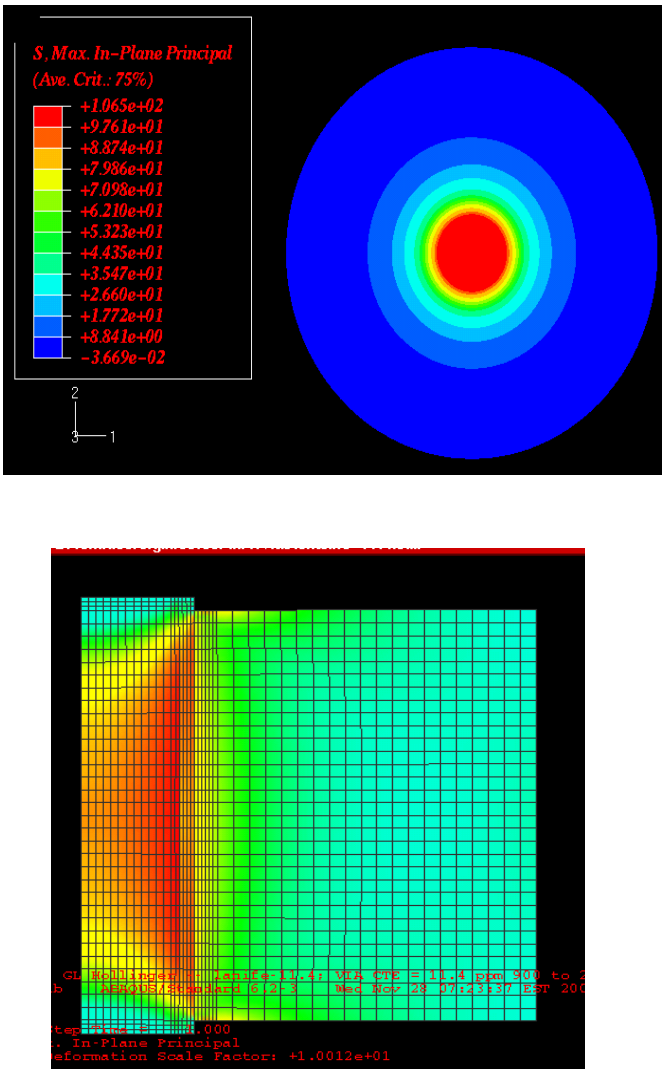


Figure 11. Simplified cylindrical conductor surrounded by a ceramic matrix was used for finite element models to assess stresses due to CTE mismatch between alternate conductor materials and the ceramic matrix.

For cells, the CTE mismatch between the anode and the electrolyte became an important issue. Finite element models for various cell designs showed that significant stresses are generated at the anode-electrolyte interface when the cells are cooled down from the sintering temperature to room temperature. In some cases, tensile stresses in the anode greater than 300 MPa were predicted. Cell fabrication experiments were performed in concert with the modeling effort. Cells fabricated under conditions for which high stresses were predicted were observed to have substantial microcracking of the anode; this confirmed that the tensile stresses in the anode exceeded the projected anode strength (~ 100 MPa). As a result of the modeling and experimental work, substantial effort was directed toward re-engineering the anode, with the

intent of reducing the CTE mismatch with the electrolyte while maintaining the electrochemical activity.

Stack Performance and Structural Modeling

Numerical modeling was performed in two areas to support the development of the multi-layer, co-fired stacks: a) stack performance modeling, and b) structural modeling of cells, interconnects and stack assemblies. The modeling work performed in these two areas is summarized below.

- Stack Performance Modeling – During Phase I, the MTI Team developed a 2-D coupled thermal/electrochemical model for the initial stack design. During Phase II, the model was modified for the new 10cm x n stack design and included the appropriate material properties and the primary geometric factors. After benchmarking the new model against the older 2-D models, calculations were performed to assess stack performance and temperature distributions for a number of stack operating conditions. A 3-D finite element structural model was also developed for the new stack design. Calculated temperature distributions for selected operating conditions were used in the finite element model to assess stress levels. The stress modeling did not reveal any area of concern within the stack, but did confirm that high stresses may exist at the electrolyte-anode interface due to the mismatch in CTE.

- Stack Performance Micro-modeling – While the thermal/electrochemical model provided useful insight into the expected operation of stacks, the MTI multi-layer SOFC stack design incorporates some unique design features that may significantly impact performance. Two specific areas were further investigated using "micro-models": a) current flow through the stack, with particular emphasis on the conductors within the interconnect, and b) diffusion of reactants from the gas flow channels within the interconnect to the active electrode surfaces.

  During operation of the multi-layer SOFC stack, current flows through the conductors within an interconnect to the cathode on the adjacent cell, through the cell, and then flows into the conductors in the interconnects that are adjacent to the anode. Experience has shown that the overall stack resistance is determined by the combination of individual resistances: cell resistance, interconnect resistance, contact resistance between cells and interconnects (on both the anode and cathode sides), and the current collector resistance. Furthermore, the resistance of the multi-layer interconnects depends on the resistivity of the conductor material and the conductor cross-sectional area (size and number of conductors). In addition, the interfacial resistance between the cells and the interconnect depends on the resistivity of the electrodes and the distribution of conductors within the interconnect that make contact with the cells. In order to better understand the relationship between the interconnect design, including the choice of conductor material and stack resistance, numerical modeling was performed. A 3-D finite element current distribution model was developed. The model incorporated all of the relevant design features and material properties. Calculations were first performed for specific test configurations; actual components incorporating the test configuration features were

fabricated and then tested to validate the models. Subsequently the model was used to estimate the interconnect and interface resistances for a range of interconnect designs and material conductivities. Improvements in the stack design and guidance for materials selection were key outcomes of this work. Toward the end of Phase II, the model was modified to facilitate analyses for various current collector designs and methods for attaching the current collectors to the multi-layer interconnects.

In addition to evaluating current flow, the MTI Team performed modeling to examine diffusion of fuel gas (hydrogen) and oxygen from the gas flow channels within the interconnects into the active portions of the anode and cathode, respectively. The gas diffusion models provided valuable insight regarding specific interconnect design features and the required thickness and porosity for the anodes and cathodes.

- Structural Modeling for Stack Assembly – Several modeling activities were performed in support of the stack assembly efforts involving co-fired cells and multi-layer interconnects. One approach to stack assembly explored by the MTI Team involved sequentially stacking together interconnects and cells, followed by application of a compressive load to insure good electrical contact and sealing between the cells and interconnects. When stacks are constructed with non-flat cells and interconnects, stresses are generated when the compressive load is applied and the components are deformed. To assess the level of stresses generated during stack assembly, physical characterization (including flatness) was performed for a number of cells and interconnects. Stiffness was also measured for these components using a specially designed fixture and a mechanical testing system. The data was then used in a finite element model for the stack and the stresses were estimated for both cells and interconnect. A key outcome from this modeling effort was guidelines regarding the desired flatness for cells and interconnects being produced under the cell and interconnect refinement task.

  In support of the stack assembly development effort, structural modeling was performed to examine several different approaches for attaching metal current collectors the multi-layer interconnects. Effective current collector attachment required good electrical contact with the conductors incorporated into the interconnect and, at the same time, low stresses. Finite element modeling was performed to estimate the expected stresses for a number of candidate current collector materials and several bonding materials (including conductive ceramic bond agents and various braze alloys). Through this work, the most promising combinations of current collector materials and bonding methods were identified.

- Cell and Interconnect Structural Modeling – Substantial structural modeling was performed during Phase II to support the design and fabrication development for co-fired cells and multi-layer interconnects. In addition to the previously mentioned finite element modeling to assess CTE and co-firing shrinkage mismatch issues for both cells and interconnects, modeling was performed to estimate the mechanical properties of the multi-layer interconnects (both the 10cm x 10cm and 10cm x n designs).

Initially, physical characterization of 10cm x 10 cm interconnects was performed, with particular emphasis on thickness profile and flatness. These data were used to generate solids models for selected interconnects and used in finite element models to estimate their stiffness and potential stresses that might be generated when these interconnects are incorporated into stacks. Measurements of actual stiffness for these interconnects were made using a mechanical load frame with appropriate fixtures. Correlation of the calculated stiffness and the measured stiffness for the interconnects showed good agreement (within 10%).

As a secondary check of the FEA model, the expected natural frequencies of an interconnect were predicted and they correlated very closely with the first four modal frequencies that were obtained from a "ping" test. In the ping test, an interconnect is struck with a "hammer" and the sound is recorded. An example of a typical ping test frequency spectrum is shown in ***Figure 12***. The first two calculated vibration modes for the interconnect are shown in ***Figure 13***.

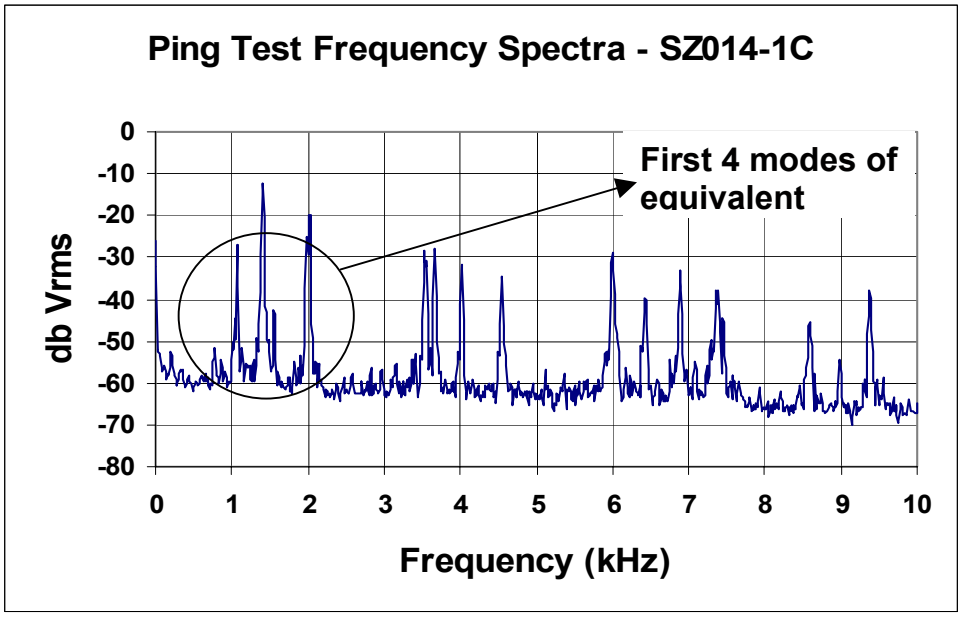


Figure 12. The measured frequency spectrum for a 10cm x 10cm multi-layer interconnect.

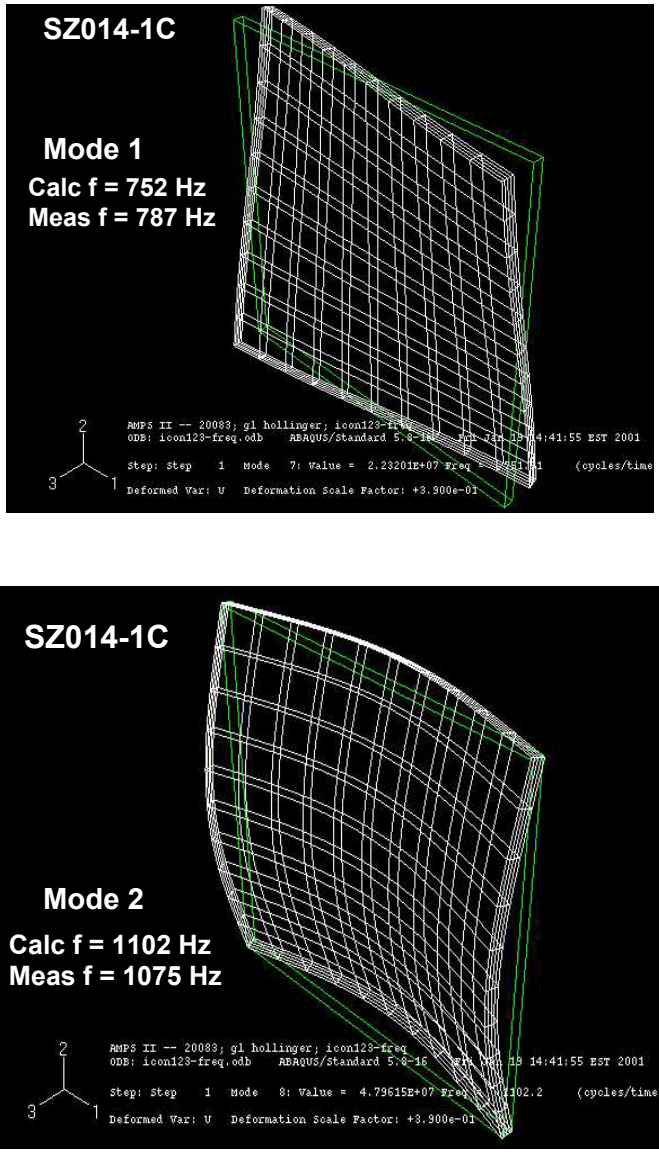


Figure 13. The first two calculated vibration modes for a multi-layer interconnect. Good agreement between the calculated and measured model frequencies was obtained.

One key outcome from this work was that the "ping test" was shown to be a good indicator of interconnect quality. A good interconnect gives a clear ring, along with well-defined modal frequencies. Conversely, an interconnect having cracks or delaminations tends to give a dull thud (substantial attenuation of the sound). Examples of typical ping test spectra for good and bad interconnects are given in ***Figure 14***. The agreement between the models and the ping test results provides additional confidence in the models and the current set of mechanical properties being used in the calculations.

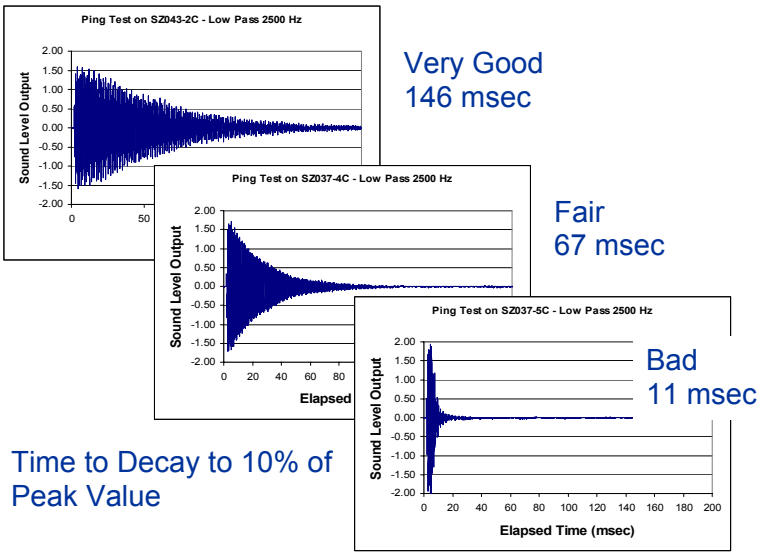


Figure 14. Ping test data for three interconnects showing the sound attenuation for good, fair and bad interconnects.

To support the structural modeling effort, the MTI Team had to perform a variety of tests on cell and interconnect materials to acquire the necessary mechanical property data. First, MTI obtained structural property data for the electrolyte and interconnect body materials using a 4-point test fixture. Virginia Tech also performed mechanical characterization for the electrolyte and interconnect body materials, using a ball-on-ring technique. Failed specimens were sent to the Idaho National Engineering and Environmental Laboratory for fractographic analysis in order to identify the strength limiting flaws that caused failure of the specimens. Penn State obtained mechanical property data at elevated temperatures for a range of cell and interconnect materials using dynamic modulus testing. Finally, as previously mentioned, MTI performed mechanical testing on complete interconnects (both the 10cm x 10cm and 10cm x n designs). The test set-up is shown in ***Figure 15***. The measured stiffness for the interconnects compared well with predicted stiffness when the above-mentioned material property data was used in the finite element models.

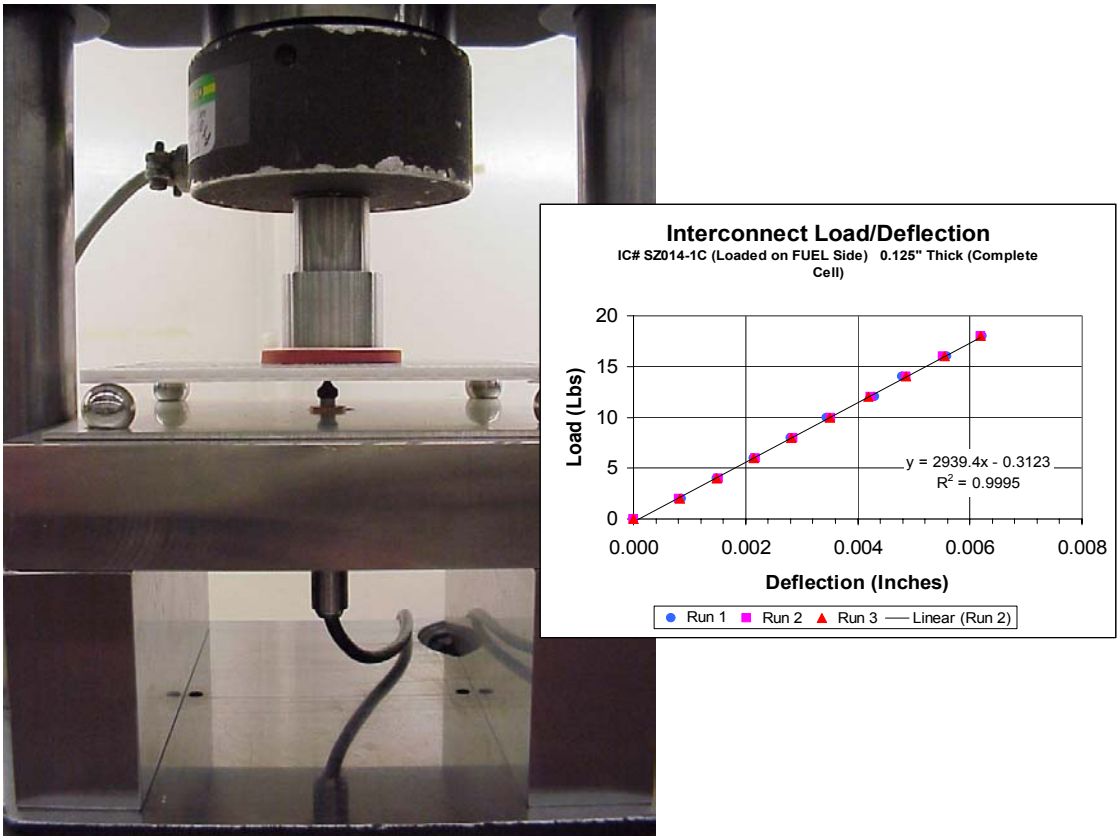
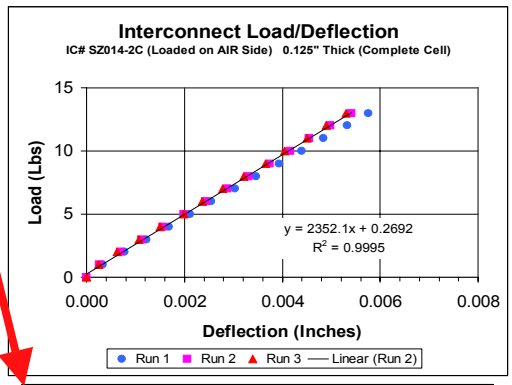


Figure 15. Mechanical testing arrangement for the multi-layer interconnects. This test was used to determine interconnect stiffness and to assess the strength of interconnects.

Interconnects were also loaded to failure, using a cycling load method. During loading, crack initiation/propagation was assessed by using acoustic sensors "listening" for snapping sounds. An example of the data obtained in testing one interconnect is shown in ***Figure 16***. In general, there was good agreement between the observed occurrences of interconnect cracking and the maximum recommended load to avoid overstress conditions based on finite element analyses.

Increasing Load Cycles SZ014-2C		
Cycle No.	Max. Load (lbs)	Observations
1	13	None
2	13	None
3	13	None
4	26	Snapping sounds at 20,22, 24, 26 lbs
5	26	Snapping sounds at 26 lbs
6	26	Snapping sounds at 26 lbs
7	45	Snapping sounds at 30, 35, 40, 45 lbs. Load dropped from 45 to 10 lbs.
8	5-10	Interconnect split in half at 5-10 lbs



FEA Analysis recommended max load of 16.7 lbs to avoid overstress situation

Figure 16. Load-to-failure data for a multi-layer interconnect. Cracking of the interconnect was observed when the applied load exceeded the maximum recommended load from finite element analyses.

Short Stack Assembly and Testing

Stack testing was performed during Phase II as an important means for obtaining critical feedback on cell and interconnect quality, in support of the cell and interconnect refinement tasks. Although limited testing was originally planned for Phase II, the level of effort directed at stack assembly and testing was significantly expanded during the Phase II period. One reason for the increased activity was the need to develop suitable materials and assembly techniques for building stacks with the co-fired cells and multi-layer interconnects. The second reason was that expected stack performance was not achieved, based on the measured performance for single cells. The source(s) for the observed "performance gap" needed to be resolved.

Stack assembly efforts initially focused on co-fired cells and metallic interconnects. These interconnects and the stack assembly method used for the early stacks was based on previous experience in building stacks with standard post-fired cells. This work was performed to insure that stacks could be constructed using the newly developed co-fired cells and to begin obtaining performance data to benchmark stacks using co-fired cells against previously tested stacks using post-fired cells. No significant issues were identified in stack assembly and electrochemical testing showed similar performance between stacks made using the two types of cells (for the same electrolyte thickness).

In parallel, an effort was initiated to develop the materials and stack assembly method for the multi-layer interconnects. The work was focused on five key areas: 1) materials and application method to make electrical contact between cell electrodes and the interconnect conductors; 2) materials for the cell-to-interconnect seal; 3) design and attachment/sealing method for the air

and fuel manifolds; 4) design and attachment method for the current collectors; and 5) method to compressively load the stack to facilitate stack assembly and subsequent installation into the stack test stand.

The basic arrangement for assembly of stacks using co-fired cells and multi-layer interconnects is shown in ***Figure 17***. For typical stacks, metal current collectors were bonded to the outer interconnects using a conductive ink. Cells were placed between interconnects and electrical contact was made using a conductor paste. A key issue that had to be overcome during the development effort was dealing with non-flat components and achieving good contact across the surface of cells. This necessitated the development of "compressible" conductor materials. Although not shown in the figure, a seal material was applied around the perimeter of each cell. Cell-to-interconnect sealing for early stacks was achieved using the seal material and application method that had been previously used for metal-interconnect stacks. Likewise, manifold designs and the compressive loading method were adapted from previous work with metal-interconnect stacks.

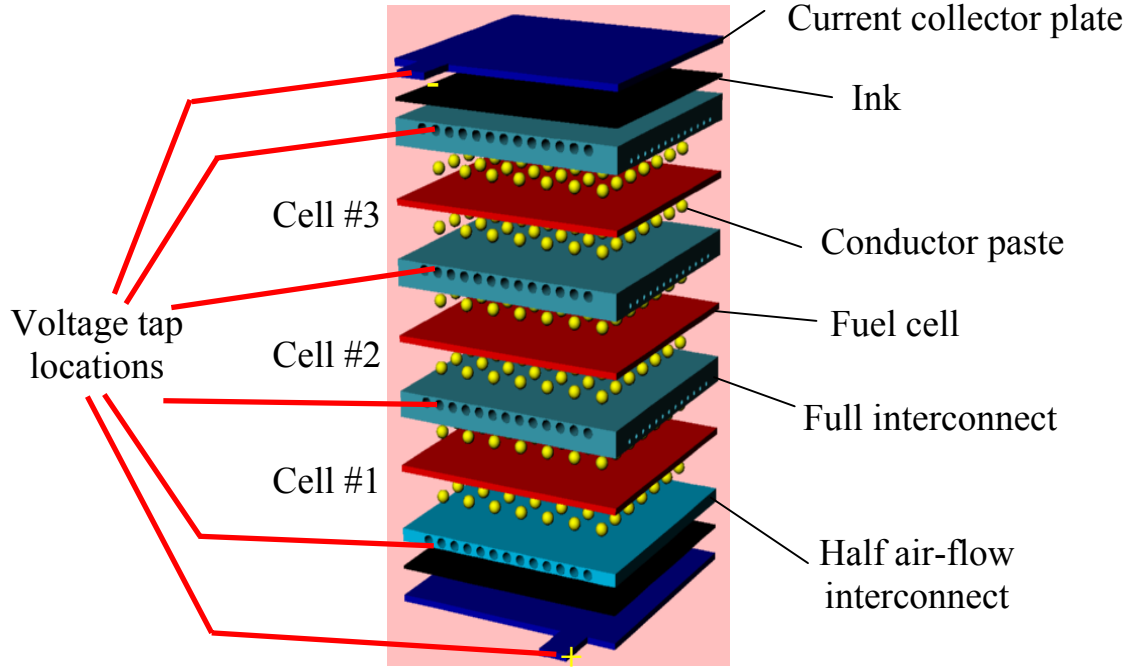
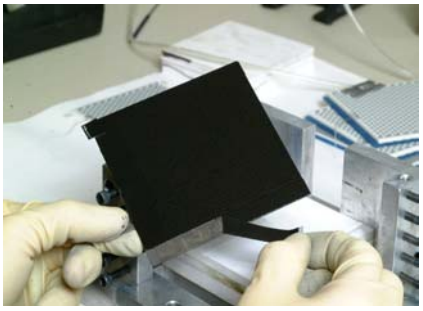


Figure 17. Schematic showing general arrangement for stacks assembled using co-fired cells and multi-layer interconnects.

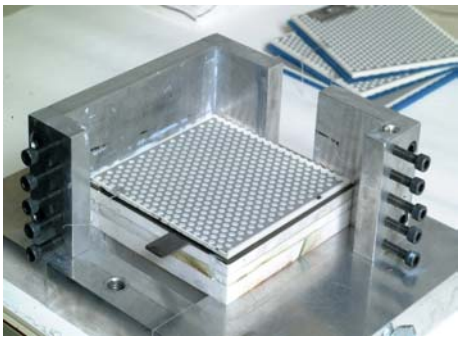
The initial steps for constructing a typical stack are shown in ***Figure 18***. As a first step, a ceramic plate (insulation) was placed in an assembly fixture. The fixture ensured proper alignment of the various stack components during the assembly process. Next, a current collector plate was coated with conductive ink and then placed on top of the ceramic plate. This was followed by placement of the bottom interconnect on top of the current collector plate. A conductor paste was then deposited onto the interconnect, followed by a cell, more conductor

Start with ceramic plate
with TC groove and zirconia paste



Apply ink to central region of
stainless steel current collector plate

Set current collector
plate on ceramic plate



Roll ink onto interconnect
and set on current collector plate

Figure 18. Initial steps for stack assembly when using co-fired cells and multi-layer interconnects.

paste and an interconnect. This sequence was repeated until the desired stack height (number of cell-interconnect repeat units) was achieved. To complete the stack, a current collector plate was bonded to the top interconnect. A 5-cell stack constructed using this method is shown in ***Figure 19***.

Stack assembly and testing activities were limited during the first two quarters of Phase II, but increased significantly in the third quarter of Phase II (starting April 2001) as the number of cells and interconnects having acceptable quality for testing increased. Initial stack tests were performed with co-fired cells using both metal and multi-layer ceramic interconnects. Reasonable power densities were achieved for the co-fired cells and stack performance was similar for both types of interconnects.

Figure 19. A completed 5-cell stack assembled with co-fired cells and multi-layer interconnects.

During the second quarter of 2001 more than 20 stacks were constructed and tested. Performance data for a typical stack constructed during this period is shown in ***Figure 20***. For this stack, the initial area specific resistance (ASR) was about 1.8 ohm-cm^2, but the ASR degraded rapidly over the first 100-150 hours to about 2.6-2.7 ohm-cm^2. Thereafter, stack performance continued to degrade, but at a much slower rate. A standard method for assessing degradation was defined, whereby the ASR versus time data was used in a linear regression

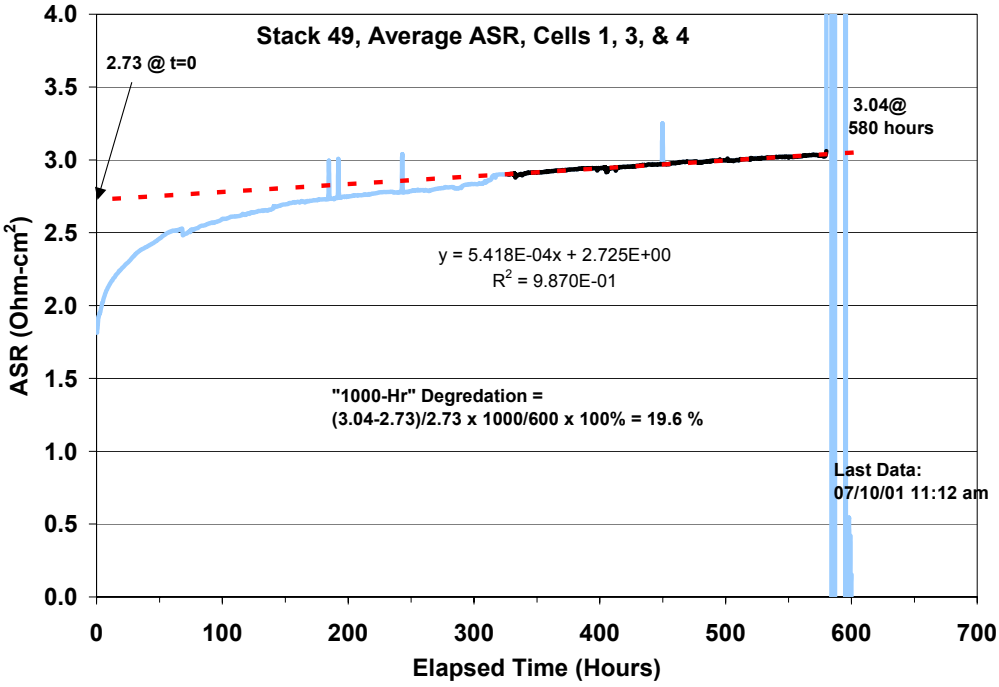


Figure 20. Electrochemical performance data for a stack constructed with co-fired cells and multi-layer ceramic interconnects.

analysis. From the results, an extrapolated ASR value at time=0 was defined, along with an initial 1000 hour ASR degradation rate. For stack 49, shown in the figure, the extrapolated $ASR_{t=0}$ was 2.73 ohm-cm^2 and the degradation rate was 20% per 1000 hours.

For the stacks constructed and tested during the second quarter of 2001, the starting ASR values were typically in the range of 1.75 to 2.25 ohm-cm^2. All stacks showed a similar rapid degradation in performance over the first 100-150 hours. However, the initial degradation rates varied over a wide range (15-50% per 1000 hours). Investigations were conducted to identify potential sources for the high ASR and degradation rates. Testing confirmed that the interconnects had a low resistance, but that the contact resistance between the cells and interconnects was high. Microscopic examinations showed that the bond between the conductor paste and the cells was not good, and separations often occurred, as shown in ***Figure 21***. In addition, leaks in the cell-to-interconnect and manifold seals were often observed.

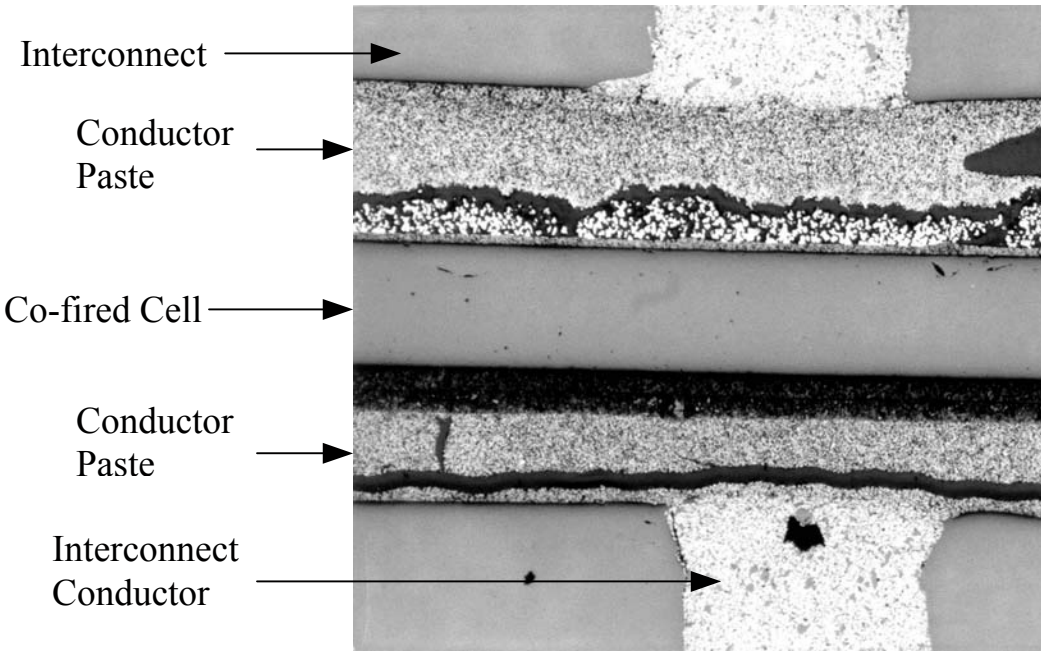


Figure 21. Cross-section of a co-fired cell in a stack showing separations between the conductor paste and the cell.

Improvements were made to the conductor paste and the cell-to-interconnect seals. As a result, the starting ASR values for stacks dropped to 1.5-2.0 ohm-cm^2. Within a number of stacks, individual cell repeat units showed ASR values in the range of 1.0-1.5 ohm-cm^2. These results were encouraging, given that ASR measurements for 2.5 cm button cells that were fabricated along with the full-size cells had ASR values in the range of 1.0-1.25 ohm-cm^2. However, degradation did not show much improvement. Stack performance generally degraded about 25-30% over the first 100 hours, and thereafter degraded at a rate of about 25% per 1000 hours. Conversely, while the button cells showed some initial degradation over the first 100 hours, the longer-term degradation was typically less than 3% per 1000 hours.

Toward the end of Phase II (first quarter of 2002), further improvements were made in the conductor paste and in the attachment of current collectors to the multi-layer interconnects. More important, a significant improvement was made in the seal material, thereby substantially reducing leakage. While there was little change in the degradation behavior over the first 100 hours, there was a large reduction in the longer-term ASR degradation. The degradation rates still varied considerably, ranging from 0% to 25% per 1000 hours.

With an apparent solution to cell-to-interconnect and manifold sealing, stack efforts for the final months of Phase II were focused on the source(s) for higher than expected electrical resistance. Three areas requiring additional work in the future were identified:

1) Degradation during the first 100 hours of electrochemical testing is largely due to the cells. This is not a stack issue, but must be addressed in future cell R&D.
2) The contact resistance between cells and interconnects remains a primary factor in high stack ASR values. Improved materials and application methods are required to reduce the contact resistance to the required levels.
3) One key source for variability in longer-term stack degradation is the occurrence of defects in co-fired cells (pin-holes, cracks, etc.) that allow gas leakage within the stacks.

Task 9 – Co-fired Short Stack Development and Characterization

During Phase I, the MTI Team successfully demonstrated the feasibility for co-fired cells and multi-layer ceramic interconnects. However, in the original proposal for Phase II it was anticipated that additional development work would be necessary to meet the quality level required for co-fired stacks. As such, the original plan called for focusing substantial effort during the first 9 months of Phase II on completing the development of the fabrication processes for 10cm x 10cm cells and interconnects. Afterward, the focus was to be shifted toward fabrication development for co-fired repeat units and short stacks.

While preparing the Phase II work plan, the MTI Team determined that a more intense effort than originally planned was required to complete cell and interconnect development. In particular, the team recognized that the ability to laminate together and co-fire multiple cell and interconnect repeat units to form stacks would be critically dependent on the quality of the green cells and interconnect layers supplied to the final lamination step. Furthermore, it was believed that the desired quality could only be achieved on a repeatable basis by transitioning cell and interconnects fabrication to a "production" environment, with all of the associated documentation and controls. To this end, the MTI Team proposed to complete the development of the fabrication processes for 10cm x 10cm cells (under Subtask 9.1) and interconnects (under Subtask 9.2) and then begin low-rate "production" of about 100 co-fired cells and interconnects per month. These cells and interconnects were to be inspected against preliminary specifications and then made available for post-fired assembly in short stacks for testing (under Subtask 8.2). Upon demonstrating that acceptable quality for green cells and interconnects had been achieved, the updated plan called for initiating development of co-fired repeat units and short stacks (under Subtask 9.3).

Subtask 9.1 Co-fired Cell Refinement

Toward the end of Phase I, the MTI Team successfully fabricated and tested a limited number of 2.5cm co-fired button cells; several of these cells had ASR values in the range of 0.9-1.2 Ω-cm^2 (at 850°C). Feasibility for fabrication of 10cm x 10cm cells was also demonstrated, but these cells were not suitable for stack assembly. For Phase II, the primary objectives were: 1) refine the fabrication processes and demonstrate repeatable fabrication of cells that meet the requirements for stack assembly and testing; and 2) demonstrate cell ASR $\leq$ 0.8 Ω-cm^2 on a repeatable basis and define a pathway to reduce the ASR to commercial targets.

The cell refinement subtask was subdivided into two areas: 1) cell R&D aimed at improving performance (reducing ASR); and 2) fabrication development for 10cm x 10cm cells. As discussed below, a substantial portion of the effort was directed at resolving materials and process issues that arose in attempting to achieve repeatable fabrication of 10cm x 10cm cells. As a result, R&D work aimed at improving cell performance was limited.

Cell Performance Improvement

Early co-fired button cells showed reasonable electrochemical performance; however, initial testing revealed a number of areas for which further development was required. First, the anode microstructure at the anode-electrolyte interface was found to be unacceptable. Although initial anode resistance was acceptable, the anode adhesion to the electrolyte was poor, particularly after reduction of the NiO phase to Ni. Second, the cathodes showed some evidence of deleterious interactions with the setter materials used during co-firing and also had an "over-fired" appearance. The result was cathodes with a higher than desired polarization resistance.

Substantial effort during Phase II was directed at improving the anode microstructure and adhesion. Initial work focused on the composition of the anode (Ni to ceramic ratio) and the characteristics of the powders used in preparing the anodes. Although the details are not revealed in the report, it is important to point out that the co-fired anode does not simply consist of NiO and YSZ. Rather, the composition is much more complicated, and includes a number of additional constituents. In any event, through careful experimentation a range of compositions and starting powder characteristics were identified that achieved the desired level of adhesion and an improved interface microstructure. A specific anode composition was selected and successfully implemented in the fabrication of 10cm x 10 cm cells. The microstructure for the improved anode is shown in ***Figure 22***. Electrochemical testing of 2.5cm button cells confirmed that a relatively low anode resistance was retained.

While overcoming the problems with the anode was difficult for the MTI Team, the problems that surfaced for the cathode were even more challenging. First, the material used for the cathode, while appearing to be suitable for co-firing with a YSZ electrolyte, showed numerous adverse interactions with the setter materials used during the co-firing process. In some cases, the reactions were severe enough to be readily observed (e.g., substantial change in color). In other cases, the reactions were much more subtle, only being observed through resistance measurements or microscopic examination of the co-fired cathode. After significant effort was expended, a suitable setter material and co-firing process was developed. Second, the

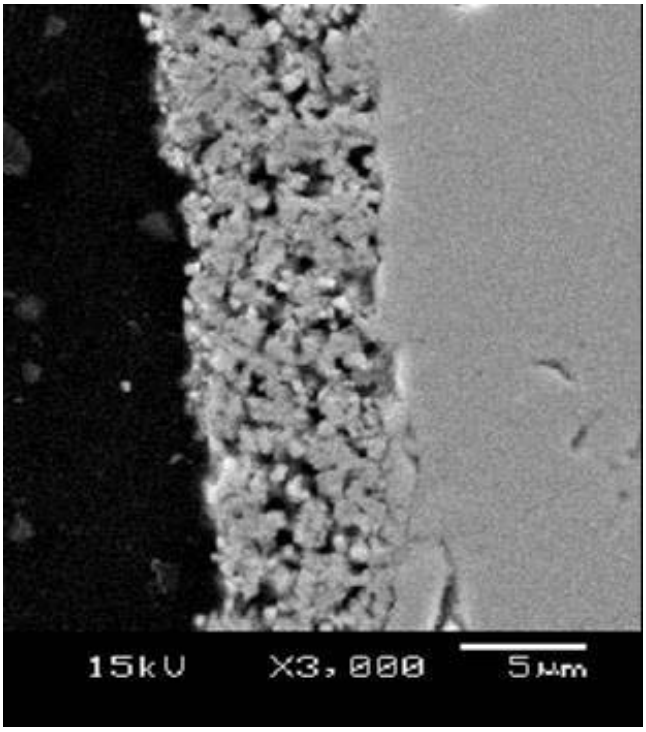


Figure 22. SEM micrograph showing the structure of the improved co-fired anode.

microstructure of the co-fired cathode often displays an "over-fired" appearance (many dense areas and non-uniform porosity). A SEM micrograph showing a typical over-fired cathode is provided in ***Figure 23***. To address this problem, the MTI Team elicited support from the University of Missouri-Rolla (UMR) and the Pacific Northwest National Laboratory (PNNL).

Fundamental characterization of the MTI cathode material and stability of the cathode during co-firing with the YSZ electrolyte material was investigated by UMR. Extensive characterization of the cathode material and cathode-electrolyte couples confirmed that no deleterious reactions occur between the cathode material and the electrolyte during co-firing. This result was confirmed by PNNL through detailed characterization of co-fired cells using analytical microscopy. Toward the end of Phase II, it was concluded that the cathode microstructure (and performance) could be substantially improved by better controlling the cathode powder characteristics and the co-firing conditions. Efforts to implement the findings from these investigations were transitioned into the Solid State Energy Conversion Alliance (SECA) program.

The work conducted to improve the anode and cathode resulted in more consistent cell performance, but did not substantially improve the ASR values. Toward the end of Phase II, button cell ASR values were generally in the range of 0.75 to 1.2 Ω-cm^2 (at 850°C), depending on the quality of the co-fired cathode. It should be noted that the theoretical ASR value for cells having an electrolyte thickness of about 180 microns is about 0.7 Ω-cm^2. Thus, the performance of the MTI co-fired cells approached the theoretical limit. To further reduce cell ASR,

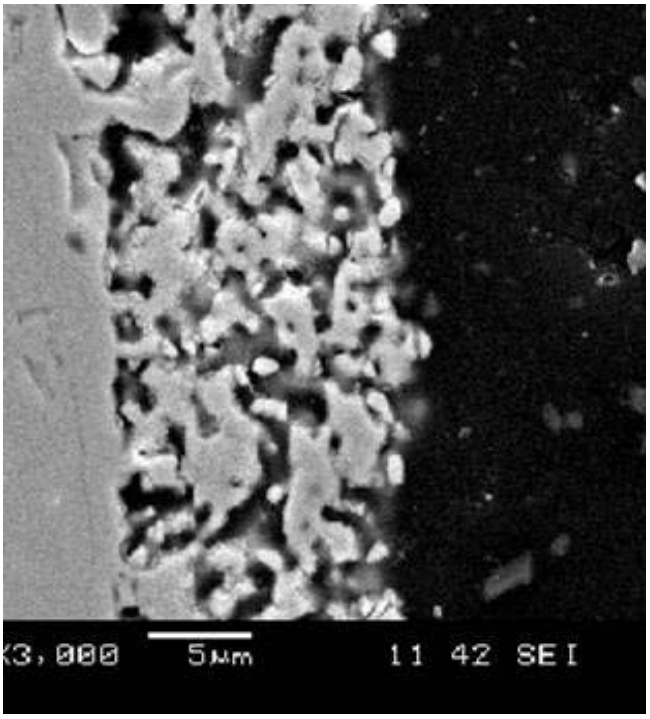


Figure 23. SEM micrograph showing a cathode with an over-fired appearance. The microstructure is not uniform and contains many dense regions.

attempts were made to fabricate cells using thinner electrolytes (~100 micron thickness). The MTI Team was successful in fabricating 2.5cm co-fired button cells and achieved ASR values in the range of 0.6-0.8 Ω-cm^2. However, attempts to fabricate 10cm x 10cm cells were generally not successful. Many of the cells fractured during fabrication or when attempting to assemble stacks. The causes for cell failure are being investigated under the SECA program.

A final outcome of the Phase II effort was the definition of a path forward for development of co-fired cells that will achieve the commercial targets for electrochemical performance. One option involves the development of a cell having an intermediate thickness electrolyte (50-75 microns), but using Sc-doped zirconia as opposed to YSZ. A second option being evaluated involves the development of electrode-supported cells having a thin electrolyte (10-20 micron thickness); the electrolyte may be either YSZ or a Sc-doped zirconia material. Cathode-supported and anode-support cell designs will be considered, as the MTI Team has the ability to co-fire either type of structure. This work will be performed under the SECA program.

Fabrication Process Development

In developing the fabrication processes for co-fired cells, the MTI Team utilized proven multi-layer ceramic manufacturing methods. As illustrated in ***Figure 24***, this involved:

- Synthesis of anode and cathode powders
- Formulation of anode and cathode inks
- Slip preparation and casting of electrolyte tape
- Screen printing the anode and cathode onto an electrolyte tape blank
- Co-firing cells using a carefully controlled temperature profile
- Physical/visual inspection of cells per specification

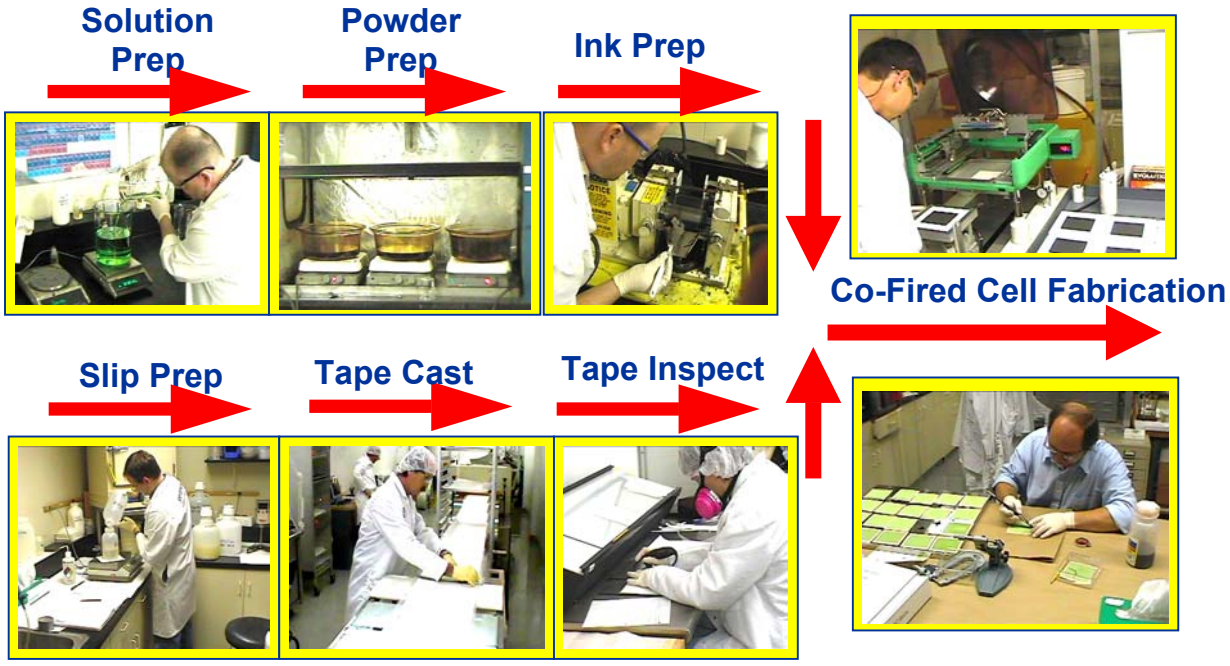


Figure 24. Process flow for fabrication of co-fired cells

A substantial portion of the activity of the cell refinement subtask was directed at manufacturing process development for full-size 10cm x 10cm cells. Very early in the effort to scale cell size from 2.5 cm button cells up to full-size cells, it became evident that the fabrication of co-fired cells was a complicated endeavor and that minor changes to the raw materials or processing conditions could significantly affect the quality of the cells. Moreover, processing conditions that appeared to work well for fabricating a few button cells sometimes did not yield the desired results when applied to the fabrication of larger batches (24 or 48 cell lots) of full-size cells. Several key areas where such difficulties were encountered were: Shrinkage match between the electrodes and the electrolyte during co-firing; settering of cells in the furnace; binder removal during co-firing; and electrode adhesion.

In developing the anode and cathode screen printing inks, adequate shrinkage match was initially obtained for button cells, thereby leading to flat cells after co-firing. However, the shrinkage match was not sufficient for 10cm cells; the cells generally showed excessive warp after co-

firing. At the same time, electrode adhesion, which appeared to be acceptable for co-fired button cells, was not acceptable for the full-size cells. Achieving acceptable flatness and electrode adhesion required further refinement of the physical characteristics (particle size, surface area) for the anode and cathode powders, along with adjustments to the ink formulations. A complicating factor in addressing the shrinkage-matching problem was that each time a change was made in the electrolyte tape, either to the processing conditions or the formulation, adjustments had to be made to the anode and cathode inks.

As previously discussed, selection of the setter materials and definition of the basic settering arrangement for co-firing was performed using button cells. Numerous problems were encountered with reactions between the electrodes, particularly the cathode, and the setters. With significant effort the problems were overcome. However, when transitioning from button cells to the full-size cells an additional set of issues arose. To achieve acceptable full-size cells, greater attention had to be directed toward specifying the porosity, flatness and size/weight for the setters. Moreover, a setter plate had to be placed on top of each cell during co-firing to ensure adequate flatness. If too little weight was used, the cells were not flat. Too much weight, however, often caused damage to the cells.

Because of the sensitivity in cell quality and performance on the processing details, the MTI Team encountered significant difficulties in transitioning from an R&D mode of fabricating a few button cells per batch to a mode of processing much larger batches (24 and 48 cell lots) of full-size cells. As a result, it became necessary to implement a production discipline with all of the associated process documentation and controls. Specific challenges addressed by the team were:

- Tape casting – Initial development for co-fired button cells was conducted using electrolyte tape produced with a bench-top tape caster. As the demand for electrolyte tape increased, a new continuous tape caster was implemented into the development line. Substantial effort was required to engineer the casting process, and thereby permit casting of electrolyte tape that was suitable for cell fabrication.

- Screen-printing – A number of issues surfaced in attempting to print electrode inks on full-size cells and processing a large number of parts. Areas that had to be addressed included: flatness of green tape; maintaining registration/alignment for tape blanks; ink consistency during extended printing campaigns (screen life); and drying the inks on the printed blanks. A number of controls were employed to monitor the printing operations. One key process control measure was to monitor the weight of anode and cathode ink printed onto the green tape. As shown in ***Figure 25***, improved consistency of the printing process was achieved for both the anode and cathode.

- Co-firing – Achieving uniform sintering when firing a full load of cells in a periodic batch furnace was found to be much more difficult than firing a small number of cells in the same furnace. Significant attention was focused on the placement of kiln furniture, the settering arrangement for the cells, and the temperature profile. Achieving a uniform temperature within the "working zone" of the furnace was critical. In addition, adequate air-flow in the furnace was required for proper binder removal. One metric used to

monitor the firing process was to track the final dimensions of the co-fired cells. ***Figure 26*** shows the average dimensions for lots of cells processed over a 9-month period. Consistent X-Y dimensions were achieved for the co-fired cells.

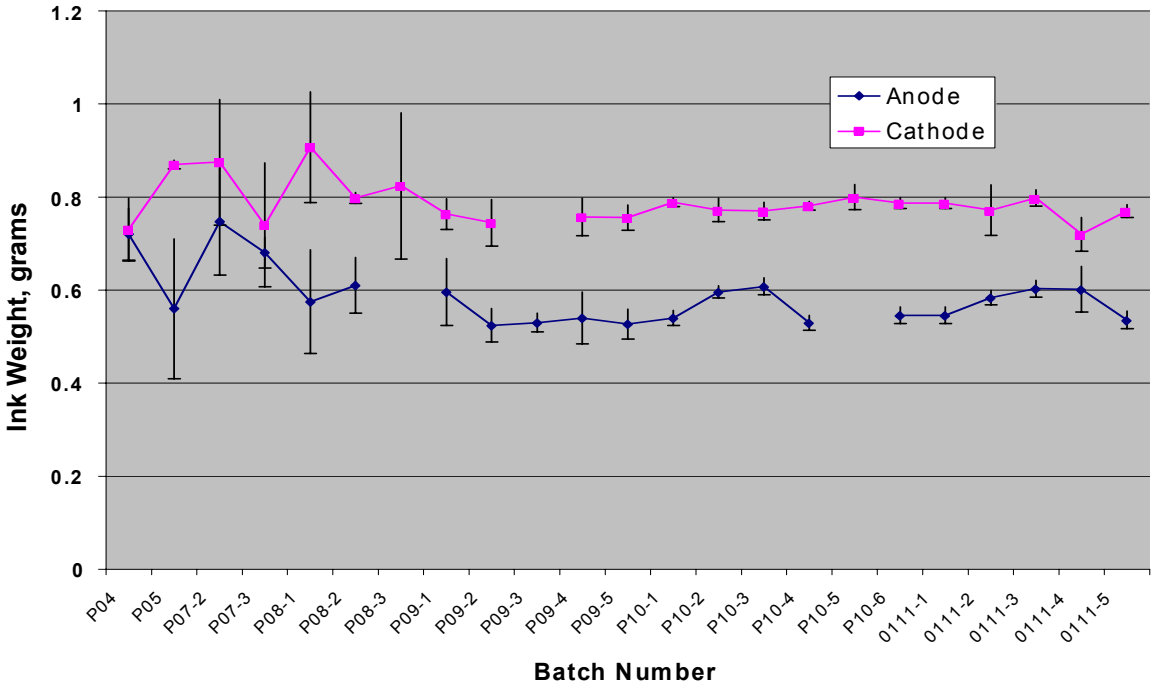


Figure 25. Average weight of anode and cathode inks screen-printed onto tape blanks for cell lots processed over a 9-month period.

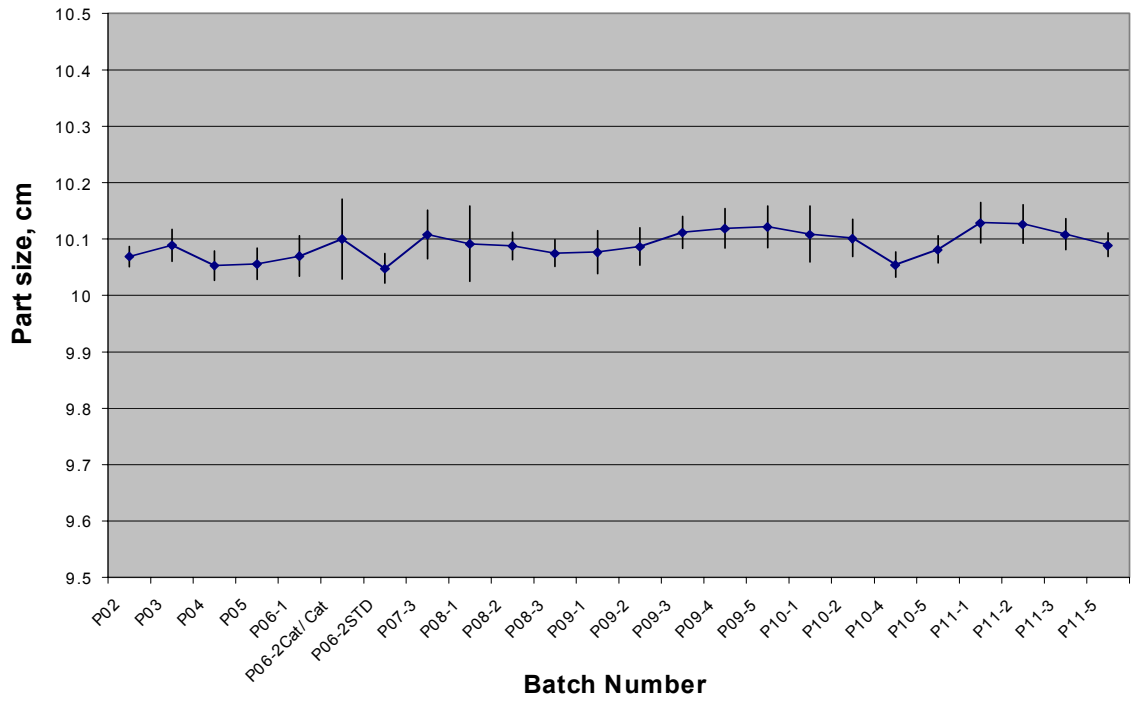


Figure 26. Average dimension (in centimeters) of cells from lots processed over a 9-month period.

- Cell inspection – In handling a few cells during visual and physical inspection, considerable care can be taken to avoid damaging the fragile cells. However, it became impractical to use the same level of care when attempting to fully inspect cells from large batches (e.g., 48-cell lots). New procedures and inspection tools were required to facilitate inspection and avoid damaging the full-size cells.

With considerable effort, the MTI Team successfully implemented low-rate production of 10cm x 10cm cells (at a rate of approximately 100 cells per month). ***Figure 27*** shows examples of small (18-24 cells) and large (typically 48 cells) production lots, along with the rider button cells that were processed with the full-size cells (using the same electrolyte tape and electrode ink batches). The rider button cells were used to assess the electrochemical performance for each lot of cells. As a result of improvements made to the materials and fabrication processes during Phase II, considerable improvement in the electrochemical performance for the rider button cells was observed. The run chart for rider button cell ASR, provided in ***Figure 28***, shows that reduced variability and improved performance were achieved. Toward the end of Phase II (first quarter of 2002), the ASR values for rider cells were generally in the range of 0.75 to 1.1 Ω-cm^2 (at 850°C). As shown in ***Figure 29***, the performance for rider cells was stable after the initial 100-hour period.

In summary, significant progress was made in the manufacturing process development for co-fired cells. Processes were established for repeatable fabrication of 10cm x 10cm cells. R&D activities were successful in improving cell performance and driving the ASR toward the

theoretical limits (based on the thickness of the YSZ electrolyte). Finally, a pathway was defined for developing a second-generation co-fired cell having a much lower resistance.

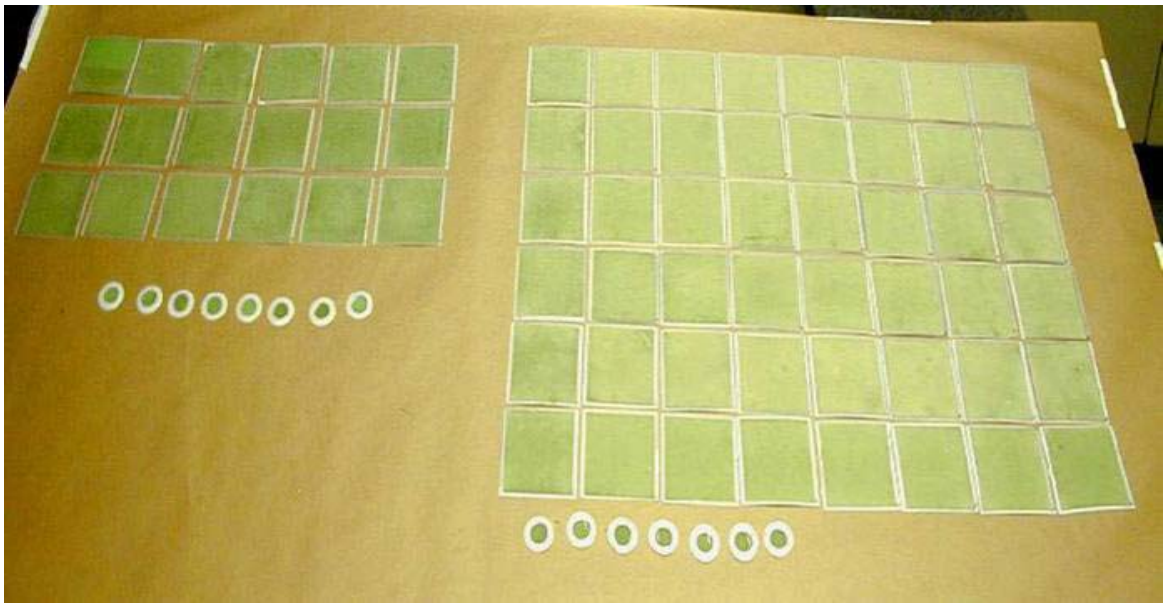


Figure 27. Typical 10cm x 10cm cells produced in small (left) and large (right) production runs, along with the rider button cells that are used to assess electrochemical performance.

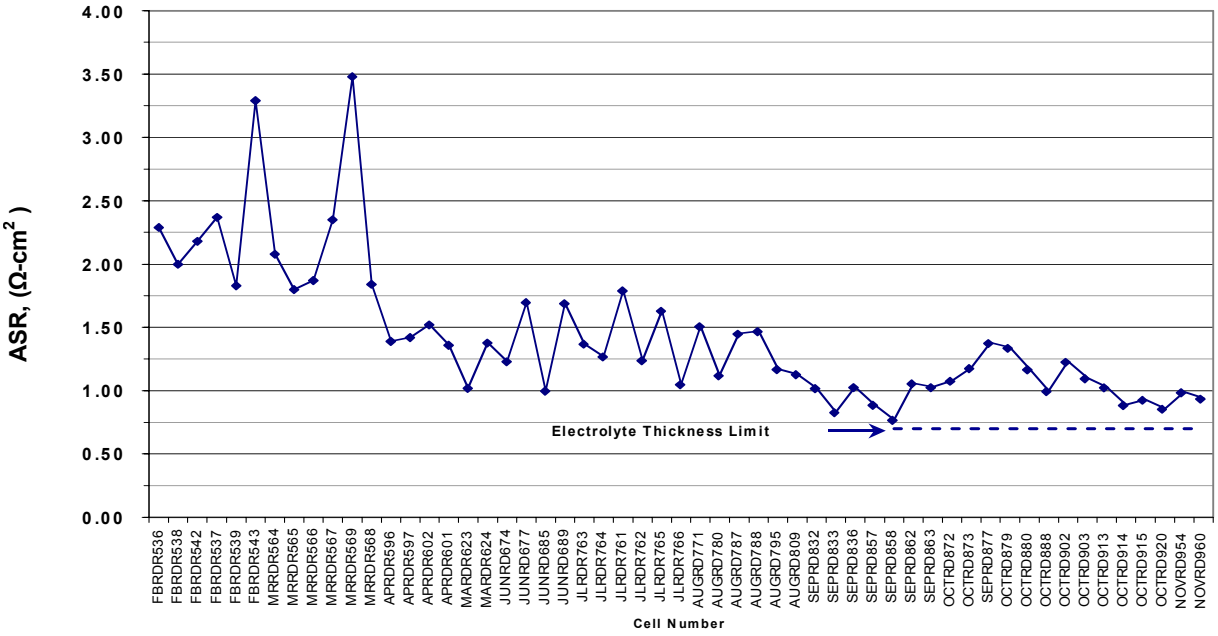


Figure 28. Run chart showing the ASR values obtained for individual rider button cells over the period of February through November 2001.

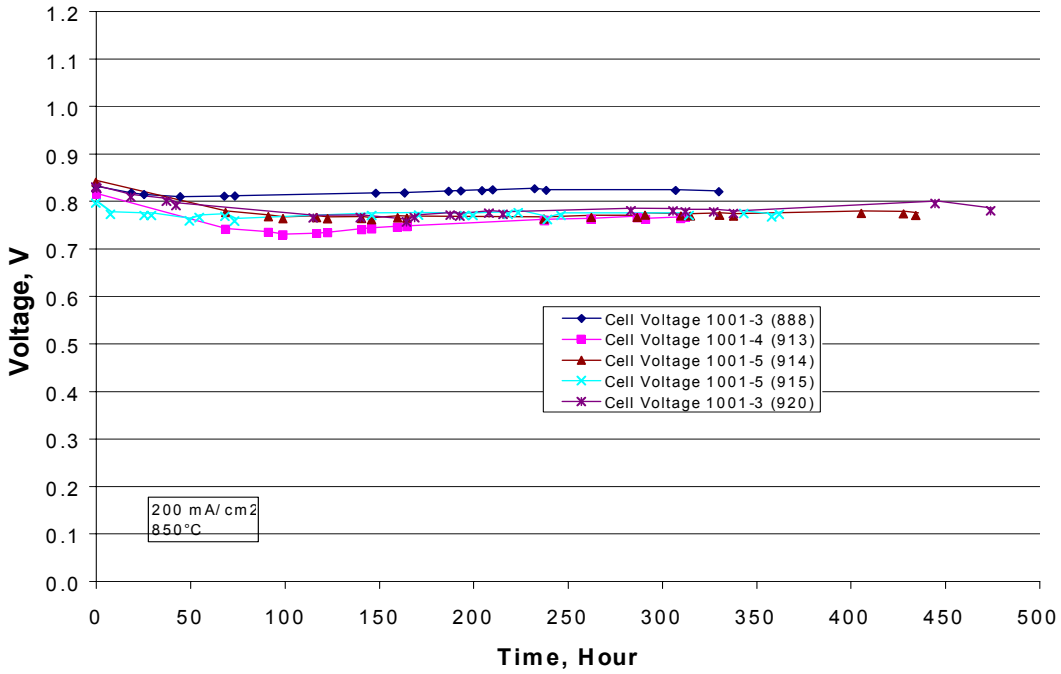


Figure 29. Performance of rider button cells produced in October 2001. The plot shows cell voltage as a function of time at a constant current density of 200 mA/cm^2.

Subtask 9.2 Multi-layer Interconnect Refinement

The objective of this subtask was to refine the materials and fabrication processes to improve the quality of the multi-layer ceramic interconnects and to establish the capability to fabricate up to 100 interconnects per month. As illustrated in ***Figure 1***, the interconnect consists of multiple dense ceramic layers which provide for the essential functions of gas separation, reactant gas flow and electrical conduction. Air and gas separation is accomplished using one or more dense layers. Current flow through the interconnect is accomplished by imbedding conducting materials, such as vias, within each layer. The use of conductive vias is well established in the microelectronics industry. Reactant gas flow is facilitated by punching holes or other structures in the gas flow layers within the interconnect. Interconnects are fabricated using standard multi-layer ceramic production operations: tape casting, punching, screen-printing, lamination, excising and co-firing.

Considerable effort was required to refine the fabrication processes and achieve the desired quality for the interconnects. Substantial challenges had to be overcome by the MTI Team in the areas of: tape formulation, continuous casting of interconnect tape, screen printing the conductors, lamination of the individual layers, and co-firing.

As a result of the fine ceramic powders used for the interconnect body, substantially greater amounts of binder had to be used to achieve acceptable tape properties as compared to standard multi-layer ceramic tape formulations. Defining the appropriate formulation required

engineering studies involving batch-casting tapes having a wide range of compositions, characterizing the mechanical properties of these tapes, and then performing lamination trials at a range of temperatures and pressures. Substantial effort was required to define a range of suitable tape formulations.

Most of the early tape casting trials were performed using a batch caster. During the early part of Phase II, tape casting was transitioned over to a 25-meter long continuous tape caster, shown in ***Figure 30***. Because of the fine ceramic powders used for the interconnect body; the tape casting slip (powder, binder and solvent mixture) required excess solvent to achieve an appropriate casting viscosity. The high levels of solvent and binder in the slip made casting and drying of the tape very difficult. This problem was exacerbated by the need for relatively thick tape layers (0.5 mm thickness) to fabricate the interconnects. Engineering studies, including numerical modeling of the tape drying process, were required to establish a continuous casting process that yielded acceptable interconnect tape.

Toward the end of Phase I, the MTI Team defined a conductor composition and screen-printing process for printing the conductive vias within the tape layers. During Phase II, modest engineering studies were required to optimize the ink formulation and printing parameters to achieve optimal filling of the holes within the interconnect tape. No significant problems were encountered, as the via pattern (shown in ***Figure 31***) was well within the standard processing window established for multi-layer ceramic packages. ***Figure 32*** shows an example of the vias formed within the interconnect layers; the vias are dense and no defects are observed.

Figure 30. Twenty-five meter long continuous tape caster at M/A-COM (Buffalo, NY) used to fabricate the interconnect tape.

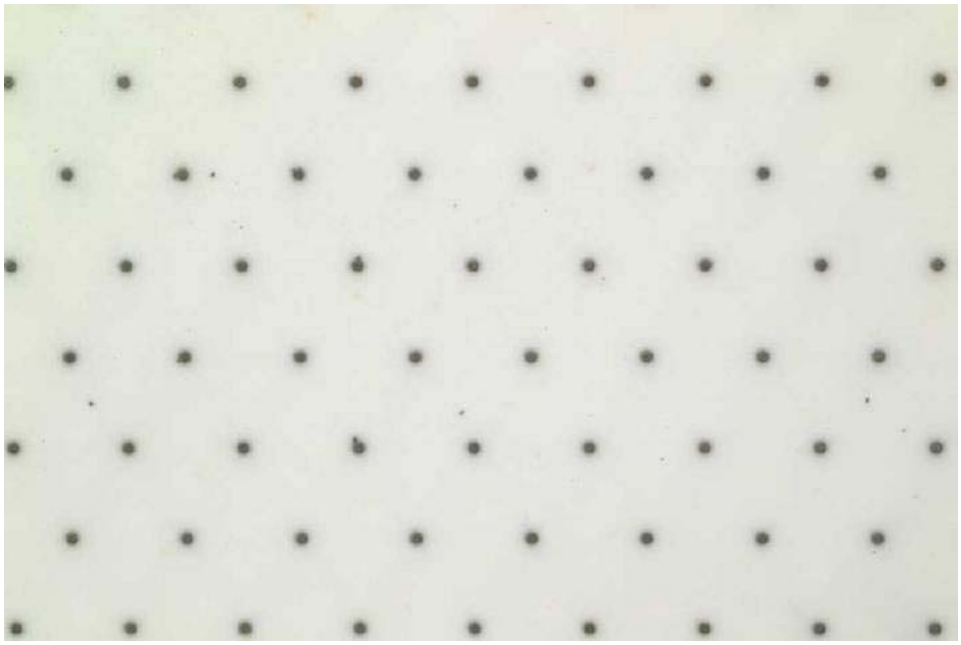


Figure 31. Arrangement of conductive vias in the separator layer of an interconnect. The size and number of vias were selected to minimize the total resistance of the interconnect.

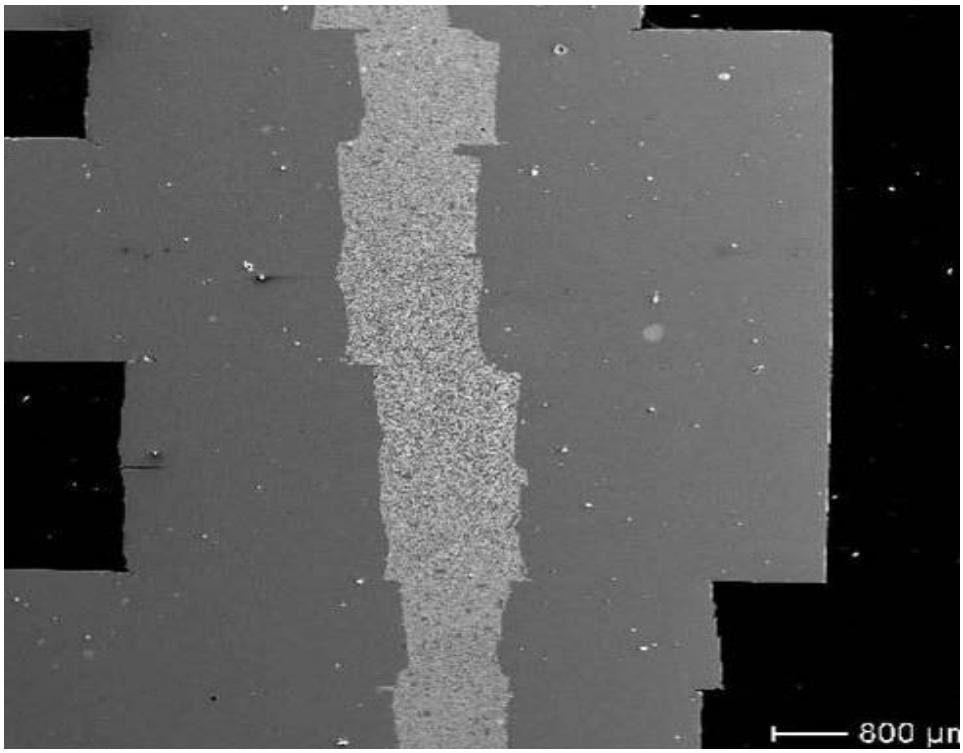


Figure 32. Cross-section of an interconnect showing dense vias within the individual layers comprising the interconnect.

Again, because of the fine ceramic powders used for the interconnect body, lamination of the interconnect tape was very difficult. The interconnect tape had a narrow range of temperature and pressure conditions that gave an acceptable lamination. Too much pressure or too high a temperature resulted in excessive deformation of flow channels and cracks. Insufficient pressure or too low a temperature resulted in poor bonding between the layers (delamination). The lamination quality was also very dependent on the tape properties, and in particular the thickness uniformity of the tape. Achieving uniform, complete lamination was difficult for interconnect tape having poor thickness control. Considerable engineering effort was required to define the appropriate lamination conditions for each interconnect tape. However, the specific process parameters were unique to a particular tape formulation. Whenever changes were made to the tape formulation, adjustments had to be made to the lamination parameters.

Co-firing large components created another set of challenges for the MTI Team. First, very uniform temperatures are required within the working zone of the co-firing furnace. Non-uniform temperature causes distortion and cracking of the interconnects due to non-uniform shrinkage. In addition, the fired parts have a wide range of final X-Y dimensions. The MTI Team was successful in achieving uniform temperatures in the periodic furnace used for interconnect firing through careful selection of kiln furniture and proper arrangement of the load. The loading arrangement used for firing interconnects is shown in ***Figure 33***. Second, removal of the binder during co-firing was found to be difficult, again because of the fine ceramic powders used for the interconnect. Improper binder burnout generally caused distortion and cracking of the interconnects. An example of a crack in a separator layer caused by too rapid binder burnout is shown in ***Figure 34***. Engineering efforts involving numerical modeling and

Figure 33. Arrangement of kiln furniture and setters in the periodic furnace used for interconnect co-firing.

firing experiments were required to define the proper firing profile (temperature ramp rate and air-flow conditions) to achieve optimal binder removal during interconnect co-firing. Relatively flat interconnects with minimal defects are presently produced when the optimized firing profile is used.

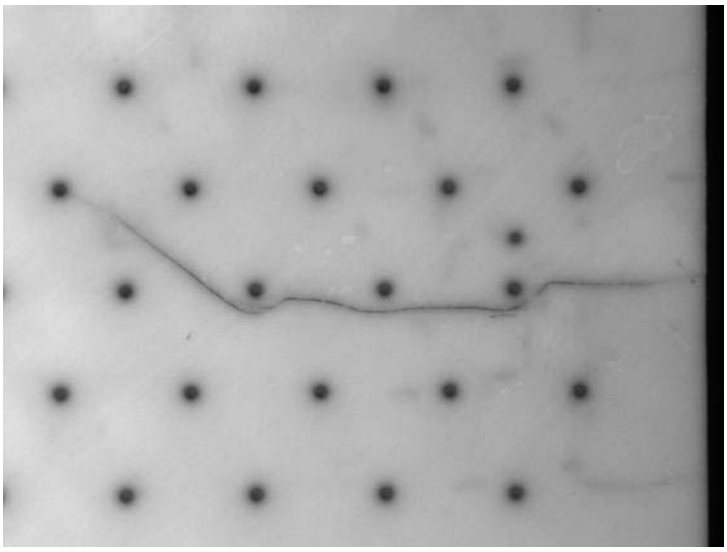


Figure 34. Crack in a co-fired separator caused by improper binder burnout. The heating rate was too high during the binder removal stage of the co-firing cycle.

In summary, during Phase II the MTI Team was successful in its efforts to improve the quality of the multi-layer interconnects and increase the fabrication yields. Interconnect fabrication was scaled-up to a rate of about 100 parts per month; a total of about 1800 interconnects were produced during the Phase II period. Process controls were implemented in the production line in order to insure repeatable fabrication of interconnects meeting specifications. Production yields often exceeded the target value of 70% once the processing parameters were locked in for a given tape. As shown in ***Figure 35***, yield dropped to 30-50% during months in which the process was being changed due to the introduction of a new tape into the line.

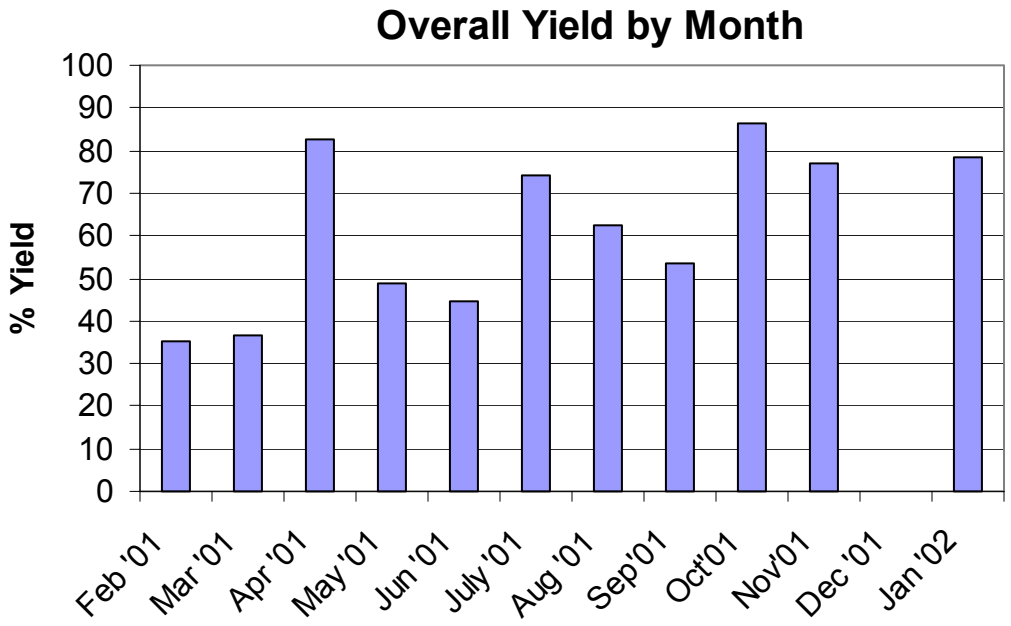


Figure 35. Monthly production yields for the multi-layer interconnect. Yields dropped during months in which process changes were being made for a new tape composition.

Subtask 9.3 Development of Co-fired Short Stacks

The objectives of this subtask were:

- Demonstrate the feasibility for laminating green cell and interconnect layers together and co-firing them into a single co-fired repeat unit (CRU);
- Assess the feasibility for laminating multiple repeat units together and co-firing them to form short stacks (3-5 cell and interconnect repeat units);
- Define a plan for future CRU and short stack development.

The basic concept for a co-fired repeat unit is illustrated in ***Figure 36***, and was previously shown in ***Figure 1***. Fabrication of a CRU is accomplished by first preparing the individual interconnect layers (printed conductors and punched features for gas flow pathways) and printing a green cell (electrolyte with electrodes). The cell and the interconnect layers are stacked, as illustrated in the figure, and then laminated to form a solid green part. CRU fabrication is completed through

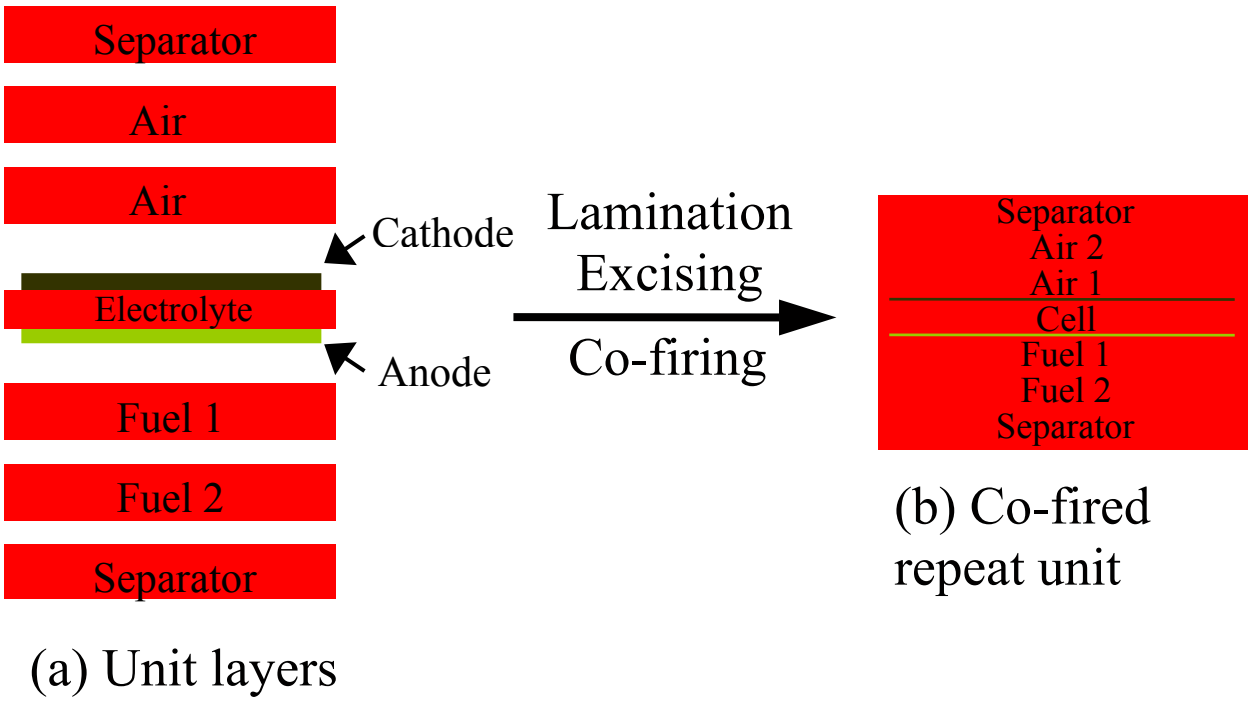


Figure 36. Illustration showing the fabrication of a co-fired repeat unit from a green cell and the individual interconnect layers.

excising and co-firing steps. To fabricate a co-fired short stack, multiple CRU laminates are combined through an additional lamination step prior to co-firing. For each repeat unit, the cell is incorporated within the interconnect structure so that the conductors within the interconnect are in intimate contact with the electrodes. The anode and cathodes are also exposed to the gas flow pathways within the interconnect so that fuel and air supply to the cell can be accomplished.

The co-fired repeat unit approach conceptually provides many benefits over the more traditional approach of building stacks using individually fabricated cells and interconnects. First, one co-firing step is required for each CRU, rather than two or more co-firing runs required to fabricate cells and interconnects. Second, the cells and the conductors within the interconnect are in intimate contact. This should lead to low contact resistance between the cell and interconnect. Third, in a CRU the cell is completely supported by the adjacent interconnect layers. As such, stresses placed on cells during handling and assembly of stacks using the traditional approach is not an issue for CRUs. As a result, the development of CRUs using cells having thin electrolyte layers should be relatively straightforward. Fourth, sealing between the cell and interconnect is accomplished during green processing (lamination).

The MTI Team initiated development of CRUs during the first quarter of 2001 using the 10cm x 10cm design. Early efforts were focused on defining the process sequence for CRU fabrication, with particular emphasis on the process for laminating the green cell with the interconnect layers. Through this work a number of key hurdles were identified; substantial effort was required to overcome these hurdles.

First, lamination of the interconnect layers to the green cell was quite difficult. To achieve acceptable bonding, higher than normal lamination pressures and/or temperatures were required. Under such conditions, severe distortion and cracking of the cells often occurred. Through laboratory experimentation and the use of numerical modeling tools (see Task 8 discussion) a number of potential solutions to this problem were identified. The ultimate solution involved changing the CRU design and improving the lamination tooling (to insure uniform pressure). In addition, a number of modifications to the electrolyte tape and electrode ink compositions were required to achieve acceptable lamination; these changes also improved the shrinkage match between the cell and the interconnect layers during co-firing.

Second, binder removal during CRU co-firing was found to be more difficult than with interconnects. The primary factor causing this difference was that the outer surfaces of CRUs consist of solid separator layers, as opposed to interconnect layers containing gas flow passages. As a result, less air was able to get into the interior of the CRU and it was harder to get the binder decomposition products out. Early co-firing trials for CRUs generally resulted in severely damaged parts. Through experimentation and numerical modeling of the burnout process (see Task 8), a new co-firing profile was defined. A much slower heating rate, particularly during the early stage of the firing cycle, was required.

Toward the end of the second quarter of 2001, the MTI Team successfully demonstrated the fabrication of 10cm x 10cm co-fired repeat units. ***Figure 37*** shows one CRU fabricated during this period. Visual examination showed that some of the CRUs had minor cracks around the perimeter of the parts, along with some small areas of delamination. Several NDE methods (e.g., microfocus X-ray radiography, C-Scan ultrasonics) were used to examine the interior of the

Figure 37. Top view of a "good" 10cm x 10cm co-fired repeat unit (CRU).

CRUs. These examinations showed additional delamination within many of the parts and some deformation and cracking of the cells. The best 10cm x 10cm CRU was electrochemically tested using a stack test stand; special air and fuel manifolds had to be fabricated for testing the single CRU. Not surprising, the electrochemical performance was poor for this CRU; however, electric power was generated. This was the first successful test for a CRU. Post-test destructive examination revealed that poor bonding between the cell and the interconnect conductors and several cracks in the electrolyte were the primary reasons for poor performance.

A decision was made early in the third quarter of 2001 to shift all CRU development efforts to the new 10cm x n design. Modifications to the design were required to facilitate CRU fabrication. The process flow and lamination procedures were readily adapted to the new design. Within several months, the MTI Team successfully demonstrated the fabrication of 10cm x n CRUs. However, a number of defects were observed in these CRUs. Of particular concern was deformation and cracking of the cell that appeared to be caused by non-uniform (and excessive) lamination pressures (see ***Figure 10***). Lamination experiments and finite element modeling (performed under Task 8) provided critical insight into this problem and potential solutions. Through changes to the lamination process and slight design changes, the deformation and cracking problem for the cells was essentially eliminated. By the end of 2001, significantly improved 10cm x n CRUs were fabricated; based on visual inspection and NDE examinations.

Early in 2002 the first successful electrochemical test for a 10cm x n CRU was performed. While substantial improvement in performance was observed, when compared to the first test for a 10cm x 10cm CRU, the ASR was much higher than the target value. Destructive examination of CRUs showed that poor contact between the cell and interconnect conductors was the primary cause for the high resistance. During the remainder of Phase II, work was focused on improving CRU quality and electrochemical performance. In addition, a work plan was defined for future CRU development, including investigation of co-fired short stacks. Because of the challenges encountered during the development of single co-fired repeat units, a decision had been made to defer work on co-fired short stacks until acceptable quality and performance had been demonstrated for CRUs.

Optional Subtask 9A – Design and Fabrication Development for Improved SOFC Stack

During the course of performing the design/modeling effort in Phase I, the MTI Team developed a preliminary design for a modular SOFC stack. This stack design included unique approaches for air and fuel gas manifolds and current collection. Preliminary analyses indicated that significant improvements in electrochemical performance and stack reliability were possible in comparison to the initial 10cm x 10cm design. Equally important, the new design represented a standardized stack configuration that appeared to be amenable to high-volume production.

To develop the 10cm x n stack, the following additional work scope was included in the Phase II effort:

- Cell and interconnect design for 10cm x n stack configuration;
- Design and procurement of new tooling;
- Process development for 10cm x n interconnects;
- Process development for 10cm x n cells;
- Development of stack assembly method, including attachment of air and fuel gas supply and exhaust piping; and
- Performance modeling for 10cm x n stacks.

Preliminary design for the 10cm x n cells and interconnects was completed in the first quarter of 2001. Fabrication trials for interconnects were then initiated in order to provide critical feedback on the design. The rapid prototyping capability at M/A-COM, including a programmable system for punching vias and patterns for gas flow passages, was used for the fabrication trials. During the first quarter, several iterations of fabrication trials and design modifications were performed. Subsequently, the design for 10cm x n cells and interconnects was locked-in. Final fabrication drawings were prepared and the procurement of screens and other tooling was initiated.

Initial lamination trials performed during the second quarter of 2001 indicated that the existing thermal-compression lamination process was not acceptable for the 10cm x n interconnects. Too much pressure led to substantial distortion of the flow passages and cracks, while insufficient pressure led to excessive delamination. There were no pressure/temperature conditions that consistently yielded the desired results. As a result, a new "solvent-assisted" lamination process was developed. After working with the process for several months, the MTI Team began producing acceptable green laminates.

With the lamination problem solved, the team shifted its efforts to the co-firing process. Early co-firing runs for 10cm x n interconnects resulted in substantial cracking, particularly at the edges, and deformation of the parts. Based on experience with the 10cm x 10cm interconnects and co-fired repeat units, it was determined that binder removal was an issue. Modification of the binder burnout portion of the co-firing cycle was successful in eliminating most of the cracks, but the parts were still not flat enough after co-firing for stack assembly. A flat-firing process had to be developed to creep flatten the interconnects and achieve the desired flatness.

During the third quarter of 2001, fabrication of 10cm x n interconnects was ramped up to about 40 parts processed per month. The processing parameters were locked in and process control data were collected for each operation in the prototype line. As shown in ***Figure 38***, good yields were achieved in the fourth quarter as a result of implementing a number of design and process changes. As with the 10cm x 10cm interconnects, yields dropped significantly whenever a new tape formulation was introduced into the line (e.g., September 2001).

In parallel with development of 10cm x n interconnects, the team also had to develop new cells. While new screens were required for printing the anodes and cathodes, no changes were required for the printing operations. Also, other than implementation of the new excising tool for the 10cm x n design, no other process changes were required. Naturally, any materials or process

changes originating from the R&D work aimed at improving cell performance were implemented, as required. Electrode microstructures and electrochemical performance of cells appeared to be the same as that obtained for the 10cm x 10cm cells.

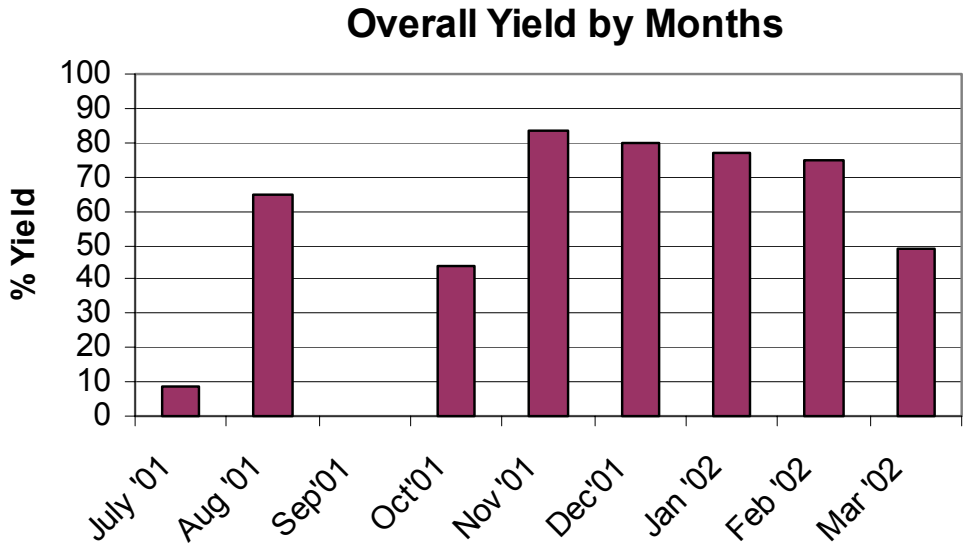


Figure 38. Fabrication yields for 10cm x n interconnects.

Stack assembly and testing was initiated in late 2001. The assembly methods and materials developed for the 10cm x 10cm cells and interconnects were adapted to the new design. The first 5-cell stack was constructed and checked for leaks. After minor repairs of key seals, the stack was heated to operating temperature (850°C). Electrochemical performance was measured for a range of air and fuel flow rates. In general, the performance of this stack did not meet expectations. Post-test examination revealed that leakage had occurred in the cell-to-interconnect and manifold seals. A second 5-cell stack was constructed using an improved sealing material for both the cell-to-interconnect and manifold seals. The new seals resulted in much better stack performance. However, temperature measurements indicated that some leakage might have occurred at the manifold seal. A third stack was constructed using fired electrolytes, rather than actual cells, to test an improved manifold sealing material. The new sealant worked very well, with no leakage observed. The new sealing material will be used in future assembly and testing of 10cm x n stacks.

In parallel with the stack assembly and testing effort, modeling was performed for the 10cm x n stack design. The 2-D thermal/electrochemical model was modified to include all of the key geometric features of the new design. Preliminary calculations confirmed that the 10cm x n design should have superior performance in comparison to the original 10cm x 10cm design. More important, the temperature distributions within the stack for a given set of operating parameters were much more uniform than for the 10cm x 10cm design. As a result, the stress levels during stack operation were predicted to be substantially lower with the 10cm x n design. An example of a typical temperature distribution within a 10cm x n stack is shown in ***Figure 39***; this should be compared to the temperature distribution for a 10cm x 10cm stack shown in ***Figure 6c***.

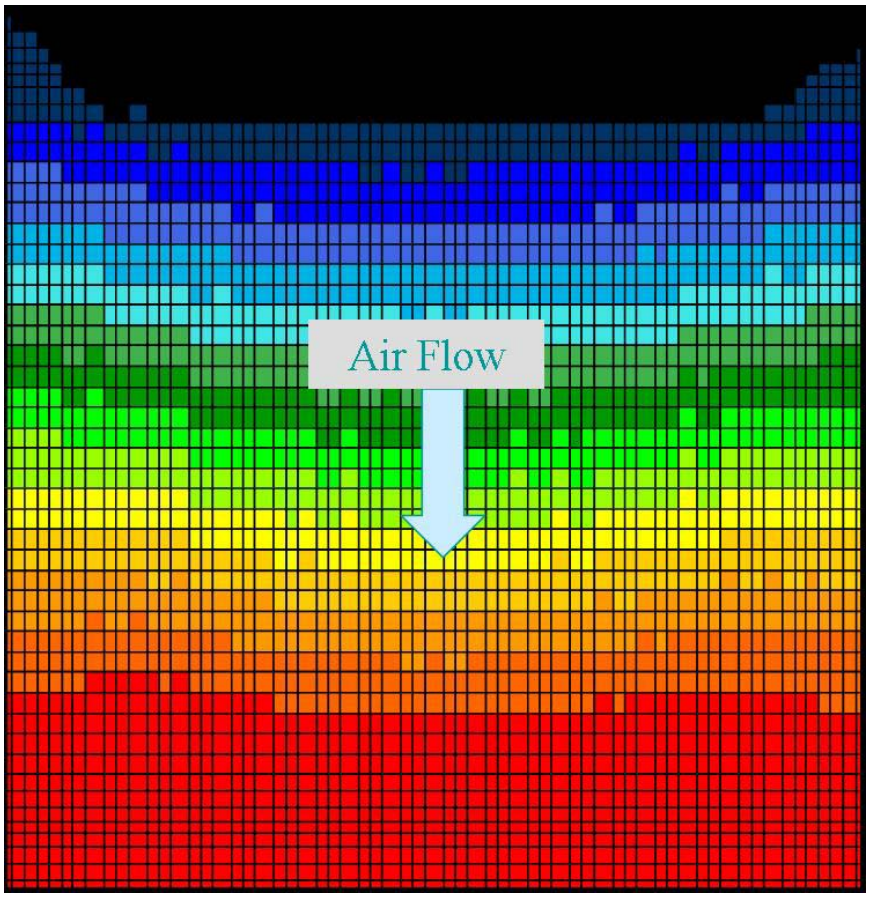


Figure 39. Typical temperature distribution for the 10cm x n stack design.

In summary, the MTI Team was successful in demonstrating the new 10cm x n stack design. Co-fired cells and multi-layer interconnects based on the new design were developed and transitioned into low-rate production. Initial stack tests yielded promising results. Toward the end of Phase II, the MTI Team made the decision to cease all activities directed at the old stack design and focus all future efforts on the 10cm x n stack.

Optional Subtask 9B – Alternate SOFC Materials

In the course of performing the Phase I effort, an initial materials set was selected for development for the co-fired cells and multi-layer interconnects. The selection criteria were driven toward achievement of key Phase I milestones related to demonstrating the feasibility of fabricating co-fired cells and interconnects. Raw material cost was not considered. As a result, the MTI Team chose to use a noble metal cermet conductor material and expensive ceramic powders for the interconnect. Furthermore, the Team elected to work with a YSZ electrolyte material for the co-fired cell development effort, rather than take an inordinate risk by working with a new electrolyte material (e.g., Sc-doped zirconia). Having made this decision, it was recognized that the cell performance (ASR) achieved in Phase I would be limited.

For Phase II, the MTI Team proposed to initiate development of an alternate set of raw materials for co-fired cells and interconnects. The plan called for investigation of the key materials comprising the cells and interconnects, with particular focus on the electrolyte material, the conductor material within the interconnect and the ceramic material used for the interconnect body. The basic research approach involved identifying candidate materials, followed by characterization and screening tests. The screening data were to be used to down-select the most promising candidate materials, which would then be subjected to more extensive evaluation. It was expected that successful materials would be used for fabrication and preliminary testing of prototype components.

Alternate Electrolyte Material and Cell Designs

As a starting point for this work, calculations were performed for the current YSZ electrolyte material to determine the approximate theoretical performance limit. Using the measured oxygen ion conductivity for the electrolyte material and an average thickness of 180 microns, the minimum ASR for a co-fired cell was projected to be about 0.7 Ω-cm^2 at 850°C (0.5-0.55 Ω-cm^2 for the electrolyte and 0.15-0.2 Ω-cm^2 for both electrodes).

Further analyses were performed to assess the potential performance of co-fired cells based on: a) alternate electrolyte materials; and b) alternate designs. A number of alternate electrolyte materials were considered in the initial assessment, including other zirconia compositions, gallates and cerium oxide based compositions. Because of the constraint imposed by co-firing, the decision was made to focus on alternate zirconia compositions. Through literature searches and discussions with powder suppliers, a number of Sc-doped zirconia compositions were identified as potential candidates. Many of these compositions have oxygen ion conductivities that are three times that of the current electrolyte material. Calculations for a cell using a Sc-doped zirconia electrolyte indicated that an ASR value approaching the 0.25 Ω-cm^2 target was possible for a cell having an electrolyte thickness of 75 microns or less.

A preliminary evaluation of alternate designs was also performed. Calculations showed that electrode-supported cells (with anode or cathode support) or alternate proprietary co-fired cell configurations having a YSZ electrolyte thickness of < 25 microns should have an ASR of about 0.25 Ω-cm^2 (at 850°C). As a result of the materials and processing problems encountered by the MTI Team in scaling cells to the 10cm size and achieving the desired performance (ASR $\leq$ 0.8 Ω-cm^2), very little work was performed during Phase II on alternate electrolyte materials or thin-electrolyte designs. Rather, this work will now be pursued in the SECA program.

Low-Cost Ceramic Interconnect Body

The objective of this effort was to define a lower cost ceramic powder to replace the material used for the multi-layer interconnect. Because of the many complexities associated with developing materials that are compatible with each other during co-firing, it was decided that the interconnect body composition would not be changed. Rather, the focus was directed developing a low-cost substitute to replace the current powder.

The team identified approximately ten initial candidate firms who might be able to supply the required powders. Powder samples were obtained from each supplier and characterized. Physical properties (particle size, particle morphology, surface area), chemical purity and sintering behavior were evaluated. While none of the powders met the preliminary specification, a number of suppliers demonstrated the ability and willingness to perform the necessary development work to meet the interconnect requirements. One key parameter evaluated was sintering behavior. In order to minimize changes to the interconnect fabrication processes, it was determined that the new powders should have a co-firing shrinkage behavior that closely matches that for the current powder. By working closely with the suppliers, MTI was successful in achieving the desired shrinkage match with a number of candidate powders. The dilatometry curves, shown in ***Figure 40***, illustrate the shrinkage match achieved with one candidate powder. Toward the end of Phase II, the MTI Team down-selected to the most promising candidate suppliers who appeared to be in the best position to meeting the quality and production volume requirements at an acceptable cost. Further development and subsequent implementation of a new powder into interconnect production is planned for the SECA program (started January 2002).

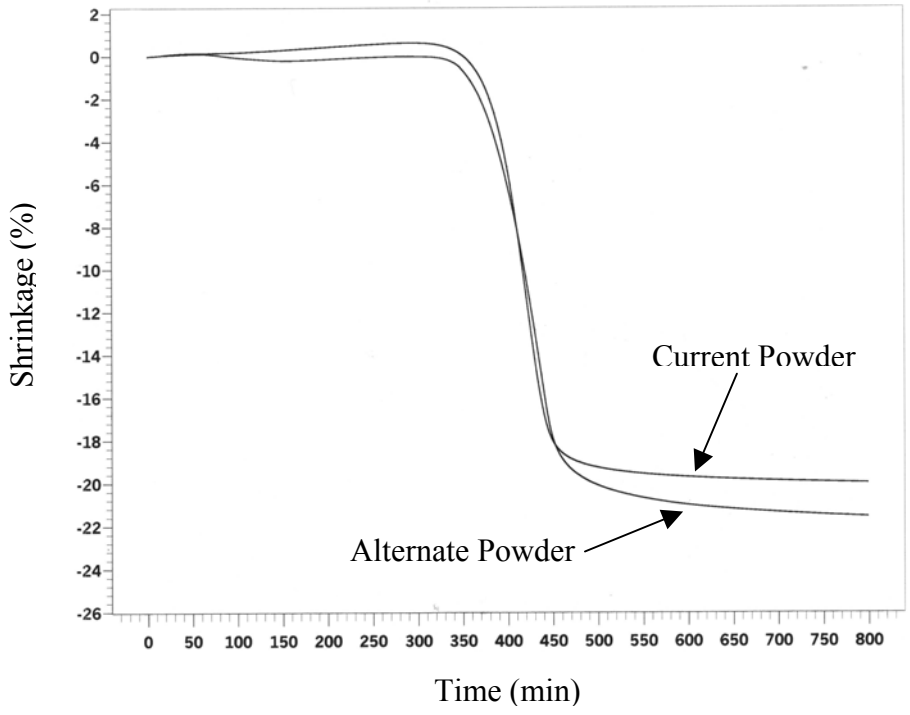


Figure 40. Dilatometry curves (shrinkage as a function of time and temperature) for the current interconnect powder and a candidate replacement. The shrinkage behavior for these two materials is well matched.

Alternate Conductor Materials for the Interconnect

Development of alternate conductor materials for the interconnect represented a significant challenge for the MTI Team. Suitable alternate conductors had to simultaneously satisfy a number of requirements: 1) CTE that is reasonably well matched to the interconnect body; 2) acceptable electronic conductivity; 3) minimal reactions with interconnect body during co-firing; 4) good match in sintering behavior (shrinkage) with the interconnect body; and 5) compatible with the operating atmosphere (e.g., oxidizing atmosphere on the air side of the interconnect and reducing atmosphere on the fuel side).

An extensive literature search was performed, followed by initial laboratory experiments. Other than noble metals, no single material was found to be suitable for the conductor. As a result, the decision was made to pursue the development of two different sets of conductor materials, one for the fuel-flow layers and a second for the air-flow layers. To narrow the search for alternate conductors, numerical modeling was performed (described under Task 8). Stack resistance was modeled to define the minimum acceptable conductivity for a replacement conductor. In addition, finite element analyses were performed to assess stress levels as a function of CTE mismatch between the conductor material and the interconnect body. An acceptable range of CTE values for a replacement conductor was defined.

After completing the preliminary assessment, a decision was made to limit the candidate fuel-side conductor materials to NiO-based compositions. After several months of effort, a number of compositions having acceptable electronic conductivity were identified. As an example, conductivity data for two candidate compositions are shown in ***Figure 41***. The conductivity samples were sintered in air, followed by reducing in forming gas prior to measuring the conductivity. Several candidate compositions also had reasonable CTE match with the interconnect body.

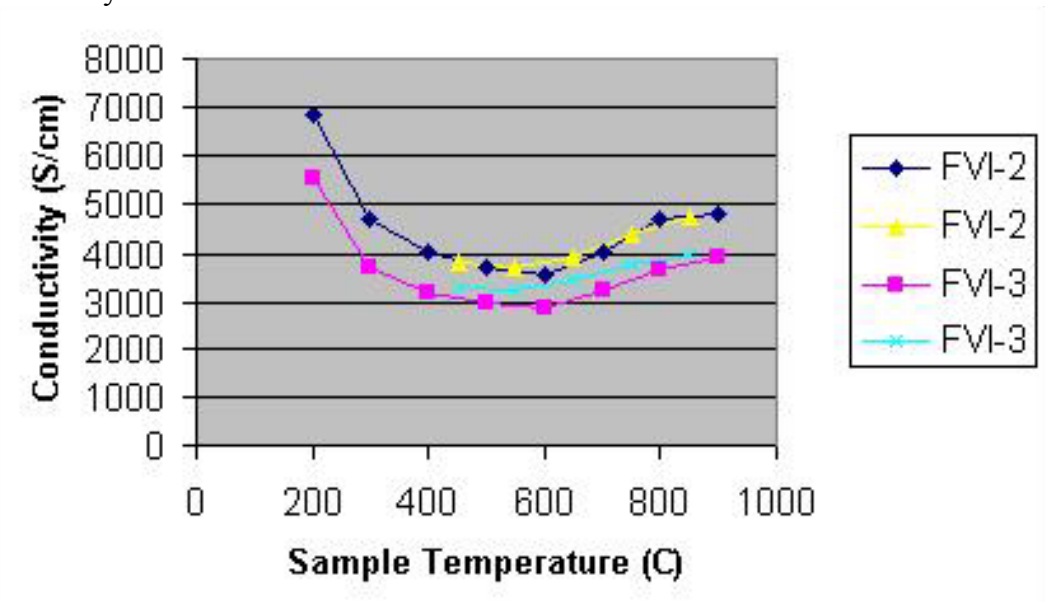


Figure 41. Conductivity as a function of temperature for two candidate conductor materials for the fuel-flow layers within an interconnect

Achieving an acceptable shrinkage match between the conductor material and the interconnect body during co-firing was difficult. However, by varying the conductor composition, starting powder characteristics (particle size and morphology, surface area) and ink formulations the desired shrinkage behavior was obtained. Conductor patterns and vias were screen-printed onto interconnect tape and successfully co-fired. An example of co-fired vias in a laminated interconnect mock-up is shown in ***Figure 42***. Good via filling was accomplished. Acceptable shrinkage matching was achieved, as evidenced by the lack of cracks in either the interconnect body or within the vias. Cracking readily occurred with poor shrinkage matching.

Detailed microstructural examinations showed that there were no deleterious reactions between the candidate fuel-side conductor materials and the interconnect body. However, a reaction between the conductor materials and the setter plate used to support the mock interconnect during co-firing was observed. Evidence of this reaction is seen in ***Figure 42***. The conductor has a high density in the interior of the part, but has excessive porosity near the exterior surfaces. Resistance measurements confirmed that the conductivity of the material near the exterior surface has been adversely affected. Potential solutions to the setter reaction problem were being investigated as Phase II ended; this work will be continued under the SECA program.

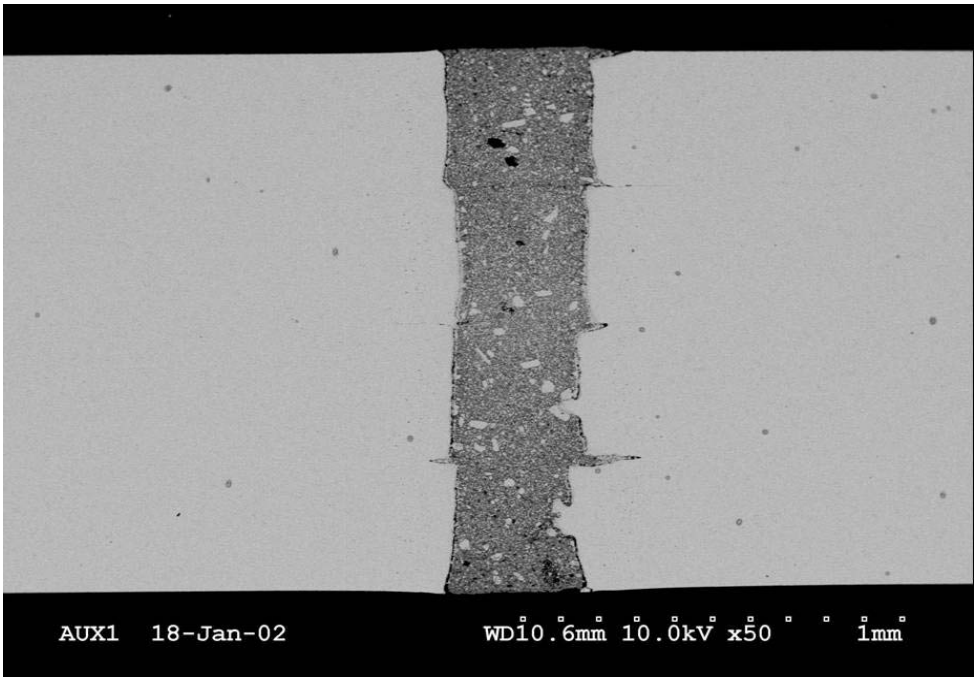


Figure 42. Fuel-side conductor (in the form of vias) within a mock interconnect. Excessive porosity near the exterior surfaces is evidence of an undesired reaction with the setter plates during co-firing.

Substantial effort was required to develop alternate conductor materials for the air-flow layers within the interconnect. The problem faced by the MTI Team was that most of the oxide materials having a high electronic conductivity also have a relatively high CTE value (e.g.,

cobaltites). In addition, many of these materials tend to react with the interconnect body during co-firing. After an extensive literature review and exploratory experimentation in the laboratory, two candidate materials were selected for further development. One material was a perovskite oxide having a moderate electronic conductivity, while the second was a novel oxide material having a much higher conductivity.

During the Phase II period, substantial progress was made in the development of the perovskite conductor. Adjustments to the composition and powder properties resulted in good shrinkage and CTE match with the interconnect body. Conductor patterns and vias were screen-printed onto interconnect tape and successfully co-fired. The conductivity of this material fired under several different conditions is shown in ***Figure 43***. While a higher conductivity is desired, the conductivity achieved with this perovskite composition is acceptable. As seen in ***Figure 44***, good via fill was achieved for mock interconnects. No deleterious reactions with the interconnect body were noted through SEM examinations. However, a problem with reactions between the perovskite conductor and the setter plates was observed. This problem is similar to that which was also observed for the candidate fuel-side via material.

By the end of Phase II, the MTI Team had identified a solution to the setter reaction problem observed for both the fuel-side conductor and the perovskite material. Further development of these two materials will be conducted in the SECA program. In addition, the MTI Team will continue to pursue the development of the second air-side conductor material. While less progress was made with this material, it appears to have a substantially higher conductivity than the perovskite composition.

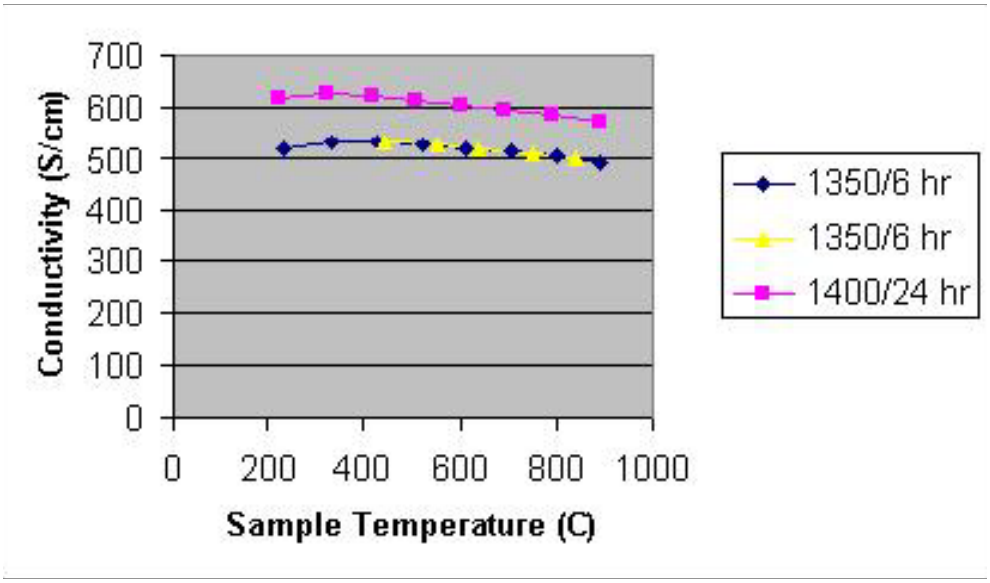


Figure 43. Conductivity as a function of temperature for the candidate perovskite oxide material sintered under different conditions.

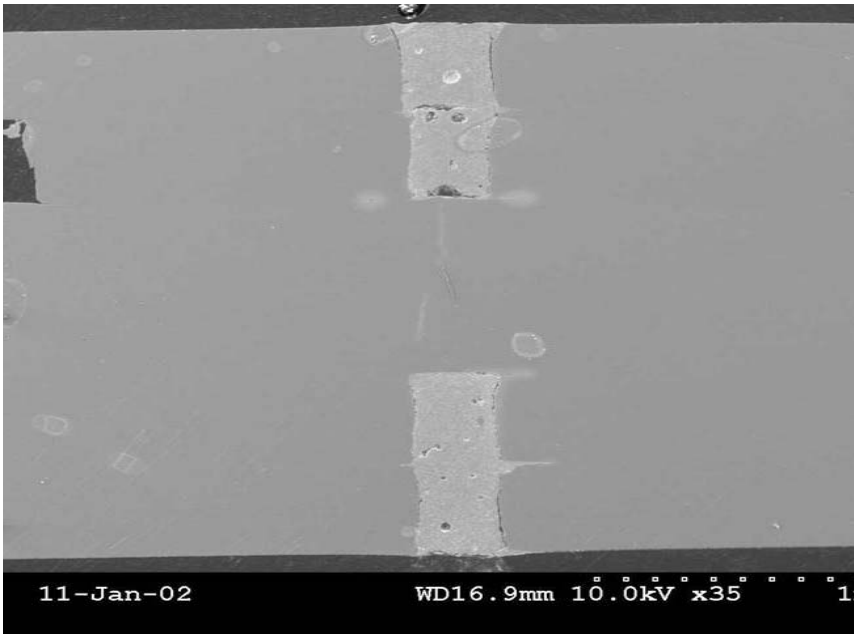


Figure 44. Co-fired perovskite conductor (in the form of vias) within a mock interconnect.

Task 10 – Test Methodology and Plan

The objective of this task was to develop characterization methods to assess the quality and performance of SOFC components and stacks. The intent was to pursue characterization/test methods to support in-process quality control during component fabrication and final component inspection. Further, the task was not meant to be directed at implementation of standard inspection methods employed in MLC manufacturing, but to focus on developing techniques that were suited to the unique requirements of the multi-layer SOFC design.

A key deliverable for Phase II was a test plan for characterization of components (cells/ interconnects) and short stacks as part of a testing effort to be conducted during Phase III. However, a decision was made by the DOE to not continue with Phase III of the AMPS Program. As a result, a test plan was not prepared.

As originally planned, the MTI Team pursued the development of non-destructive, destructive and electrochemical characterization methods. However, greater emphasis was placed on the evaluation of non-destructive examination methods that might be suitable for in-process and final component inspections. The methods investigated were:

Green Tape Inspection:
- Time domain reflectometry
- Air-coupled ultrasonics
- Microfocus X-ray radiography

Green and Fired Cell Inspection:
- Ultrasonic C-scan imaging
- Microfocus X-ray radiography
- Electronic speckle pattern interferometry (ESPI)
- Shadow Moiré imaging

Green and Fired Interconnect Inspection:
- Ultrasonic C-scan imaging
- Microfocus X-ray radiography
- Electronic speckle pattern interferometry (ESPI)
- Shadow Moiré imaging
- IR thermography
- Resonant ultrasonic spectroscopy

Green and Fired CRU Inspection:
- Ultrasonic C-scan imaging
- Microfocus X-ray radiography
- Shadow Moiré imaging
- IR thermography

Green tape inspection methods were investigated in cooperation with the Idaho National Engineering and Environmental Laboratory (INEEL). Evaluation of time domain reflectometry was performed using a sheet of green tape in which holes of different diameters were formed (see ***Figure 45***). As shown in ***Figure 46***, the resolution of time domain reflectometry was determined to be poor. Thus, further work with this method was terminated. Air-coupled

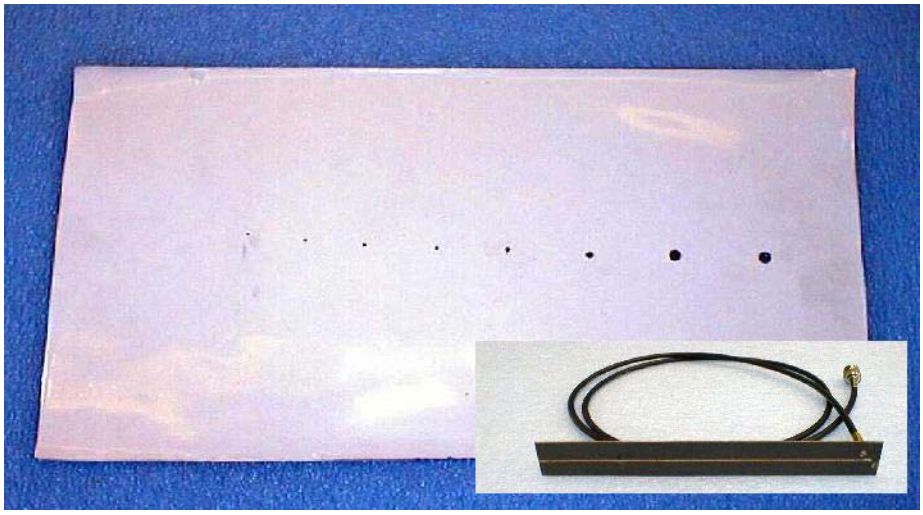


Figure 45. Green electrolyte tape containing punched holes of the following diameters: 1.4 mm, 2.0 mm, 2.6 mm, 3.5 mm, 5.9 mm and 6.0 mm.

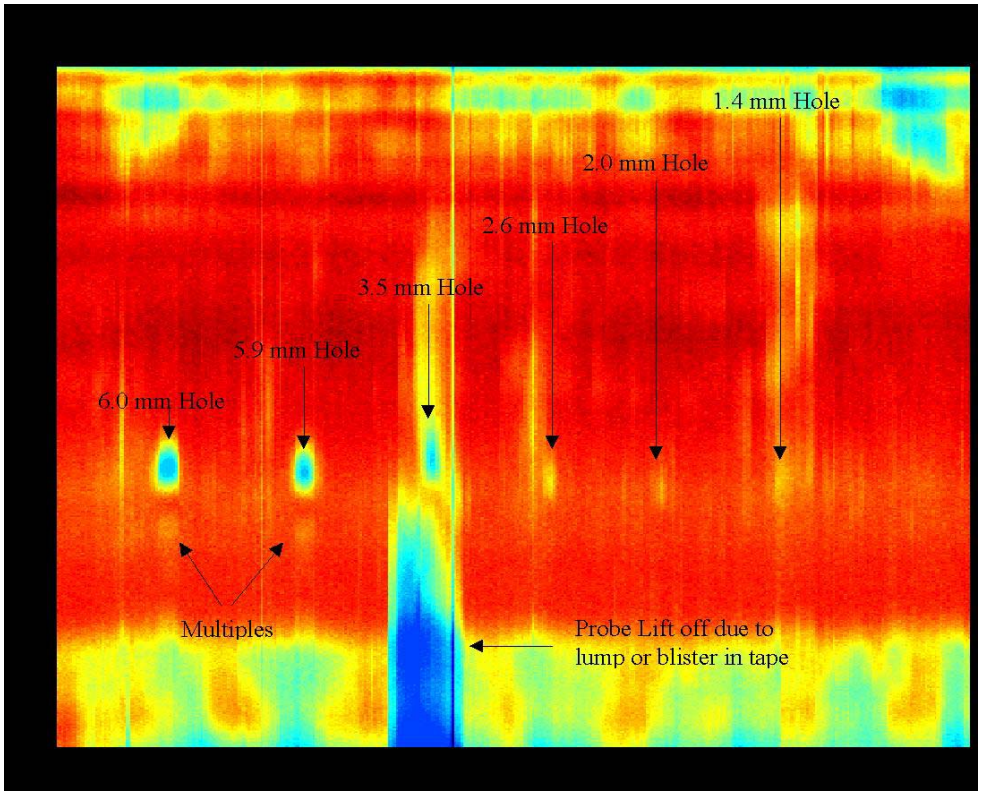


Figure 46. Time domain reflectometry results for green tape containing holes. The resolution was found to be poor.

ultrasonics was also evaluated by INEEL. Poor resolution was also observed for this method, possibly because of some limitations in the equipment at INEEL. As a result, method was not pursued any further. Microfocus X-ray radiography was shown to be sensitive to density and thickness variations within the green tape. The scanning rate, however, was determined to be a potential limitation with this method.

Evaluation of inspection methods for green cells was complicated by the presence of screen-printed electrodes on the surface of the tape. Ultrasonic C-scanning and microfocus X-ray radiography were sensitive to density variations, and to a lesser extent thickness variations. However, the presence of the electrode inks made data interpretation somewhat difficult. Shadow Moiré imaging was found to be an effective tool for inspection of both green and fired cells. This rapid optical inspection method was very sensitive (micron resolution) to surface features. As such, information could be obtained about the overall flatness of a cell, along with detailed data on specific surface features. This method was also effective in measuring the thickness of screen-printed and fired electrodes (as illustrated in ***Figure 47***).

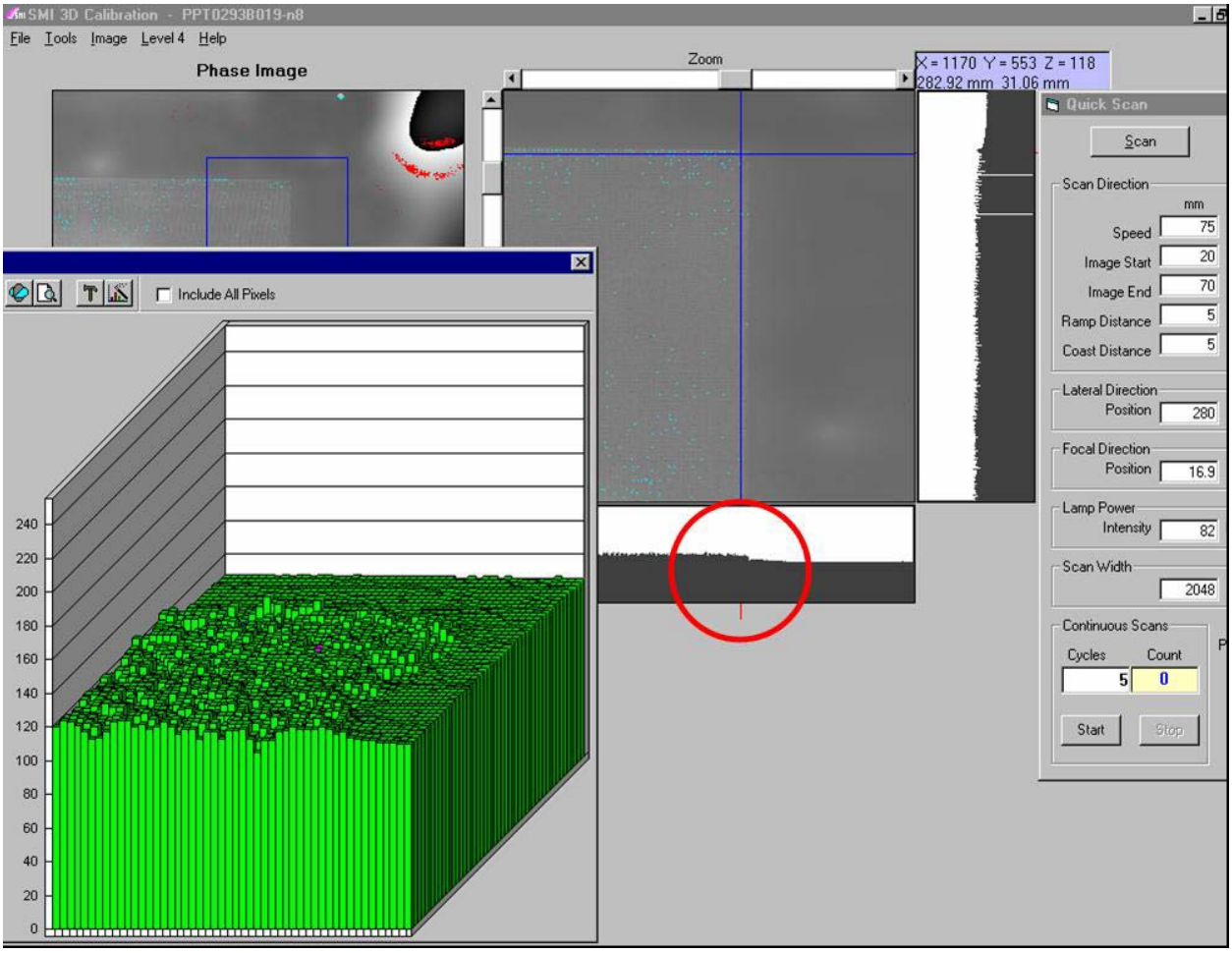
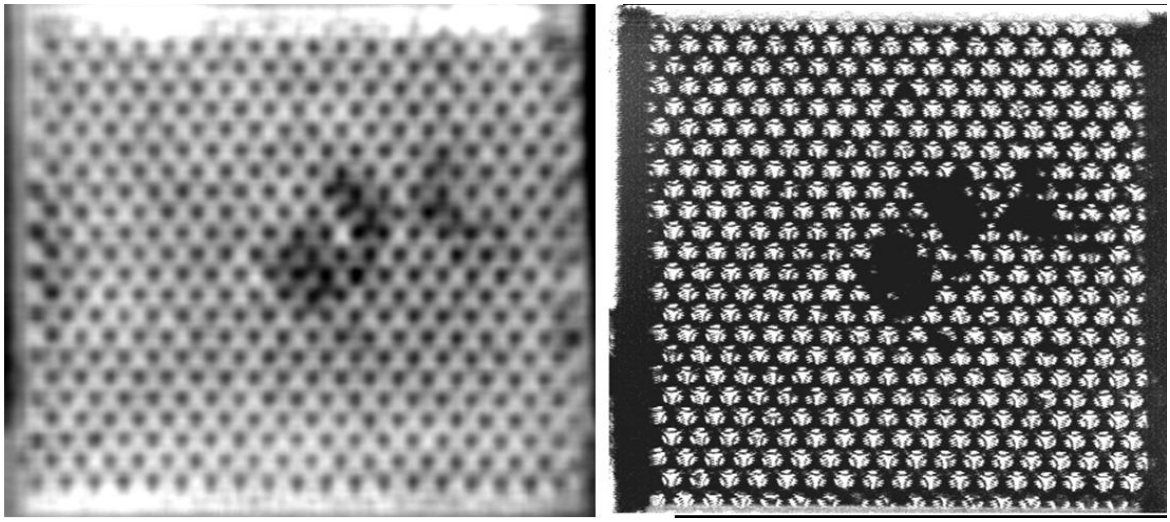


Figure 47. Graphical output from a Shadow Moiré imaging system. Green tape with a screen-printed electrode has been scanned to determine the thickness of the electrode.

Much of the Task 10 effort was directed at evaluating methods for the inspection of green and co-fired multi-layer interconnects. Ultrasonic C-scanning was found to be effective in locating delaminations and large cracks within co-fired interconnects, but was not particularly effective in identifying defects in green components. On the other hand, IR thermal imaging was found to be effective in locating delaminations in both green and fired interconnects. A comparison of the ability of thermal imaging and ultrasonic C-scanning to identify delaminations in a co-fired interconnect is provided in ***Figure 48***. In both cases, the delaminated regions were clearly observed. The ability of thermal imaging to locate delaminations in a green interconnect is illustrated in ***Figure 49***.



IR Thermal Image **Ultrasonic C-Scan (100 MHz)**

Figure 48. Inspections of a mock interconnect to locate possible delaminations using IR thermal imaging (left) and ultrasonic C-scanning (right). Delaminations are seen as dark regions in the images.

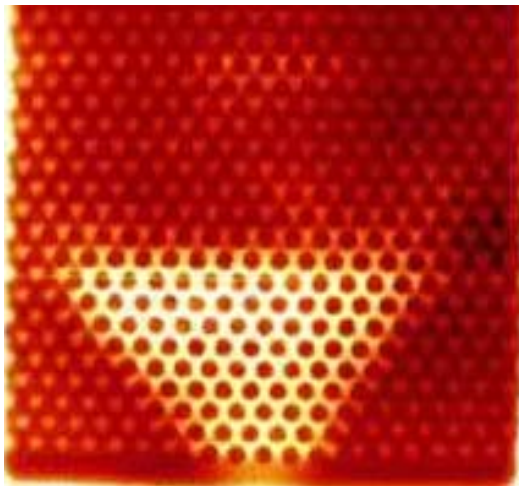


Figure 49. IR thermal image showing large delaminations (bright area in image) in green mock interconnect.

While ultrasonic C-scanning was effective in identifying delaminations inside interconnects, this technique was less effective in locating internal cracks. However, microfocus X-ray radiography was very effective in providing detailed information regarding internal features in co-fired interconnects, including alignment of adjacent layers and size/location of cracks. Although it is not possible to show actual images of inspected interconnects (due to the proprietary nature of the design details), real-time microfocus radiography was determined to be an attractive commercial-ready method for component inspection.

Likewise, Shadow Moiré imaging was also found to an attractive, commercial-ready technology for inspection of interconnects (and cells). Global surface inspections of an interconnect are possible in 3-4 seconds, as are detailed inspections for specific features. As an example, measurements were made of a screen printed via to ascertain the surface profile. The Shadow Moiré image for a via is shown in ***Figure 50***. 2-D and 3-D surface profile information was obtained in less than 4 seconds. These results compare favorably to the profile data obtained using other inspection methods, including scanning electron microscopy.

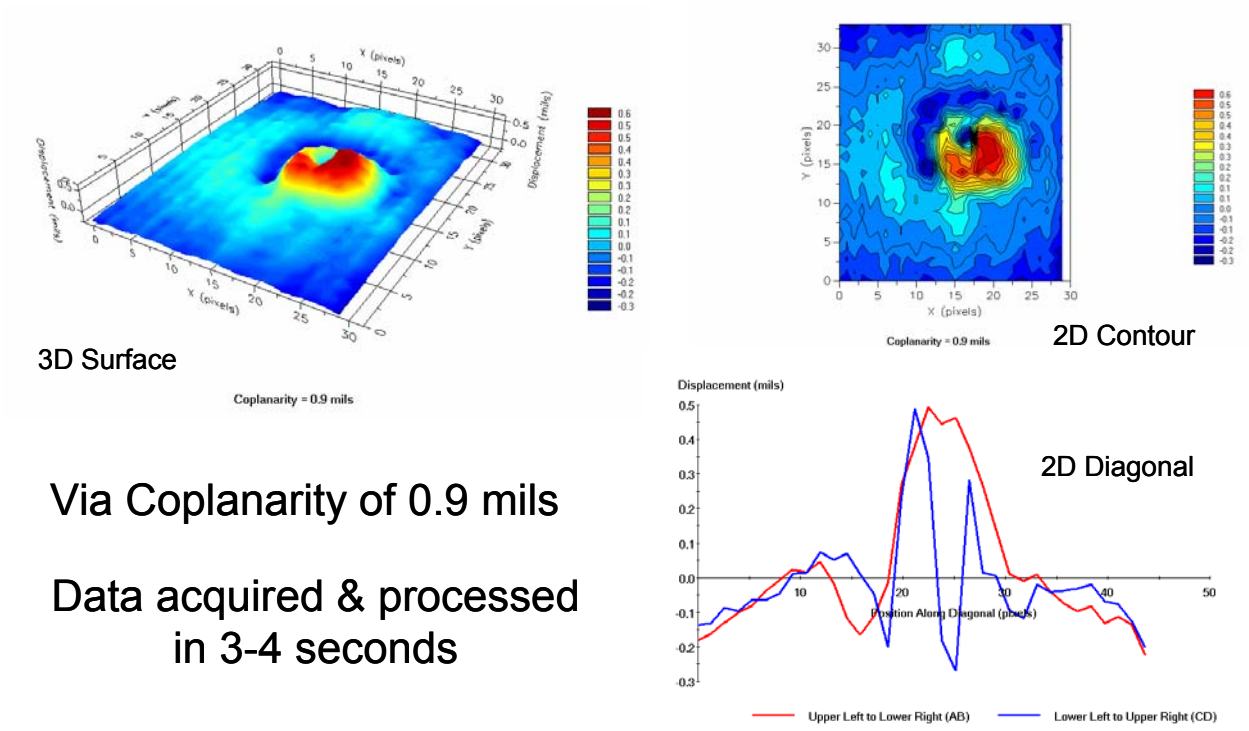


Figure 50. Surface inspection of a green via on an interconnect using Shadow Moiré imaging.

Finally, inspections for co-fired repeat units were successfully performed using many of the same methods that were effective for the multi-layer interconnects. Microfocus radiography and ultrasonic C-scans were particularly effective in locating internal defects, such as delaminations, cracks and misaligned layers.

At the completion of Phase II, the evaluations of all of the non-destructive examination methods were compiled. Recommendations were made regarding the most promising inspection methods for future implementation into the cell and interconnect production development efforts, for both in-process and final component inspection.

Task 11- Short Stack Fabrication and Cost Verification

As originally proposed, this task was comprised of two primary activities:

- Fabrication of a series of 3-10 cell short stacks for subsequent inspection and testing in Phase III; and
- Detailed manufacturing cost analyses to confirm that the low-cost potential of the MLC manufacturing approach can be realized in the production of SOFC stacks.

As a result of the decision by the DOE to end the AMPS Program upon completion of Phase II, fabrication of additional stack for testing was not performed. In reality, as previously described under Task 8, the MTI Team had been fabricating and testing stacks during most of the Phase II period. However, the intent of the Task 11 effort was to fabricate components and stacks that would undergo extensive inspection prior to testing. Such work will be deferred to the SECA program.

During Phase I, an initial production model providing high-level cost estimates for production of multi-layer SOFC stacks was developed. This model included most of the raw material inputs and production factors (labor rates, equipment through-put and capacity, yields, etc.) associated with each manufacturing operation. This model was substantially revised during Phase II. Details for each manufacturing operation and the raw materials were updated. The model was extended to include a range of component sizes (10cm x 10 cm up to 20cm x 20cm). Sensitivity analyses were performed to examine the impact of key production variables. Toward the end of Phase II, the model was used to generate cost estimates for the SECA proposal. The model confirmed that stack costs of less than $200 per kW could be achieved at modest production volumes (~ 200 MW/year plant size).

Task 12 – Program Management and Reporting

All project management activities necessary to organize task activities, ensure adherence to project schedules and control costs were performed on a routine basis. Effective project execution was achieved by maintaining a unified team comprised of three different organizations in four geographic locations (MTI-Alliance, MTI-Lynchburg, Ceramatec-Salt Lake City, and M/A-COM-Buffalo). Open, direct communication between team members and technical assistance/collaboration between team members was accomplished. We also initiated or continued activities involving external resources, such as Sandia National Laboratory, the Idaho National Engineering and Environmental Laboratory, Pacific Northwest National Laboratory, the University of Missouri-Rolla and Virginia Tech.

LIST OF ACRONYMS AND ABBREVIATIONS

AMPS	Affordable Multi-Layer Ceramic Manufacturing for Power Systems
ART	Advanced Refractory Technology, Inc. (now M/A-COM Ceram, Inc.)
ASR	Area specific resistivity (ohm-cm2)
CFD	Computational Fluid Dynamics
cm	Centimeter
CRD	Contract Research Division, a unit of MTI
CRU	Co-fired Repeat Unit
CTE	Coefficient of Thermal Expansion
D	Dimensional
deg. C	degrees Centigrade (Celsius)
DOE	U.S. Department of Energy
FEA	Finite Element Analysis
IR	Infrared
kHz	kilohertz
mA/cm2	milli-amps per centimeter squared
MLC	Multi-Layer Ceramic
Mpa	mega-Pascals
MTI	McDermott Technology, Inc.
MW	Megawatts
NDE	Nondestructive Examination
NEPA	National Environmental Policy Act
NETL	National Energy Technology Laboratory
Ni	Nickel
NiO	Nickel Oxide
PNNL	Pacific Northwest National Laboratory
R&D	Research and Development
Sc	Scandium
SECA	Solid State Energy Conversion Alliance
SEM	Scanning Electron Microscope
SOFC	Solid oxide fuel cells
TC	Thermocouple
TGA	Thermogravimetric Analysis
UMR	University of Missouri - Rolla, MO
V	Voltage
YSZ	Yittria stabilized Zirconia