

High-speed Nuclear Quality Pulse Height Analyzer for Synchrotron-based Applications

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Abstract--A high throughput Pulse Height Analyzer system for synchrotron-based applications requiring high resolution, high processing speed and low dead time has been developed. The system is comprised of a 120ns 12-bit nuclear quality Analog to Digital converter with a self-adaptive fast peak detector-stretcher and a custom-made fast histogramming memory module that records and processes the digitized data. The histogramming module is packaged in a VME or VXI compatible interface. Data is transferred through a fast optical link from the memory interface to a computer. A dedicated data acquisition program matches the hardware characteristics of the histogramming memory module. The data acquisition system allows for two data collection modes: "standard" data acquisition mode where the data is accumulated and read in synchronization with an external trigger and "live" data acquisition mode where the system operates as a standard Pulse Height Analyzer. The acquisition, standard or live, can be performed on several channels simultaneously. A two-channel prototype has been demonstrated at the Stanford Synchrotron Radiation Laboratory accelerator in conjunction with an X-ray Fluorescence Absorption Spectroscopy experiment. A detailed description of the entire system is given and experimental data is shown.

I. SUMMARY

A fast high resolution and low dead time Pulse Height Analyzer (PHA) system for Synchrotron-based applications has been developed. This module is an addition to and completes the previously designed custom electronics for XAFS applications [1, 2]. The PHA system receives analog information from a low dead time pulse processing front-end section. The low dead time PHA system is comprised of a fast high resolution Analog to Digital Converter (ADC), a fast histogramming memory and a VME or VXI compatible interface. The VME-based system consists of one complete data acquisition channel. The VXI-based PHA system addresses the problem of simultaneous data acquisition from multiple channels. Both systems were tested at the Stanford Synchrotron Radiation Laboratory in conjunction with an X-ray Fluorescence Absorption Spectroscopy experiment. The block diagram of a single acquisition channel is shown in Fig. 1.

The analog input section is built around a fast self-adaptive peak detector-stretcher described in [1]. The peak detector-stretcher includes all the necessary logic to provide pileup rejection and gating functions. The stretched signal is fed to a commercial ADC chosen to maximize throughput without compromising the differential non-linearity (DNL). This ADC is an 8MSPS unit, providing 14 bit of resolution with no missing code over the full temperature range, and with an intrinsic DNL of $\frac{1}{2}$ LSB. In order to improve the DNL (not adequate for nuclear spectroscopy applications), only the first 12 most significant bits are used. A 6-bit sliding scale correction [3] lowers the DNL to less than 1%. Including delays, the conversion time of the ADC is 120ns. The electronic pulse-processing amplifier, in its fastest version, shapes the energy events coming from the detector with a 250ns peaking time fourth-order, pseudo-gaussian shaping function. The conversion time of the ADC does not add to the dead time associated with the pulse-shaping amplifier.

Data collection is either gated by an external synchronization signal such as an accelerator beam clock or a precise clock signal to time-stamp the data collection and measure count rates. After an analog to digital conversion has taken place, the ADC board control logic sends a request to the histogramming memory module. When the histogramming memory controller acknowledges the request, it uses the ADC data to increment by one the content of the corresponding address memory location. The entire operation lasts 130ns, which is less than the dead time of the pulse-processing amplifier. Therefore, the histogramming operation does not increase the overall event-by-event processing time of the entire system. The histogramming memory module is packaged in a VME or VXI compatible interface and is built around a dual-port static random access memory. One port is dedicated to data accumulation while the second port is mapped to the VME or VXI address and data buses. The transfer to the computer is controlled by either the synchronization signal in the form of an interrupt signal sent to the VME or VXI controller, or by the computer accessing the memory at regular time intervals. The former corresponds to the "standard" acquisition mode and the latter to the "live" mode. In standard mode the content of the histogramming memory must be erased (zeroed) before collecting any new data set.

This work was supported by the Director, Office of Energy Research, Office of Basic Energy Sciences, Chemical Science Division of the U.S. Department of Energy under Contract No. DE-AC03-76SF00098.

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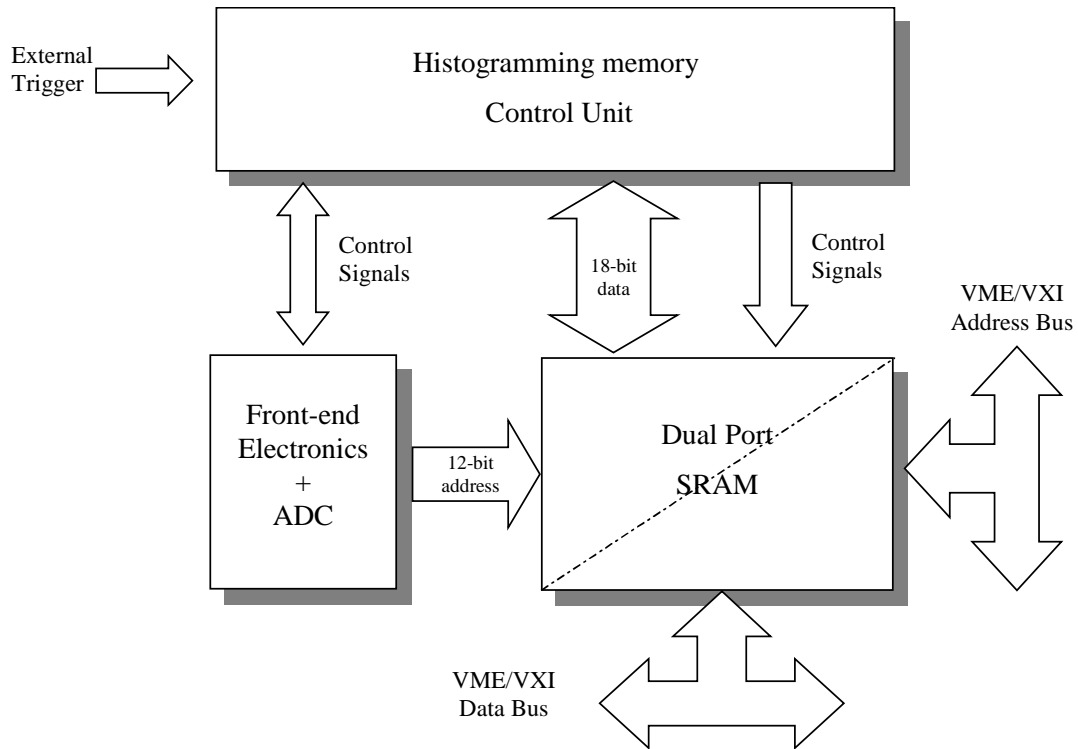


Figure 1: Histogramming Memory Module Block Diagram

In the VME based system this operation is performed simultaneously with the data transfer: while a memory location is addressed its content is read out and then erased during the same cycle. In the VXI based system the erasing of the memory takes place separately from the readout and simultaneously on all channels.

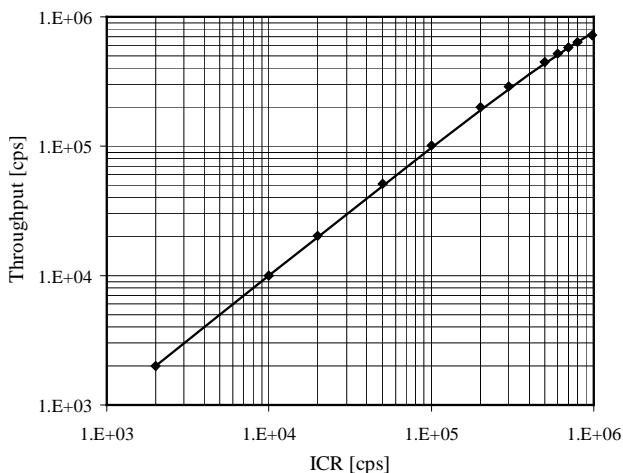


Figure 2: Total throughput rate versus Incoming Count Rate (ICR).

The memory access and data transfers are performed at the maximum speed allowed by the controller interface. The data acquisition program offers the possibility of selecting the data collection mode and was written to match the hardware requirements of the histogramming memory module. Figure 2 shows the total throughput rate for the whole system (solid dots) as a function of incoming count rate (ICR). The shaping function was, as mentioned above, a fourth-order, pseudo-gaussian with 250ns peaking time. The figure also shows the best fit of the experimental points assuming a paralyzable dead-time model (continuous line) [4]. The dead-time from the interpolation results equal to 275ns, in good agreement with the expected analytical result.

I. REFERENCES

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