SAND2000-0508C

Comparison of Electrical CD Measurements and Cross-Section Lattice-Plane Counts of Sub-Micrometer Features Replicated in Silicon-on-Insulator Material[¶]

Michael W. Cresswell[§,a], John E. Bonevich[a], Thomas J. Headley[c], Richard A. Allen[a], Lucille A. Giannuzzi[b], Sarah C. Everist[c], Rathindra. N Ghoshtagore[a], and Patrick J. Shea[c]

[a] National Institute of Standards and Technology, Gaithersburg, MD 20899

[b] University of Central Florida, Orlando, FL 32816

[c] Sandia National Laboratories, Albuquerque, NM 87185

RECEIVED
MAR 20 2000
OSTI

Keywords: Silicon-on-insulator, cross-bridge resistor, electrical CD, CD-SEM measurements, calibration, HRTEM, traceability, standards, linewidth, silicon micro-machining, focused ion beam

ABSTRACT

Electrical test structures of the type known as cross-bridge resistors have been patterned in (100) epitaxial silicon material that was grown on Bonded and Etched-Back Silicon-on-Insulator (BESOI) substrates. The CDs (Critical Dimensions) of a selection of their reference segments have been measured electrically, by SEM (Scanning-Electron Microscopy) cross-section imaging, and by lattice-plane counting. The lattice-plane counting is performed on phase-contrast images made by High-Resolution Transmission-Electron Microscopy (HRTEM). The reference-segment features were aligned with <110> directions in the BESOI surface material. They were defined by a silicon micro-machining process which results in their sidewalls being atomically-planar and smooth and inclined at 54.737° to the surface (100) plane of the substrate. This (100) implementation may usefully complement the attributes of the previously-reported vertical-sidewall one for selected reference-material applications. The SEM, HRTEM, and electrical CD (ECD) linewidth measurements that are made on BESOI features of various drawn dimensions on the same substrate is being investigated to determine the feasibility of a CD traceability path that combines the low cost, robustness, and repeatability of the ECD technique and the absolute measurement of the HRTEM lattice-plane counting technique. Other novel aspects of the (100) SOI implementation that are reported here are the ECD test-structure architecture and the making of HRTEM lattice-plane counts from both cross-sectional, as well as top-down, imaging of the reference features. This paper describes the design details and the fabrication of the cross-bridge resistor test structure. The long-term goal is to develop a technique for the determination of the absolute dimensions of the trapezoidal cross-sections of the cross-bridge resistors' reference segments, as a prelude to making them available for dimensional reference applications.

1. INTRODUCTION

1.1 Relationship to Earlier Work

Earlier papers have described electrical linewidth test structures replicated in (110) SOI material, referred to here as the "(110) implementation."[1,2,3] In the (110) implementation, intersecting features are oriented non-orthogonally in lattice ⟨112⟩ directions.[4] **Figure 1** illustrates the relevant lattice vectors. An example of features delineated by KOH etching, otherwise known as silicon micro-machining, a {110} bulk silicon surface having silicon-nitride *in-situ* masking, and with features aligned in a [112] direction having sub-micrometer linewidths, is shown in **Figure 2**. The vertical, sidewalls are coincident with lattice {111} planes and generate high levels of contrast for the pitch calibration of electron-beam CD systems.[5] Note that the silicon-nitride caps on the features, having served for *in-situ* masking, had not been removed when this image was recorded. The aspect ratio of their overhang is a measure of the lattice-plane selectivity of the KOH etching and/or misalignment of the axes of the lithographically-projected reference features with respect to a lattice <112> direction in the substrate surface plane.

¶ Contribution of the National Institute of Standards and Technology; not subject to copyright.

§ Correspondence: Email: michael.cresswell@nist.gov; WWW:http://www.nist.gov/cgi-bin/wwwph/cso.nist.gov?Query=cresswell; Telephone: 301 975 2072; Fax: 301 975 5668

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, make any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.

In the (100) implementation, the subject of this paper, intersecting features of cross-bridge resistors are orthogonal and are oriented to lattice ⟨110⟩ directions. Their sidewalls have slopes inclined at exactly 54.737° to the surface (100) plane of the substrate. In both implementations, feature delineation by silicon micro-machining provides atomically-smooth feature sidewalls coincident with lattice {111} planes.

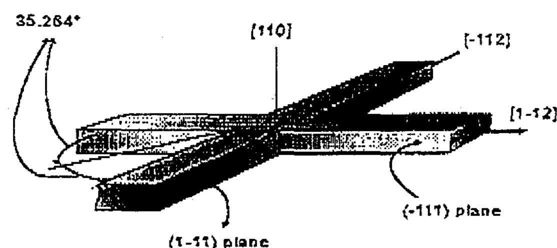

Figure 1. Lattice vectors pertinent to the (110) SOI implementation.

1.2 Purpose of the Current Work

The purpose of the current work is to supplement the potential usefulness of reference features of the (110) implementation with that of ones having known sidewall slopes less than 90°. Such reference features may be of comparable, or greater, value in metrology applications, such as instrument calibration, either when used alone, or when used in conjunction with the those generated in the (110) implementation. For example, the non-orthogonal intersection of the sidewall and respective top-surface planes of the reference-segment features may address suspected difficulties encountered with atomic-force microscope (AFM) applications where it has been reported that probe-tip control at the sharp 90-degree corner of the sidewalls with the upper surface is sometimes challenged. The new (100) implementation also opens the possibility of developing traceable reference materials for step-height applications. However, the specific near term purpose is to assess the repeatability and robustness of the new (100) implementation and its suitability for applying the proposed CD reference-material traceability strategy described below.

1.3 End Use and CD-Traceability Strategy

As in the case of the (110) implementation, the intention here is to develop traceability of (100) reference materials through HRTEM imaging of the silicon lattice constituting the reference features. The HRTEM technique has successfully been used for gate-CD and oxide-thickness measurements in special applications.[6] However, its cost and destructiveness appears to render it impracticable for lattice-plane imaging on every feature that is to be distributed to end users for CD reference purposes. The current strategy is, therefore, after fabrication of wafers on which the cross-bridge resistor test-structures are replicated, and after whole-wafer ECD test, to perform imaging of a selection of reference segments at a selection of die sites. Lattice plane counts provided by a the selection of HRTEM images are then used to express the ECD measurements of all reference segments on that wafer in terms of absolute dimensions. In this way, the ECD measurements serve as a secondary reference means. That is, the ECD measurements are effectively calibrated by the HRTEM measurements, the primary reference means. Traceability is thereby imparted to all reference features whose ECDs have been measured. The strategic emphasis on electrical linewidth metrology as a secondary reference means results from its unique robustness and repeatability, sometimes referred to as its precision. The key characteristic that is being sought is a useful level of correlation between electrical linewidth results and absolute measurements. Without calibration by HRTEM, or some other means, electrical CD measurements have not yet been shown to be able to provide traceability with acceptably low levels of uncertainty.

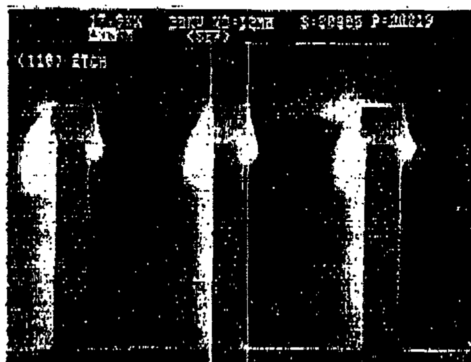

Figure 2. SEM image of line-features characteristic of the (110) implementation.

2. TECHNICAL APPROACH

2.1 Feature-Lattice Orientation for the (100) Implementation

In the (100) implementation, cross-bridge resistor test-structure features, such as those serving as reference segments, test-pads, and voltage taps, are orthogonal and oriented to lattice ⟨110⟩ directions. **Figure 3** and **Figure 4** respectively

show an image of the cross-section of a line feature and a map of pertinent lattice vectors of the (100) implementation.

2.2 BESOI Starting-Material

The merits of SIMOX and BESOI silicon-on-insulator options for the subject application have been compared previously.[7] Each of these materials has previously been shown to provide physically uniform features with planar vertical sidewalls in the (110) implementation. While the SIMOX material is relatively inexpensive and easy to acquire, the BESOI material provides physical advantages including a user's ability to specify an arbitrary thicknesses of the surface film in which the cross-bridge resistors are patterned, and a more sharply defined interface to the buried oxide. Additionally, the Kelvin-measurement $\langle V/I \rangle$ databases from which sheet resistance and reference-segment ECDs are extracted generally have much less statistical variability. ECDs extracted from cross-bridge resistors replicated on BESOI material are generally more consistent with the drawn CDs than those extracted from SIMOX wafers. Because of the resulting metrology advantages, BESOI material is preferred for this CD reference-material application.

2.3 Sheet-Resistance Metrology Issues

Sheet resistance, R_S, is typically the largest contributor to uncertainty in the measured electrical CD value, w_E, of the reference segment of the cross-bridge resistor. The ECD value, w_E, is derived basically from sheet resistance, R_S, and Kelvin $\langle V/I \rangle$ measurements, according to the relationship

$$w_E = \frac{(L - \delta L)}{\langle V/I \rangle} \cdot R_S \qquad (1)$$

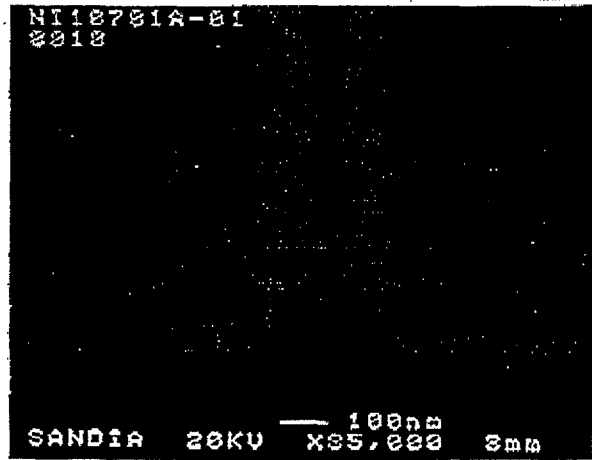

Figure 3. SEM image of orthogonal intersecting line-features characteristic of the (100) implementation.

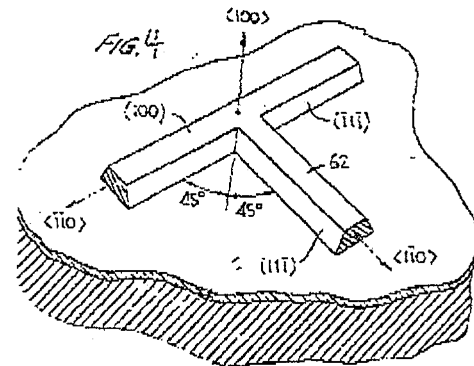

Figure 4. The pertinent lattice vectors of the (100) SOI implementation.

where δL is the reference-length, L, shortening factor that has been introduced and described previously.[8,9,10] Statistical analyses of $\langle V/I \rangle$ measurement databases that are acquired from multiple multi-segment cross-bridge resistor test structures, and based on Eq. (1), are found to have certain benefits over the latter's local application as described elsewhere.[2]

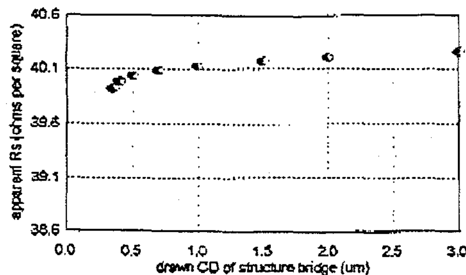

Figure 5. R_S results for a set of Greek-Cross four-terminal sheet resistors that were tested at a particular die site by using the second of two approaches described in the text.

One approach to obtaining an appropriate value of R_S is to determine a correction factor, obtained by means of current-flow modeling, to apply to the apparent sheet resistance determined from the set of $\langle V/I \rangle$ measurements normally extracted from planar four-terminal sheet resistors.[11] A second approach is to use four-terminal Greek-Cross configurations, for example, with large dimensions to minimize the impact of the non-planarity that is characteristic of the (100) implementation. In this context, *non-planarity* means that is the attribute of structures patterned in a film of uniform composition and thickness with vertical sidewalls on the entire perimeter. We employed the second approach and obtained the results shown in **Figure 5** for a set of structures tested at a single die site. The applicable structure is

identified on the right in **Figure 6**. In **Figure 5**, the diminution of sheet resistance for cross-bridge resistors having the smaller CDs is due to real spatial variations of R_S with the location of the respective sheet resistors. All the sheet resistors had the same dimensions that were independent of the drawn CDs of the reference segments of the associated cross-bridge resistor, and therefore were expected to generate sheet-resistance values that had no correlation with the drawn CDs of their respective reference segments.

2.4 Cross-Bridge Resistor Test-Structure Design

Figure 6 shows a multi-reference-segment cross-bridge-resistor test structure which is patterned with 7 different drawn linewidths ranging from 0.35 µm to 3.0 µm on each die site. It has provisions for the determination of δL drawn CDs by two different approaches. This quantity may, on the one hand, be extracted from measurements of the widths of the voltage tap and the reference-segment linewidth in conjunction with its expression in terms of these linewidths derived from current-flow modeling, as in the case of the (110) implementation.[12] On the other hand, δL in Eq. **(1)** may be extracted from analysis of a set of (V/I) measurements made on multiple reference-length segments of each cross-bridge resistor at a particular die site, as described in previous work.[4] The two four-terminal sheet resistors in are intended to allow a useful comparison of R_S values extracted from the respective four-terminal sheet-resistor implementations.

2.5 Cross-bridge Resistor Fabrication Process

The BESOI wafers which generated features such as those shown in **Figure 3** were fabricated according to an established SOI micro-machining process flow that has been reported previously. An etch of 19% by weight of KOH in water at 80°C is commonly used to define structures in bulk silicon material having {111}-planar faces.[7] The pattern to be transferred is typically replicated first in a 500-Å silicon-nitride hard mask. An alternative etch is tetramethyl ammonium hydroxide. An appropriate hard mask in this case is silicon dioxide.[13] In either case, the buried oxide serves as an effective vertical etch stop while {111} planes of exposed silicon etch significantly slower than any others. Material surfaces remaining at the completion of an etch are either those that are protected by the in-situ hard masking, the buried oxide, or by silicon surfaces having one of the orientations of the {111} family.

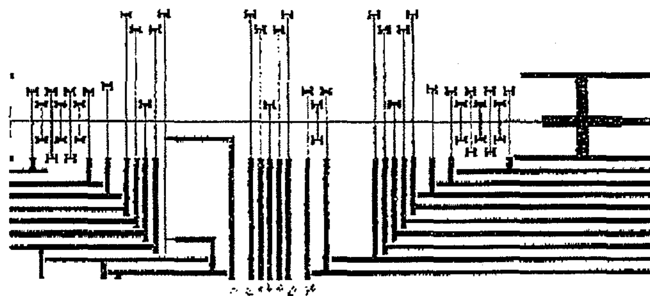

Figure 6. Test structure of (100) implementation which is patterned with 7 different drawn linewidths ranging from 0.35 µm to 3.0 µm on each die site.

Table 1. Selection of cross-bridge resistor reference-segment CDs. (Die site 8,1)

Drawn CD (µm)	top (µm)	bottom (µm)	mean (µm)
0.35	0.254	1.743	0.998
0.40	0.285	1.775	1.130
0.40	0.304	1.793	1.049
0.50	0.393	1.882	1.356
0.70	0.611	2.101	1.600
1.00	0.856	2.345	1.600
1.50	1.359	2.848	2.103
3.00	2.894	4.384	3.639

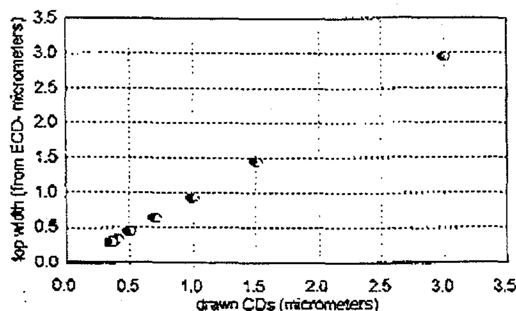

Figure 7. An example of the top-surface widths, computed from their known height and measured electrical CDs, as a function of drawn linewidths for a selection of structures

3. MEASUREMENT RESULTS

3.1 Cross-Section SEM Measurements

A selection of reference-segment features having drawn linewidths ranging from 0.35 µm to 3.0 µm at die site

(11,2) on a 150-mm (110) BESOI wafer were measured using cross-section images of the type shown in **Figure 3**. In order to not to have to rely on the use of the magnification marker, the magnification of each image was determined from the constancy of the local film thickness and the known feature sidewall slopes. That is, the relationship of the difference between the measured feature top CD, and the corresponding CD of the feature bottom, and its height was known. The height, was determined as that which generated the most linearity between the measured top and drawn CDs. The actual value so obtained was 1.13 μm, which matched another value obtained separately by an independent means. The results shown in **Figure 7** include the width at half height which is the dimension registered by corresponding electrical CD measurements.

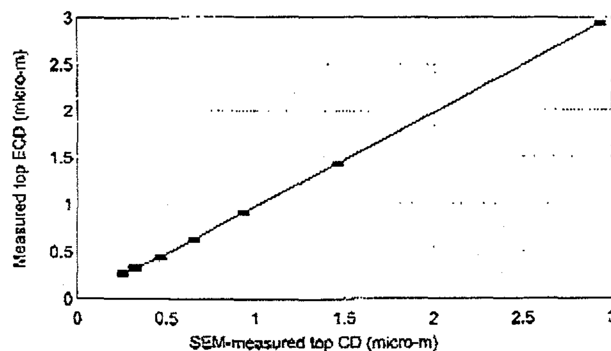

Figure 8. The electrically-determined feature-top CD is plotted against the SEM-determined feature-top CD.

3.2 Electrical CD Measurements

An example of the electrical versus drawn linewidths, obtained from a die-site on a 150-mm (100) BESOI wafer in close proximity to that from which the measurements shown in **Figure 7** were obtained, is shown in **Figure 7**. The electrical CDs ideally correspond to the half-height physical widths of the reference feature. In **Figure 7**, the electrical CDs have been converted to feature-top widths to facilitate a comparison of the measurements from the respective die sites with the drawn CDs. In **Figure 8** the electrically-determined feature-top CDs for the die site are plotted against the SEM-determined feature-top CDs from the adjacent die site. The degree of correspondence is within the low tens of nanometers. However, no definitive comments on the degree of matching are appropriate since the linewidths featured in the figure were actually extracted from different corresponding features on adjacent die sites having the same drawn linewidths.

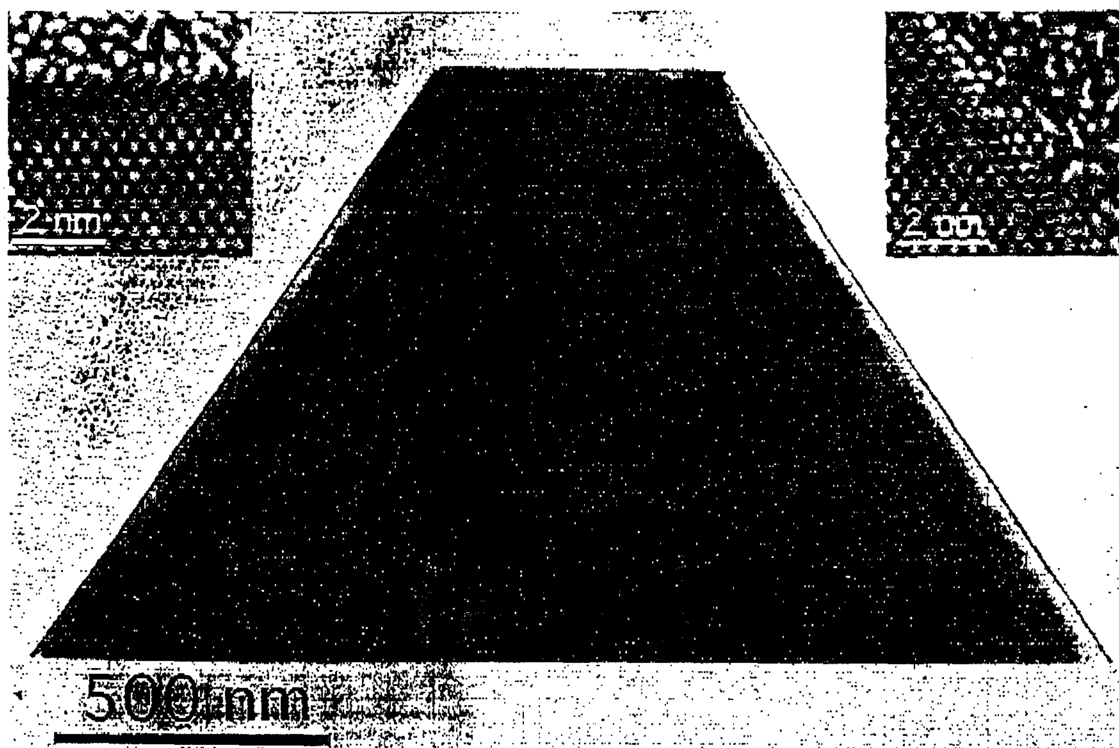

Figure 9. Large-scale TEM image of the trapezoidal cross-section of a feature with a drawn CD of 0.7 micrometer. The insets show atomic scale resolution of the top (001) surface in the upper left and the (bar1 1 bar1) sidewall surface in the upper right.

3.3 HRTEM Imaging of Features with Trapezoidal Cross Sections

To resolve the atomic lattice-plane fringes in the silicon feature using HRTEM,[14] a cross-section of the feature must be thinned to approximately 20 nm. The procedure to produce HRTEM specimens was as follows: first the silicon features were encapsulated with an epoxy and a glass cover slip to act as a transparent, protective layer. The wafer was then diced with a diamond wafering blade and subsequently mechanically polished with diamond slurries to 0.05 micrometer finish. The second side of the cross-section was likewise polished, but at a 6 degree angle to produce a wedge shaped specimen suitable for mounting on a 3 mm copper slotted washer. The specimen was then thinned to 20 nm in an ion mill using 4 kV Ar ions at 4 degrees. Atomic scale observations were conducted in a 300 kV microscope with a point resolution of 0.17 nm.

Micrographs of the cross-sectioned silicon containing 0.7 micrometer features tilted to the [110] zone were recorded at 150 kX so that the atomic lattice fringes were visible across the entire top (001) surface facet. This micrograph was then scanned at 2000 dpi to obtain a digital image suitable for analysis. **Figure 9** shows a large scale TEM image of the trapezoidal cross-section of a feature with a drawn CD of 0.7 micrometer. The insets show atomic scale resolution of the top (100) surface in the upper left and the (bar1 1 bar1)sidewall surface in the upper right. The (1 bar1 0) lattice fringes across the top facet were then counted to determine the absolute width of the silicon feature. The silicon (1 bar1 0) lattice spacing corresponds to 0.3840 nm (0.5431/sqrt(2) nm), and 1345 (1 bar1 0) fringes were counted across the top of the silicon feature, thus the feature width is 516.52 nm.

Specimens prepared by focused ion beam (FIB) techniques[15] using 30 kV Ga ions were also examined by 300 kV HRTEM. Micrographs of the 0.5 micrometer silicon features were digitized as above for analysis. Although the {110} fringes were not discerned in these thicker specimens, the image of the silicon feature was calibrated so that its height corresponded to 1075 nm. The width of the feature was then measured to be approximately 464 nm. The uncertainties of these measurements are larger than those of the previous specimen. A conservative upper bound,[16] is 2.50 nm.

4. SUMMARY

We have previously reported the physical properties of features having sub-micrometer linewidths that were micro-machined into SOI films. The silicon surface films had a (110) surface orientation and were produced by epitaxial growth on BESOI material. The reference feature edges of these previously reported electrical test-structures were aligned with <112> lattice vectors and were delineated by a lattice-plane selective etch that resulted in the features' having atomically-smooth and planar sidewalls that wereparallel to lattice {111} planes which were normal to the (110) silicon surface. When applied to features having these unique properties, electrical critical dimensions metrology presents an opportunity to establish traceability of the physical widths of the features to fundamental constants, thereby enabling the features to be used as linewidth standards. The role of ECD is that of a secondary reference means, for which it is well suited as a consequence of its high repeatability and relatively low cost. As for the primary reference means, we have previously used top-down HRTEM (High-Resolution Transmission-Electron Microscopy) imaging to reveal a lattice-plane count across the entire width of a 0.586-μm line patterned in (110) epitaxial silicon with atomically planar sidewalls normal to the substrate surface. However, the highly labor-intensive nature of sample preparation for HRTEM imaging, and its destructiveness, makes it desirable to avoid having to use it for *every* feature whose absolute linewidth is to be determined for reference-material applications. On the other hand, its use to determine the extent of any offset between the ECD measurements, and corresponding absolute physical dimensions, of all features replicated on a particular substrate, may be economically acceptable. This paper is a first report on the necessary set of metrology tools applied to reference features that were patterned in (100) epitaxial silicon material grown on BESOI (Bonded and Etched-Back SOI) substrates. Reference features aligned with <110> directions that are patterned in the surface of such material are distinguished from those used in the earlier work by their having atomically-planar {111} sidewalls inclined at 54.737° to the (100) plane of the substrate surface. Their sidewalls are otherwise rendered as smooth and planar, as those studied previously, by the chemical polishing provided by the delineating etch. The (100) implementation may offer advantages over, or complement the attributes of, the vertical-sidewall one for selected reference-material applications. As before, analysis of the offsets between the HRTEM and ECD linewidth measurements that are made on the same SOI features is being investigated to establish the feasibility of a traceability path at acceptable cost. Other novel aspects of the (100) SOI implementation that are reported here are the ECD test-structure architecture and that the HRTEM lattice-plane counts are derived from feature cross-sectional, rather than top-down, imaging of the {111} lattice planes.

5. ACKNOWLEDGMENTS

Wafer processing for this research was conducted partially at Sandia National Laboratories, a multi-program laboratory operated by Sandia Corporation, a Lockheed-Martin Company, for the United States Department of Energy, under contract DE-AC04-94AL85000. The Sandia effort is specifically being supported through the Sandia/SEMATECH Cooperative Research and Development Agreement (CRADA Number 1082). Financial support was also provided by the National Semiconductor Metrology Program at NIST. The authors acknowledge computer-aided drawing services provided by David Renninger and Colleen Ellenwood. Jack Martinez and Dan Josel at NIST and Jeff Sniegowski at Sandia are thanked for technical reviews. Jane Wilkes, Katherine Cresswell, and Erik Secula are thanked for editorial reviews.

Thanks to FEI Company and Micro Optics, Inc., for the use of their equipment.

The following should exactly occupy one full line between margins...

These instructions show the desired format and appearance of a manuscript prepared for the Proceedings of SPIE. The

6. REFERENCES

1. R. A. Allen, P. M. Troccolo, J. C. Owen III, J. E. Potzick, and L. W. Linholm, Comparisons of Measured Linewidths of Sub-Micrometer Lines Using Optical, Electrical, and SEM Metrologies, SPIE Vol. 1926, Integrated Circuit Metrology, Inspection, and Process Control VII, pp. 34-43 (1993)

2. M.W. Cresswell, R.A. Allen, W.F. Guthrie, J.J. Sniegowski, R.N. Ghoshtagore, and L.W. Linholm, "Electrical Linewidth Test Structures Fabricated in Mono-Crystalline Films for Reference Material Applications," IEEE Trans. Semiconductor Manufacturing, Vol.11, No. 2, May 1998, pp. 182-193.

3. Monocrystalline Test Structures, and Use for Calibrating Instruments, M. W. Cresswell, R. N. Ghoshtagore, L. W. Linholm, R. A. Allen, and J. J. Sniegowski, United States Patent Number: 5,684,301.

4. M.W. Cresswell, J. J. Sniegowski, R. N. Ghoshtagore, R. A. Allen, W. F. Guthrie, A. W. Gurnell, L. W. Linholm, R. G. Dixson, and E. C. Teague, Recent Developments in Electrical Linewidth and Overlay Metrology for Integrated Circuit Fabrication Processes, Jpn. J. Appl. Phys. 35, Part 1 (12B), 6597-6609 (December 1996).

5. Y. Nakayama and K. Toyoda, "New Sub-micron Dimension Reference for Electron-Beam Metrology System," Integrated Circuit Metrology, Inspection, and Process Control, Vol. 2196, pp. 74-78 (1994)

6. G. Timp, A. Agarwal, F. H. Baumann, T. Boone, M. Buonanno, R. Cirelli, V. Donnelly, M. Foad, D. Grant, M. Green, H. Gossmann, S. Hillenius, J. Jackson, D. Jacobson, R. Kleiman, A. Kornblit, F. Klemens, J. T. C. Lee, W. Mansfield, S. Moccio, A. Murrell, M. O'Malley, J. Rosamilia, J. Sapjeta, P. Silverman, T. Sorsch, W. W. Tai, D. Tennant, H. Vuong, B. Weir, Low leakage, Ultra-thin Gate Oxides for Extremely High Performance sub-100nm MOSFETS, IEDM 97 Proceedings, pp. 930-933.

7. R.A. Allen, R.N. Ghoshtagore, M.W. Cresswell, L.W. Linholm, and J.J. Sniegowski, "Comparison of Properties of Electrical Test Structures Patterned in BESOI and SIMOX files for CD Reference Material Applications," Proceedings SPIE 3332 (1998) 124-131

8. R.A. Allen, M.W. Cresswell, and L.M. Buck, "A New Test Structure for the Electrical Measurement of the Widths of Short Features with Arbitrarily Wide Voltage Taps," IEEE Electron Device Letters, 13 (6), 322-324 (1992).

9. L.W. Linholm, R.A. Allen, and M.W. Cresswell, Microelectronic Test Structures for Feature-Placement and Electrical Linewidth Metrology, Handbook of Critical Dimension Metrology and Process Control, SPIE Critical reviews of Optical Science and Technology Volume CR52, pp. 91-118, (1993)

10. R. A. Allen, M. W. Cresswell, and L. M. Buck, A New Test Structure for the Electrical Measurement of the Widths of Short Features with Arbitrarily Wide Voltage Taps, IEEE Electron Device Letters, 13 (6), 322-324 (June 1992).

11. M.W. Cresswell, N.M.P. Guillaume, W.E. Lee, R.A. Allen, W. F. Guthrie, R.N. Ghoshtagore, Z. Osborne, N.Sullivan, and L.W. Linholm, "Extraction of Sheet Resistance from Four-Terminal Sheet Resistors Replicated in Monocrystalline Films With Non-Planar Geometries," IEEE Transactions on Semiconductor Manufacturing, Vol. 12, No. 2, pp. 154-165, (1999)

12. W. E. Lee, W. F. Guthrie, M. W. Cresswell, R. A. Allen, J. J. Sniegowski, and L. W. Linholm, Reference-Length Shortening by Kelvin Voltage Taps in Linewidth Test Structures Replicated in Mono-Crystalline Silicon Films, Proceedings of the IEEE International Conference on Microelectronic Test Structures (ICMTS 97), Vol. 10, pp. 35-38.

13. M. Shikida, K. Sato, K. Tokoro, and D. Uchikawa: Comparison of Anisotropic Etching Properties between KOH and TMAH Solutions, Proc of IEEE Int. MEMS-99 Conf. (Orlando, 17. 21. Jan. 1999), 315-320.

14. Spence, J.C.H., Experimental High-Resolution Electron Microscopy (Oxford University Press, New York, 1988).

15. L.A. Giannuzzi, J.L. Drown, S.R. Brown, R.B. Irwin, and F.A. Stevie, Focused Ion Beam Milling and Micromanipulation Lift-Out for Site Specific Cross-Section TEM Specimen Preparation," Materials Research Society, Symposium Proceedings Volume 480, eds. Ronald M. Anderson and Scott D. Walck, 19, Materials Research Society, Pittsburgh, (1997).

16. B.N. Taylor and C.E. Kuyatt, *Guidelines for Evaluating and Expressing the Uncertainty of NIST Measurement Results*, NIST Technical Note 1297 (1994).