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Micromachined Systems-on-a-Chip: Infrastructure, Technology and Applications

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Abstract

A review is made of the infrastructure, technology and capabilities of Sandia National Laboratories for the development of micromechanical systems that have potential space applications. By incorporating advanced fabrication processes, such as chemical mechanical polishing, and several mechanical polysilicon levels, the range of micromechanical systems that can be fabricated in these technologies is virtually limitless. Representative applications include a micro-engine driven mirror, and a micromachined lock. Using a novel integrated MEMS/CMOS technology, a six degree-of-freedom accelerometer/gyroscope system has been designed by researchers at U.C. Berkeley and fabricated on the same silicon chip as the CMOS control circuits to produce an integrated micro-navigational unit.

I. Introduction

The employment of MEMS for space applications has the potential to lead to a significant reduction in the cost of a mission due to the miniaturization of critical components, such as navigational systems and sensors, and can potentially improve reliability due to the small incremental cost of adding redundant systems. By integrating a wide array of sensors on-chip, the capabilities of low-cost space vehicles, probes and microsatellites will be dramatically improved. Thus advances in the MEMS field today to produce low-cost sensors and actuators will have a direct impact on the cost, capabilities and ultimate feasibility of future space missions.

At the forefront of this revolution in silicon surface micromachining is the Microelectronics Development Laboratory (MDL) at Sandia National Laboratories. Established in 1945, Sandia has a long history of pioneering achievements in the microelectronics field, and is now leading the way in developing the technologies and capabilities required for the next generation of MEMS components. In this paper we review the extensive fabrication facilities at Sandia, as well as several technologies under development for MEMS applications. These technologies include a baseline fabrication process available to the public as a foundry for agile prototyping applications, an advanced MEMS technology employing five structural layers of mechanical polysilicon, and a unique integrated MEMS/CMOS technology that was recently licensed to industry to produce integrated sensor, control and actuator systems.

II. Infrastructure and Process Development

MEMS work carried out at Sandia is primarily done at the MDL, Figure 1, which has 15,000 square feet of Class 1 cleanroom space dedicated to the development of CMOS integrated circuits and MEMS. Baseline CMOS technologies are fabricated alongside MEMS, sharing an extensive semiconductor toolset and knowledge base.

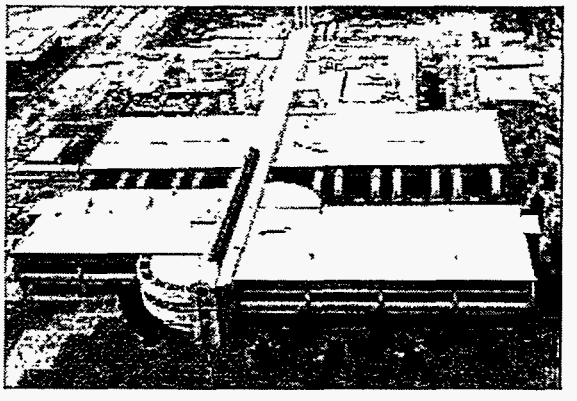


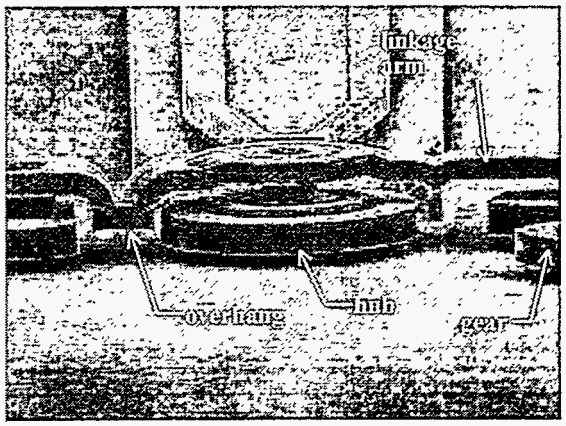
Figure 1. The Microelectronics Development Laboratory (MDL) at Sandia National Laboratories.

MEMS development is constrained to be compatible with conventional CMOS technologies, which in turn makes the processes and technologies developed at Sandia seamlessly transferable to industry.

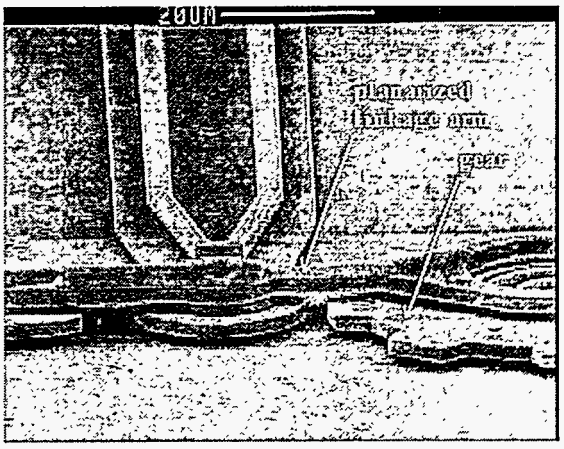
To design highly functional, complex microsystems, a technology must be capable of incorporating several layers of structural polysilicon. However, internal stresses in the polysilicon layers can distort the mechanical structure and lead to stiction effects, which typically lowers device yield. Sandia has carried out extensive characterization of it's fine-grained polysilicon, and developed proprietary techniques to anneal out internal stresses *in-situ* so as to mitigate these effects. The result is that Sandia's fine-grained polysilicon displays a low internal stress of less than 5 MPa after proper annealing cycles, producing small deflections of less than 1 μm [1], for structures up to 1000 μm in length.

An important component of many of the multi-layer MEMS processes developed at Sandia is Chemical Mechanical Polishing (CMP) for the planarization of the upper layer of mechanical polysilicon. In a typical MEMS device, the topology can produce features as high as 12 μm. This surface topology can constrain the movement of upper polysilicon layers after these conformal films are deposited, patterned and released in HF. A process was developed to CMP sacrificial oxides deposited from TEOS [2] prior to polysilicon deposition, using an alkaline abrasive slurry. The result is a flat, non-conformal mechanical polysilicon layer over underlying topography and electrical interconnects. This capability enabled the fabrication of complex interlocking gear trains, discussed in a later section, as well as the fabrication of optically smooth surfaces for MEMS based adaptive optical systems [3]. Figure 2 shows the impact of CMP on complex MEMS components. Figure 2(a) shows the overhang produced by an upper layer of polysilicon on either side of gear hub, leading to mechanical interference with the adjacent gear. This mechanical interference can be eliminated by planarizing the sacrificial oxide between the gear/hub and linkage arm levels of polysilicon, as shown in Figure 2(b).

By tailoring many of the processes commonly available in a CMOS fabrication line for MEMS, such as polysilicon deposition and annealing conditions and CMP, a comprehensive fabrication technology has been synthesized which can be used to produce a wide array of MEMS components.



(a)



(b)

Figure 2. (a) Impact of conformal polysilicon on an unplanarized surface, leading to mechanical interference (overhang) with underlying polysilicon layers. (b) Elimination of mechanical interference by CMP of sacrificial oxide.

III. Technology and Applications

SUMMiT-IV Technology

A baseline fabrication process, called the Sandia Ultra-planar Multi-level MEMS Technology (SUMMiT), has been developed to explore novel concepts in MEMS design. The SUMMiT-IV technology is the only foundry process available which utilizes three layers of releasable polysilicon, for a total of four layers (including a ground plane), as shown in Figure 3.

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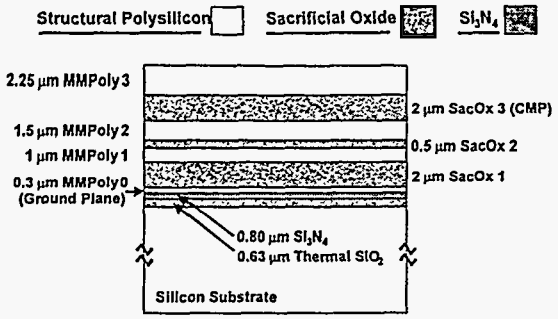

Figure 3. Composition of alternating layers of polysilicon and sacrificial oxide used in the SUMMiT-IV Technology.

The SUMMiT process was developed to be compatible with a wide range of standard MEMS components. For example, by using a ground plane (poly 0) and a single layer of mechanical polysilicon (poly 1), one could create an electrostatic comb drive or scratch drive for actuation. By adding a poly 2 layer to the process, one can create a gear mechanism constrained to rotate on a hub, as well as out-of-plane mirrors and hinges [3]. By adding a CMP step to planarize the third sacrificial oxide layer, and a third mechanical layer of polysilicon, one can form linkages between actuators and output gears, as well as components for a wide array of micro-mechanical, optical and fluidic systems[1].

A major program driving the development of the SUMMiT process is the stronglink micromechanical lock, used for weapon safety applications. At the heart of the stronglink is a set of electrostatically driven microengines [4], which are formed by connecting orthogonal comb drives through linkages to an output gear, which is capable of delivering moderate amounts of torque to a load. The top speed of the microengine has been measured at 300,000 rpm, using a ~90V amplitude drive signal tailored for the microengine [5]. To increase the torque at the expense of speed, a micro-transmission was developed [6] using a set of 3:1 and 4:1 reduction gears. By cascading several of these 12:1 gear trains, a gear reduction ratio of 3 million to 1 was recently demonstrated, with a corresponding increase in torque. By incorporating a rack and pinion assembly to convert rotational to linear motion, controllable step sizes as small as 0.8 nm have been realized. Figure 4 shows a component of the stronglink in which a microengine, micro-transmission and a rack and pinion assembly are used to drive a polysilicon mirror out of plane. The benefits of CMP in the SUMMiT-IV technology are clearly evident for this type of system, resulting in smooth optical surfaces on the polysilicon mirrors. It is noted that the basic elements used in the Stronglink system can be adopted for a wide range of MEMS applications. Additional devices fabricated using the SUMMiT-IV technology include deformable piston mirror arrays for phase detection and modulation [3], as well as optical shutters for lasers and fiber optic applications.

Figure 4. Polysilicon mirror driven out of plane using a microengine, microtransmission and rack and pinion assembly.

SUMMiT-V Technology

The need for greater functionality in the Stronglink design, led to the recent development of the SUMMiT-V Technology. This process includes several additional steps to the SUMMiT-IV Technology, including an additional sacrificial oxide layer and a second CMP step as well as a fifth mechanical layer of polysilicon (including a ground plane). The goal of this work was to include a 24-bit mechanical discriminator to the Stronglink design, which when accessed could direct an optical data signal using two opposing polysilicon mirrors. Thus, the additional layer of polysilicon allows for the fabrication of a range of critical features such as a linear pin-in maze discriminator, as well as gear trains on moveable platforms [7]. Figure 5 is a schematic of the most recent Stronglink design, showing one half of the complete system. This award winning design [8] is considered to be the most complex, fully actuated, surface micro-machined system fabricated to date.

[1] The SUMMiT-IV process, as well as the Integrated Technology (discussed later), is available to the public through our Agile Prototyping Program, allowing researchers to fabricate state-of-the-art MEMS designs in a well characterized, base-line technologies. More information is available at *http://www.mdl.sandia.gov/Micromachine*

Using the additional flexibility of the SUMMiT-V technology, many of the standard components developed in the SUMMiT-IV technology were completely redesigned. This includes electrostatic comb drives used in the microengine, which benefit from stacking several mechanical layers of polysilicon, leading to a dramatic increase the z-axis stiffness of the support springs. In addition, advanced designs for the microengine linkage assembly were implemented to reduce the deleterious effects of stiction [7]. As with the SUMMiT-IV process, several annealing steps are included in this technology to reduce stress in the polysilicon and sacrificial oxide layers.

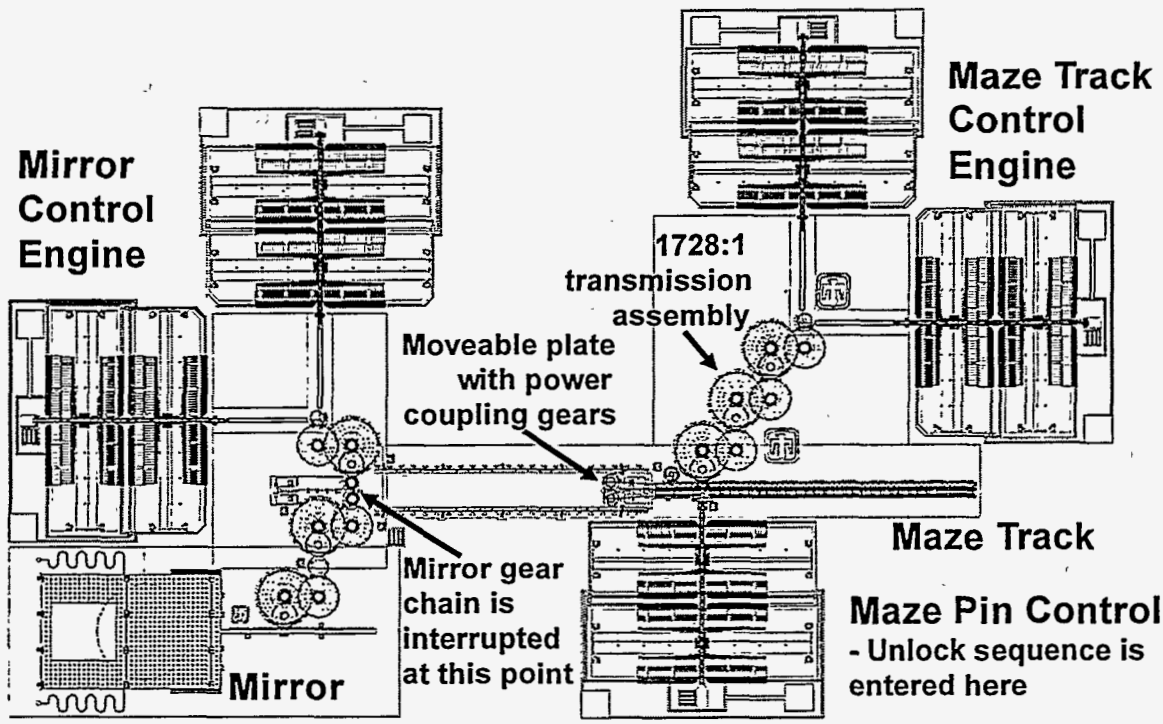

Figure 5. Latest generation Stronglink micromechanical lock system fabricated using the SUMMiT-V Technology, incorporating several standard components redesigned for the new technology (one half of complete system).

Integrated MEMS Technology

A significant improvement in device functionality, and a high level of integration can be obtained by integrating the control circuits and MEMS devices on the same silicon chip. In some cases in which the input stimuli produce low-level signals, as with certain types of capacitive sensors, the sense and control electronics have to be integrated on-chip so as to reduce parasitic noise from interconnects. Previous attempts to integrate MEMS and CMOS have tried to process the MEMS devices after the CMOS [9], using refractory metals that can withstand the high temperature annealing cycles required to relieve stress in structural polysilicon. Still other approaches have tried to interleave the necessary MEMS processing steps with the CMOS steps [10], leading to a rigid, constrained process flow. Sandia has developed a novel approach toward integrating surface micromachined components with the conventional CMOS circuits, by first fabricating the MEMS components, and then continuing with conventional CMOS processing.

Since the surface topology of typical MEMS devices (2-6μm) is significantly different than that of conventional CMOS circuits (1-2 μm) the MEMS components are fabricated in a shallow (~5 μm) trench etched into the wafer surface. Upon completion of the MEMS devices, the trench is backfilled with sacrificial oxide, planarized by CMP, and capped with a silicon nitride membrane. After a stress relief annealing cycle, the wafer is ready for conventional IC processing.

The additional thermal budget of CMOS processing has a negligible effect on the MEMS devices, and can in fact further lead to a reduction of built-in stress. To release the MEMS portion of the system, the CMOS circuits are protected with photoresist, and the nitride membrane and sacrificial oxide are removed in buffered HF [11]. At the present time the integrated process employs two layers of polysilicon (including the ground plane), with a four-layer process currently under development.

A cross section of a microsystem during fabrication is shown in Figure 6. The MEMS and CMOS components are fabricated in a 6 μm, arsenic-doped epilayer. Electrical interconnects between the CMOS circuitry and MEMS are through polysilicon studs which are at the height of the wafer surface and are connected to the MEMS groundplane (MM Poly 0). It is noted that with Sandia's modular approach towards integration, any type of microelectronic processing can be undertaken, including techniques to fabricate radiation-hard circuits and Bipolar and BiCMOS circuits.

The integrated MEMS/CMOS process has been well received by the semiconductor industry, having recently been awarded an R&D 100 award as one of the 100 most technologically significant new products of the year. Analog Devices Inc. has licensed Sandia's Integrated Technology for their next generation inertial sensors. In collaboration with researchers at the Berkeley Sensor and Actuator Center (BSAC), several advanced prototype accelerometers and oscillators have been fabricated in the Integrated Technology [12, 13].

One of the recent results from this collaboration with BSAC was a six-degree of-freedom Inertial Measurement Unit (IMU), incorporating a 3 axis accelerometer and XY- and Z-axis gyroscope [14], for a small, self-contained navigational system. Figure 7 shows the layout of the IMU, incorporating the accelerometer, gyro's and on-chip control circuitry, in a circuit less than 1 cm^2. Initial measurements on the individual components show that the +/- 25g accelerometer demonstrated an in-plane axis rms noise floor of 110 μg/√Hz and an 84 dB dynamic range at 100 Hz bandwidth [15]. Further testing on the complete system is currently underway.

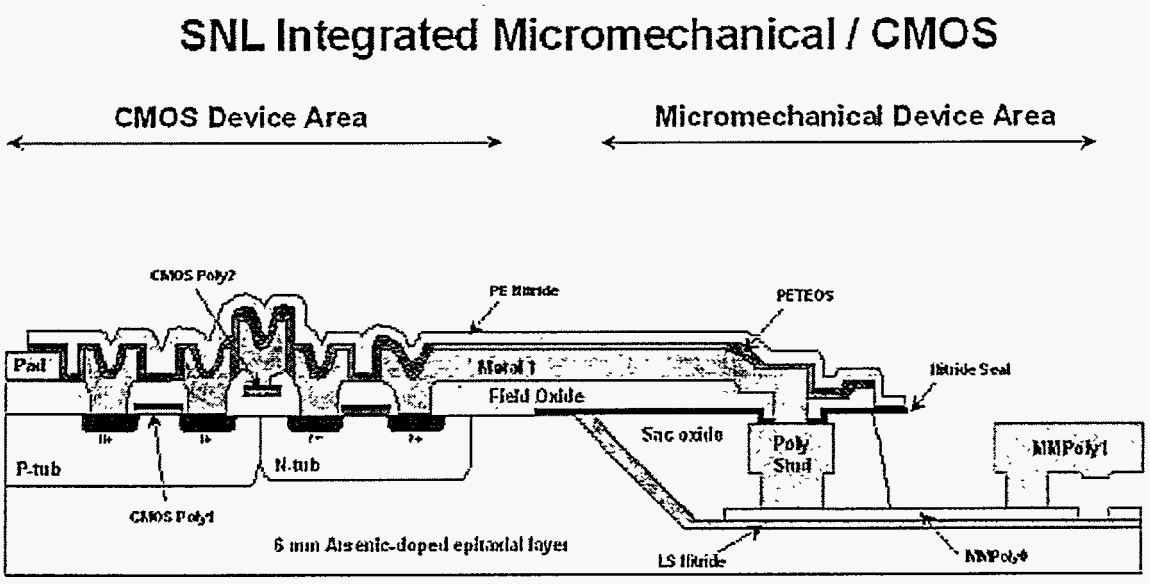

Figure 6. Integrated MEMS/CMOS Technology developed at Sandia National Laboratories for the monolithic integration of CMOS control circuits and MEMS sensors and actuators, on the same silicon chip. To handle the differences in surface topography, the MEMS components are fabricated in a shallow trench below the wafer surface proior to CMOS processing.

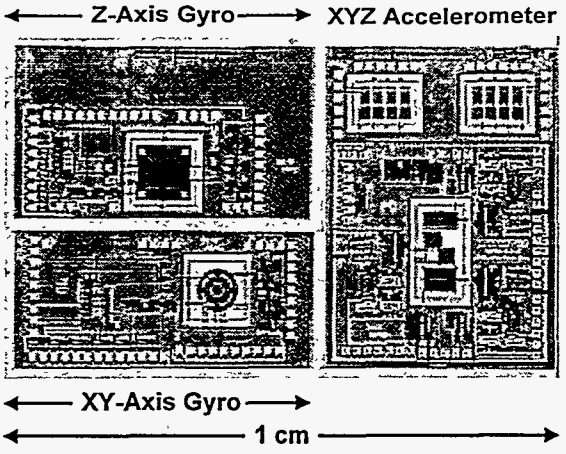

Figure 7. Six degree of freedom micro-navigational system fabricated in Sandia's MEMS/CMOS Integrated Technology (Design by U.C. Berkeley).

IV. Conclusions

Micromachined systems are poised to have a far reaching impact on the capabilities and feasibility of future space missions. By performing tasks in the microworld, payload costs are significantly reduced, and reliability could be dramatically improved through the use of inexpensive redundant systems fabricated en masse using conventional integrated circuit/surface micromachining technology. Sandia National Laboratories is leading the way in MEMS technology development with it's baseline SUMMiT-IV process, and it's advanced 5-level polysilicon SUMMiT-V process. By further integrating MEMS sensors and actuators with CMOS circuits in the Integrated Technology, Sandia is establishing a new paradigm for micromachined systems-on-a-chip.

V. Acknowledgements

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