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Impurity Gettering

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I. Gettering Requirements and Processes

Transition metal impurities are well known to cause detrimental effects when present in the active regions of Si devices[1-3]. Their presence degrades minority carrier lifetime, provides recombination-generation centers, increases junction leakage current and reduces gate oxide integrity. Thus, gettering processes are used to reduce the available metal impurities from the active region of microelectronic circuits. In recent years, gettering technology has become an indispensable process tool in the manufacture of VLSI circuits, being particularly important, for example for DRAMs.

Gettering processes are usually divided into intrinsic (or internal) and extrinsic (or external) categories. Intrinsic refers to processing the Si wafer in a way to make available internal gettering sites, (e.g. heat treating to form oxide precipitaties), whereas extrinsic implies externally introduced gettering sites (e.g. by introducing damage on the backside of the wafer, by phosphorus diffusion, etc.). Intrinsic gettering technology has been optimized through widespread use and is presently a standard manufacturing process. It involves temperature cycling Czolchralski (CZ) Si to create oxide precipitates in the bulk of the wafer along with a defect free, low impurity denuded zone near the surface for the device active area. Epitaxial wafers (e.g. p on p^+ subtrates) are often used to further enhance the process. Intrinsic gettering works by providing nucleation sites at strained

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internal interfaces around the internal oxide precipitates which cause the precipitation of the metal impurities (typically as metal silicides). Often, this approach incorporates existing high temperature processing steps to optimize the formation of the denuded zone and the bulk oxide precipitates.

For future device generations integrated circuit processing will necessitate much lower thermal budgets to achieve the required reductions in feature sizes. At the same time the acceptable level of metal impurities will steadily decrease, (see Table 1)[4]. For some next generation circuits metallic impurity limits are expected to be as low as 10^9 atoms/cm^3. These combined trends raise special concerns for intrinsic gettering. Not only will the formation of the precipitated oxide and denuded zone be difficult to achieve with the lower thermal budgets, but another inherent limit may set in. In this or any process which relies on the precipitation of metal silicides the impurity concentration can only be reduced as low as the solid solubility limit. However, the solubilities of transition metals relative to silicide formation are typically found to be $\gtrsim 10^{12}/cm^3$ at temperatures of 800° C and above, and thus inadequate to getter to the needed concentration levels. Therefore, new gettering techniques, such as impurity trapping which will extend on down below solubility levels may be needed to meet future requirements.

It is thus anticipated that future microelectronic device processing will require one or more of the following advances in gettering technology: 1) new and more effective gettering mechanisms; 2) quantitative models of gettering to allow process optimization at low process thermal budgets and metal impurity concentrations, and/or 3) the development of front side gettering methods to allow for more efficient gettering close to device regions. These trend-driven needs provide a driving force for qualitatively new approaches to gettering and provide possible new opportunities for the use of ion implantation in microelectronics processing.

II. Ion Implantation as Gettering Process

Ion implantation damage was shown to getter metal impurities more than two decades ago and various groups have explored implantation as a gettering technique. However, since implantation has not been the standard process, such studies have not been extensive. Further, the entire area of gettering has not received much attention in terms of quantitative, predictive modeling.

With the above recent trends, ion implantation offers several inherent advantages and as a result there has been considerable interest in reexamining this approach as a process tool for gettering. For example, ion implantation is a standard process tool for doping and is inherently compatible with front side (proximity) methods for introducing gettering sites. Further, the advent of high energy implantation provides the possibility of introducing damage or impurity species into the silicon below the active device region. Also, it can readily be used in conjunction with lateral patterning for the selective introduction of gettering regions.

Recently, there have been several new gettering approaches based on ion implantation which have been explored and appear promising. These approaches include the deeper introduction of extended defects (such as dislocation loops),[5,6] the introduction of three dimensional cavity defects with new gettering characteristics,[7] and the introduction of impurities (such as carbon) with stronger gettering behavior.[8] We now discuss the status and future prospects for these three areas of implantation gettering.

III. Implantation Damage

The gettering of metal impurities at ion implantation produced damage in silicon was first demonstrated in the early 1970's.[9,10] Impurities such as Fe, Co, Ni, Cu, and Au were shown to be gettered after implanting a variety of ion species.

More recently, channeled and high energy Si self implantation has been examined in more detail as a gettering mechanism. End-of-range dislocation loops and other defects provide gettering sites. For example, Si implant formed buried amorphous layers regrow to leave a layer of defects where the two internal crystalline-amorphous interfaces meet upon solid phase epitaxial regrowth.[5] These defects have been demonstrated to effectively getter Cu from the Si surface region with the process being most efficient at 600° C. Other studies have focused on proximity gettering of Fe and have demonstrated through reduced junction leakage currents the electrical benefits of high energy Si self implantation for gettering heavy metals.[6] In general it is found to be more difficult to getter Fe than Cu impurities. Also, the use of boron implantation, as is standardly employed for high energy well implants, is not found to provide effective gettering, presumably due to the lesser defect introduction.[11] An inherent advantage of purely intrinsic damage gettering due to Si implantation is the lack of the introduction of any other impurity or dopant species. However, it is not yet known whether sufficiently effective gettering can be achieved in this manner for future generation circuits. Also, the gettering mechanisms need to be further clarified.

IV. Implantation-Formed Nanocavities

A recently developed new approach to gettering is the formation of a layer of microscopic cavities within the silicon.[7] These nanocavities are formed by high fluence He implantation, which upon annealing to 700° C or higher result in He outgasing from the silicon, leaving behind the microscopic cavities (see Fig. 1).. These cavities are highly stable, persisting to processing temperatures as high as 1200° C. The internal free Si surfaces of these cavities are found to provide strong traps for transition metal impurities and offer the possiblitity of a new gettering mechanism. The process is found to be one of chemisorption onto the internal cavity surface. It provides a distinct approach from the metal silicide precipitation of intrinsic gettering and offers the possibility of gettering impurities to much lower concentrations since it is based on a trapping, rather than second phase formation, mechanism. Gettering by helium implantation induced nanocavities has been shown for Cu, Ni, Co, Fe, and Au, and this process has now been demonstrated by a number of groups.[7,12-17]

The nucleation of stable cavities requires the implantation of a sufficient concentration of He to induce He gas bubbles within the Si.[18] Thus, as a function of He implantation fluence a relatively sharp threshold is observed with the onset of gas bubble formation at which the gettering becomes much more effective as the process changes from defect gettering to nanocavity gettering.[14-15] For example, for 30 keV He implants at room temperature followed by annealing, the onset of cavity formation occurs between 1 and $2x10^{16}$ He/cm2, indicating a threshold He concentration of ≈1.6 at.%. As implanted the cavities are typically of a size of only 1 to 2 nm in diameter, whereas after annealing to 700° C the average nanocavity diameter is 8.5 nm, and after 900° C the cavities become much larger with average diameters of 20 nm. The formation of gas bubbles due to inert gas implantation has been known for some time,[18] but the role of these open volume defects in gettering in silicon was only recently identified.[7] From TEM observations the ripening of the cavities upon annealing has been inferred to be due to internal migration of the cavities rather than to dissolution of vacancies. Extensive studies of cavity properties have been carried out, including the effects of internal faceting, of their electrical and of their hydrogen trapping properties.

The trapping of Cu at nanocavities has been studied in detail, leading to a quantitative understanding of this gettering process. In Fig. 2 is shown an example of such studies where the Cu has been introduced by implantation into the backside of a Si wafer and He implantation used to form nanocavities in the front side of the wafer. Heat treatment results in Cu silicide formation and subsequent heating leads to the transport of Cu across the wafer and trapping within the nanocavities. The results of trapping vs. time are in good agreement with quantitative modeling where the diffusivity and solubility of Cu in Si is accounted for, as well as the heat of solution of 1.7 eV for Cu relative to Cu_3 Si. The saturation level of Cu within the nanocavities is found to agree well with the expected number of bonding sites available at the cavity surface as determined by TEM measured cavity surface area and assuming 7 Si bonds per nm square available on {111} and 1x2 reconstructed {100} Si surfaces.[14] These results provide strong support for the assumption of chemisorption bonding of Cu on the cavity walls. Numerous experiments for various temperatures and layer combinations have been used to confirm this interpretation.[13]

The process of chemisorption of the metal impurities onto the internal cavity surface has important consequences in terms of the gettering process.[13] In particular it is distinct from the metal silicide formation process which is the primary mechanism operative in currently used gettering schemes. Trapping due to chemisorption offers a thermodynamic advantage over precipitation in that trapping will persist to arbitrarily at low concentrations and maintain a constant of proportionality between the amount of impurity remaining in the solution and the fractional occupation of the trapped sites. For precipitates in near local equilibrium between the precipitated phase and the impurity in solid solution, one may express the concentration in solid solution as

$$C_{sp} = C_o \exp(-Q_p/kT) \quad , \qquad (1)$$

where C_{sp} is the solution concentration expressed as an atomic fraction, C_0 is a temperature independent factor and Q_p is a binding energy relative to the solution. In contrast for trapping the concentration of trapped species is described as

$$C_{st} = [\theta/(1-\theta)] \exp(-Q_t/kT) \quad , \qquad (2)$$

where θ is the average fractional occupancy of the traps and Q_t is the trapped energy. Here it is assumed that the cavity binding sites are not influenced by occupation of neighboring sites and that C_{sp} is the solubility for the silicide phase independent of the number of precipitated atoms. Note that the concentration at traps C_{st} is proportional to θ for occupations where $\theta \ll 1$ and thus, the solution concentration can be reduced far below the impurity solid solubility provided the trap energy is sufficiently large relative to kT and the trap sites are not all filled. Based on this mechanism an example is shown in Fig. 3 demonstrating for the case of Cu the predicted many orders of magnitude further reduction in gettering available by the nanocavity mechanism relative to conventional silicide precipitation gettering at low temperatures.

Systematic studies have been carried out for Cu, Ni, Co, Fe, and Au for nanocavity trapping and saturation concentrations.[12-14] Gold is found to be trapped up to approximately one monolayer of internal cavity surface, similar to Cu. However, Ni is found to saturate available traps at a lower coverage. This result has been understood in terms of external Si surface studies where Ni on the {111} Si surface absorbs with a $\sqrt{19}$ ordered structure with one Ni atom per unit cell at high coverages. This result is consistent with the observed cavity surface saturation at about the same fractional coverage. These results along with saturation coverages for Co and Fe are given in Table 2. In the case of Co and Fe considerably lower monolayer coverages of the cavity surfaces were observed for the trapped metal. For Fe the cavity coverage was approximately 0.0062 ML and for Co approximately 0.0026 ML. Studies where the cavity trapping was equilibrated with silicide precipitates allowed the chemisorption energy to be inferred for Co and Fe on the nanocavity surface (accounting for the reduction of $\approx$1/7 expected for Co surface coverage and $\approx$1/2 for Fe. In the case of Co and Fe the silicide binding is stronger than that for chemisorption, corresponding to a chemisorption to silicide energy ratio of $\approx$0.6 in both cases. Thus, the traps would be expected to be only partially occupied. In general, the heat of solution for silcides increases upon moving across the 3d transition element row from Cu/Ni to Co/Fe. Even under these conditions however, there is still a sizable binding energy (~1.5eV) and thus substantial fractions of metal impurities such as Fe can be gettered relative to levels which would be expected to be present for silicon wafers under integrated circuit processing conditions. Therefore, the results obtained so far suggest that this new gettering mechanism may provide substantially more effective trapping than available by conventional approaches, as well as extending down to much lower levels than previously available.

Several other relevant features have been established for nanocavities which would be important considerations in an actual processing application. First, these internal surfaces strongly bind hydrogen, and in fact the surface silicon-hydrogen bond energy (2.6eV) has been established through cavity experiments.[13] This strength is sufficiently large as to displace the bonding of eg, Cu at cavity walls in the presence of hydrogen, and the process is reversible (i.e.,if the H is removed the Cu can be retrapped at nanocavity surface). It also has been shown in CZ Si wafers that for the higher O content of this material O can be trapped by cavities, although a substantial number of sites remained available for metal impurity trapping.[14] Finally it should be noted that the electrical properties of cavity surfaces in Si have been investigated and their deep levels established (they can charge either positively or negatively by trapping electrons or holes).[13] Thus, electric fields within a Debye screening distance of nanocavities may be present depending on the particular conditions experienced and need to be taken into account in the case of short distance proximity gettering.

V. Implanted Impurities

Carbon implantation into Si has been recently shown to be a particularly effective impurity species for Au, Fe, and Cu gettering.[8,17,19] Typical implantation doses in the range of 10^{15} to $10^{16}/cm^2$ have been used in these studies. However, surprisingly low fluences of 10^{12} C/cm^2 have been reported to be effective for Fe gettering as measured by PN junction leakage currents for high energy (1.3 MeV) carbon implants.[19] Also, it has been shown that the C implantation is much more effective than oxygen and that given sufficient He doses to form nanocavities, these latter traps are significantly more effective than the C or O for gettering.[17] The C was inferred not to be simply enhancing the nucleation of oxide precipitates for its effect.

Carbon is also known to have a number of interesting effects on implantation damage, including promoting the reduction of end-of-range defects. The influence of carbon on gettering is thus of considerable interest, although the microscopic nature of the gettering process is not understood at this time. The major potential advantage of impurity gettering by species like C is the ability to achieve gettering at lower fluences than may be required for nanocavities. However, the carbon induced gettering centers must have sufficient stability if they are to be used in semiconductor processing. This knowledge, as well as a quantitative understanding of the process to establish the potential of this approach, still remains to be established.

VI. Perspective on Implantation Gettering

Ion implantation offers the possibility of several new methods to deal with the increasingly stringent requirements on metal impurity control in semiconductor processing. Although, even the addition of only one more implantation step to a process would not be taken lightly, the need for reduced thermal budgets in combination with the further reduction in gettering levels beyond what may be achievable by silicide precipitation mechanisms point to possible opportunities for ion implantation approaches. Further potential benefits for implantation are its inherent compatibility with front side/proximity gettering approaches and the fact that it is a long established process for microelectronics manufacturing. An additional secondary advantage of ion implantation and related ion beam analysis techniques, is that they offer the possibility of developing a more quantitative description of gettering processes, whether for implant gettering or other approaches.

A potential qualitative change in future generation microelectronics fabrication is the possible introduction of silicon on insulator (SOI) material for microelectronic circuits. If SOI material becomes the standard, processes to getter impurities within the top Si layer may become important and implantation into laterally confined regions for proximity gettering could be readily adaptable to this case.

For implantation gettering to become a viable process considerable advances are required in the understanding and quantitative characterization of the gettering processes. At present the nanocavity gettering has received the most detailed quantitative characterization and this approach appears to provide the strongest mechanism for implantation gettering. However, much remains to be learned to establish this or any of the implantation approaches as a gettering technology for semiconductor processing.

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Table I. Metal impurity limits as a function of device generation (from the SIA roadmap).[4]

Year	1995	1998	2001	2004	2007
Feature size (μm)	0.35	0.25	0.18	0.13	0.10
Wafer diameter (mm)	200	200	300	300	400
Metal impurity limit (at/cm^2)	$5x10^{10}$	$2.5x10^{10}$	$1x10^{10}$	$5x10^9$	$2.5x10^9$

Table II. Summary of nanocavity gettering measurements for various impurity metals in Si. Results given are the amount of trapped solute expressed in monolayers of available cavity surface, the cavity surface chemisorption energy for the impurity expressed relative to solution in the Si lattice and the ratio of this energy to the heat of solution for the corresponding silicide formation.

Metal	Trapped (ML)	Chemisorption Energy	Chemisorption Energy/Silicide Energy
Cu	≅1	2.2eV	1.4
Au	≅1	>2.0	>0.8
Ni	0.06	>1.5	>0.9
Co	0.003	1.7	0.6
Fe	0.006	1.6	0.6

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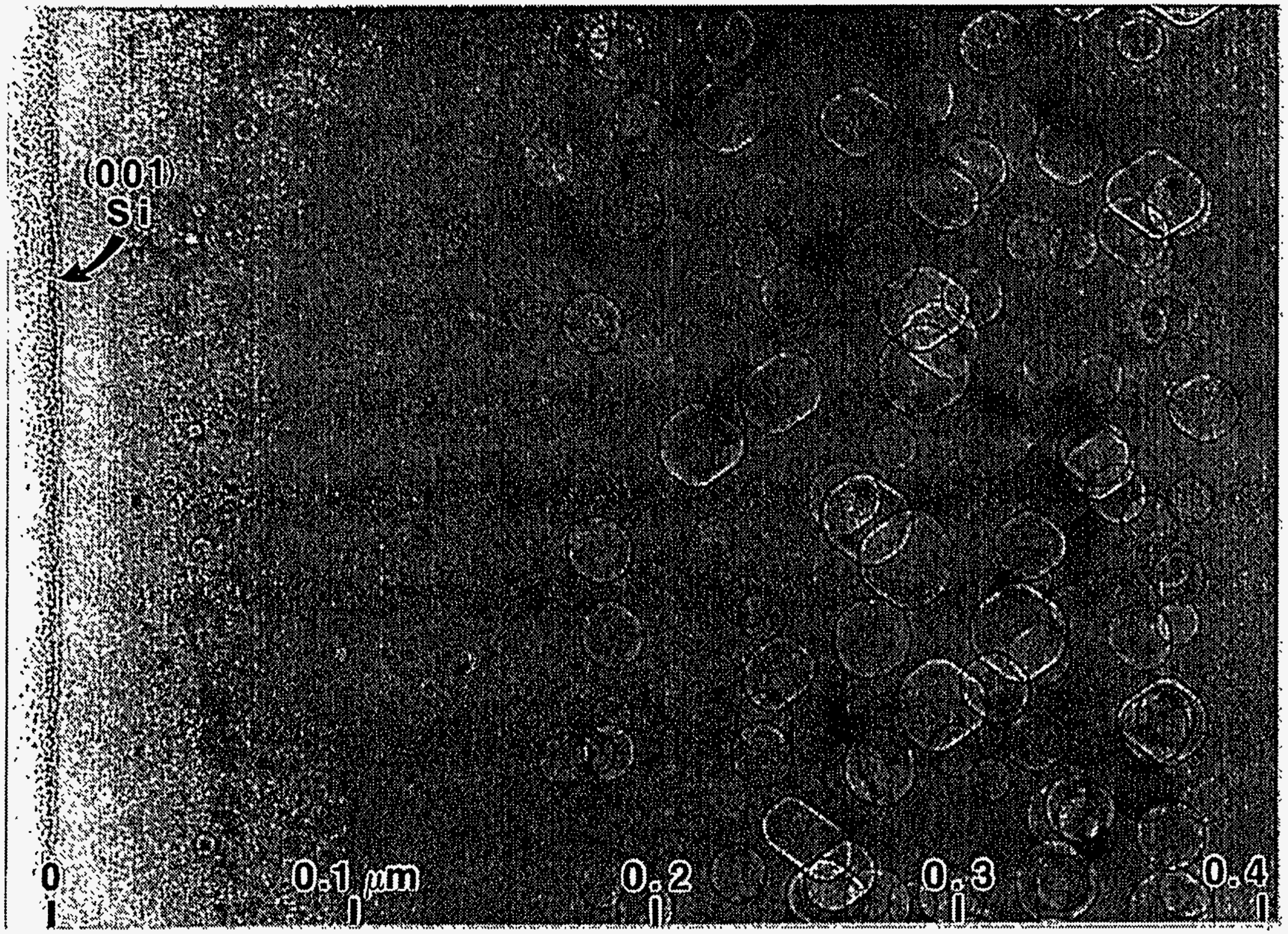
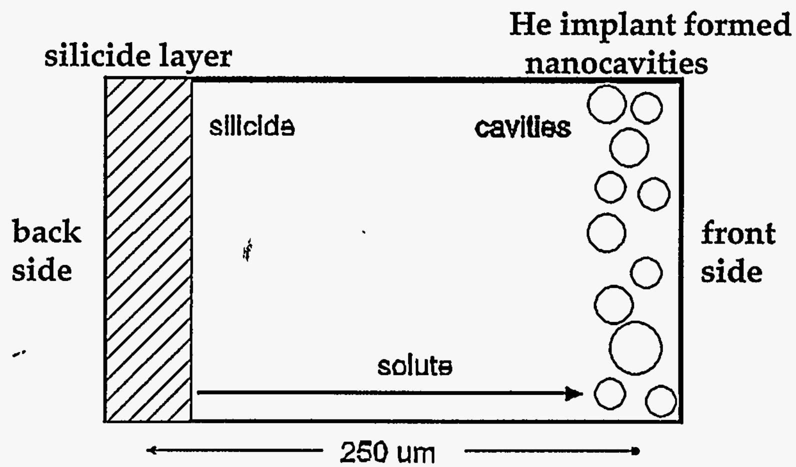
Cavities in He-Implanted Si



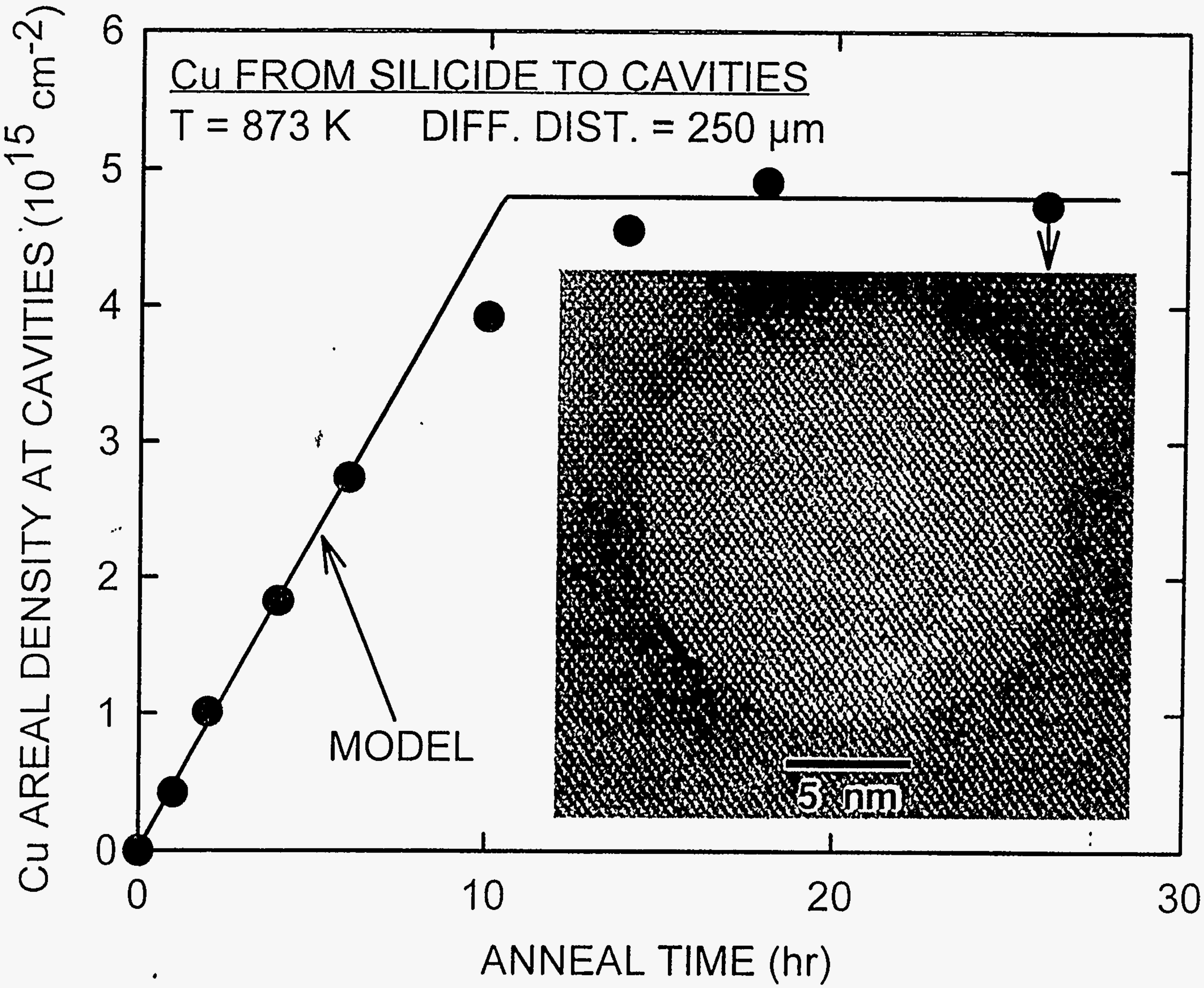
[110] cross-section TEM

1×10^{17} He/cm^2 at 30 keV
1 hour at 900°C

Fig. 1


He implant formed
nanocavities
silicide layer
silicide
cavities
back
side
front
side
solute
250 um

2a


Cu FROM SILICIDE TO CAVITIES
T = 873 K
DIFF. DIST. = 250 μm
MODEL
5 nm
Cu AREAL DENSITY AT CAVITIES (10^15 cm^-2)
ANNEAL TIME (hr)
0
1
2
3
4
5
6
0
10
20
30

97

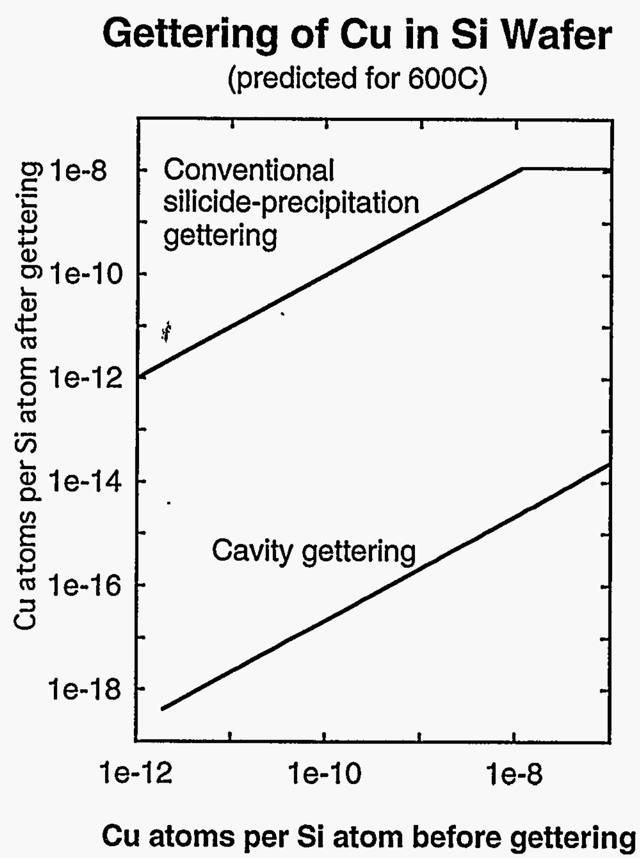

Gettering of Cu in Si Wafer
(predicted for 600C)
Conventional
silicide-precipitation
gettering
Cavity gettering
1e-8
1e-10
1e-12
1e-14
1e-16
1e-18
Cu atoms per Si atom after gettering
1e-12
1e-10
1e-8
Cu atoms per Si atom before gettering

Fig. 3