SAND98-0608C
SAND--98-0608C
CONF-980504--

DEEP HIGH-ASPECT RATIO SI ETCHING FOR ADVANCED PACKAGING TECHNOLOGIES

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Deep high-aspect ratio Si etching (HARSE) has shown potential application for passive self-alignment of dissimilar materials and devices on Si carriers or waferboards. The Si can be etched to specific depths and lateral dimensions to accurately place or locate discrete components (i.e. lasers, photodetectors, and fiber optics) on a Si carrier. It is critical to develop processes which maintain the dimensions of the mask, yield highly anisotropic profiles for deep features, and maintain the anisotropy at the base of the etched feature. In this paper we report process conditions for HARSE which yield etch rates exceeding 3 µm/min and well controlled, highly anisotropic etch profiles. Examples for potential application to advanced packaging technologies will also be shown.

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INTRODUCTION

Pattern transfer into Si has been very successful by both wet chemical and plasma etch techniques.[1-5] However, as design rules shrink and device complexity increases process limitations are often encountered. For example, wet chemical etching is typically fast, often exceeding several µm/min, but can be isotropic, crystallographic, and difficult to control. Reactive ion etching (RIE) of Si in either chlorine or fluorine based plasmas can yield anisotropic, non-crystallographic, highly directional etching but at rates typically < 0.5 µm/min. High-density plasma etching including electron cyclotron resonance (ECR) etching and inductively coupled plasma (ICP) etching can result in rates > 2.5 µm/min with anisotropic profiles (at temperatures < 0°C) but aspect ratios that are ≤ 10:1. The recent development of a high-aspect ratio Si etch (HARSE) process has resulted in anisotropic profiles at room temperature, etch rates > 3.0 µm/min, and aspect ratios often > 30:1.[6] Additionally, HARSE has etch selectivities to photoresist > 75:1 thereby eliminating the process complexity of hard etch masks for features deeper than 100 µm.

The HARSE process has revolutionized how to conceive and implement "mixed technology" integration and packaging. Such a process capability will enable passive self-alignment and packaging of dissimilar materials. For example, a Si substrate can be used as an "optical bench" for III-V based photonic devices.[7, 8] Using the HARSE process, the Si substrate may be etched to multiple, specific depths while retaining accurately controlled dimensions in the mask plane. This permits accurate alignment of dissimilar components to one another (modulators, lasers, fiber, etc.). Additionally, HARSE can be used to integrate a variety of microsystem components, including sensors, resonators, or surface acoustic wave (SAW) devices, electronic devices, including Si CMOS, bipolar, or high-frequency GaAs technologies, and MEMS. Other applications include through-the-wafer via holes for optical or electrical interconnects, high-aspect ratio trenches for chip-to-chip assembly, and self-assembly of LIGA-formed components.

The HARSE process relies on the deposition of a sidewall polymer etch inhibitor to prevent lateral etching of the Si thus resulting in highly anisotropic profiles at reasonably high etch rates for deep-etched features. The HARSE process uses an ICP reactor and a fluorine-based plasma to etch the Si. In this study we report Si etch results using the

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HARSE deep etch process as a function of pressure, cathode rf-power, and ICP source power. These results are compared to Si etch results obtained in a SF_6/O_2-based ICP plasma at -40°C.

EXPERIMENTAL

Si wafers were patterned with AZ-4330 photoresist which was spun on to a thickness of ~3.4 µm. The Si etch results were obtained in a load-locked Plasma-Therm SLR 770 ICP etch system with a Plasma-Therm 2 MHz ICP source. Ion bombardment energies were modified by superimposing a rf-bias (13.56 MHz) on the sample. Samples were mounted with a low vapor pressure thermal paste on a 6 inch Si wafer carrier which was coated with ~ 2 µm of thermal SiO_2 to minimize loading of the etch process. The Si wafer carrier was clamped to the cathode and cooled to 20°C with He gas. Etch gases were introduced through an annular region at the top of the chamber. Si etch rates were calculated from the depth of the etched feature measured with an Alpha Step stylus profilometer following removal of the photoresist. The etch rates represent maximum values for the given set of plasma conditions since they were calculated for 10 minute plasma exposures and were measured on 20 µm diameter features. Since the aspect ratios for these features were < 2:1, transport of reactants to the etch area and etch products from the etch area were not an issue but will be for larger aspect ratios. Each sample was approximately 1 cm^2 and depth measurements were taken at a minimum of three positions. Selectivities were reported as the ratio of Si etch rate to resist erosion rate. The resist erosion rate was calculated from the depth of the resist measured with the profilometer before and after exposure to the plasma relative to the depth of the Si removed during the etch. Etch profile, surface, and sidewall morphology were evaluated with a scanning electron microscope (SEM).

RESULTS AND DISCUSSION

Figure 1 shows a schematic diagram of a Si substrate which could be used as an "optical bench" for mixed technology integration and packaging. For example, a feature could be etched into the Si which could be used as a "device locator" to accurately position a hybrid device such as an edge-emitting laser or a vertical cavity surface emitting laser (VCSEL) onto the Si carrier. Using a second photolithography step, a trench could be etched into the Si to a precise depth and location relative to the laser in order to passively align a fiber optic. Additionally, through-wafer via holes could be etched for use as either optical or electrical interconnects to frontside controlling and/or drive circuitry. The HARSE process could also be used to accurately align two Si wafers to one another for either packaging purposes or to integrate components on two different wafers. Using a series of alignment pins and holes, 2 wafers could be aligned with enough precision to enable interwafer die passive self-alignment.

Several of these concepts are demonstrated in Figure 2 where a SEM micrograph shows Si features etched simultaneously to a depth of ~250 µm. In Figure 2a the central square or "device locator" could be used to accurately position a hybrid structure while the trench features could be used for either electrical interconnects or extended to the edge of the wafer for a fiber optic. In Figures 2b and 2c high magnification SEM micrographs show the high anisotropy, and smooth etch morphology of the sidewalls and the field. Vertical striations were observed in the sidewalls possibly due to striations in the

photoresist mask which were transferred into the Si during the etch. It is also important to notice there is no sign of a foot or a fillet at the interface of the etched sidewall and field.

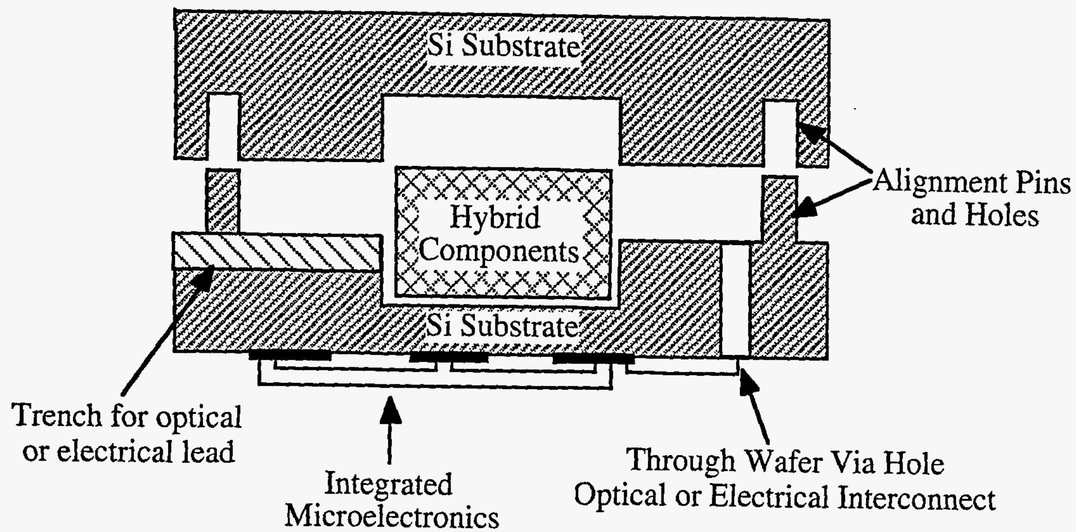
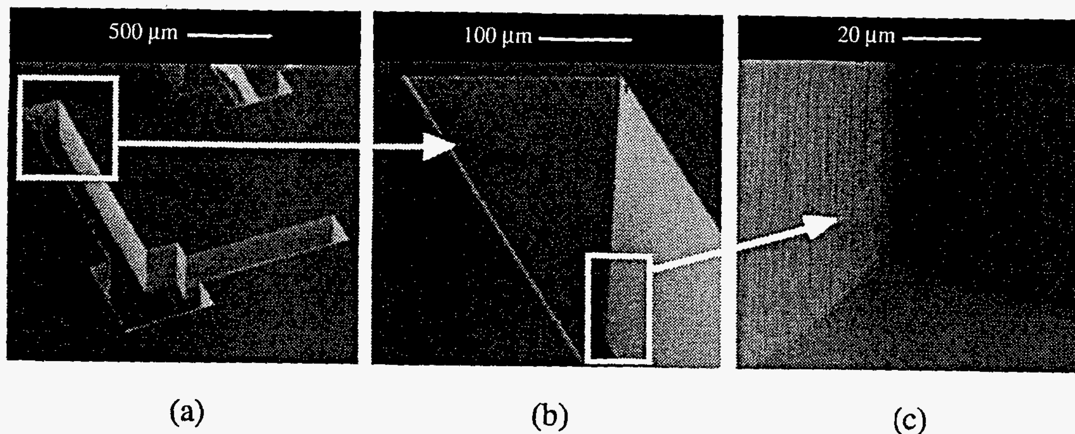


Figure 1: Schematic diagram of optical bench for III-V hybrid components. The HARSE process could be used to etch "device locators", alignment pins and holes, trenches, and vias.



(a) (b) (c)

Figure 2: SEM micrograph of a device locator feature and 2 trenches for electrical or optical leads.

In order to achieve highly accurate positioning for passive self-alignment, etch parameters were studied as a function of chamber pressure, cathode rf-power, and ICP source power. In Figure 3, Si etch rates and etch selectivity of Si to photoresist are shown as a function of pressure while the cathode rf-power, ICP source power, and gas flows were held constant. Plasma conditions change quite dramatically as a function of pressure, in particular the mean free path decreases, the dark space decreases, and the collisional frequency increases as the pressure is increased. This typically results in changes in both ion energy and plasma density which strongly influences the etch properties. Si etch rates

increased with the pressure suggesting a reactant limited regime at lower pressures. Selectivity of Si to photoresist reached a maximum of ~95:1 at 25 mTorr. Such high etch selectivity relative to resist enables deep Si etching (often > 600 μm) with high-aspect ratios.

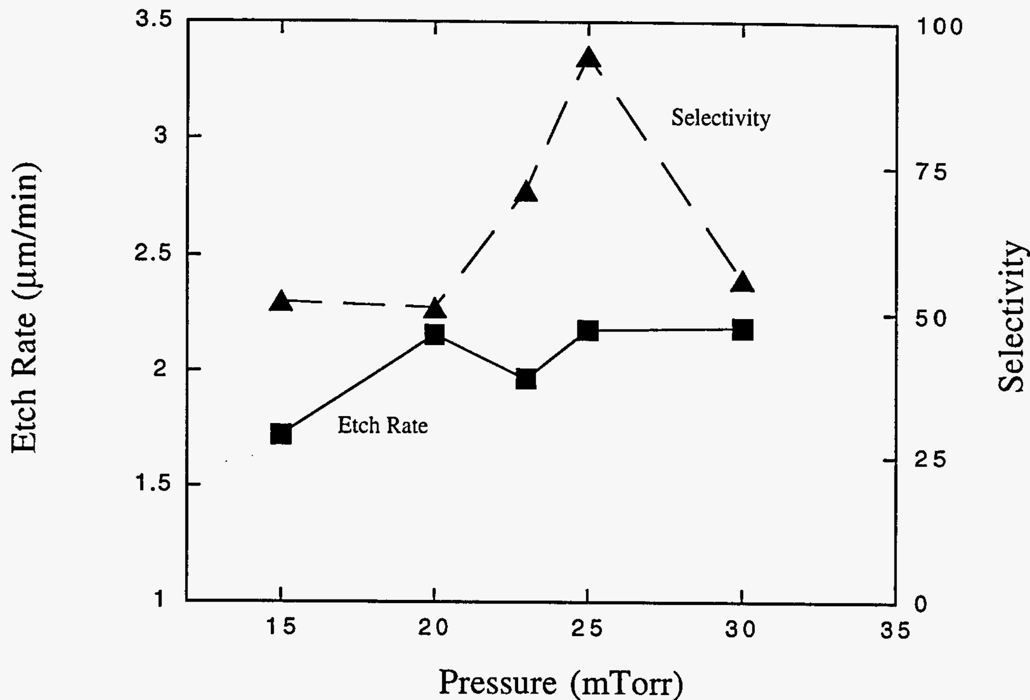


Figure 3: Si etch rates and etch selectivity of Si to photoresist as a function of pressure in the HARSE process.

Etch characteristics normally show a strong dependence on ion energy and plasma density. Ion energies influence the physical component of the etch whereas plasma density can effect both the physical and chemical components of the process. In Figure 4, Si etch rates and etch selectivity of Si to photoresist are plotted as a function of cathode rf-power while all other plasma parameters are held constant. Si etch rates increased monotonically by almost a factor of 3 as the rf-power increased. Since cathode rf-power is closely related to dc-bias and ion bombardment energy, higher etch rates at higher ion energies implies improved sputter desorption of etch products from the surface and/or more efficient bond breaking of the Si surface molecules. As the ion bombardment energy increases so does the sputtering efficiency of the polymer in the Si field area which is deposited during the deposition cycle of the HARSE process. Under low ion energy conditions, the polymer may not sputter as efficiently thereby increasing the etch initiation time of the HARSE process and reducing the Si etch rates. Despite faster Si etch rates, the etch selectivity decreased quite dramatically as the rf-power increased due to higher effective sputtering of both the polymer and the resist.

Although faster etch rates were observed under high cathode rf-power plasma conditions, the etch profile became re-entrant. In Figure 5, SEM micrographs show Si etched at (a) 8 and (b) 25 W cathode rf-power. At 8W, the etch profile was highly anisotropic and the etch depth was ~ 23 µm. At 25 W, the etch depth was ~30 µm and a prominent re-entrant profile was observed. At higher rf-power the re-entrant etch profile was possibly due to sputter removal of the sidewall polymer etch inhibitor at higher ion energies which resulted in lateral etching of the Si.

As a function of increasing plasma density or ICP source power, etch rates typically increase due to 1) higher concentrations of reactive species which increase the chemical component of the etch mechanism and 2) higher ion flux which increases the sputter desorption component of the etch mechanism. The effects of ion energies and plasma densities are more obvious for high density plasma systems, since ion energies and plasma densities can be more effectively decoupled as compared to RIE. In Figure 6, the Si etch rates increased by ~30% as the ICP source power increased. The etch selectivity data was less constant ranging from ~55:1 to 90:1. The low selectivity observed at 800 W ICP source power is not fully understood.

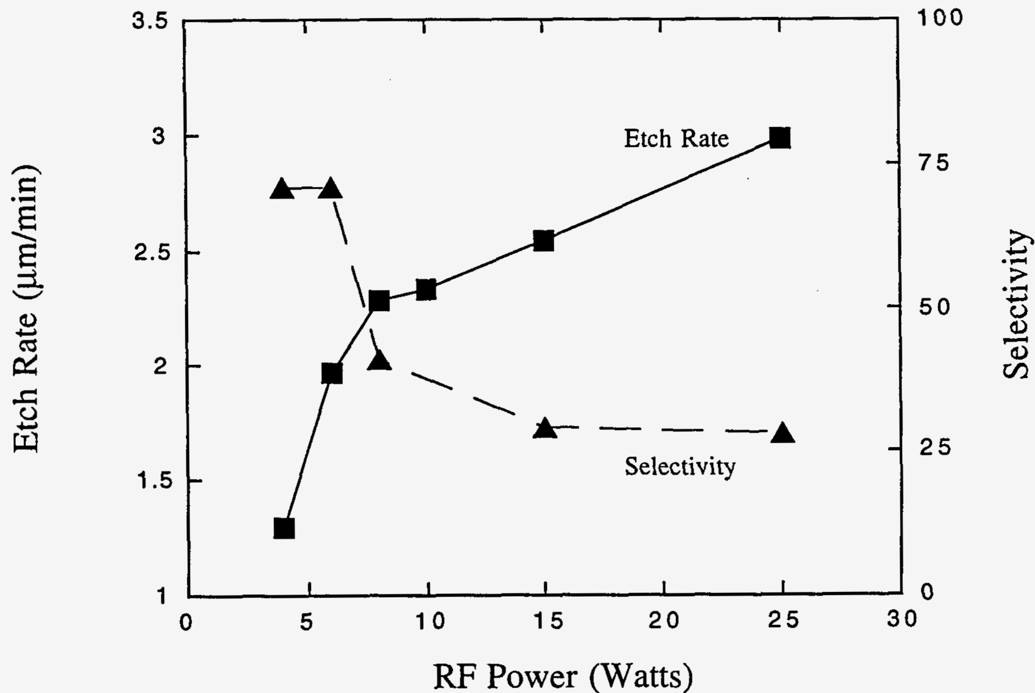


Figure 4: Si etch rates and etch selectivity of Si to photoresist as a function of cathode rf-power for the HARSE process.

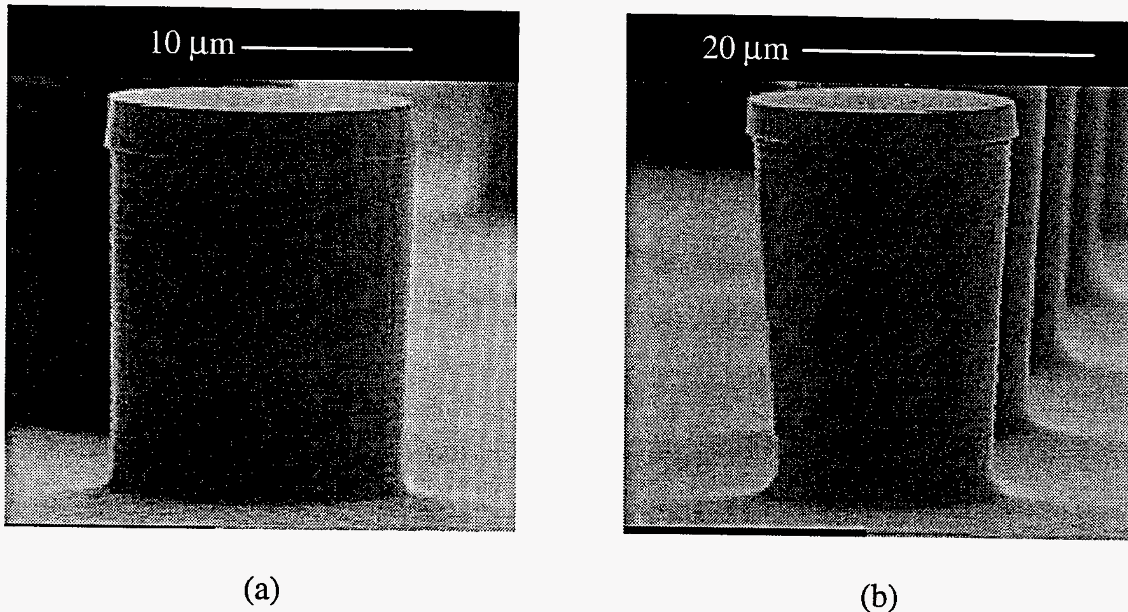


Figure 5: Si etched at (a) 8W and (b) 25 W cathode rf-power.

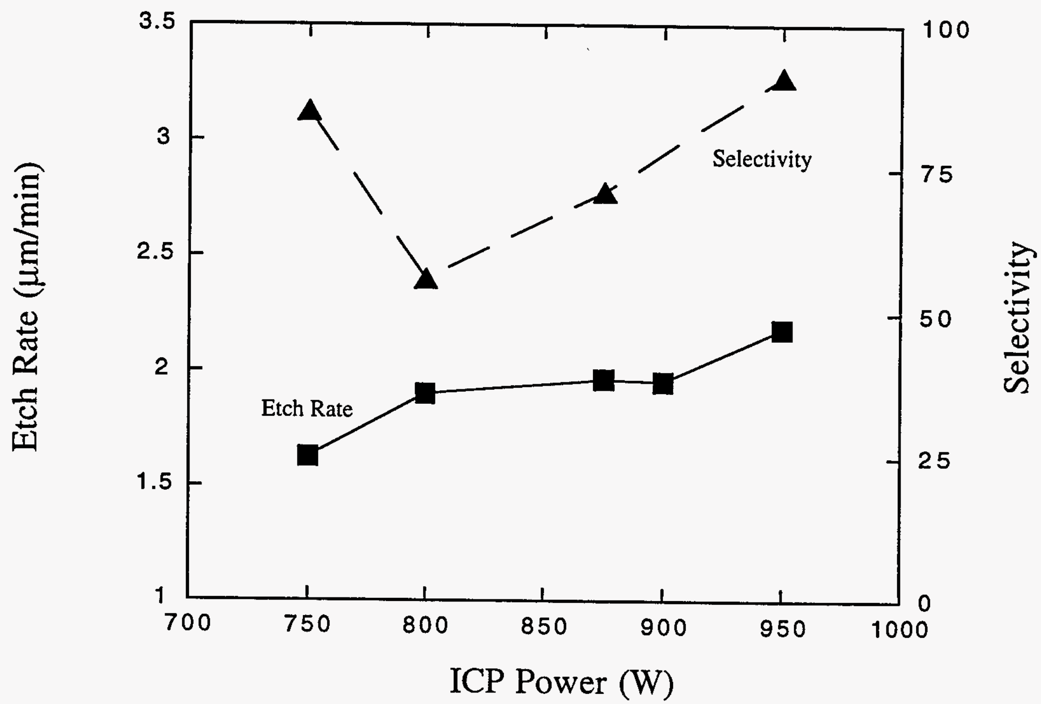
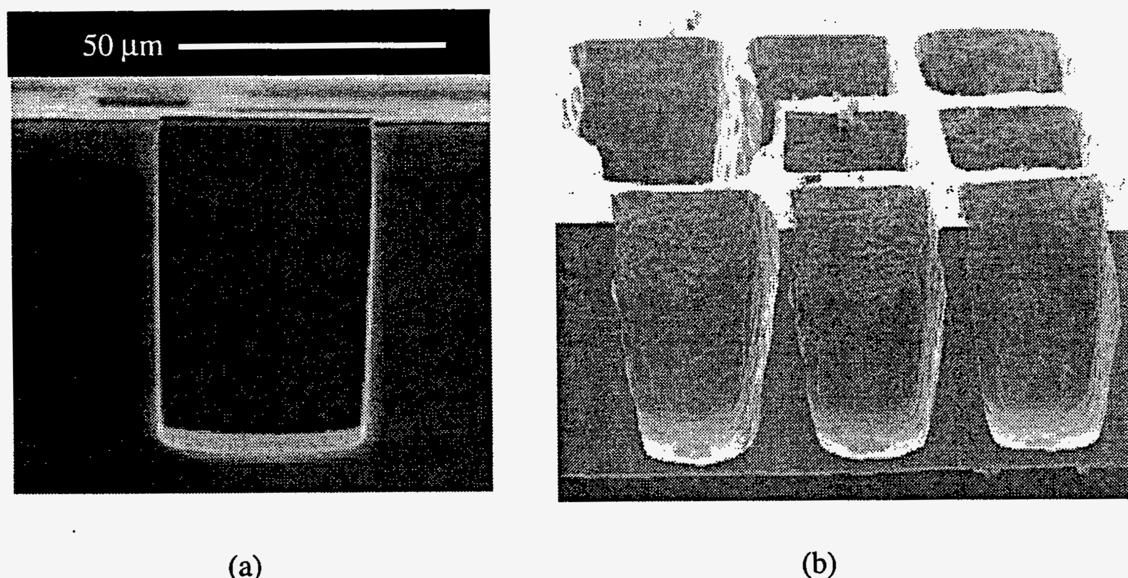


Figure 6: Si etch rates and etch selectivity of Si to photoresist as a function of ICP source-power for the HARSE process.

In Figure 7, SEM micrographs show Si vias etched by (a) the HARSE process and (b) an ICP-generated SF_6/O_2 plasma. The via etched using the HARSE process was ~ 40 µm wide and etched to a depth of ~65 µm while the vias etched in the ICP were 50 µm wide and etched to a depth of ~150 µm. The ICP etch conditions were 5 mTorr pressure, 50 sccm SF_6, 10 sccm O_2, 10 sccm Ar, 500 W ICP source power, 250 W cathode rf-power with a corresponding dc-bias of -350 V, and -40°C substrate temperature. Etch selectivity of Si to photoresist in the ICP was typically ≤ 2:1, therefore a hard Ni mask was used to achieve the deep etched features. The ICP etch rate was ~1 µm/min. The HARSE process used a photoresist mask due to etch selectivities > 75:1 and low dc-biases (~ -35 V). The high etch selectivity observed in the HARSE process may be attributed to the deposition of the sidewall inhibitor polymer which also deposits on the resist. Despite ion bombardment of the surface, the deposited polymer enhances the integrity of the resist and reduces the erosion rate significantly. Additionally, lower dc-biases in the HARSE process (≤ -50 V compared to -350 V in the ICP) significantly reduces the resist erosion rate. The HARSE process yielded an etch rate of ~1.9 µm/min, highly anisotropic etch profiles, and smooth etch morphologies. The via etch profile obtained in the ICP was poorly controlled with a concave sidewall profile and a much wider opening at the top of the via than that obtained at the bottom of the via. Additionally, the sidewall morphology was much rougher than that obtained with the HARSE process. The isotropic nature of the ICP etch is somewhat surprising under the low temperature (-40°C) conditions used. Low temperature Si etching is believed to improve the etch anisotropy by passivating the sidewalls and minimizing the lateral etch rate.

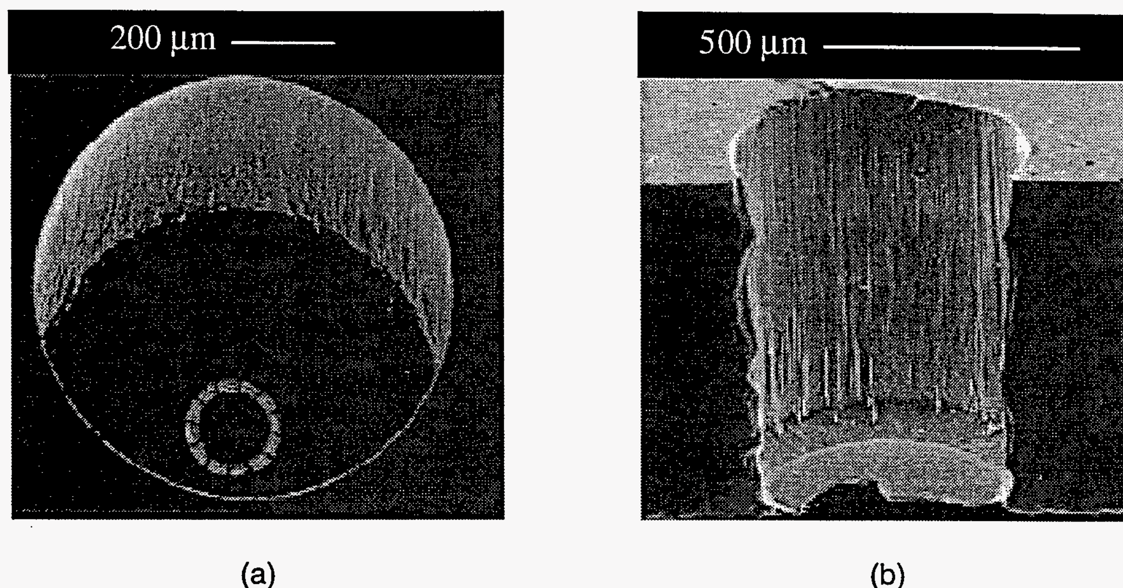


(a) (b)

Figure 7: SEM micrograph of Si vias etched (a) by the HARSE process for a 40 µm wide via etched to a depth of ~65 µm and (b) by ICP for a 50 µm wide via etched to a depth of ~ 150 µm.

In Figure 8, the versatility of the HARSE process is further illustrated by the SEM micrograph of a Si via etched to a depth of ~685 µm at a rate of ~3.5 µm/min. The patterned via was ~400 µm wide and the etch stopped on a 2 µm thick thermal SiO_2 layer. The etch selectivity of Si to thermal SiO_2 was estimated to be > 100:1. The via was highly anisotropic and maintained the dimension of the mask, however the sidewall morphology

was somewhat rough due to vertical striations and a slight Si fillet was observed at the base of the sidewall. The features observed at the bottom of the via in Figure 8b were frontside metal features which could be seen through the transparent thermal SiO_2 film.



(a) (b)

Figure 8: SEM micrographs of a Si via HARSE etched to a depth of ~685 μm to a thin thermal SiO_2 layer which acts as an etch stop due to an etch selectivity > 100:1. The via diameter is ~400 μm.

CONCLUSIONS

Etch rates ranging from 1 to 3.5 μm/min with highly anisotropic profiles and smooth etch morphologies were demonstrated for several HARSE process conditions. Si etch rates and profiles were strongly dependent on cathode rf-power. As the ion energy increased, the etch rate increased and the etch profile became more re-entrant. The re-entrant etch profile was possibly due to sputter removal of the sidewall polymer etch inhibitor. Si etch characteristics were much less dependent on chamber pressure and ICP source power. The HARSE process operated at room temperature and did not require hard photomasks due to the high etch selectivity to resist (> 75:1). In comparison to ICP SF_6/O_2 etching, the HARSE process yielded more anisotropic etch profiles, higher selectivity to resist, and faster Si etch rates at lower dc-biases. The HARSE process is expected to enable "mixed technology" integration and packaging for passive self-alignment of dissimilar materials and devices on Si carriers or waferboards.

ACKNOWLEDGMENTS

Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy under Contract DE-AC04-94AL85000.

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KEYWORDS

High-aspect ratio Si etching (HARSE)
Si vias
Inductively coupled plasma
Optical bench

M98003344

Report Number (14) SAND--98-0608C
CONF-980504--

Publ. Date (11) 199805

Sponsor Code (18) DOE/CR, XF

UC Category (19) UC-900, DOE/ER

DOE