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49191-00-105

CONF-960850--23
ANL/MSD/CP--92825

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**Proceedings of the 1996 Applied Superconductivity Conference, Pittsburgh, PA, August 25-30, 1996, to be published by IEEE Trans. on Superconductivity.**

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Work supported in part by AFOSR Contract F49620-94-C-0021, USAF WL/ML Contract No. F33615-93-C-5355, and ONR Contract N00014-96-C-0007; at Argonne by the U.S. Department of Energy, BES-Materials Sciences under contract #W-31-109-ENG-38; and by the National Science Foundation Office of Science and Technology Centers for Superconductivity under contract #DMR 91-20000.

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# Materials Basis for a Six-Level Epitaxial HTS Digital Circuit Process

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*Abstract* — **We have developed a process for fabrication of HTS single-flux-quantum logic circuits based on edge SNS junctions which requires six epitaxial film layers and six mask levels. The process was successfully applied to fabrication of small-scale circuits (≤ 10 junctions). This paper examines the materials properties affecting the reproducibility of YBCO-based SNS junctions, the low inductance provided by an integrated YBCO ground plane, and electrical isolation by $SrTiO_3$ or $Sr_2AlTaO_6$ ground-plane and junction insulator layers. Some of the critical processing parameters identified by electrical measurements, TEM, SEM, and AFM were control of second-phase precipitates in YBCO, oxygen diffusion, Ar ion-milling parameters, and preparation of surfaces for subsequent high-temperature depositions.**

## INTRODUCTION

Practical application of Single Flux Quantum (SFQ) logic circuits fabricated in High-$T_c$ Superconductors (HTS) is limited at present by a low level of integration of Josephson junctions with sufficiently uniform characteristics. SFQ gates must have a low inductance, L, consistent with a quantum of flux, $LI_c \sim \Phi_o = 2$ mA-pH, and a Josephson critical current, $I_c$, on the order of 0.5 mA for thermal noise stability. Two approaches for achieving such low inductances are to use an integrated thin-film HTS groundplane or to use submicron lithography. We chose to follow the former approach in the process described here.

The requirements for junction reproducibility are shown in Fig. 1 following the discussion in [1]. Reproducibility is expressed as the standard deviation of Josephson critical currents, $I_c$. The calculation of junction count for a particular level of junction reproducibility assumes a Gaussian distribution of critical currents, and circuit component margins of 30%, which have been shown to be realistic in both simulations and LTS circuit measurements for SFQ circuits. Since there is always some chance with a Gaussian distribution that a junction's $I_c$ will fall outside of circuit margins, circuit yield is expected to be < 100% even for small-scale circuits with low junction counts.

Manuscript received August 27, 1996.
This work was supported in part by AFOSR Contract F49620-94-C-0021, USAF WL/ML Contract No. F33615-93-C-5355, and ONR Contract N00014-96-C-0007. Work at Argonne was supported by the U.S. DOE Office of Basic Energy Sciences (#W-31-109-ENG-38) and the National Science Foundation Office of Science and Technology Centers (DMR 91-20000).

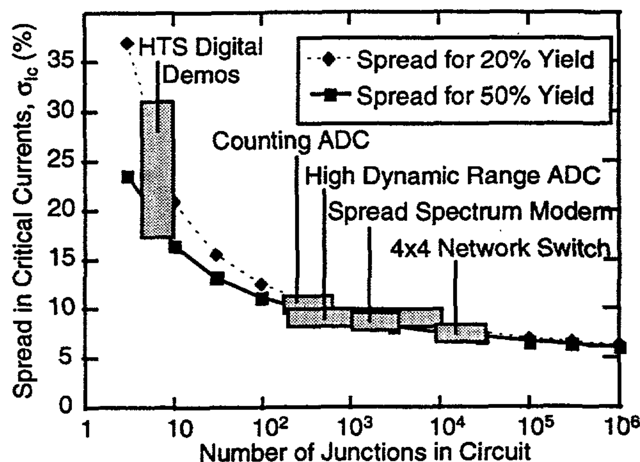


Fig. 1. The spread in junction critical currents, $\sigma_{Ic}$, required to produce circuits with a given junction count. Small-scale circuit demonstrations made to date are consistent with relatively large spreads in $I_c$ of 20-30%. To fabricate SFQ circuits of practical interest with hundreds to thousands of junctions and reasonable yields, $I_c$ spreads must be reduced to ≤ 10%.

Fig. 1 shows that one should expect no more than the small-scale SFQ circuit demonstrations made to date as long as $\sigma_{Ic}$ = 20-30%. To fabricate circuits of practical interest with hundreds to thousands of junctions and reasonable yields, $I_c$ spreads must be reduced to ≤ 10% while still satisfying the requirement for $LI_c \sim \Phi_o$.

Details are published elsewhere of junction electrical properties and some process issues [2-3], inductance measurements [4], and one of the circuits fabricated with this process [5]. The emphasis of this paper is in showing how the materials properties needed for groundplane integration and improved junction reproducibility are affected by the details of our integrated circuit fabrication process. Although the number of essential film layers is exactly the same, it is important to distinguish the multilayer film process for HTS digital circuits described here from that needed for integrating magnetometer pick-up coils with SQUIDs as in [6]. In the case of magnetometers, there is a minimal overlap of YBCO film layers which occurs only at crossovers. Junctions are fabricated directly on the substrate.

## INTEGRATED CIRCUIT FABRICATION PROCESS

Major process steps we followed to integrate edge SNS junctions on an HTS groundplane are shown in Fig. 2. A minimum of six mask levels and six epitaxial oxide film

layers are needed for this process. Two additional epitaxial film layers were sometimes used, a 300 Å $SrTiO_3$ (STO) buffer layer between the substrate and groundplane, and a 300 Å STO cap layer deposited on top of the groundplane to protect the YBCO surface during processing. Since neither the presence or absence of these layers affected the sequence of process steps, we omitted them from the schematic cross sections of multilayers. Next we will describe each of the six steps shown in Fig. 2 in detail.

*1. Groundplane Deposition and Patterning*

YBCO groundplane films 2250 Å thick were deposited by 90° off-axis rf magnetron sputtering with a process described in [7]. In all cases, $NdGaO_3(110)$ substrates were used. In some cases, 2-inch diameter wafers were used which were diced into 1 cm × 1 cm chips at some point before circuit fabrication was completed so deposition parameters for the junction films could be varied while keeping groundplane fabrication parameters constant.

Fig. 3 shows the mask layout for (3a) a wafer, (3b) a chip, and (3c) a standard junction test subchip. The dark band on the subchip is the base electrode with two wire bond pads. The rest of the bonding pads are connected in pairs to the top electrodes of 20 devices. The edge SNS devices face in all four in-plane directions since this is a constraint imposed by the need for low-inductance connections in SFQ circuits. Junctions are spread out across each subchip to give a more complete measurement of junction uniformity.

Film patterning was done with photoresist masks reflowed for 5 min at 130°C. Wafers were tilted 50° from normal and rotated during 150 eV Ar ion milling to produce edges that angled 20-30° from the substrate plane. The same process was used to pattern single or multiple layers. SIMS endpoint detection prevented over-milling.

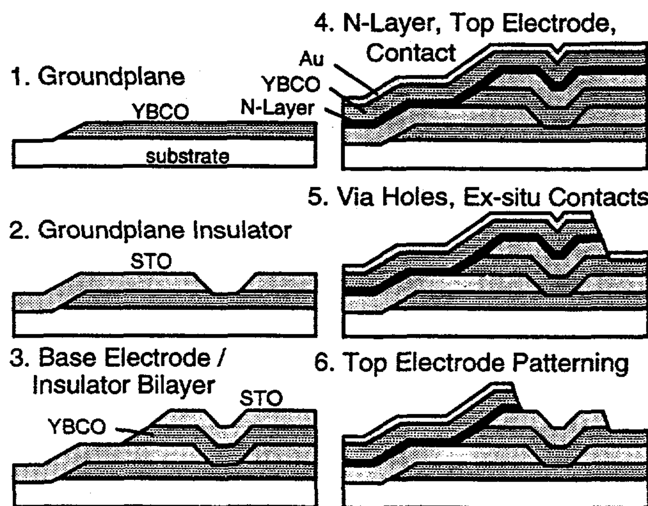


Fig. 2. The major process steps for fabrication of SFQ circuits with SNS junctions integrated on grounplanes for low inductance. The effect of each step on materials properties critical for groundplane integration and junction reproducibility are described in the text.

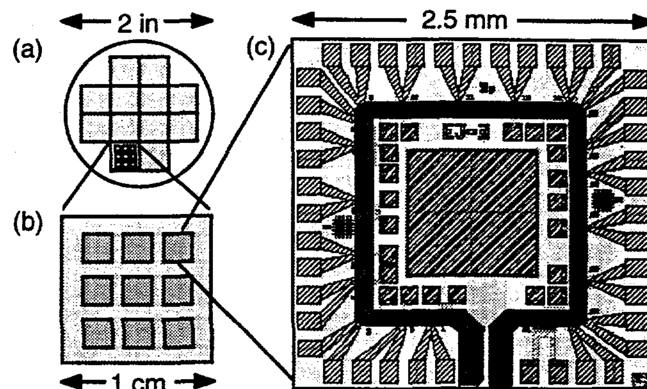


Fig. 3. YBCO groundplanes were deposited and patterned on 2-inch wafers (a) which were diced into 1 cm × 1 cm chips (b) for deposition of subsequent layers. Each chip had nine subchips where (c) was one of our standard patterns for measurement of twenty 3-μm-wide devices.

*2. Groundplane Insulator Deposition and Patterning*

Before we brought any patterned wafer up to ~700°C for deposition of a subsequent epitaxial layer, we cleaned the surface with an *ex-situ* oxygen plasma and a 150 eV $Ar/O_2$ ion mill to remove ~100 Å from the surface. XPS studies were used to ensure that hydrocarbon and fluorine residues were completely removed by the time the sample was brought to the desired deposition temperature [8].

Both $SrTiO_3$ and $Sr_2AlTaO_6$ (SAT) grown by off-axis sputtering were developed for epitaxial insulator films. Groundplane insulators were nominally 2400 Å thick but films used for insulator development varied in thickness between 1000 Å and 3000 Å without apparent thickness dependence. The important properties for the groundplane insulator were good electrical isolation and vias to ground capable of carrying currents greater than the junction critical currents (Fig. 2b).

A series of experiments were performed to determine which process parameters had the greatest effect on whether a minimum electrical isolation of $2 \times 10^4$ Ω-cm was achieved in YBCO/insulator/YBCO trilayer capacitors. We found that the insulator growth temperature in the range of 660-750°C, whether the layers were deposited without breaking vacuum, interfaces exposed to air, or interfaces exposed to ion-mill processing, were not significant factors. We also found that room temperature measurements were good predictors of isolation at 77K.

However, roughness of the first YBCO layer was found to be the key factor in determining electrical isolation. Fig. 4 shows the defect density in insulators inferred from the fraction of 35 capacitors per chip ranging in area from 1 mm × 1 mm to 250 μm × 250 μm. In [9], the defect density, D, is calculated from the "yield," the fraction of capacitors exceeding the minimum resistivity criterion, based on,

$$\text{yield} = (\#\ \text{working}) / (\#\ \text{tested}) = \exp(-D / \text{Area}) \qquad (1)$$

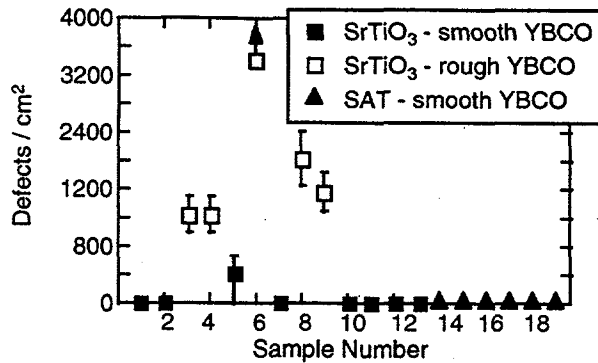


Fig. 4. Defect density for a series of 19 samples with 35 YBCO / SAT or STO / YBCO trilayer capacitors on each. Samples labeled as "smooth" had $\leq 10^3$ copper oxide precipitates per $cm^2$ in the lower YBCO film and, for all but one sample, no measured electrical defects.

Since we used two capacitors in series to measure yield, D was determined from,

$$\text{yield} = 1 - (1 - \exp(-D / \text{Area}))^2 \quad (2)$$

The data in Fig. 4 are for a numbered series of samples with STO deposited on either rough or smooth YBCO base layers and SAT deposited on smooth YBCO. Error bars were based on potential changes in the yield by ±1 capacitor. For smooth films, only one leaky capacitor was found in 14 samples with a total of 490 capacitors. Nearly all of the capacitors exceeded the resistivity criterion by 4 or 5 orders of magnitude.

The definition of "rough" and "smooth" films in this case was based on the density of copper oxide precipitates which can be clearly seen, identified, and counted in an SEM. Smooth films had a density of $\leq 10^3/cm^2$ such "boulders," whereas rough films typically had $10^5$-$10^6/cm^2$.

A cross-sectional TEM image of a YBCO edge SNS junction without a ground plane is shown in Fig. 5 to show the contrast between relatively smooth film layers, with rms roughness as low as 10-15 Å, and copper oxide boulders which disrupt insulator growth if they nucleate in one of the lower YBCO film layers.

Results of measurements of SAT and STO dielectric constants are shown in Figs. 6(a) and (b), respectively. Both data sets were independent of frequency in the measurement range up to 10 kHz. For SAT, $\varepsilon(77K) \cong 26$ is in good agreement with SAT films grown by pulsed laser deposition [10], but is significantly higher than for bulk samples where $\varepsilon(90K) = 11.8$ [11]. For STO, $\varepsilon(300K)$ is in reasonable agreement with bulk samples but our STO films showed much less dependence on temperature than expected from bulk. Although we have made no direct measurements of dielectric loss, the anomalous behavior of STO films compared with bulk appears to be favorable since average voltage measurements of toggle flip-flips fabricated with STO groundplane and junction insulators indicated that they operated up to 15 GHz [12].

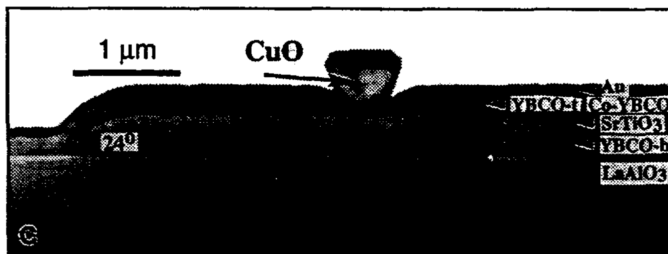


Fig. 5. Cross-sectional TEM image of an edge SNS junction without a ground plane showing the contrast between relatively smooth film layers and the potential for copper oxide "boulders" to disrupt multilayer structures. In this case, the boulder nucleated in the YBCO counterelectrode so it only disrupted the Au contact layer.

*3. Base Electrode / Junction Insulator Formation*

A YBCO base electrode 2250 Å thick and a junction insulator 1500 Å thick were sputter-deposited and patterned to form the structure shown in Fig. 2(c). The edge patterned at this step deserves special consideration since it formed one interface of SNS junctions. In addition to the *ex-situ* ion-mill cleaning described earlier, this edge was subjected to an *in-situ* 100 eV Ar ion mill to remove a few monolayers just before deposition of the normal-conducting, "N-layer."

*4. N-Layer and Counterelectrode Processing*

Results in [13] and [14] showed that the N-layer in SNS junctions which had the closest structural match to YBCO

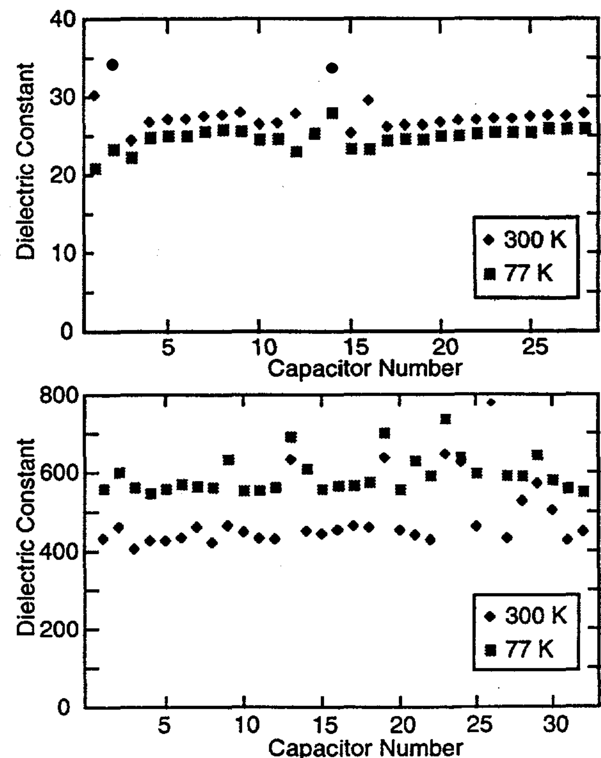


Fig. 6. Dielectric constants for (a) SAT and (b) STO epitaxial thin films deposited on YBCO. In comparison with bulk dielectrics, the most significant difference is the weak temperature dependence of STO.

led to junction characteristics which could best be explained by the standard model of proximity effects at S-N interfaces. Fig. 7 summarizes the dependence of junction critical current density, $J_c$, on N-layer thickness for three different N-layers based on doping YBCO with sufficient cobalt, calcium, and praseodymium, respectively, to reduce $T_c$ to ~50K. For these N-layer evaluation experiments, we did not use a ground plane or rotate the samples during ion milling so all junction edges face the same direction.

Each data point in Fig. 7 represents the average $J_c$ for all junctions on a chip and the error bars indicate the $J_c$ spread. The normal-state coherence lengths, $\xi_n(77K)$, calculated

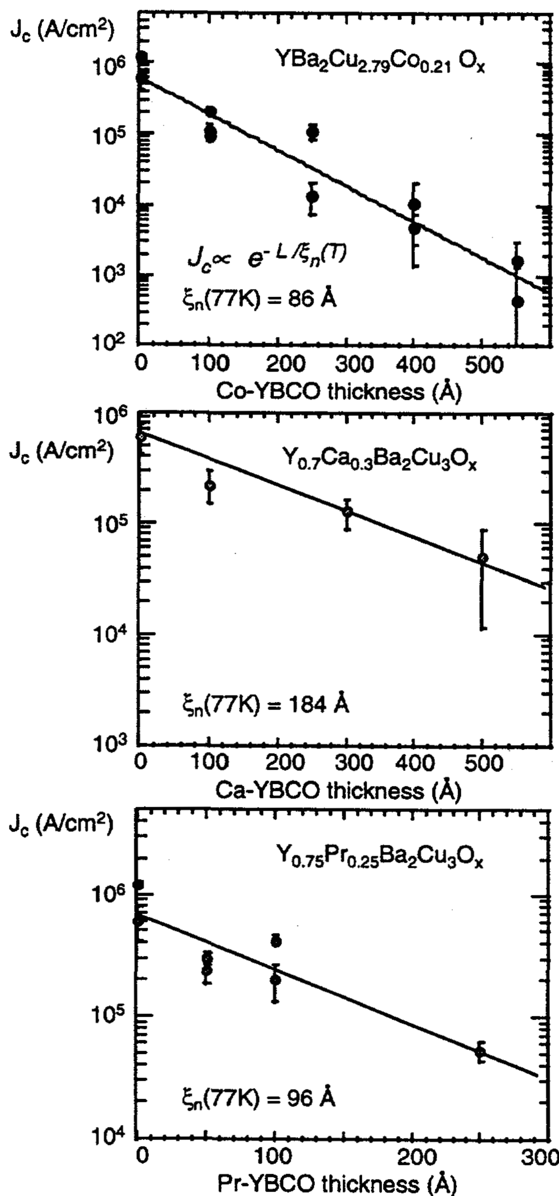


Fig. 7. Junction critical current density, $J_c$, plotted as a function of N-layer thickness for Co, Ca, and Pr-doped YBCO N-layers. Each data point represents the average $J_c$ for all junctions on a chip and the error bars indicate the $J_c$ spread. The exponential dependence of $J_c$ on N-layer thickness shows the extent of our control over S-N interfaces and N-layer film growth.

from the slope of the lines drawn in Fig. 7 are larger than expected from resistivites, $\rho(77K)$, that varied from low values of 60-100 μΩ-cm for Ca-YBCO to high values of 300-600 μΩ-cm for Co-YBCO. However, the fact that $J_c$ was an exponential function of N-layer thickness indicated that both edge formation and N-layer film growth on tapered edges were controlled processes.

High $I_cR_n$ products for Co-YBCO junctions, 160-180 μV at 77K and ~500 μV at 65K, led us to focus on Co-YBCO. The Pr-YBCO junctions had $I_cR_n$ products that were just marginally lower but $I_cR_n$ for the Ca-YBCO junctions was a factor of 4 lower.

As shown schematically in Fig. 2(d), the selected N-layers, typically 75-200 Å thick, YBCO top electrodes 2000 Å thick, and 1000 Å Au contact layers were deposited sequentially without breaking vacuum. Although this process was originally developed using rf sputtering, indications of inhomogeneity in sputtered Co-YBCO encouraged us to fabricate junctions with N-layers, and necessarily, top YBCO electrodes, grown by pulsed laser deposition (PLD). Fig. 8 shows the differences in typical $\rho(T)$ curves for sputtered and PLD Co(7%)-YBCO where the higher $T_c$, broader transition, and higher $\rho(T)$ for the sputtered film were interpreted as signs of inhomogeneity. So far, the properties of our PLD junctions were not grossly different from sputtered junctions but the single chip with the tightest spread in $I_c$ was fabricated with PLD.

### *5. Via Holes and Base Electrode Contacts*

Fig. 2(e) shows the circuit structure after a via hole was ion milled to the YBCO base electrode and an *ex-situ* Au contact to the base electrode was patterned by lift-off. Via holes, crossovers, and step coverage were the subjects of a separate study of such passive structures for HTS digital circuits [8]. SEM micrographs of a test via and crossover are shown in Figs. 9(a) and (b), respectively. The most important characterization of these structures were

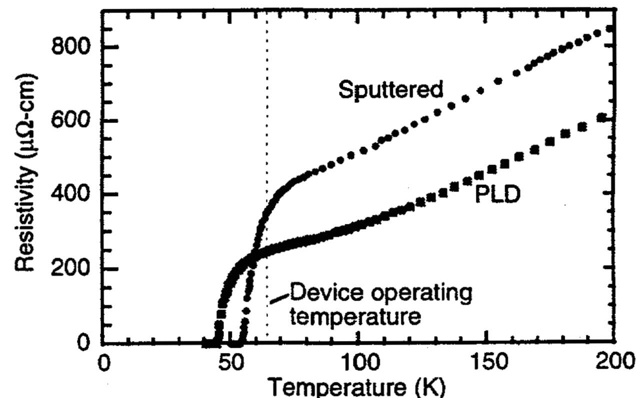


Fig. 8. Resistivity vs. temperature for typical Co-(7%)-YBCO films deposited by sputtering and PLD. Although sputtered films have resulted in junctions with desirable properties, their higher $T_c$, broader transition, and higher $\rho(T)$ were interpreted as signs of inhomogeneity

measurements of electrical isolation (Fig. 4) and measurements of critical currents through vias and for films over steps. We designed vias in our circuits to have a large perimeter for contact compared to junction widths so they were never found to limit $I_c$. Fig. 10 shows that $J_c(T)$ for YBCO films covering 20 steps in either an STO underlayer or STO isolating YBCO cross-unders, was degraded by approximately one order of magnitude but could be kept larger than typical $J_c$s for either SEGB or SNS junctions.

*6. Top Electrode Patterning*

The last mask level was used to pattern the trilayer consisting of the N-layer, top YBCO electrode, and *in-situ* Au contact layer. Typical variations in the morphology of sputtered trilayers are shown in Fig. 11. Junctions for all three pictures had smooth base electrode films. In Fig. 11(a), both the Co-YBCO layer and YBCO top electrode were deposited at a low total sputter pressure of 125 mtorr. Under these conditions, it is relatively easy to avoid formation of copper oxide boulders and a-axis oriented YBCO outgrowths, and to obtain smooth surfaces on planar film regions. However, step coverage was poor as can be seen both in the junction area and in the rough pattern transferred by ion milling along the entire base electrode edge.

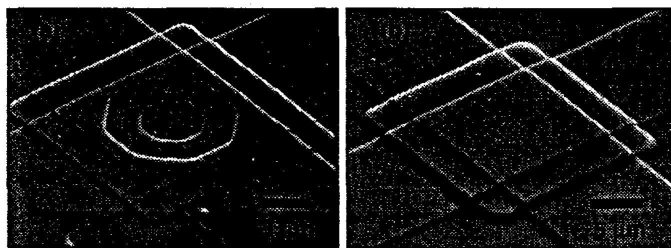

Fig. 9. Scanning electron micrographs of (a) a via hole and (b) a crossover test structure. These passive structures were characterized by measurements of electrical isolation as in Fig. 4, and $J_c$ measurements as in Fig. 10.

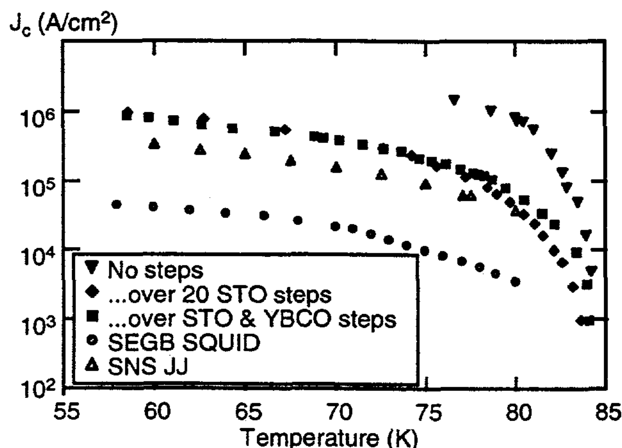


Fig. 10. Critical current density, $J_c(T)$, comparisons for YBCO films showing that coverage over multiple 20-30° steps degrades $J_c$ by approximately an order of magnitude but not enough to cause a problem for SEGB or SNS-based circuits.

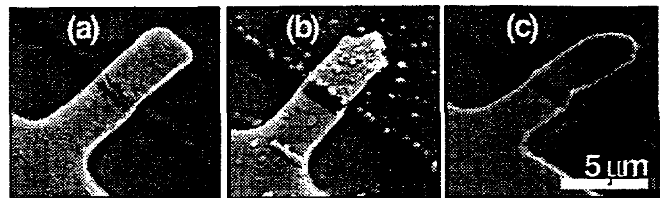


Fig. 11. Junctions 3 µm wide fabricated on smooth YBCO base electrodes. N-layers and YBCO top electrodes grown at low pressure (a) tended to exhibit poor step coverage whereas films grown at high pressure (b and c) were susceptible to boulder formation as in (b).

Figs. 11(b) and (c) show Co-YBCO and YBCO films deposited with the same Ar:$O_2$ ratio of 2:1 as in Fig. 11(a), but with a total pressure of 185 mtorr. In these cases, good step coverage was achieved but both the N-layer and top electrodes were susceptible to boulder formation. We believe that the difficulty in obtaining the film morphology shown in Fig. 11(c) was the greatest contributing factor to spread in junction critical currents.

A cross-sectional TEM micrograph of a junction without a ground plane is shown in Fig. 12. This sample had a 100 Å thick sputtered Co-YBCO N-layer (not distinguishable in the image) and a smooth edge as in Fig. 11(c). Simulations of phase contrast showed that the cobalt-doped layer could only be seen for a few select specimen thicknesses and defocus conditions. Nevertheless, it was observed that the bottom film was nearly free of defects up to the interface while the top electrode had stacking faults in the junction region.

## POSSIBLE ORIGINS OF JUNCTION VARIABILITY

Having established a baseline process for SNS junction and HTS digital circuit fabrication, we examined whether variations in the critical currents of junctions produced in this way were due to fluctuations in the parameters we controlled or due to intrinsic materials properties. In this section, we will present the results of experiments designed

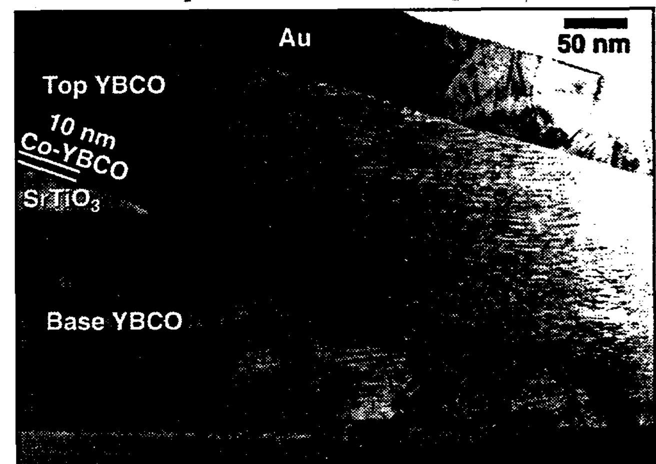


Fig. 12. Cross-sectional TEM micrograph of a junction with Co-YBCO N-layer and a smooth edge as in Fig. 11(c). Since the Co-doped layer could not be distinguished, the only visible defects are stacking faults in the top YBCO film in the vicinity of the junction.

to test whether some intrinsic materials properties of YBCO were limiting junction reproducibility.

We always aligned photomasks so junction edges faced in YBCO <100> in-plane directions. However, some of our 20-device subchips (Fig. 3c) had 4 junctions with edges facing in <110> directions to test whether crystal anisotropy or twinning affected $J_c$ uniformity. Fig. 13 shows $J_c$ data for two such chips with the <110> data highlighted. Typically, YBCO <110> junctions tended to have different $J_c$s than <100> but not consistently larger or more uniform.

To test these ideas further, we fabricated junctions with $Y_{1-x}Ca_xBa_{2-x}La_xCu_3O_y$ (YCBLCO, x = 0.4) tetragonal electrodes. YCBLCO was shown to be highly resistant to corrosion [15], and we measured lower oxygen diffusion rates with in-furnace resistivity measurements at 400-500°C than in undoped YBCO films. I-V characteristics for 10 junctions on one chip fabricated with YCBLCO electrodes are shown in Fig. 14. Junction resistance tended to be high so $I_cR_n$ at 65K was 500 µV even though the electrode $T_c$ was just 78K. Junction $I_c$ uniformity was poor over large areas because these initial sets of YCBLCO films had a $10^5$/cm$^2$ density of CuO boulders.

## Conclusions

The YCBLCO experiment confirms the conclusion stated previously that the most important attribute for integration of junctions with groundplanes and for improved $I_c$ uniformity is to produce smooth multilayer film surfaces. Small-scale circuits could be fabricated and demonstrated with our process because we have some control over this factor. However, experiments designed to determine intrinsic limits to $I_c$ uniformity will not be definitive until this extrinsic factor is completely controlled.

## Acknowledgment

We acknowledge the assistance of J. H. Uphoff, J. C. Brown, J. G. Faychak, G. A. Madia, D. M. Matuza, R. Nye, and S. J. Pieseski, discussions with C. L. Pettiette-Hall, J. M. Murduck, J. Luine, H. Mallison, K. Char, and S. Berkowitz., and long-standing contributions from J. R. Gavaler.

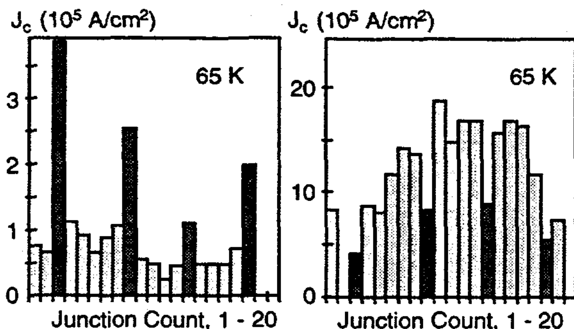


Fig. 13. Junction critical current density vs. junction number for two chips with Co-YBCO N-layers. YBCO <110> junctions (highlighted) tended to have different $J_c$s than <100> but not consistently larger or more uniform.

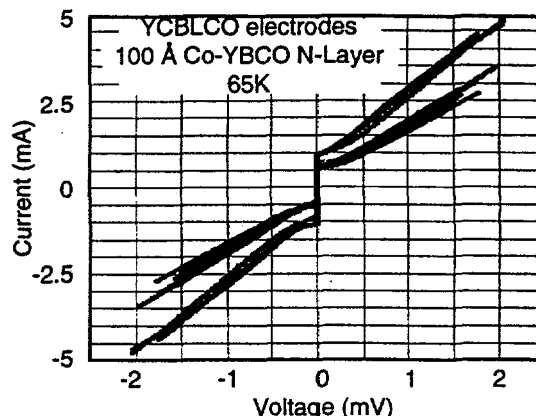


Fig. 14. I-V characteristics for 10 junctions fabricated with YCBLCO electrodes and Co-YBCO N-layers to test the effects of tetragonal structure and lower oxygen mobility.

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