

CONF-970711--1

SAN097-0559C

Radiation Hardness Assurances Categories for COTS Technologies

G. L. Hash, M. R. Shaneyfelt, F. W. Sexton, and P. S. Winokur
Sandia National Laboratories, Albuquerque, NM, 87185-1083

Abstract

A comparison of the radiation tolerance of three commercial, and one radiation hardened SRAM is presented for four radiation environments. Burn-in is shown for the first time to reduce functional failure levels.

RECEIVED

MAR 11 1997

OSTI

MASTER

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

HH
DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.

I. Introduction

In June, 1994, SECDEF Perry issued a directive on acquisition reform whose goal was to reduce costs by buying more commercial product, making greater use of commercial buying practices, and using industrial specifications in place of military specifications. The success of this reform depends on eliminating those government practices and standards that do not add value to products and services purchased by the government, while at the same time controlling risk. In the case of integrated circuits (ICs) that must survive radiation environments, the tradeoff between increased benefit and reduced risk is unclear. The complexity of radiation hard devices usually run a generation or two behind that of commercial; therefore, system designers could implement more sophisticated designs with up-to-date technology and at a reduced cost if commercial-off-the-shelf (COTS) components could be used. However there are significant risks involved when using commercial components. For example, in COTS technologies, processes that affect radiation hardness are not controlled and lot-to-lot variability may cause future lots to have an entirely different radiation response [1].

In Table 1, we have identified three categories of integrated circuits: radiation hardened, radiation tolerant, and COTS. In this classification, a radiation-hardened device is one that is intentionally designed, fabricated, and assembled in a technology and manufacturing line for a specific radiation hardness level. Techniques, such as statistical process control (SPC), are used to control the radiation hardness of the process. This category of device would find use in applications where high radiation levels are expected. The radiation tolerant category of devices are commercial devices that are inherently hard to a specific level of radiation. Here, radiation hardness is a byproduct of the design and/or technology, but is not intentionally built into the product, nor is radiation

hardness controlled using SPC. This category is applicable in low to medium radiation requirements [1]. The COTS category includes devices that are designed and fabricated without regard to radiation hardness and no radiation related SPC is employed. Radiation hardness for this category is typically low and their use is limited to applications with benign radiation requirements. Please note that the specific breakpoints in Table 1 between these categories are for guidance only.

Within each of the above categories one must be certain of the heritage of the devices that were used to establish the reported radiation hardness levels. Research by several groups [2-4] and work described in this paper show that burn-in affects the total dose hardness of devices for some technologies. It has been common practice to perform radiation characterization on devices before burn-in, rather than on more expensive burned-in devices. This can lead to an inaccurate estimate of device radiation hardness.

II. Experimental Details

Devices

In this work we evaluate the radiation hardness of three commercial 256K and one radiation-hard 1M static random access memories (SRAM) in total dose, dose-rate, and single event effects (SEE) environments. We then assign each to one of the above categories based on its radiation response. The first device was manufactured by Paradigm Corporation and is a non-hardened high-performance CMOS SRAM organized as 32K x 8 bits. This product is produced in a 0.8- μm , proprietary bulk CMOS technology. The device operates from a single 5 V power supply and all inputs are fully TTL compatible. The low-current version (PDM41256LA) was evaluated in this work. The test devices were packaged in plastic 28-pin 300-mil surface mount J-leaded (SOJ) packages. A second SRAM from Paradigm (PDM31256L) was also selected for evaluation. This 3.3-V device is functionally equivalent to and the same design as the PDM41256LA. These devices were also packaged in plastic 28-pin 300-mil surface mount J-leaded (SOJ) packages. The 3.3-V devices were fabricated in Japan and the 5-V devices in San Jose, CA.

The third commercial device type evaluated was a Cypress CY7C1399. It is a 3.3-V high performance SRAM which is organized as 32K x 8 bits. This device is fabricated using a 0.5- μm technology with 14.5 nm gate oxide, and bulk (non-epi) p-substrates. The devices

Table 1. Radiation Levels for COTS Categories

Rad-Hardened	Rad Tolerant	COTS
Total Dose 100k to 1 Mrad	20 to 100 krad	< 20 krad
Transient Rad. > 10^9 rad/s	10^7 to 10^9	< 10^7
Latchup not allowed or low risk	Customer evaluation and risk	Customer evaluation and risk
SEE > 80 MeV- cm^2/mg	20-80 MeV- cm^2/mg	< 20 MeV- cm^2/mg

studied in this work were packaged in 300-mil 28-pin dual-in-line (DIP) ceramic packages.

Finally a radiation hardened SRAM manufactured by Lockheed Martin Federal Systems was selected. The LOR1M8C1399 is organized as 128K x 8 bits and is fabricated using Lockheed Martin's 0.5- μ m, 12-nm gate oxide, epitaxial radiation-hardened CMOS process (HMCOS) [5]. Polysilicon cross-coupling resistors are used to provide single event upset (SEU) hardness. The device is specified to be immune to latchup, survive a dose rate $> 1 \times 10^{12}$ rad(Si)/s, exhibit no dose-rate upset below 1×10^9 rad(Si)/s, withstand total doses $> 1 \times 10^6$ rad(SiO₂), and have an SEU rate $< 1 \times 10^{-10}$ errors/bit-day. The test device was a 3.3-V version packaged in 40-pin ceramic flatpack packages.

Electrical Characterization

Electrical characterization of the test devices at all facilities was performed with an HP82000 D50 digital ASIC tester. Functional tests were performed using checkerboard, checkerboard-not, all ones, and all zeros test patterns. Parametric characterization, including I_{DD} , t_{AVQV} , V_{ob} , V_{ih} , was performed before and after all irradiations at room temperature. In this summary, we show functional failure data only. Parametric data will be shown in the full paper.

Irradiations

Co⁶⁰ irradiations were performed using a Gammacell 220 irradiator at Sandia National Laboratories at a fixed dose-rate of ~ 90 rad(Si)/s. Testing was performed in accordance with MIL-STD 883D, Method 1019.4 procedures. A rebound test was performed on all devices and results will be presented in the full paper. A physical checkerboard pattern was stored in the SRAM prior to irradiation. Devices were biased at their nominal V_{DD} during irradiation.

Prompt total integrated dose (TID), dose-rate upset, and dose-rate latchup characterization were performed on a 10 MeV Linear Accelerator (LINAC) located at the Boeing Aerospace Corporation Physical Sciences Laboratory, Seattle, Washington. The LINAC produced dose-rates up to $\sim 1 \times 10^{11}$ rad(Si)/s at the device under test (DUT). The radiation pulse width was adjustable continuously from 10 ns to 10 μ s. A 20 ns radiation pulse width was used during dose-rate upset and dose-rate latchup characterization, while a 9 μ s pulse width was used during prompt TID testing. Dose rate was varied by changing the distance between the DUT and the LINAC exit window, or by changing the beam current of the LINAC.

Single event effects (SEE) testing was performed at the Brookhaven National Laboratory SEU Test Facility. This facility uses a Tandem Van de Graaff accelerator to deliver a wide range of heavy ions at the DUT. All device irradiations were performed at ambient temperature.

Burn-in

All test samples were obtained from the manufacturer without a previous burn-in. Half of the devices of each type for these experiments were then burned-in for one week at 150 °C with nominal values of V_{DD} applied during burn-in. Chip enables and output enables were tied inactive during the burn-in procedure and all other inputs were tied in a non-conflicting manner to either high or low.

IV. Results and Discussion

Co⁶⁰ TID

In Table 1 we show the Co⁶⁰ total dose hardness levels measured for all devices. For the 5-V Paradigm SRAM, only a small dependence on burn-in was observed with functional failure levels of 16 and 18 rad(Si) for burned-in and non-burned-in devices, respectively. These data place this part in the COTS category.

In contrast, the 3.3-V Paradigm samples showed an extreme burn-in effect with burned-in devices first failing functionally at 35 krad(Si) and non-burned-in at 75 krad(Si). These data illustrate the importance of performing TID characterization on burned-in devices if system specifications require burned-in parts. Based on these failure levels, the 3.3-V Paradigm devices are assigned to the radiation-tolerant category.

Cypress SRAMs failed functional test following 75 krad(Si) with no apparent burn-in effect. This failure level places this part in the radiation tolerant category.

Finally since the specified total dose failure level for burned-in Lockheed Martin LOR1M8C1399 devices is so high (> 1 Mrad(Si)), these devices were not tested in a Co⁶⁰ environment. Manufacturer's data has been presented earlier[5]. The high failure level of these devices definitely places them in the radiation hard category.

Table 2. Co⁶⁰ Total Dose Failure Levels

Device	with burn-in, rad(Si)	without burn-in, rad(Si)
PDM41256LA	16 k	18 k
PDM31256	35 k	75 k
CY7C1399	75 k	75 k
LOR1M8C1399	> 1 M	> 1 M

Prompt TID Testing

For strategic systems, it is important to perform total-dose testing at dose rates that closely replicate the expected threat dose rates. At these higher dose rates (prompt TID), devices may fail at lower total doses than in a Co^{60} test because there is less time for charge to anneal. During these tests, it was necessary to keep the individual pulse dose-rate below the device upset level to assure that the exposure pattern written to the memory was maintained. This, along with the fact that the LINAC has low repetition rates, limited the average dose-rate to approximately 900 rad(Si)/s. Unfortunately, this was only a factor of 10 higher than the dose-rate used during Co^{60} testing. A DC machine would be required to approach strategic dose-rates.

Burned-in Paradigm 5-V devices first failed functionally at 12 krad(Si) compared to non-burned-in parts, which failed at 18 krad(Si) — a 33% reduction due to burn-in (Figure 1). These failure levels place the 5-V Paradigm SRAM in the COTS category. In this environment, there appears to be a slightly larger burn-in effect compared to the Co^{60} data, but this may be an artifact of the small sample sizes. Alternatively, this may indicate that for this technology burn-in affects the annealing rate of charge in the oxides.

Examination of the Paradigm 3.3 V data in Figure 1 shows a definite burn-in effect with non-burned-in devices first failing at 80 krad(Si) vs. 40 krad(Si) for burned-in devices. No difference in functional failure level was observed between Co^{60} and prompt TID dose rates, indicating a slow oxide trapped charge annealing rate.

Consistent with Co^{60} results, the Cypress devices showed no significant reduction in the total-dose response as a result of burn-in. In fact, there appears to

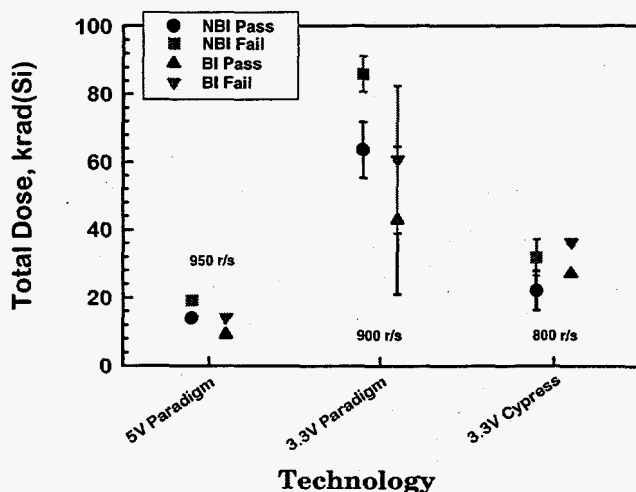


Figure 1: Prompt TID results for the devices tested. A pronounced burn-in dependence was observed for some of the technologies.

be a slight increase in the functional failure level of the burned-in Cypress devices, which first failed at 36 krad(Si) vs non-burned-in parts which failed at 28 krad(Si). However, there is a significant reduction (nearly a 50%) in failure level when comparing Co^{60} TID to prompt TID dose rates, consistent with longer annealing time at the lower dose rate.

The LMFS LOR1M8C1399 test results are not shown in Figure 1 because of their high failure level. Both burned-in and non-burned-in devices were still functional following 10 Mrad(Si). If any changes occurred due to burn-in or between Co^{60} and prompt TID results, they are considered insignificant at these levels.

Dose-rate Upset Testing

Dose-rate upset levels for the four SRAM types are compared in Figure 2. The 5-V Paradigm SRAM was found to upset at 9×10^8 rad(Si)/s while the 3.3-V Paradigm SRAM upset at 6×10^9 rad(Si)/s. Both devices are fabricated on bulk silicon and a contact at Paradigm believes there was no die shrink in going to 3.3-V. If this were true, the collection volume [6] should be nearly the same for both devices, so one would expect the 3.3-V devices to upset slightly lower due to lower operating voltage. This indicates that, in reality, there must be processing or layout changes which improve the dose-rate upset level of the 3.3-V devices. In the full paper we will provide more information.

Cypress devices upset at 5×10^8 rad(Si/s) and LMFS at 3×10^9 rad(Si/s). These data place the Paradigm 3.3-V and LMFS devices in the radiation hard category if only dose-rate upset is considered, while Paradigm 5.0-V and Cypress devices are in the radiation tolerant category. We observed no burn-in effect in a dose-rate

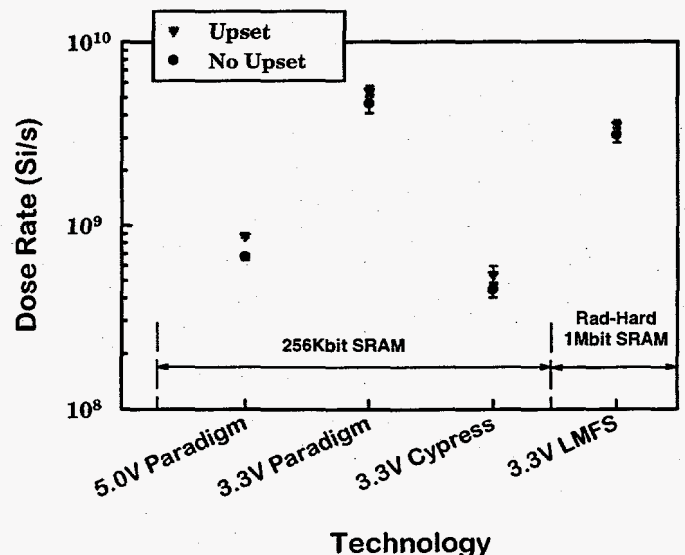


Figure 2: Dose-rate upset comparison. Surprisingly, the Paradigm 3.3 V technology outperformed the 5 V technology.

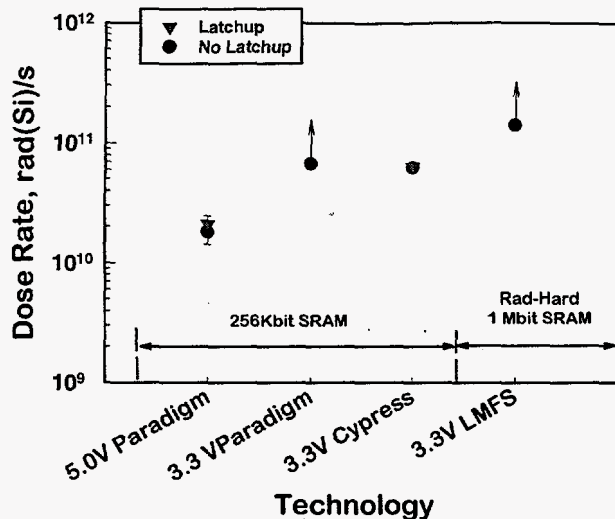


Figure 3: Dose rate latchup comparison.

environment (data not shown).

Dose-rate Latchup Characterization

Figure 3 shows the result of latchup testing for each of the four device types. The Paradigm 5-V and Cypress 3.3-V SRAMs latched up at 2×10^{10} and 6×10^{10} rad(Si)/s, respectively. The Paradigm 3.3-V and LMFS devices could not be latched at the maximum dose-rate of 6.7×10^{10} and 1×10^{11} rad(Si)/s obtained for each device, respectively. The difference between latchup dose-rate threshold measured for the 5-V and 3.3-V Paradigm devices is a natural consequence of the lower operating voltage.

These data place the Paradigm 3.3-V and the LMFS devices in the radiation-hard category, while the Paradigm 5-V and Cypress 3.3-V could be, at the users discretion, placed in either radiation tolerant or COTS categories.

SEE Test Results

SEU and SEL data are presented in Table 3. Both Paradigm devices and the Cypress SRAM were found to have SEU thresholds of < 0.5 MeV-cm²/mg which places them in the COTS category. Lockheed Martin's radiation hard SRAM neither upsets nor latches at an LET of 120 MeV-cm²/mg [5]. The 5 V Paradigm SRAM latched at an LET of 30 MeV-cm²/mg. Hardware problems made the SEL results of the Cypress part inconclusive.

V. Conclusions

A designer must consider all required radiation environments when selecting integrated circuits for system designs. This work has shown the difficulty associated with strictly categorizing a device based solely on its radiation response, since its category

Table 3. Single Event Effects Test Results

Device	SEU MeV-cm ² /mg	SEL MeV-cm ² /mg
PDM41256	0.4	30
PDM31256	0.4	>120
CY7C1399	0.5	inconclusive
LMFS 1 M	>120	>120

depends on the specific radiation environment considered. For example, the 3.3-V Paradigm SRAM could be considered a radiation-tolerant device except for its SEU response. A more useful classification depends on the methods the manufacturer uses to ensure radiation hardness, i.e. whether specific design and process techniques have been used to harden the device. Finally this work has shown that burned-in devices may fail functionally as much as 50% lower in total dose environments than non-burned-in devices. No burn-in effect was seen in dose-rate upset, latchup, or SEE environments. The user must ensure that total dose lot acceptance testing was performed on burned-in devices.

Acknowledgments

Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy under Contract DE-AC04-94AL85000. The support of the Defense Special Weapons Agency is gratefully acknowledged. The authors also thank Leonard Riewe, Chris Applett, and Paul Dodd for their support during these tests.

References

- [1] M. R. Shaneyfelt, P. S. Winokur, T. L. Meisenheimer, F. W. Sexton, S. B. Roeske, and M. G. Knoll, "Hardness Variability in Commercial Technologies," IEEE Trans. Nucl. Sci., vol. 41, pp. 2536-2543 (1994).
- [2] M. R. Shaneyfelt, D. M. Fleetwood, J. R. Schwank, T. L. Meisenheimer, and P. S. Winokur, IEEE Trans. on Nucl. Sci., vol. 41, pp. 2550-2559 (1994).
- [3] S. D. Clark, J. P. Bings, M. C. Maher, M. K. Williams, D. R. Alexander, and R. L. Pease, IEEE Trans. Nucl. Sci., vol. 42, pp. 1607-1614 (1995).
- [4] M. R. Shaneyfelt, P. S. Winokur, D. M. Fleetwood, J. R. Schwank, and R. A. Reber, Jr., IEEE Trans. Nucl. Sci., vol. 43, pp. 865-872 (1996).
- [5] N. F. Haddad, J. D. Maimon, S. Doyle, L. Jacunski, T. Hoang, D. Lawson, D. Jallice, and T. Scott, 1994 Radiation Effects Data Workshop.
- [6] L. W. Massengill and Sherra E. Diehl-Nagle, IEEE Trans. Nucl. Sci., NS-31, pp. 1337-1343 (1984).