COMPUTATIONAL CONTINUUM MODELING OF SOLDER INTERCONNENTS*

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Abstract

The most commonly used solder for electrical interconnections in electronic packages is the near eutectic 60Sn-40Pb alloy. This alloy has a number of processing advantages (suitable melting point of 183C and good wetting behavior). However, under conditions of cyclic strain and temperature (thermomechanical fatigue), the microstructure of this alloy undergoes a heterogeneous coarsening and failure process that makes prediction of solder joint lifetime complex. A viscoplastic, microstructure dependent, constitutive model for solder which is currently in development was implemented into a finite element code. With this computational capability, the thermomechanical response of solder interconnects, including microstructural evolution, can be predicted. This capability was applied to predict the thermomechanical response of various leadless chip carrier solder interconnects to determine the effects of variations in geometry and loading. In this paper, the constitutive model will first be briefly discussed. The results of computational studies to determine the effect of geometry and loading variations on leadless chip carrier solder interconnects then will be presented

Introduction

Solder joints were initially designed to be simple electrical interconnections between mechanically interlocked components in electronic packages. As technology advanced, electrical component size decreased, and the number of input/output terminations increased. To accommodate these changes, the number of solder joints per package have increased, while joint dimensions have decreased. The mechanically interlocked components were replaced by plated-through-hole technology which is now being pushed aside by surface mount technology (SMT). With each technological advance, the solder was expected to be not only an electrical conductor but also an increasingly important structural member with smaller and smaller feature size. The benefits of shrinking solder joint dimensions are numerous (e.g., increased speed, greater packing density, etc.) but reliability concerns increase exponentially. A key issue of solder joint reliability is joint failure due to thermal cycling since individual components that are soldered together in an electronic package have differing thermal expansion coefficients. Most current methodologies for evaluating and/or predicting solder joint reliability are empirically based. In these methodologies, specimens are manufactured and tested to failure for given sets of test conditions and failure models are developed (usually based upon some form of Coffin-Manson relations). These failure models are then applied to similar geometries under different loading conditions to "predict" reliability. There are two major drawbacks to this methodology. First, substantial testing is required for each technology change such as geometry or material (e. g. lead free solder) and testing is expensive and time consuming. Second, it is difficult, if not impossible, to assess the effects of critical parameters on reliability through testing alone. To address these drawbacks, validated computational modeling is increasingly being used to assess solder joint response and reliability.

Computational modeling of solder interconnects is exceedingly difficult. To predict the thermal / structural response of any system, three elements must be defined; the geometry, the loading (including boundary conditions) and the material response (including failure). Solder interconnects present challenges in each of these elements. First, solder interconnects form during processing, therefore the local geometry of the solder interconnects will vary in size, shape, and may have imperfections. Additionally, the size of the solder interconnects are small relative to the package but are numerous. Therefore, obtaining the required resolution within the solder interconnects along with the required package geometry is computationally challenging. Second, the loading that can cause thermal-mechanical fatigue failure is essentially infinitely variable. Environmental thermal parameters such as temperature cycle range, hold times, and rates of temperature change can all effect solder interconnect reliability. Internal heating of electronic components can additionally effect reliability. Finally, mechanical loading such as shock and vibration can affect reliability. Third, the material response of solder is exceeding difficult to model computationally. Solder is a viscoplastic material in which the material parameters depend upon the microstructure, initial microstructure depends upon processing, and the microstructure changes during thermomechanical loading. Additionally, even if the stress and strain response in solder could adequately be computed, predicting failure is an additional challenge.

Sandia National Laboratories efforts have focused upon the development of a viscoplastic, microstructurally dependent, constitutive model for solder. While this model is still being researched and developed, it shows promise to accurately predict the stress state, the evolution of the stress state with thermomechanical loading, and possibly provide a methodology to estimate the initiation of failure in solder interconnects. In this paper, the current constitutive

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model will be briefly discussed. The current constitutive model will then be applied to predict the thermomechanical response of various geometries of leadless chip carrier (LCC) solder interconnects subjected to various thermomechanical load conditions.

Internal State Variable Constitutive Model

A number of viscoplastic models have been developed for solder [1-5]. Several of these models include the initial grain or phase size as a material constant that does not change during the simulations. The viscoplastic model currently being developed is similar in may respects to the previous models; however, this new model incorporates grain size as an internal state variable which changes during the simulation. A scalar state variable is used to capture isotropic hardening and recovery and a second order state tensor is used to capture kinematic harding and recovery. Coarsening is expected to have a significant effect on the state of the material, and a state variable which accounts for the reduction in flow stress with coarsening which follows the Hall-Petch relationship is included in the new model.

The proposed internal state variable model for solder has the following standard constitutive relation

$$\dot{\sigma} = \mathbf{E}:(\mathbf{d} - \mathbf{d}^{in}) \tag{1}$$

where $\dot{\sigma}$ is the Cauchy stress in the unrotated configuration, E is the fourth-order, isotropic elasticity tensor, d is the total deformation rate in the unrotated configuration, and $\mathbf{d}^{in}$ is the inelastic deformation rate in the unrotated configuration[6]. The inelastic deformation rate is given by the following equation

$$\mathbf{d}^{in} = \frac{3}{2}\gamma\,\mathbf{n} = \frac{3}{2} f \exp\left(\frac{-Q}{R\theta}\right)\left(\frac{\lambda_o}{\lambda}\right)^p \sinh^m\left(\frac{\tau}{\alpha(c+\hat{c})}\right)\mathbf{n} \tag{2}$$

where γ is the magnitude of the inelastic rate, f, p, m and Q are material parameters, R is the gas constant (1.987 cal/mole/K), θ is the absolute temperature, λ is the current grain diameter, λ_o is the initial grain diameter, α is a scalar function of the absolute temperature, c and $\hat{c}$ are state variables, and $\mathbf{n}$ is the normalized stress difference tensor which is given by,

$$\mathbf{n} = \frac{\mathbf{s} - \frac{2}{3}\mathbf{B}}{\tau} \tag{3}$$

where $\mathbf{s}$ is the stress deviator, $\mathbf{B}$ is the state tensor which accounts for kinematic hardening. τ is a scalar measure of the stress difference magnitude

$$\tau = \sqrt{\frac{3}{2}\left(\mathbf{s} - \frac{2}{3}\mathbf{B}\right):\left(\mathbf{s} - \frac{2}{3}\mathbf{B}\right)} \tag{4}$$

Competing hardening and recovery mechanisms are captured by the evolution equations for the internal state variables c and $\mathbf{B}$. Evolution of the scalar state variable c is given by

$$\dot{c} = A_1\gamma - (A_2\gamma + A_3)(c - c_o)^2 \tag{5}$$

where c_o, A_1, A_2, and A_3 are material parameters. Evolution of the second-order state tensor $\mathbf{B}$ is given by

$$\dot{\mathbf{B}} = A_4\mathbf{d}^{in} - (A_5\gamma + A_6)\sqrt{\left(\frac{2}{3}\mathbf{B}:\mathbf{B}\right)}\ \mathbf{B} \tag{6}$$

where A_4, A_5, and A_6 are material parameters. The reduction in flow resistance with grain coarsening is captured by the scalar state variable $\hat{c}$. The state variable $\hat{c}$ is related to the current grain diameter, λ, by

$$\hat{c} = A_7\left(\frac{\lambda_o}{\lambda}\right)^{A_8} \tag{7}$$

where A_7 and A_8 are positive material parameters, and λ_o is the initial grain diameter. Note that as the grain diameter, λ, increases, $\hat{c}$ decreases in magnitude which has the effect of reducing the flow resistance of the material. Evolution of the grain diameter, λ, is given by the following equation

$$\dot{\lambda} = A_{11}\frac{(v_x + v_o)}{\lambda} \tag{8}$$

where A_{11} is a material parameter, v_x is the excess vacancy concentration and v_o is the equilibrium vacancy concentration. Finally, the generation of excess vacancies due to inelastic deformation is given by

$$\dot{v}_x = A_9\gamma - A_{10}v_x \tag{9}$$

where A_9 and A_{10} are material parameters.

This model was implemented into the finite element codes JAC2D [6], JAC3D [7], and JAS3D [8]. A complete description of the constitutive model development and implementation of the constitutive model into a finite element setting is the topic of a paper currently in preparation.

Applications

The currently implemented three-dimensional, time-dependent, viscoplastic, microstructural dependent capability was applied to predict the thermomechanical response of various LCC solder interconnects to determine the effects of variations in geometry and loading. The initial (baseline) geometry selected was a one element thick slice of a LCC solder interconnect as shown in Figure 1. This

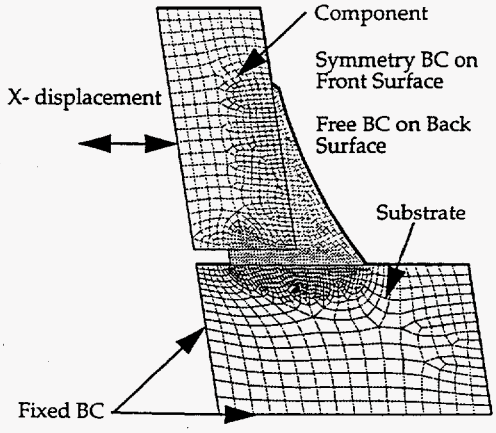

Figure 1: Baseline Geometry

geometry can be considered to be a solder interconnect at the centerline of the LCC package. The substrate was assumed to be a ceramic material with a coefficient of thermal expansion (CTE) of $5x10^{-6}$ in/in C. The component was also assumed to be a ceramic material with a CTE of $6x10^{-6}$ in/in C. The CTE of the solder used was a handbook value of $25x10^{-6}$ in/in C. The initial microstructure of the solder was assumed to be uniform. The properties used for the viscoplastic solder model are given in Table 1. The substrate

Table 1: Constants For 60/40 Solder

Property	Value
SHEAR MODULUS	1.72e6
BULK MODULUS	8.03e6
FLOW RATE	-0.287
SINH EXPONENT	10.40
GROWTH EXPONEN	3.00
ALPHA	1.00
BETA	1.00
A1	0.00
A2	0.00
A3	0.00
A4	3.26e5
A5	6.61e-2
A6	4.18e-6
A7	4455.0
A8	0.5
A9	1.00e-3
A10	16.6
A11	5.81e-5
FLOW STRESS	2500.
GRAIN SIZE	35.4e-6
VACANCY CONCEN	1.00e-9

was assumed to be rigidly restrained as shown. A symmetry boundary condition was applied to the front surface and the back surface was free. A uniform time-dependent temperature history was applied. Simultaneously, a time-dependent displacement was applied to the component with magnitude of the applied displacement corresponding to the thermal expansion difference between the component and substrate assuming that the distance from the center of the component to the edge of the LCC component was 0.46 inch. The applied uniform temperature histories used in these computations are shown in Figure 2 and the applied displacement history is shown in Figure 3. The response of the solder interconnect was computed for six complete thermal cycles. In Figure 4, the computed shear force (resultant load) is plotted as a function of time. This plot clearly shows the time-dependent creep response at high temperature and essentially elastic response at low temperature. In Figure 5, the computed

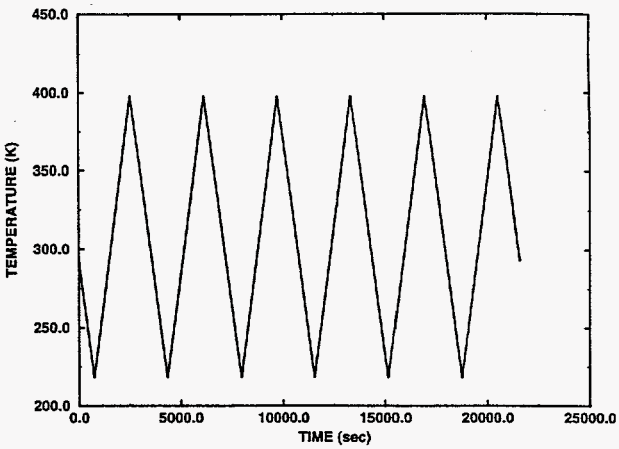

Figure 2: Applied Thermal Loading History

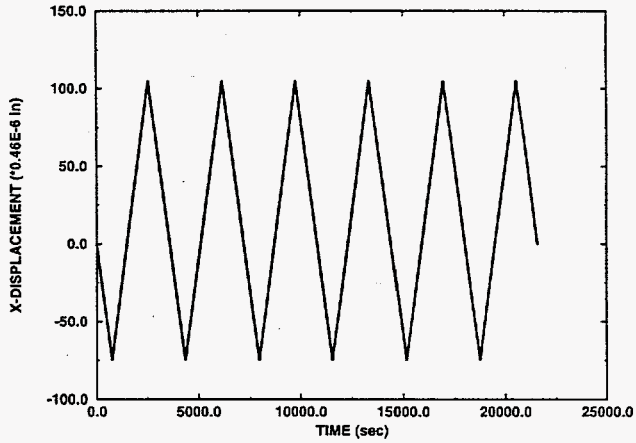

Figure 3: Applied Displacement History

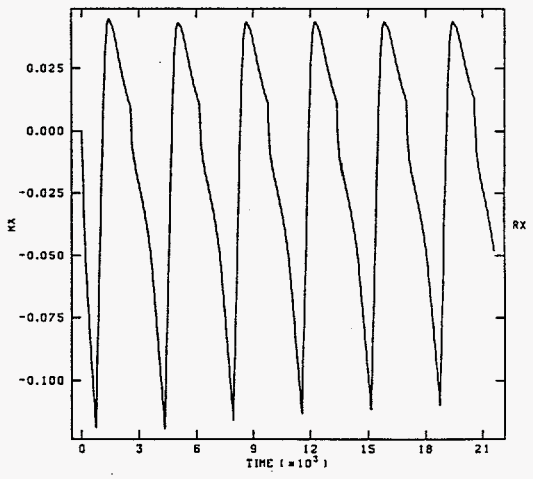

Figure 4: Computed Shear Force vs. Time

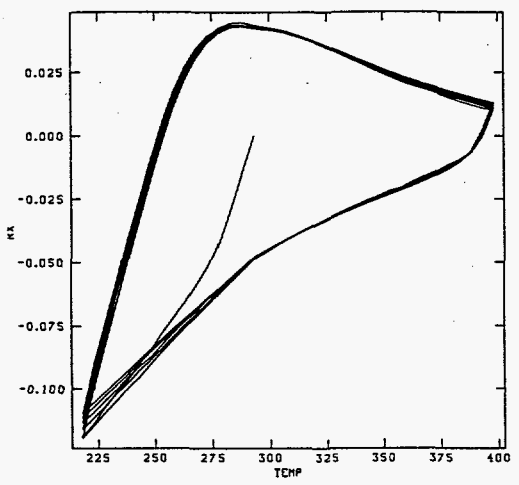

Figure 5: Computed Shear Force vs. Temperature

shear force is plotted as a function of temperature. This plot shows the characteristic hysteris loops and starts to show the effect of microstructural changes on the response. In Figure 6, contours of the accumulated plastic strain the solder interconnect at the end of six complete cycles is plotted. This plot indicates that the highest

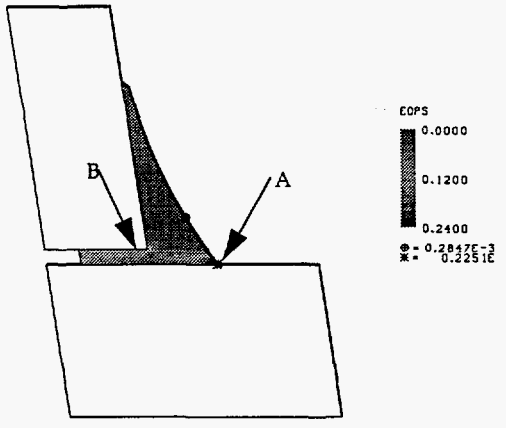

Figure 6: Computed Accumulated Plastic Strain @ 6 Cycles

magnitude accumulated plastic strain is at the toe (point A) of the solder interconnect. The accumulated plastic strain at points A and B are plotted as a function of time (or cycles) in Figure 7 and clearly indicates that the computed strain at the toe of the interconnect is higher than at point B (underneath the component). In Figure 8, contours of the computed microstructural coarsening parameter in the solder interconnect at the end of six complete cycles is plotted. This plot indicates that the highest magnitude of microstructural coarsening is also at the toe (point A) of the solder interconnect, however, as shown in Figure 9 microstructural coarsening parameter at point A is only slightly larger than the microstructural coarsening parameter at point B. The microstructural coarsening parameter can be considered to be a "damage" parameter and believed to be an indicator of initial cracking in the solder. Further research is needed, however, to relate the magnitude of the "damage" parameter to initial cracking. These results suggest that initial cracking should initiate at the toe of the interconnect, however, crack initiation may also appear underneath the component. This is in agreement with experimental observations.

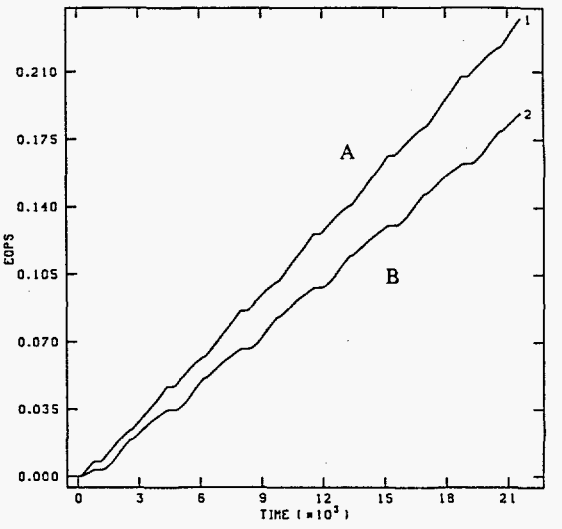

Figure 7: Accumulated Plastic Strain @ Points A and B vs. Time

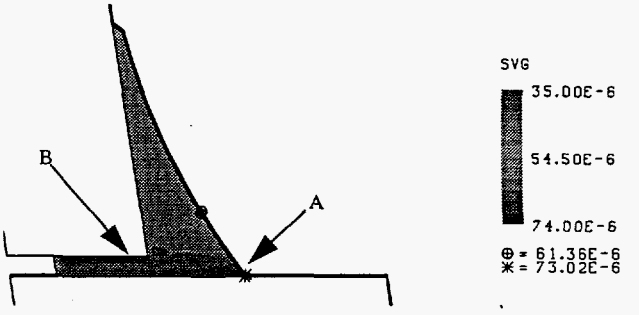

Figure 8: Computed Microstructural Parameter @ 6 Cycles

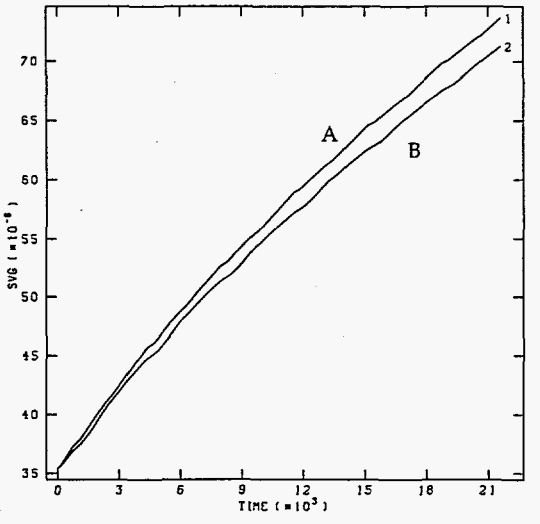

Figure 9: Microstructural Parameter @ Points A and B vs. Time

Effect of Loading

In the baseline computation, a sawtooth thermal history from T = -55C (218K) to T = 125C (398K) was applied at a rate of one cycle per hour. Two additional loading cases were considered. First, the effect of a 200 second dwell time at both high and low temperature extremes was computed. Second, the effect of isothermal mechanical load only was computed. In Figures 10, contours of the computed microstructural coarsening parameter in the solder interconnect at the end of six complete cycles is plotted for the 200 second dwell time and for isothermal loading. Comparison of these plots indicate differences in the microstructural parameter or "damage" response as a function of loading. The computed

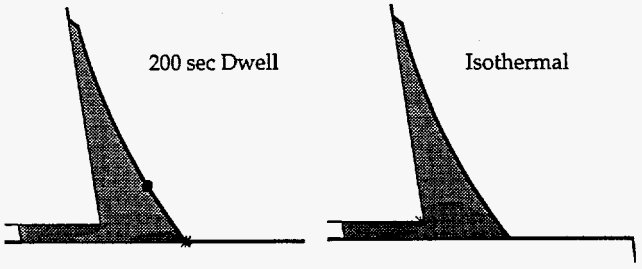

Figure 10: Computed Microstructural Parameter @ 6 Cycles

quantitative values of the microstructural parameter are plotted as a function of number of cycles in Figure 11 (@point A) and Figure 12 (@point B), respectively. These results indicate that even a minimal dwell increases the magnitude of the microstructural or damage parameter and isothermal mechanical loading is less severe than thermomechanical cycling. These computational observations are qualitatively in agreement with experimental observations.

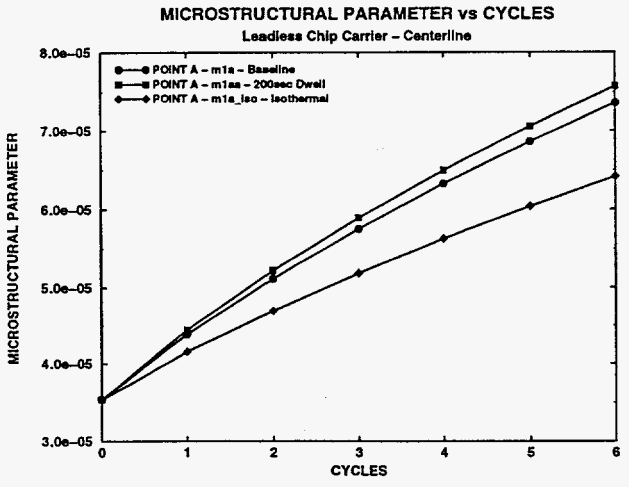

Figure 11: Microstructural Parameter vs. Cycles - Point A

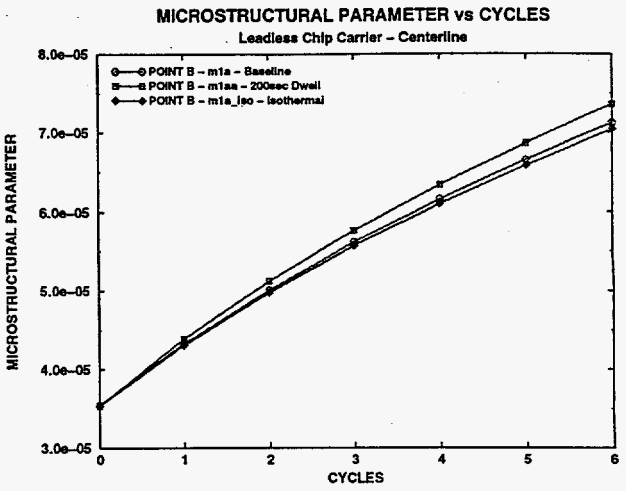

Figure 12: Microstructural Parameter vs. Cycles - Point B

Effect of Fillet Height

The effect of the geometry of LCC solder interconnects on reliability continues to be a topic of much discussion, therefore, a series of computations to evaluate the effect of solder fillet height on solder response was completed. In these computations the baseline computation (Figures 1 and 4-9) was assumed to be a full fillet height. Additional computations were completed for fillet heights of 3/4, 1/2, 1/4 and no fillet. In Figures 13, contours of the computed microstructural coarsening parameter in the solder for these geometry variations are shown. The computed quantitative

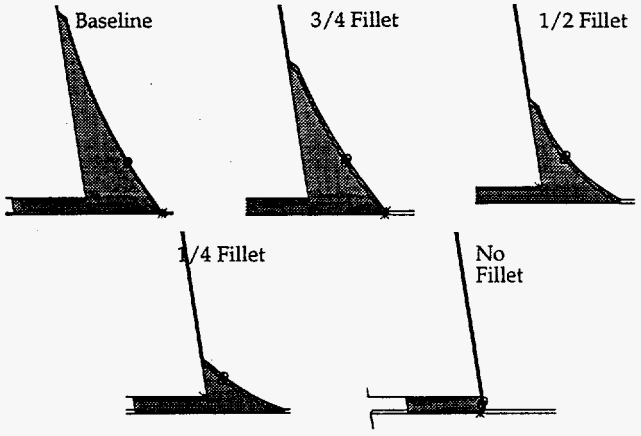

Figure 13:Computed Microstructural Parameter @ 6 Cycles

values of the microstructural parameter are plotted as a function of number of cycles in Figure 14 (@point A) and Figure 15 (@point B), respectively. These results indicate that reducing the fillet height significantly influences the microstructural or damage parameter at the toe of the interconnect (@point A), however, the microstructural underneath the component is not affected. This suggest that initial cracking of the solder underneath the component, which is considered by many to be the most damaging crack, is not affected by fillet height geometry.

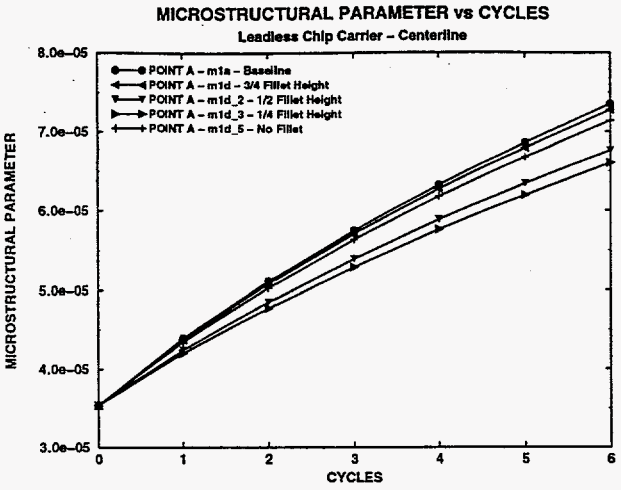

Figure 14: Microstructural Parameter vs. Cycles - Point A

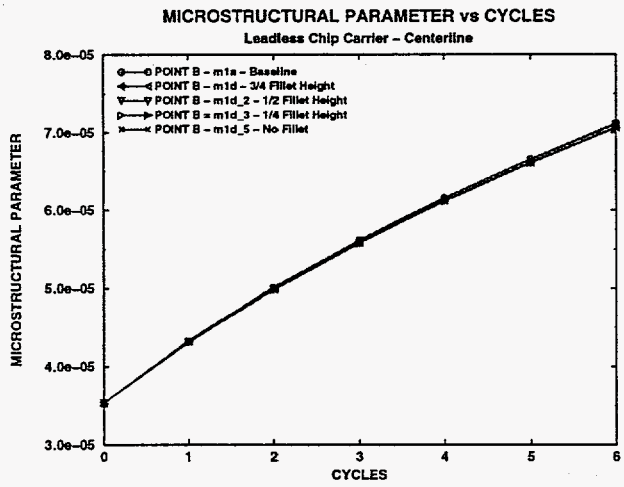

Figure 15: Microstructural Parameter vs. Cycles - Point B

Effect of Height Off Substrate

The effect of height of the component off the substrate is a geometric variable which can be controlled and may have a significant effect on solder interconnect reliability. A computation in which the thickness of the solder was reduced to one-half of the baseline geometry was completed. The computed values of the microstructural parameter (both at point A and B) are plotted as a function of number of cycles in Figure 16. This plot clearly indicates that the microstructural or damage parameter dramatically increases as the component height off the board decreases. This suggests that significant attention needs to paid to controlling the component height (within processing and design limitations) to maximize reliability.

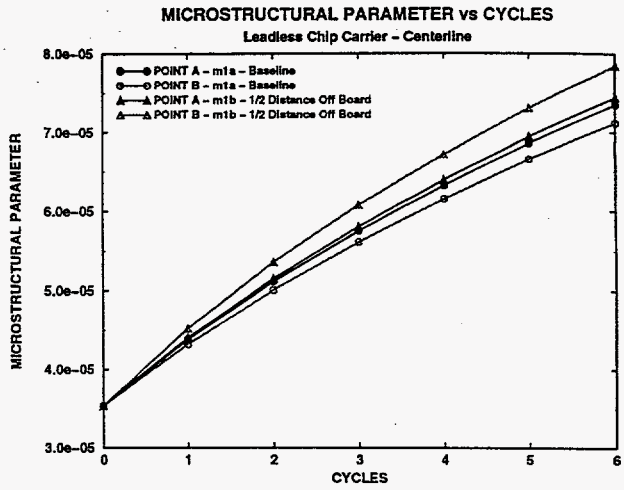

Figure 16: Microstructural Parameter vs. Cycles - Height Off Substrate

3D Model on Centerline

The geometry used in the preceding computations was a slice of a LCC interconnect on the centerline of the component. In reality an actual LCC interconnect is wider than assumed previously and both the component and substrate extend beyond the interconnect. A three-dimensional computation of a more realistic LCC interconnect on the centerline of the package was completed. The geometry, shown in Figure 17, was loaded identically to the previous baseline computation. Contours of the computed microstructural coarsening parameter in this solder interconnect at the end of six complete cycles are also plotted in Figure 18 and the results indicate that the peak values of the microstructural parameter are slightly higher than baseline computation. This indicates that there is a solder interconnect width effect.

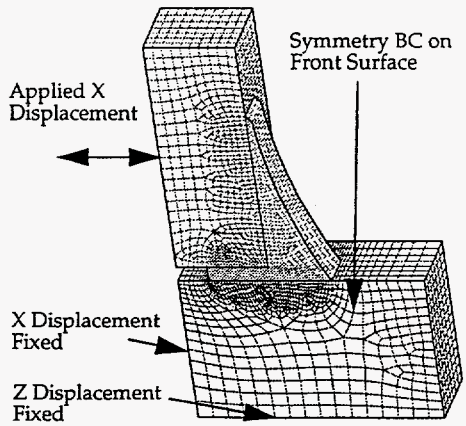

Figure 17: Geometry of LCC Interconnect on Centerline

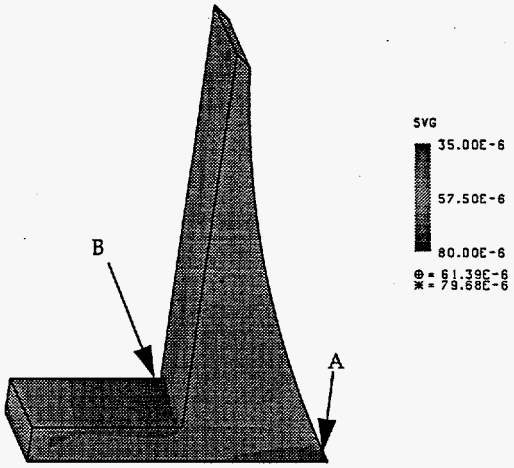

Figure 18: Computed Microstructural Parameter @ 6 Cycles

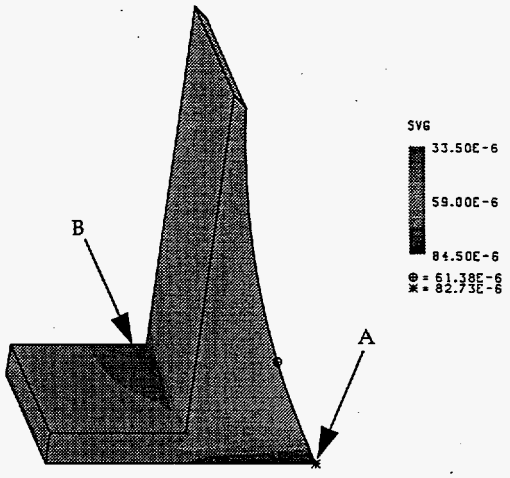

Figure 20: Computed Microstructural Parameter @ 6 Cycles

3D Model at Corner of LCC

Finally, it is common knowledge that the most severe interconnect in a LCC package is the corner interconnect. A complete 3D geometry was modeled and subjected to thermomechanical loading representative of loading at the corner interconnect of a 0.46 inch rigid LCC package, Figure 19. Contours of the computed microstructural coarsening parameter in this solder interconnect at the end of six complete cycles are plotted in Figure 20, and the computed quantitative values of the microstructural parameter are plotted as a function of number of cycles in Figure 21. The results indicate that the magnitude of the damage parameter is increased at both the toe and underneath the component as compared to an interconnect at the centerline. The magnitude of the damage parameter underneath the component is substantially increased. Additionally, the location of the high magnitude microstructural parameter underneath the component is shifted to the inside edge. This is due to the two components of shear forces that the interconnect is being subjected. These results suggest that the corner interconnect would be less reliable as is experimentally observed.

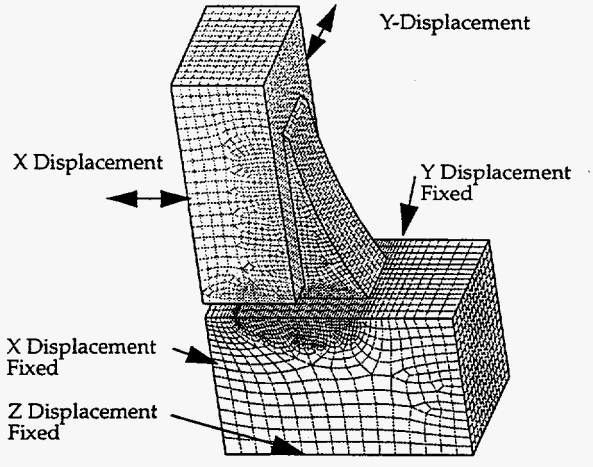

Figure 19: Geometry - 3D Model of Corner LCC Interconnect

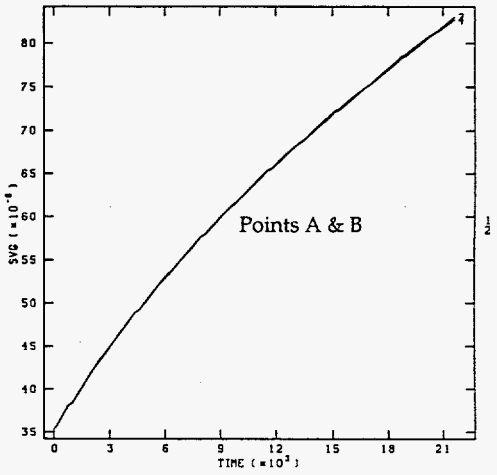

Figure 21: Microstructural Parameter @ Points A and B vs. Time

Summary and Conclusions

In this paper, the viscoplastic, microstructural dependent constitutive model currently being developed was briefly discussed. The model, which was implemented into a 3D finite element code setting, was applied to predict the thermomechanical response of various geometries of leadless chip carrier (LCC) solder interconnects subjected to various thermomechanical load conditions. These results indicate that: 1) even a minimal dwell time increases the magnitude of the microstructural or damage parameter, 2) isothermal mechanical loading is less severe than thermomechanical cycling, 3) reducing the fillet height significantly influences the microstructural or damage parameter at the toe of the interconnect (@point A) However, the microstructural underneath the component (the most damaging) is not affected, 4) component height off the board is critical, 5) interconnect width has a slight effect and, 6) the corner LCC interconnect is the most susceptible to damage.

While this model is still being researched and developed, this study shows that the computational capability shows promise to accurately predict the stress state, the evolution of the stress state with thermomechanical loading, and possibly provide a

methodology to estimate the initiation of failure in solder interconnects. Additional research will focus on obtaining accurate parameters that control the evolution of the microstructure, developing a crack initiation criteria so that cycles to failure can be predicted, and accelerating the computations.

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