Stresses From Flip-Chip Assembly and Underfill; Measurements with the ATC4.1 Assembly Test Chip and Analysis by Finite Element Method[†]

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Abstract

We report the first measurements of in-situ flip-chip assembly mechanical stresses using a CMOS piezoresistive test chip repatterned with a fine pitch full area array. A special printed circuit board substrate was designed at Sandia and fabricated by the Hadco Corp. The flip-chip solder attach (FCA) and underfill was performed by a SEMATECH member company. The measured incremental stresses produced by the underfill are reported and discussed for several underfill materials used in this experiment.

A FEM of a one-quarter section of the square assembly has been developed to compare with the measured as-assembled and underfill die surface stresses. The initial model utilized linear elastic constitutive models for the Si, solder, underfill, and PC board components. Detailed comparisons between theory and experiment are presented and discussed.

Introduction

The manufacturability and reliability of a flip-chip assembled package are strongly influenced by the mechanical stresses developed in the die-solder ball-substrate region. These stresses are produced by differential thermal contraction between substrate and die, and the stress distribution and magnitude can be significantly changed by the presence of an underfill material. It is highly desirable to model these stresses using the Finite Element Method (FEM) stress analysis technique so that the susceptibility to mechanical failure during thermal cycling can be predicted for new geometries and combinations of materials without costly experimentation. However, the solder ball interface between an assembled flip-chip and substrate is particularly difficult to model precisely due to uncertain knowledge of both the elastic properties of the assembly constituents and the strain boundary conditions at material interfaces. The FEM analysis accuracy is improved significantly by "calibration" using an *in situ* stress measurement technique, such as that described here and in previous work [1, 2] employing piezoresistor stress sensors. (A thorough treatment of Si piezoresistor stress measurement theory is contained in Ref. [3])

A flip-chip on laminate substrate, though somewhat simpler to model than a molded IC, is under a complex state of stress and strain due to large differences in thermal expansion between die and substrate. Interfacial stress is generally relieved through bending of the assembly and the magnitude of these stresses can be approximated with relatively simple "bimetallic strip" models. Hall [4] describes a spreadsheet technique that calculates in-plane stress at each interface of a multilayer structure. This method assumes a constant radius of curvature and does not account for end effects, but is useful for determining maximum states of compression or tension along the z dimension of an assembly. Suhir [5] described a more sophisticated model that accounts for end effects and calculates the distribution of in- and out-of-plane stresses (σ_{xx}, σ_{yy}, and σ_{zz}), along with interfacial shearing stress (τ_{xz}, τ_{yz}). There are numerous journal articles describing similar approaches, but we will use these two examples in the results section to compare with FEM calculations and experimental measurement data obtained from *in situ* stress sensors. The assembled flip chip has the unique quality that its surfaces can be easily measured for deflection, an important parameter that, combined with *in situ* stress data, can be very effective in validating analytical and FEM techniques.

Experimental

Test Vehicle Description

The ATC4.1 Assembly Test Chip, with a side dimension of 11.6 mm (0.456 in.) was repatterned for area array using a Cu-polyimide process. The eutectic solder bump array is square with 42 bumps per row (1764 total bumps) and a 0.0254 mm (0.010 in.) bump pitch. The chip contains 100 addressable stress sensing cells plus ring oscillators, resistive heaters, and diode thermometers described elsewhere [6]. All CMOS signals are brought out through perimeter balls, while inner balls are used for daisy chain and Kelvin ball resistance circuits. For the experiments discussed in this work, a special printed circuit board substrate was designed at Sandia and fabricated by the Hadco Corp. The flip-chip solder attach and underflow assembly was performed by a SEMATECH member company using a no clean flux process. The layout for a single ATC4 die prior to redistribution and bumping is shown in Fig. 1. A SEM micrograph of a bumped QUAD is shown in Fig. 2.

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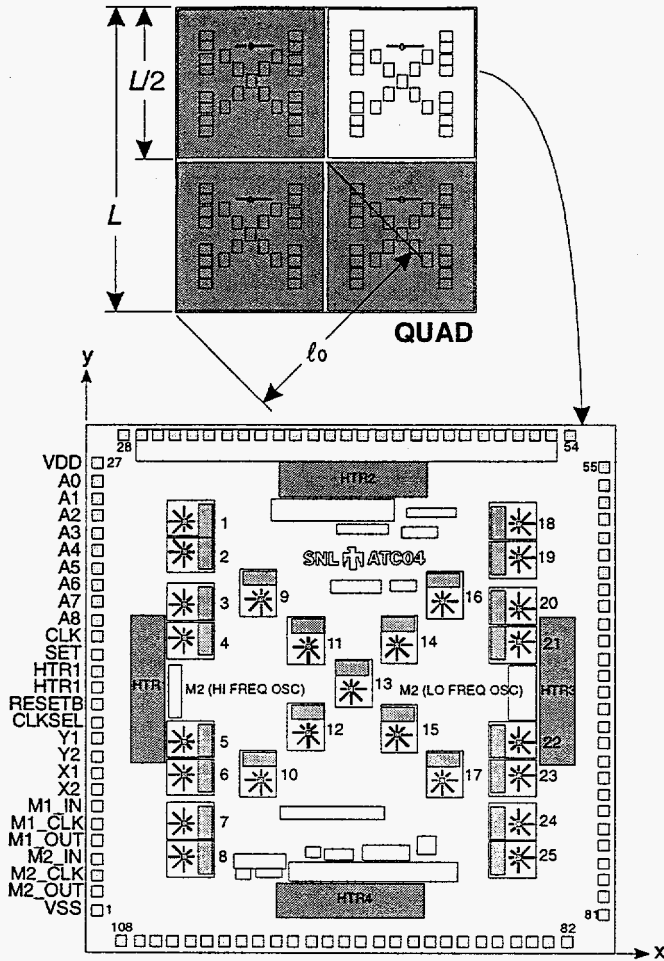
Fig. 1 Layout of 1 of 4 die in an ATC4 QUAD prior to redistribution and solder bumping. The first 27 perimeter bondpads are replicated around the die, so that the QUAD has perimeter access to all stress measurement circuitry. QUAD diagonal and width dimensions are shown.
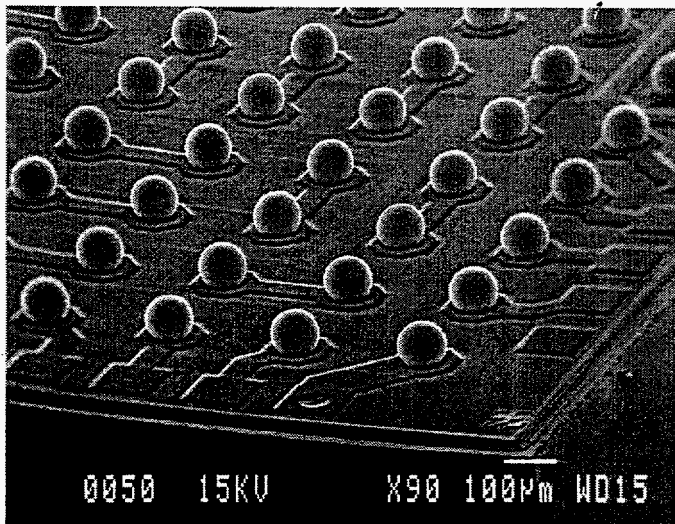

Fig. 2 SEM micrograph of the corner of an ATC04.1 QUAD showing the redistributed pads and 0.0254 mm (0.010 in.) pitch solder bump array formed on the IC surface.
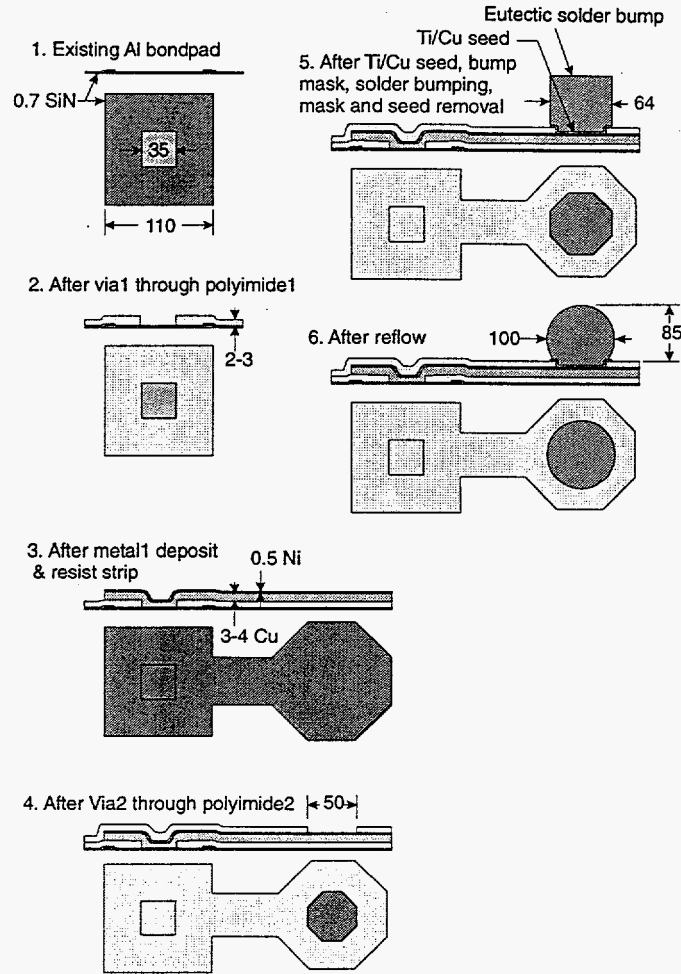

Fig. 3 ATC4.1 wafer level repattern and solder bump process flow by Aptos Corporation. Dimensions are in microns.
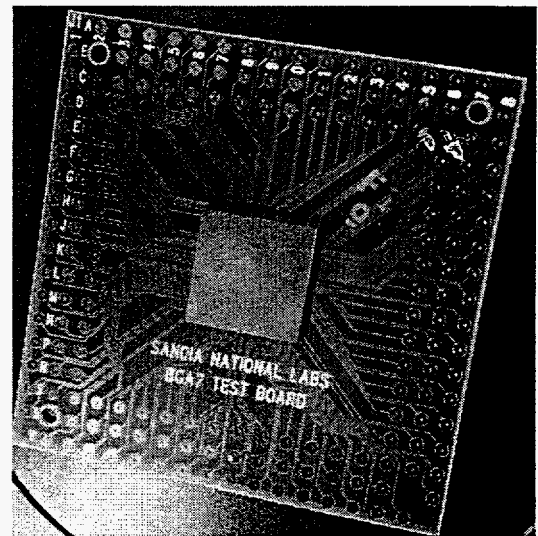

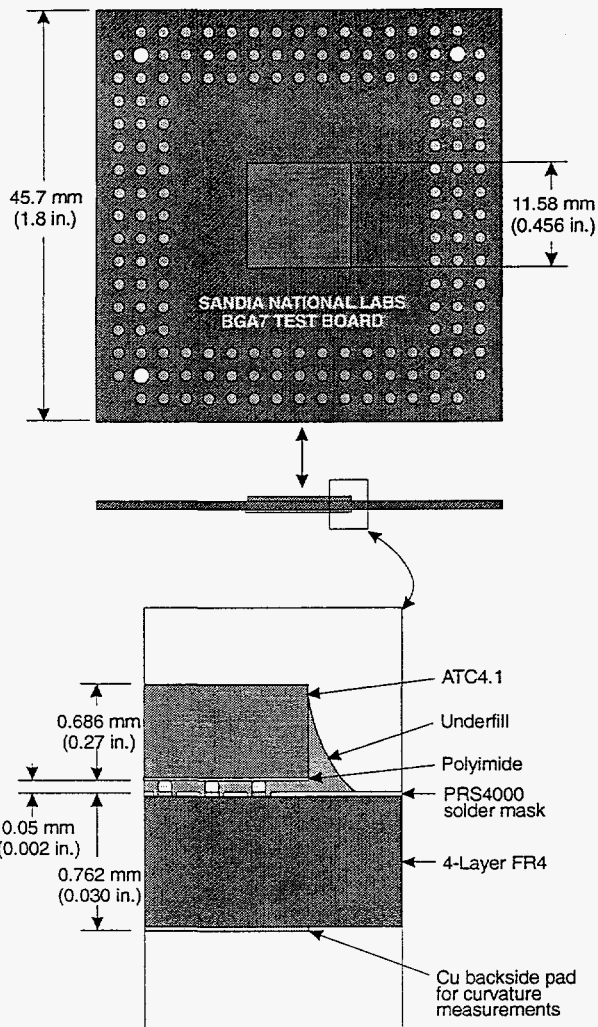**Fig. 4** ATC4.1 QUAD assembled to FR-4 test board prior to underfill.

Fig. 5 Construction details of ATC4.1 QUAD flip-chip assembled on FR-4 test board.
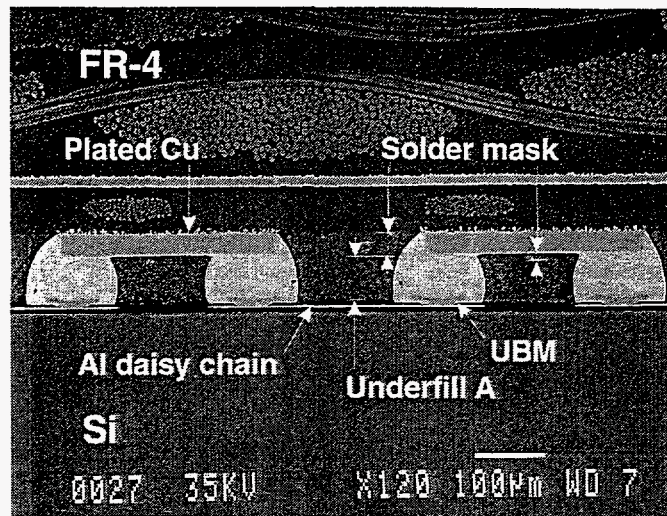

Fig. 6 SEM micrograph of ATC4.1 QUAD A11-03 cross-section.

Material properties used in the analytical and FEM simulations are contained in TABLE I. An additional solder property, yield stress = 34 MPa, was used in the FEM simulation prior to underfill. Many of the values used for these calculations were handbook properties because we did not have more accurate values available at the time.

Fig. 3 contains the repattern and bump process flow along with critical dimensions. An assembled part is shown in Fig. 4 and Fig. 5 shows relevant board and cross-section dimensions. Fig. 6 contains an SEM micrograph of an assembly cross-section.

Electrical and Mechanical Measurements

In order to relate changes in piezoresistor values due to changes in the state of die stress, it is necessary to develop a set of "reference" measurements at the wafer level. The die are not stress free at this point, but are considered to be under negligible stress compared to that seen during subsequent packaging operations. A manual wafer level probe is made, in which all 25 stress cells in each die are sequentially interrogated under PC control through a common 4-point measurement bus using a precision current source and digital voltmeter. There are 900 floating point data per QUAD associated with these measurements that are entered into a reference data base. After redistribution and solder bumping, known good diced QUADs are identified and separated from the wafer using the results from these initial measurements.

A custom-made test fixture makes electrical connection to the three rows of perimeter pads on the FR-4 substrate using pogo pins. Signals are routed to a 144 I/O general purpose PC controlled test system via an interface board. The test system instruments are functionally equivalent to those used at the wafer level probe and provide similar short and long term accuracy. The assembled ATC4.1 QUADs contain more test structures than available at the wafer level—4-point solder ball resistance structures and daisy chains. Measurements are made on these structures along with stress cell resistance and diode measurements at defined test intervals during the course of an experiment, and are entered into a data base. Processing and analysis of these data are described in the Experimental Stress Analysis section. Test intervals for the work described here were before and after underfill.

Deflection of die and substrate were measured along the x-axis and y-axis using a Mahr S8P profilometer with a

TABLE I
MATERIAL PROPERTIES.

	Si	Under-fill	Solder	FR-4
Thickness (mm)	0.69	0.51	0.51	0.762
Length, width (mm)	11.6	11.6		45.7
CTE (10^{-6}/°C)	2.6	22 (A) 35 (B)	25	17
Elastic modulus (GPa)	106.9	7.0 (A) 6.5 (B)	43.1	18.6
Poisson's ratio	0.25	0.30	0.365	0.20

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Focodyn laser stylus. A machined fixture was used to ensure proper alignment of the part during each of the four measurements. The tool was set to measure maximum deflection over a 6.35 mm (0.250 in.) path straddling the center of the 11.6 mm QUAD die. Measurements were made before and after underfill.

2D Theoretical Stress Analysis

There are a number of closed form analytical solutions to the tri-material die-on-substrate problem based on generalizations of the classical "bimetallic strip" problem. These solutions assume no external forces act on the structure and the sum of all forces and moments must be zero. The Hall [4] theory of stress in n layers is based on uniform layers in an axisymmetric disc ($\sigma_{xx} = \sigma_{yy}$) where the thickness is much less than the in-plane dimensions. This solution does not take into account edge effects and assumes constant radius of curvature throughout the structure. Displacements are calculated at each material interface. Strain is assumed to vary linearly from one interface to the next within a layer as a function of the coordinate normal to the surface and is continuous across material boundaries. Within a given layer, stress is also assumed to vary linearly as a function of z, but is generally discontinuous between layers. The theory is implemented in a convenient spreadsheet formulation.
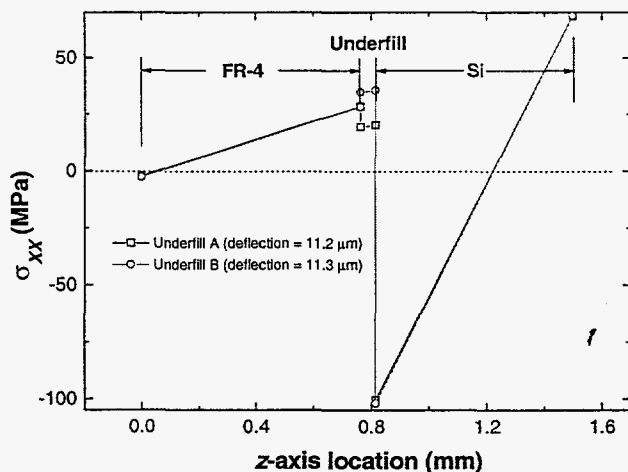

Fig. 7 In-plane stress calculated along z-axis for ATC4.1 QUAD using spreadsheet from Hall [4]. Calculations were done for underfill A and B with $\Delta T = 140\ °C$.

Fig. 7 shows a calculation of the vertical or z variation of the in-plane stress along the x-axis at the interface of each layer calculated using the Hall theory together with parameters from TABLE I and thickness dimensions from Fig. 5. It is based on stresses developed during cooldown from a stress free temperature of 160 °C to 20 °C ($\Delta T = 140\ °C$). The solder ball underfill region is represented as a uniform homogeneous layer with the parameters of underfill, as given in TABLE I. The spreadsheet also calculates radius of curvature of the assembly and assumes that it is constant throughout the plane. To facilitate comparison with experimental measurements of deflections using a laser profilometer, the radius of curvature

at the center (r) is converted to the deflection (h) of an arc from its chord (a), $h = r - (r^2 - a^2/4)^{1/2}$, where $a = 6.35$ mm (0.250 in.). The Hall theory predicts slightly higher compressive stress and deflection for the underfill B material, which has both higher CTE and elastic modulus.

Suhir [7] has presented a tri-material stress analysis model applicable to both face-up and flip-chip die attach methods. The model can be greatly simplified for the case when the thickness and/or elastic modulus of the interstitial layer, in this case the solder ball array and underfill, are small. The simplified model is essentially a bi-material solution. Suhir subsequently improved the model's estimation of the out-of-plane shear stress distribution (τ_{xz}) and peel stress (σ_{zz}) magnitude [5]. Since the simplified Suhir model does not take into account the CTE and modulus of the underfill region, it makes no distinction between underfill A and underfill B. The calculations shown in Fig. 8 are arbitrarily based on data for underfill A contained in TABLE I and $\Delta T = 140\ °C$. In this figure, the half width of the QUAD has been normalized, so that $y = 0$ represents the QUAD center and $y = L/2$ is the edge, coordinate, or furthest distance from the neutral point along an axis. The model also calculates the radius of curvature distribution along an axis in the x-y plane. These local radii are relatively uniform in the center region of the die and an estimate of deflection based on curvature at the center is included in the figure.
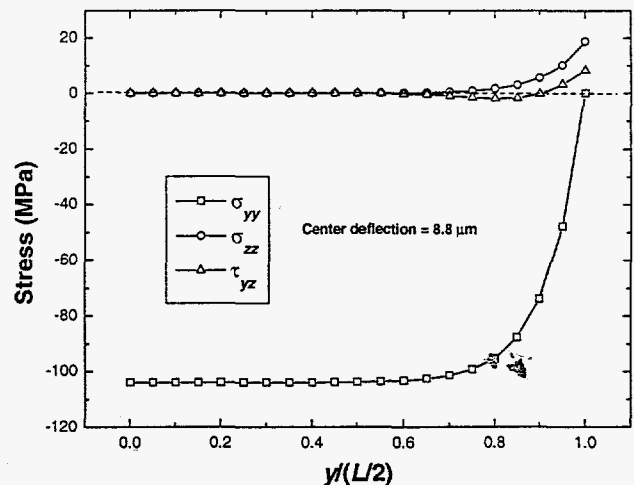
Fig. 8 Estimations of in and out of plane stress components based on Suhir [5,7] from QUAD center to edge. Half width of QUAD is normalized. Calculations were done for underfill A with $\Delta T = 140\ °C$.

3D Theoretical Stress Analysis

A 3D finite element model (FEM) was applied to predict the stress, strain, and deformation response of the ATC4.1 test vehicle due to 1) cool down to room temperature from the soldering temperature prior to underfill, and 2) due to cool down to room temperature from the cure temperature following underfill. The finite element idealization, shown in Fig. 9, utilizes two planes of symmetry resulting in one quarter of the package being modeled. This includes 441 solder

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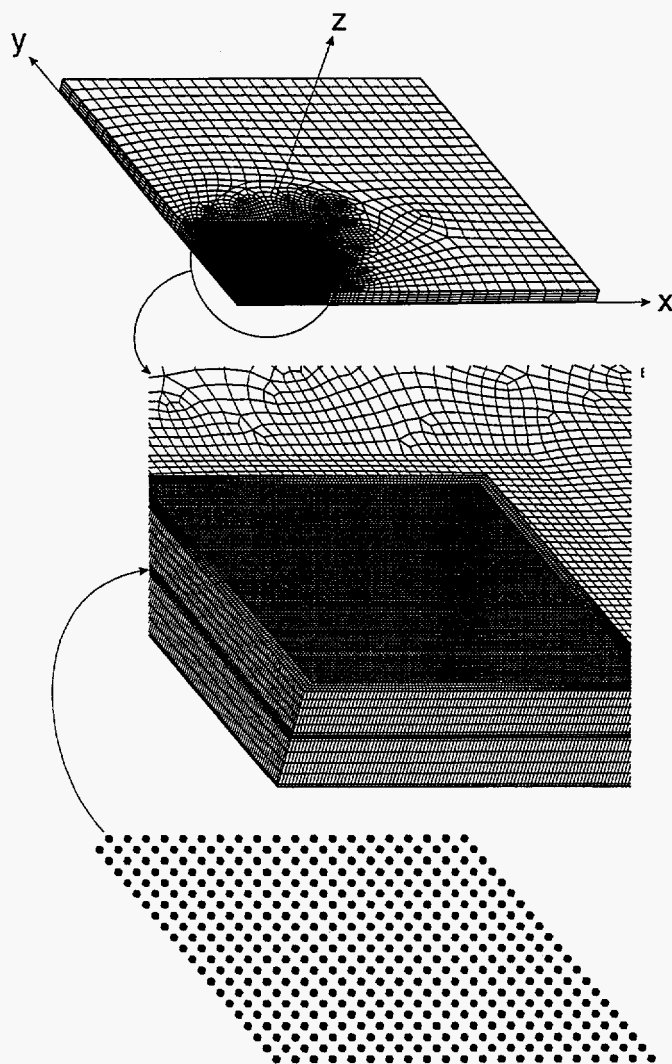Fig. 9 Finite element mesh of ATC4.1 test vehicle quarter section for FEM analysis. Solder ball array elements are shown in enlargement at bottom.

interconnects modeled using three eight-node brick elements per solder ball, to capture the response of the solder.

The solder was assumed to respond as an isotropic temperature dependent elastic/plastic material with power law hardening. This model neglects the time dependent (creep) and microstructural dependent response known to occur in eutectic SnPb solder. The underfill was assumed to respond as an isotropic temperature dependent linear elastic material which neglects time dependent effects known to occur in polymers. The Si die was assumed to respond as an isotropic linear elastic material and the FR-4 substrate was assumed to respond as a temperature dependent, isotropic, linear elastic material.

In the first computation, it was assumed that the assembly prior to underfill was stress free at 180 °C and the temperature was uniformly cooled to 20 °C. In the second computation, the assembly after underfill A was assumed to be stress free at 160 °C and the temperature was uniformly cooled to 20 °C. The thermomechanical response was computed as a function of temperature using the Sandia

proprietary finite element code JAS3D and properties for underfill A in TABLE I. In- and out-of-plane stresses based on the after underfill computation for die locations corresponding to stress cells 1–8 in Fig. 1, are shown in Fig. 10.
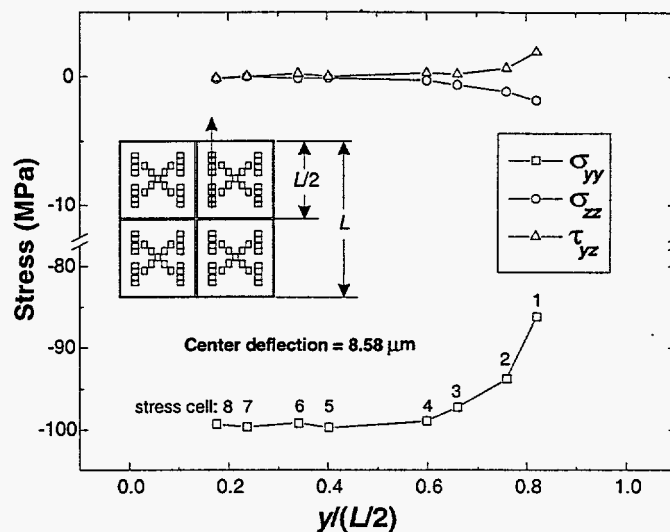

Fig. 10 Stress predictions from 3D FEM. Data points correspond to stress cells 1–8 in Fig. 1 and half width of QUAD is normalized.
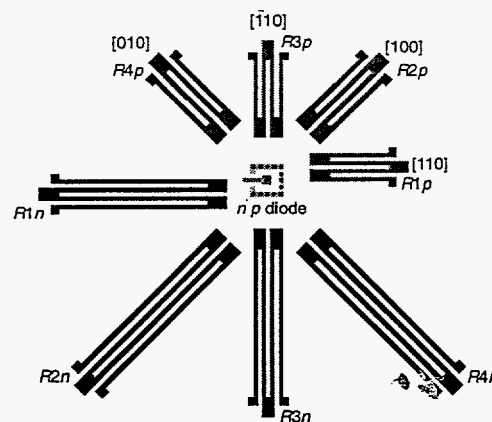
Fig. 11 Stress sensor cell piezoresistor rosette showing numbering and alignment of p-type and n-type diffused resistors with crystallographic axes.

Experimental Stress Analysis

The subject of deriving stress data from experimental ATC04 stress measurements has been discussed extensively in Sweet et. al [8]. Here we provide some summary information to specify the data analysis process. In each stress sensor cell, there are 4 n-type and 4 p-type implanted resistors. They are numbered 1-4 and oriented at; 0, 45, 90, and 135°, respectively, with respect to the chip bottom edge, as shown in Fig. 11. These resistors have nominal values in the range 8-10 kΩ, and stress induced changes typically are in the range 1-10 Ω, or about 0.1-1%. If the resistors are measured at some initial state (0) and again at some final state (f) after an

intervening manufacturing or environmental process step, then the change in certain stress tensor components at the cell site can be derived from the resistor shifts, $\Delta R_i = R_{if} - R_{i0}$, where the index i runs over the resistors in the cell.

It can be shown that all stress data depend on the ΔR values for a given resistor type only through the sum S or difference D of the relative resistor shifts of two resistors oriented 90° apart. These quantities, designated $\delta R_{ij}{}^{S,D}$, where i and j are 1 and 3 (0°, 90°) or 2 and 4 (45°, 135°) and S, D, refer to + and –, respectively, are given by,

$$\delta R_{ij}^{S,D} = \left(\frac{\Delta R_i}{R_{i0}} \pm \frac{\Delta R_j}{R_{j0}} \right). \qquad (1)$$

In the case of δR^D, any shift in resistance values produced by a temperature shift ΔT in the ambient temperature between initial and final measurements cancels out. Thus stresses which depend only on a δR^D value are intrinsically temperature compensated in that they do not require a correction for the temperature shift. In the case of stresses which depend on δR^S values, a correction term, $2\alpha\Delta T$ is required, where α is the relative temperature coefficient of resistivity for the given resistor type, the fractional change in resistance per unit temperature change at constant external stress.

The quantities which may be derived from δR^D measurements are the in-plane shearing stress τ_{xy} and the difference of in-plane compressive stresses, $\sigma_{xx} - \sigma_{yy}$. These quantities are given by,

$$\tau_{xy} = \frac{\delta R_{24}^D}{2\pi_D}, \qquad (2)$$

and,

$$\sigma_{xx} - \sigma_{yy} = \frac{\delta R_{13}^D}{\pi_{44}}. \qquad (3)$$

The quantity π_D in Eq.(2) is given by $\pi_D = \pi_{11} - \pi_{12}$, where π_{11}, π_{12}, and π_{44} are the fundamental coupling constants or "pi" coefficients which relate stress changes to resistance shifts. π_D has a large magnitude only for the n-type resistors, so the diagonal or 2-4 n-type resistor data are used to derive τ_{xy}. In the case of $\sigma_{xx} - \sigma_{yy}$, π_{44} for the p-type resistors has about five times the magnitude of the n-type π_{44}, so we use p-type data to derive the in-plane compressive stress difference from Eq.(3).

One other general relation which may be found for the stress tensor components is given by,

$$\sigma_{xx} + (\pi_{12}/\pi_S)\sigma_{zz} = \frac{\delta R_{24}^S - 2\alpha\Delta T}{2\pi^S} + \frac{\delta R_{13}^D}{2\pi_{44}}, \qquad (4)$$

where $\pi_S = \pi_{11} + \pi_{12}$. Using the π coefficients in Ref. [8], the quantity $\pi_{12}/\pi_s \approx -1.2$. In the case of a flip-chip attachment to a substrate, the magnitude of σ_{zz} is very small relative to that of σ_{xx} at all sensor locations and hence we shall just report data derived from the right hand side of Eq.(4) as σ_{xx}. Eq.(4) is equivalent to Eq.(7) in [8], but the latter equation has an error in the last term on the right where a factor of 2 in the denominator was omitted.

One final point which can be made is that the quantities $\delta R_{24}{}^S$ and $\delta R_{13}{}^S$ are theoretically equal, so a better experimental value for the first term on the RHS of Eq.(4) can be found by using the average value of these quantities to derive σ_{xx}. The expression used to find σ_{xx} is given by,

$$\sigma_{xx} = \frac{\left(\delta R_{24n}^S + \delta R_{13n}^S \right)/2 - 2\alpha_n \Delta T}{2\pi_n^S} + \frac{\delta R_{13p}^D}{2\pi_{44p}}. \qquad (5)$$

In some cases, we are interested in looking at σ_{yy} in addition to σ_{xx}. σ_{yy} can be found by subtracting Eq. (3) from Eq.(5), resulting in the expression,

$$\sigma_{yy} = \frac{\left(\delta R_{24n}^S + \delta R_{13n}^S \right)/2 - 2\alpha_n \Delta T}{2\pi_n^S} - \frac{\delta R_{13p}^D}{2\pi_{44p}} \qquad (6)$$

The π coefficient values and other constants used in the data reduction are given in TABLE II. These values were determined from a recent reanalysis of calibration data and are slightly different from the values reported in [8]. The p-type π_{11}, π_{12}, and π_S values are very small in magnitude and could not be determined accurately. They are not used in any of the calculations reported in this paper.

TABLE II
π AND TEMPERATURE COEFFICIENTS.

Coefficient	n-type	p-type
π_{11} (10^{-5}/MPa)	-26.7	
π_{12} (10^{-5}/MPa)	14.2	
π_S (10^{-5}/MPa)	-12.5	
π_{44} (10^{-5}/MPa)	-16.1	72.2
α (°C^{-1})	0.001473	0.001147
$\Delta T/\Delta Vbe$ (°C/V)	557.2	

Results

Experimental Stress Measurements

Prior to underfill

For the measurement of initial or as-assembled stresses, the initial condition was taken at the wafer level, prior to redistribution and bump processing. The final state was the measurement on the parts after flip-chip assembly to the FR-4 substrates. As discussed above, the differential thermal contraction between die and substrate after cooling from the solder reflow temperature to room temperature produces bending of the assembly with the consequent development of stresses in the die, substrate, and solder attachments. Since the substrate has a larger coefficient of thermal expansion than the Si die, the substrate shrinks more than the die, thus producing a convex or upward bending of
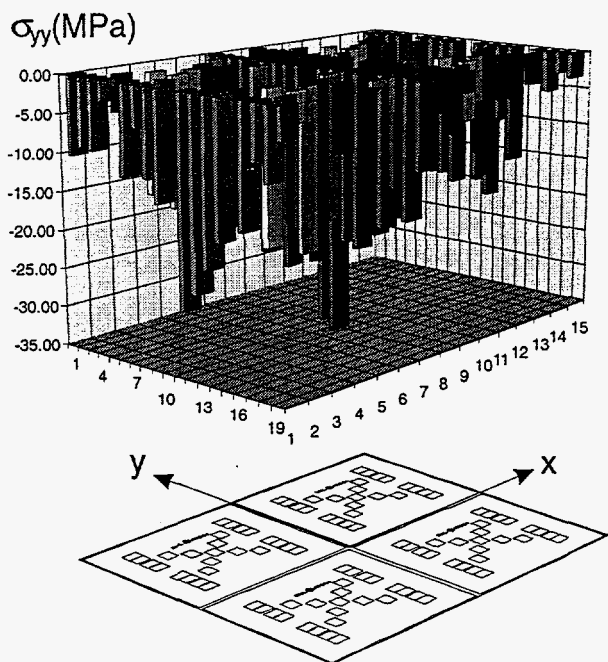
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Fig. 12 Measured distribution for σ_{yy} showing decrease in stress magnitude as $y \to \pm L/2$.

the die, with the bottom or active surface of the die in compression and the top or back surface in tension. We might expect that the outer solder bumps will take up some of the strain energy, with a consequent increase in bending radius along a path from the die center to the perimeter.

This effect is illustrated for a typical part in the measured compressive stress distribution for σ_{yy} shown in Fig. 12. In this plot, from our data analysis software, the rows and columns are on an equally spaced grid and hence the plot somewhat distorts the spatial variation of the stress. The distribution shows a decrease in the magnitude of σ_{yy} as $y \to \pm L/2$, where L = chip width. The distribution in measured σ_{xx} or σ_{yy} stress values across the chip surface is relatively "noisy" or variable from cell to cell as compared with similar measurements made on molded parts.

The assembled part under study has nominal square symmetry. This symmetry condition implies that the variation of a compressive stress tensor component along any diagonal path from the chip center to a corner should be identical. Hence it is useful to examine the variation of σ_{yy} along the four chip half diagonals. A plot of $|\sigma_{yy}|$ data together with an average value curve is shown in Fig. 13. Although there is a fair amount of scatter in the data, there is a clear trend for the stress magnitude to decrease as the diagonal position moves from the chip center to a corner.

An experimental quantity determined more precisely is the in-plane compressive stress difference function, $\sigma_{xx} - \sigma_{yy}$. By symmetry, we expect this quantity to be small at the chip center and along diagonal paths. The maximum variation is expected to be along the chip edge paths, $x = \pm L/2$ and $y = \pm L/2$. A plot of $|\sigma_{xx} - \sigma_{yy}|$ for the four vertical paths through the outer vertical sensor columns, such as the path through cells

18–25, is shown in Fig. 14. The spread in values at each sensor location is relatively small for these data. At the four sensor locations nearest the die center, $\sigma_{xx} - \sigma_{yy} \approx 4$ MPa for this part (not shown in figure), indicating that there is not perfect symmetry in the assembly. This could occur either from an anisotropy in the elastic properties of the substrate or possibly from a misalignment of the die relative to the substrate.
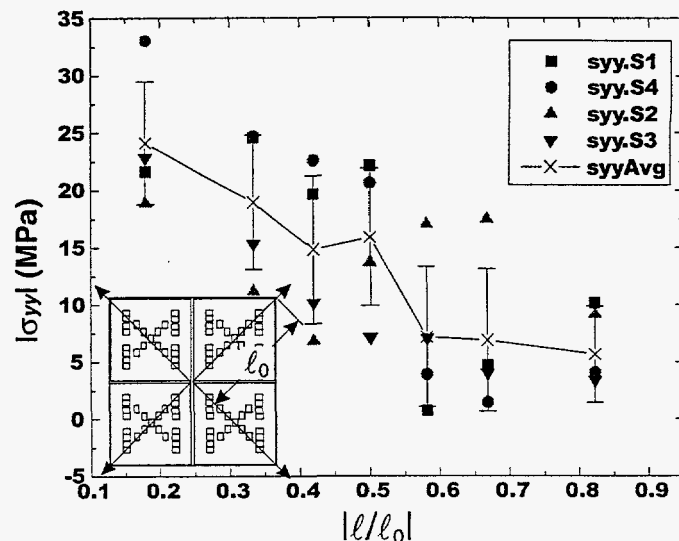

Fig. 13 Variation of $|\sigma_{yy}|$ along the chip diagonals for part Q13 after assembly and prior to underfill. Points represent data along four diagonals, where ℓ_0 = QUAD half diagonal length. Error bars represent standard deviation.
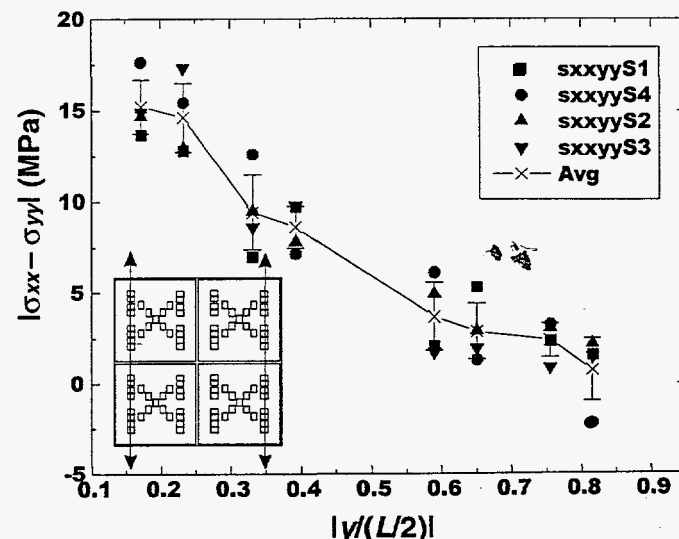

Fig. 14 Variation of $|\sigma_{xx} - \sigma_{yy}|$ along the four vertical edge paths. Solid line is the average value and error bars indicate standard deviation at each sensor location.

The measured in-plane shearing stress, τ_{xy}, is quite small for this part, but predominately positive over the die surface. A 3D distribution plot of τ_{xy} is shown in Fig. 15. The average value of τ_{xy} is ≈ 1.2 MPa. Other parts in the group show a smaller average value than this part, indicating that the cause may be misalignment rather than board anisotropy. A
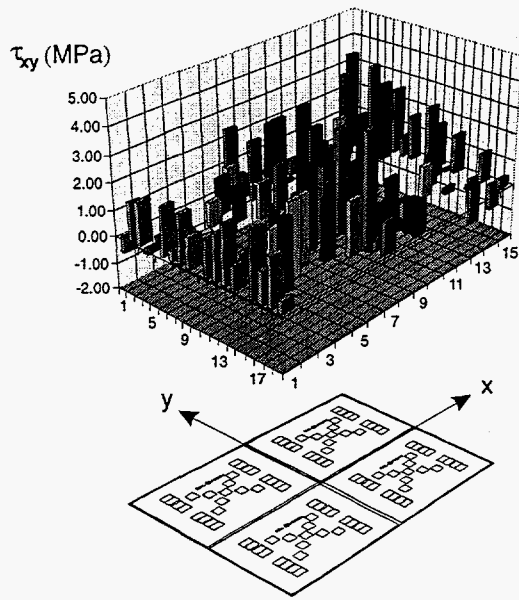
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Fig. 15 Measured shearing stress distribution τ_{xy} for part Q13 after solder reflow assembly to the PC board.

misalignment of chip and board could produce a small shift in the chip bending axes relative to the die edges. The precision of the shearing stress measurement is about ±0.5 MPa, so the positive average value is believed to be a real effect. Another part, M17 showed no significant average value, while part G17 had an average value of 3.2 MPa. Thus, the average shearing stress is small but varies considerably from part to part.

Post Underfill

After underfill, the in-plane compressive stress components become larger in magnitude and much more uniform over the chip surface, indicating that the state of chip bending is also more uniform. The average stress for the center four cells changed from $\approx$ –18 MPa to $\approx$ –90 MPa, indicating a state of increased bending with a smaller radius of curvature. A plot of the measured diagonal variation of σ_{yy} for part Q13 after underfill is shown in Fig. 16.

It is interesting to examine the changes in stress tensor components which occur between the assembly and underfill states because the predictions of these changes is a sensitive test for a finite element model analysis. The change in the in-plane shearing stress, $\Delta\tau_{xy}(x,y)$, is small in amplitude except in the immediate vicinity of the chip corners. A 3D bargraph distribution plot is shown in Fig. 17. Most of the measured $\Delta\tau_{xy}$ values are at the limit of resolution for the technique, about ± 1 MPa, but the stresses in the cells near the QUAD corners go to an amplitude $|\Delta\tau_{xy}| \approx$ 2–4 MPa.

The change in the in-plane compressive stress difference function, $\Delta(\sigma_{xx} - \sigma_{yy})$ is especially interesting because it has a significant variation over the die surface. A 3D bar distribution plot of this measured stress function is shown in Fig. 18. The function peaks at a value $\approx$ 25 MPa along the vertical die edges approximately half way between the QUAD centerline and the top or bottom QUAD y
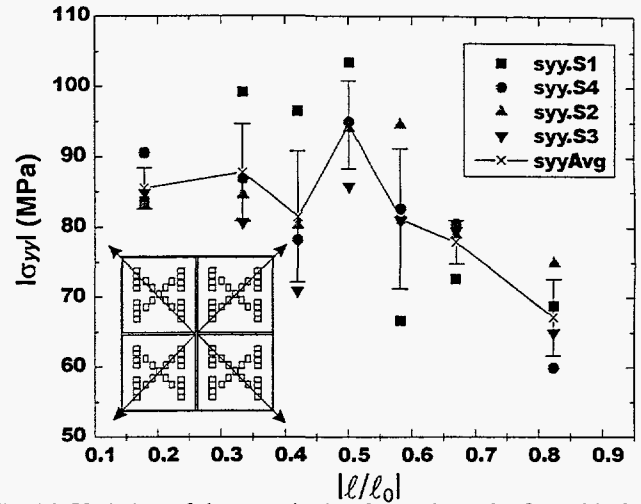

Fig. 16 Variation of the magnitude of σ_{yy} along the four chip half diagonals after underfill. The solid line indicates the average value for the four measurements.

coordinates. In the center it has a minimum with a value $\approx$ 9 MPa. The detailed spatial variation in this measured stress function provides an especially sensitive test or point of comparison for a finite element model. An examination of the in-plane compressive stress difference function with wafer level as the initial state and post-underfill as the final state shows that $\sigma_{xx} - \sigma_{yy} \approx$ 15 MPa at the die center. Since both σ_{xx} and σ_{yy} are compressive in nature, this result indicates that there is more bending (smaller radius of curvature) in the y direction than the x direction. This was also true prior to underfill, but the difference then was only $\approx$ 3 MPa.
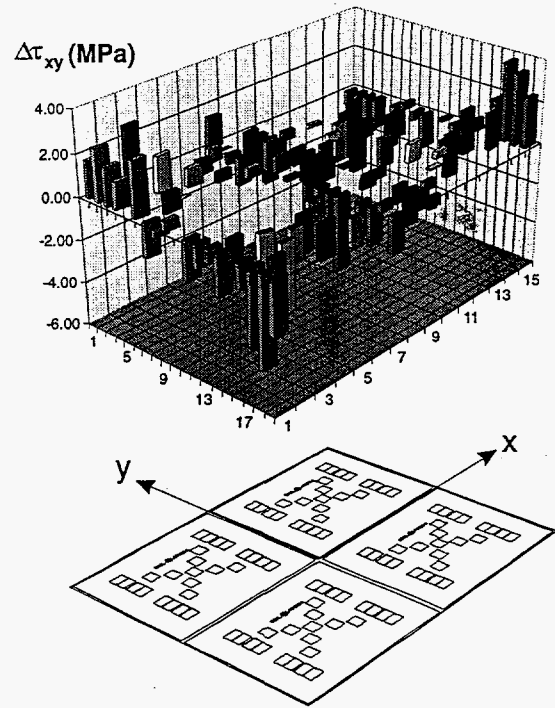

Fig. 17 Change in the in-plane shearing stress between assembly and underfill.
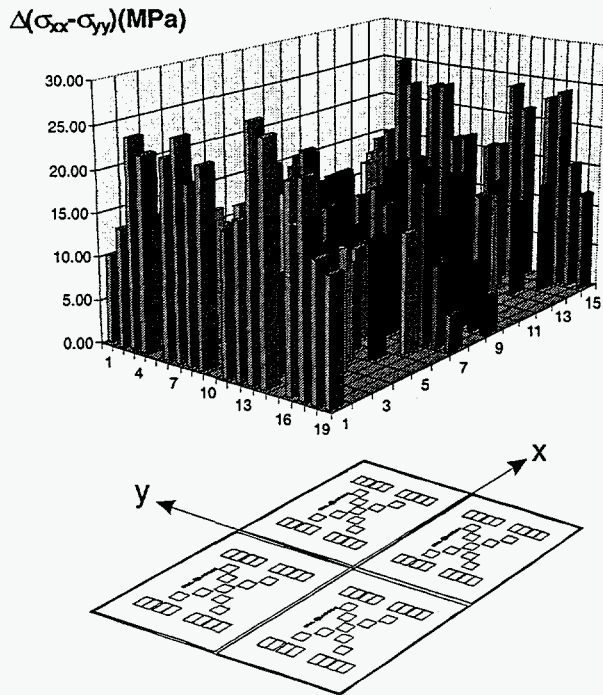
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$\Delta(\sigma_{xx}-\sigma_{yy})$(MPa)

Fig. 18 Change in the in-plane compressive stress difference between assembly and underfill.

To test the hypothesis that the PC board anisotropy in elastic modulus and/or coefficient of thermal expansion was responsible for the residual in-plane compressive stress difference at the die center, some parts were assembled with the die rotated 90° from the usual orientation. On these parts, the value of $\sigma_{xx} - \sigma_{yy}$ at the die center reversed sign, but had approximately the same magnitude, thus tending to confirm the anisotropy hypothesis.

TABLE III
DIE AND SUBSTRATE DEFLECTION. (SD IN PARENTHESES)

	Si		FR-4	
	x-axis (μm)	y-axis (μm)	x-axis (μm)	y-axis (μm)
Before UF (n=25)	1.09 (0.15)	1.46 (0.20)	1.54 (0.49)	1.57 (0.39)
After UF (n=47)	9.21 (0.20)	10.70 (0.30)	8.30 (1.33)	10.01 (1.30)

Comparison of Experimental to Theoretical Calculations

Deflection of die and substrate were measured as described in the previous section. These data are shown in TABLE III as averages and standard deviations, before and after underfill, respectively. An asymmetry is evident in these data along the x and y axes indicating anisotropy in the x-y plane of the FR-4 boards. Deflections averaged ~16% and ~20% greater along the y-axis than along the x-axis, in the die and FR-4 substrate, respectively, after underfill. If these data are analyzed in terms of underfill material, die deflections averaged ~3.5% greater for underfill B than for underfill A parts. These deflection data can be compared to theoretical
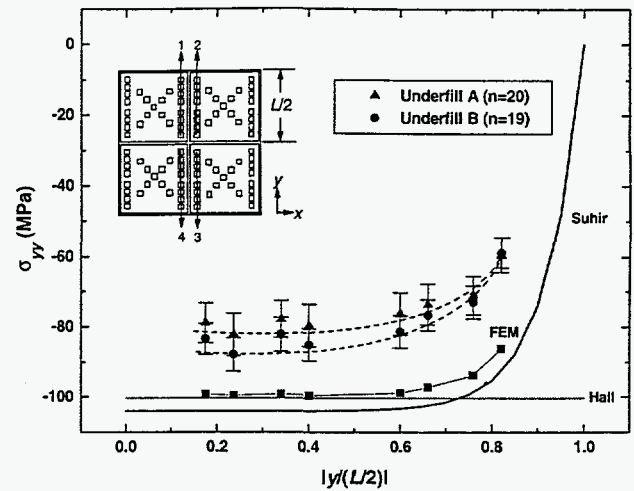

Fig. 19 Comparison of in-plane compressive stress σ_{yy} experimental measurements to theory along paths 1–4, as shown in inset. Dashed lines are curve fits to experimental data.

calculations from Hall (11.2 (A) – 11.3 (B) μm), Suhir (8.8 μm), and FEM (8.6 μm). These calculations did not account for board anisotropy.

Theoretical calculations for the in-plane compressive stress component σ_{yy} are collected in Fig. 19 for comparison with experimental measurements. The experimental data are grouped according to the two underfills A and B and include standard deviation error bars. Each data symbol represents the average of n QUAD measurements, where n is indicated in the legend. Each QUAD measurement was averaged across 4 cells equidistant from the QUAD center along paths 1, 2, 3 and 4 in Fig. 19.

Discussion

The work discussed above demonstrates that many aspects of the measured die surface stresses in an underfilled flip-chip assembly can be successfully predicted with analytical tools. What hasn't been shown is the FEM simulation for the case prior to underfill. The stress distributions and deflection were approximately half the measured values. Plasticity and creep occur simultaneously during cool down from reflow temperature and we clearly need a better constitutive model and possibly more elements per solder ball to accurately predict this behavior, and this is the subject of continuing work. After underfill, the compressive stress variation along vertical paths near the die centerline (Fig. 19) shows quite good agreement across the analytical tools. The absolute accuracy of the calculated σ_{yy} values is limited by a lack of accurate values for the material properties of the underfill and PC board. Subsequent to the FEM calculations, we have obtained improved estimates of some of these parameters, and are working on the remainder. Although the simplified Suhir theory does a reasonable job of predicting both stress magnitudes and deflections, the latter affecting the "shape" of the stress distribution from center to edge, it does not account for underfill material properties. Experimental data show that these properties can not be

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neglected in this particular assembly. It is likely that the "full" Suhir theory will improve the accuracy of these calculations, and we plan to implement it in future work.

The agreement between FEM and Suhir theory shown in Fig. 19 suggests that, for calculation of die stresses after underfill, it is reasonable to represent the underfill-solder ball region as a homogeneous layer with properties of the underfill. The assembly appears to be in a state of near uniform biaxial bending and is thus suitable for stress analysis with simplified analytical models.

The measurements of the in-plane compressive stress difference function, $\sigma_{xx} - \sigma_{yy}$, Fig. 14 and Fig. 18 show that the FR-4 board CTE and/or elastic modulus are anisotropic. The die deflection data in TABLE III show a variation that is consistent with the stress difference data. This anisotropy was not built into the FEM model used for the analysis in this paper, but will be included in future model updates. Our result demonstrates how an experimental measurement of stress can be used to aid the development of more refined and accurate analysis techniques and to validate properties data used in the models.

The measured in-plane shearing stress after assembly, τ_{xy}, in Fig. 15, is small in magnitude, in agreement with the theoretical FEM prediction for this component. After underfill, there are small but measurable changes in this component, as shown in Fig. 17. The FEM analysis also predicts small values, but the accuracy of both the measurements and the calculation are not sufficient at this time to enable a detailed comparison of the values. However, it appears from both experiment and analysis that die shearing stresses are not significant for the system we have studied. This can be compared to the situation for encapsulated parts, where the in-plane shearing stress becomes appreciable in magnitude near the die corners [8].

Conclusions

We have demonstrated that the die surface stress encountered in flip-chip assembly can be measured in detail with a piezoresistive test die. These measurements indicate that, after solder attach of a die to a laminated PC board, there is a moderate compressive stress at the die surface, with considerable stress relief near the die edges. Presumably, this stress relief occurs at the expense of the development of large shearing stresses in the outer solder balls. The underfill process increases the magnitude of the compressive stress but also makes it more relatively more uniform, thus relieving the outer solder ball stresses. More detailed comparisons of experiment and analysis will require improved properties data for the PC board and underfill material.

Acknowledgments

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