Micromachined Sensor Systems on a Chip: The integration of MEMS with CMOS and its applications

J. Smith, S. Montague, J. Sniegowski, C. Barron, J. Allen, B. Davies,
J. Fleming, J. Murray, and P. McWhorter
Intelligent Micromachine Department
Sandia National Laboratories
Albuquerque, NM 87185-1080

R. Howe, B. Boser, A. Pisano, M. Lemkin, T. Roessig, W. Clark, and T. Juneau
Berkeley Sensor and Actuator Center
University of California at Berkeley
Berkeley, CA 94720

KEYWORDS

MEMS, CMOS, Micromachine, Inertial Sensor, Accelerometer, Integration

ABSTRACT

The monolithic integration of micromechanical devices with their controlling electronics offers potential increases in performance as well as decreased cost for these devices. Analog Devices has demonstrated the commercial viability of this integration by interleaving micromechanical fabrication steps with microelectronic fabrication steps to produce a single-axis accelerometer on a chip. A next-generation integrated technology developed at Sandia National Laboratories eliminates many of the constraints associated with Analog's process. This new technology enables the manufacture of complex micromachined sensor systems on a chip. An overview of Sandia's micromachined system-on-a-chip technology along with application of the technology to inertial sensor systems designed by researchers at U. C. Berkeley will be given.

MONOLITHIC INTEGRATION OF MICROELECTRONICS AND MICROMECHANICS

Recently, a great deal of interest has developed in manufacturing processes that allow the monolithic integration of MicroElectroMechanical Structures (MEMS) with driving, controlling, and signal processing electronics. This integration promises to improve the performance of micromechanical devices as well as the cost of manufacturing, packaging, and instrumenting these devices by combining the micromechanical devices with an electronic sub-system in the same manufacturing and packaging process. For example, Analog Devices has developed and marketed an accelerometer[1] which illustrates the viability and commercial potential of this integration. They accomplished this task by interleaving, combining, and customizing their manufacturing processes which produce the micromechanical devices with the processes that produce the electronics. In another

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approach, researchers at Berkeley[2] have developed a modular integrated approach in which the aluminum metallization of CMOS is replaced with tungsten to enable the CMOS to withstand subsequent micromechanical processing. The results of Sandia's implementation of Berkeley's CMOS-first approach have previously been presented.[3]

In order to maintain the modularity of the Berkeley approach but overcome some of the manufacturing challenges of their CMOS-first approach, Sandia has developed a MEMS-first process. This process places the micromechanical devices in a shallow trench, planarizes the wafer, and seals the micromechanical devices in the trench. These wafers with the completed, planarized micromechanical devices are then used as starting material for a conventional CMOS process. This technique is equally applicable to other microelectronic device technologies such as bipolar or BiCMOS. In our facility, both 2 μm and 0.5 μm CMOS technologies on 6 inch wafers are available; the 2 μm process is being used as the development vehicle for the integrated technology. Since this integration approach does not modify the CMOS processing flow, the wafers with the subsurface micromechanical devices can also be sent to a foundry for microelectronic processing. Furthermore, the topography of multiple polysilicon layers does not complicate subsequent photolithography. A high-temperature anneal is performed after the devices are embedded in the trench prior to microelectronics processing. This anneal stress-relieves the micromechanical polysilicon and ensures that the subsequent thermal budget of the microelectronic processing does not affect the mechanical properties of the polysilicon structures. This anneal can affect the doping profile of commonly used epitaxial starting material; however, this effect can be easily addressed by increasing the epitaxial layer thickness of the starting material.

THE EMBEDDED MEMS PROCESS

This process was been described previously in more detail.[4] Figure 1 is a schematic cross-section of the integrated technology. First, alignment marks are etched onto the surface of wafer in order to provide reference locations for subsequent processing. A shallow trench (~ 6 μm for the single-level polysilicon structures described here) is etched in (100) silicon wafers using an anisotropic etchant. The alignment marks from the top surface of the wafer are used as references to generate another set of alignment marks on the bottom surface of the trench.

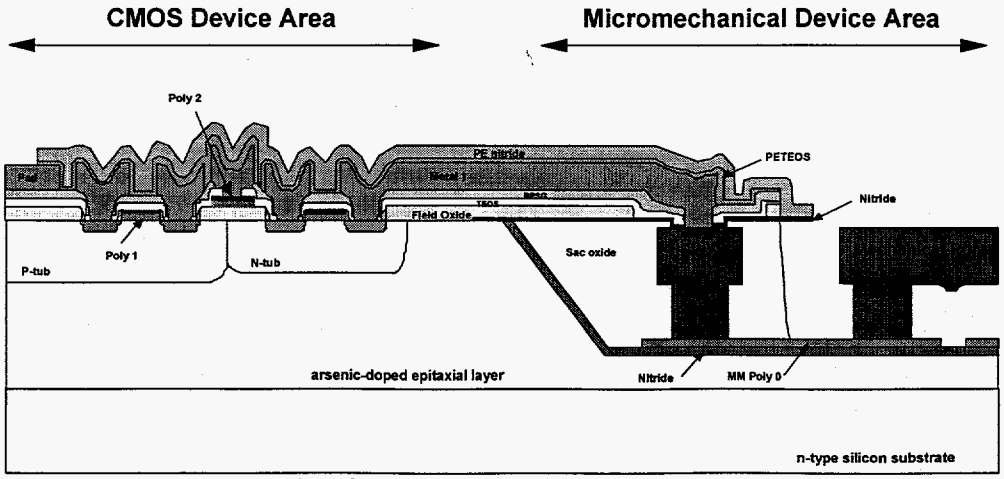

Figure 1. A cross-sectional schematic of the subsurface, embedded MEMS integrated technology.

A silicon nitride film is deposited to form a dielectric layer on the bottom of the trench. Sacrificial oxide and multiple layers of polysilicon are then deposited and patterned in a standard surface micromachining process. Polysilicon studs provide contact between the micromechanical devices and the CMOS; the depth of the trench is sized so that the top of the polysilicon stud lies just below the top of the trench. The shallow trenches are then filled with a series of oxide depositions optimized to eliminate void formation in high-aspect-ratio structures. The wafer is subsequently planarized with chemical-mechanical polishing (CMP). The entire structure is annealed to relieve stress in the structural polysilicon and sealed with a silicon nitride cap. At this point, conventional CMOS processing is performed. The backend of the process requires additional masks to open the nitride cap over the micromechanical layer prior to release of the micromechanical structures.

Photoresist is used as a protection layer over the exposed bond pads during the release process. The slow etching of the undoped, densified glasses used as sacrificial layers and the ability of this photoresist to withstand long, HF-based etches is presently a factor that imposes limits on the design rules used for spacing of release access holes in the structure.

Figure 2 shows a cross-sectional view of an anchor point for the MEMS device within a trench after planarization. The silicon nitride dielectric layer, the ground plane polysilicon, the micromechanical polysilicon and the sacrificial/planarizing layers are easily seen in this Scanning Electron Micrograph (SEM). Completed MEMS next to their controlling CMOS are shown in Figure 3.

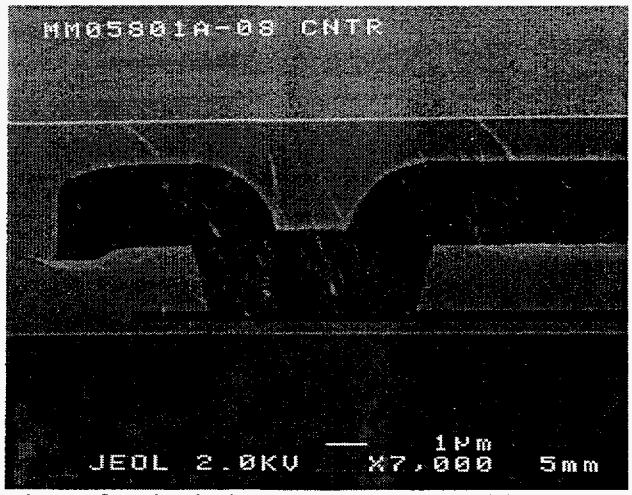

Figure 2. A cross-sectional view of a single-layer polysilicon (with ground plane) structure in a trench. The trench has been refilled with oxide and planarized using chemical-mechanical polishing. This planar structure is ready for standard CMOS processing.

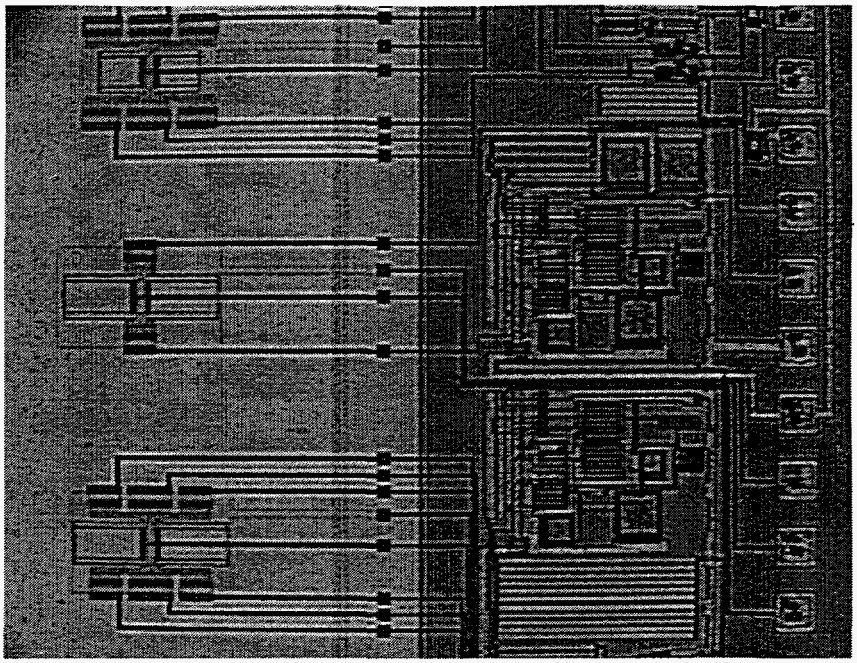

Figure 3. Surface-micromachined polysilicon resonators built in a trench alongside their CMOS sensing electronics. The marks on the bonding pads were caused during wafer-level testing.

This integration process is not limited to the single-level polysilicon process described here. This process can be used with more intricate micromechanical processes such as the three-level polysilicon technology previously developed at Sandia.[5]

INERTIAL SENSORS

One of the principal commercial products utilizing surface-micromachining is inertial sensors as illustrated by Analog Devices' ADXL150[6] and Motorola's XMMAS40GWB[7]. These accelerometers find their primary application as airbag-deployment sensors in the automobiles, but are also being used as tilt sensors or shock sensors. (In the following discussion, please not the use of *g* for the unit of Earth acceleration and g for gram). The Motorola device is a +/- 40*g* (full scale) single-axis accelerometer with a noise floor of 400 mg (400 Hz bandwidth, peak) and has an analog output.[7] The Analog Device accelerometer is available as either a single- (ADXL150) or dual-axis device (ADXL250), has a +/- 50*g* full scale output, an analog output, and a noise floor of 10 mg (100 Hz bandwidth, rms).[6] It should be noted that the use of peak vs. rms noise specifications along with the difference in bandwidth specifications on each device do not lead to a direct comparison between the devices.

The application of these types of accelerometers to inertial measurement units is limited by the need to manually align and assemble them into three-axis systems, the resulting alignment tolerances, their lack of on-chip A/D conversion circuitry, and their lower limit of sensitivity. In order to overcome some of these limitations, a three-axis, force-balanced accelerometer was designed at U.C. Berkeley[8] for the integrated MEMS/CMOS described earlier in this paper. This three-axis accelerometer system-on-a-chip is shown below in Figure 4.

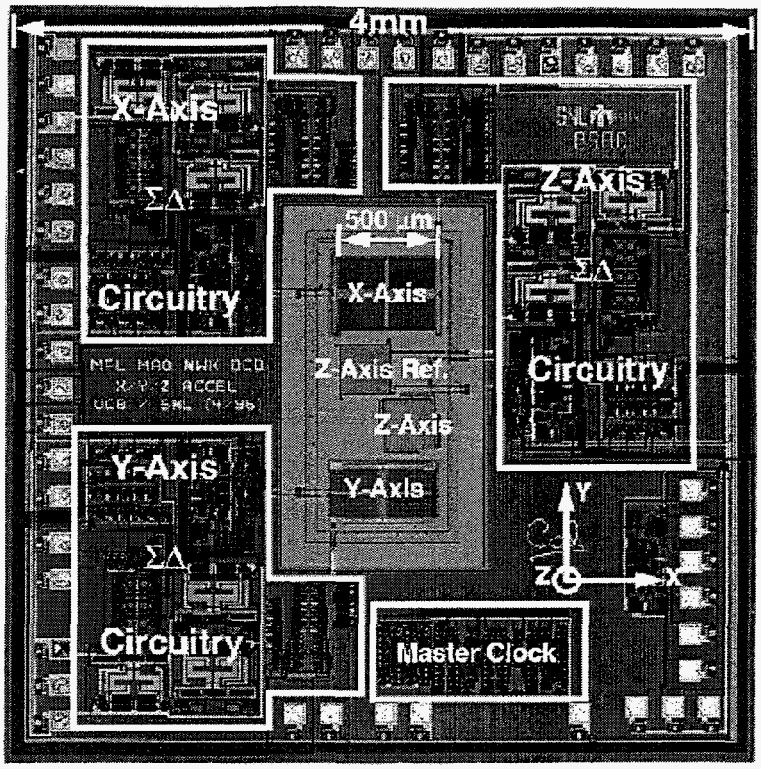

Figure 4. Three-axis accelerometer micrograph with labeling of functional units.

The performance of the device is summarized in Figure 5 below. Approximately an order of magnitude increase in sensitivity is seen over the commercial devices described previously. The accelerometer chip also includes clock generation circuitry, a digital output, and photolithographic alignment of the sense axes. Thus, this system-on-a-chip is a realization of a full three-axis inertial measurement unit that does not require manual assembly and alignment of sense axes.

Parameter	X-axis	Y-axis	Z-axis
Noise Floor (μg/√Hz)	110	160	990
Dynamic Range (dB, 100 Hz Bandwidth)	84	81	70
Proof Mass (μg)	0.38	0.26	0.39
Resonant Frequency (kHz)	3.2	4.2	8.3
Power Dissipation (mW)	45	45	45
Sampling Rate (kHz)	500	500	500

Figure 5. Performance of the three-axis accelerometer as reported by Lemkin, et al.[8]

Although the bias stability of this accelerometer system is yet to be assessed, these noise numbers indicate that this system can now begin to find application in military systems such as

- tamper detection
- stability control

•attitude heading reference
•short time of flight navigation
•environmental sensing for weapon safing and arming

and commercial applications such as

•automotive control
•automotive diagnostics
•automotive navigation
•virtual reality environmental sensing.[9]

A combined X/Y-axis rate gyro and a Z-axis rate gyro have also been designed by researchers at U.C. Berkeley and are presently being fabricated in this new manufacturing process to yield a full six-axis inertial measurement unit on a single chip. The estimated size for this system is approximately 4 mm by 1.0 mm.

In addition to this three-axis accelerometer, a single-axis, high-shock accelerometer[10] has also been built using the integrated process described previously. This device shown in Figure 6 is mechanically designed to monitor high shock environments to 50 kg, but demonstrates saturation of its electronics at 15kg.

Nominal parallel-plate capacitance for the 50 kg sensor is 100 fF at a 2 μm gap. This capacitance level is constrained by the necessity to interface with sensor electronics developed for a previous application. The nominal capacitance requirement and nominal gap spacing translated into a plate overlap area of 22, 500 μm^2 (Å 150 μm x 150 μm square area). The resonant frequency of the sensor suspension is constrained to be greater than 100 kHz to accomodate sampling frequencies and the induced vibration caused by the sampling voltage electrostatic attractive force. A range of 0.4 to 0.6 for damping ratio to obtain adequate response and robustness was also a design target.

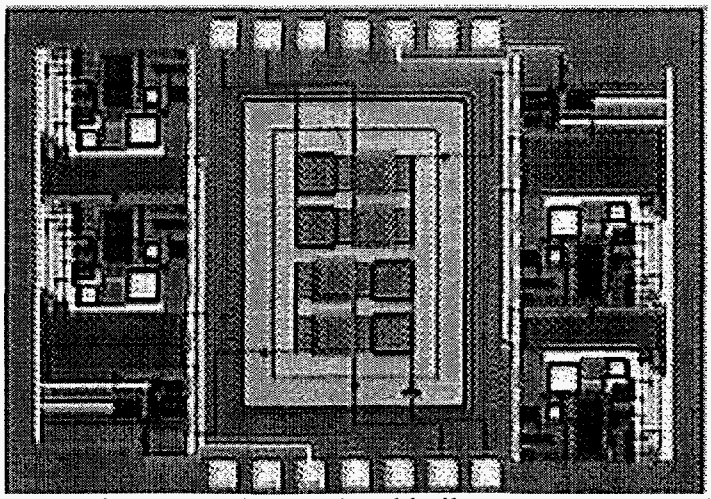

Figure 6. A robust, wide-range accelerometer designed and built at Sandia for monitoring high shock environments.

CONCLUSIONS

The manufacturability of a technology that integrates surface-micromachined polysilicon structures with microelectronics in a modular fashion has been demonstrated. This technology does not impose additional limits on the size, thickness, or number of layers of the micromechanical polysilicon structures. The modularity of the process allows changes to be made to either the micromechanical process or the microelectronic process without affecting the other process. Excellent CMOS parametric data and yield along with the application of the process to multi-axis inertial sensors has been demonstrated.

ACKNOWLEDGMENTS

The process development engineers, operators, and technicians of Sandia's Microelectronics Development Laboratory should be acknowledged for their contributions to the process development and fabrication of these devices. Programmatic support from Michael Callahan of Weapon System 2010 and Tom Hitchcock of Joint DoD/DOE Munitions Technology is greatly appreciated. Sandia is a multi-program laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy under contract DE-AC04-94AL85000.

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