Environmental Evaluation of Surface Mounted Devices (SMD)

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Abstract

We evaluated the comparative reliability of solder interconnections used for Leadless Chip Carriers (LCCs), J-leaded, and flat-pack hybrid microcircuits mounted on FR-4 glass epoxy printed wiring boards (PWBs). The board assemblies, with solder attached microcircuits, were repeatedly thermal cycled from -65 to +125°C. We recognize that this temperature range far exceeds most testing of assemblies. The purposes of these tests were to evaluate worst-case conditions and to obtain comparative information. Identical PWB assemblies, using these three component types, were subjected to both thermal shock testing (1 cycle every 42 minutes) and temperature cycle testing (1 cycle every 3 hours). The double testing evaluated the differences in stress application and evaluated the potential of replacing slow transition, expensive temperature cycle testing (which has been an industry standard for years) with the much more rapid thermal shock testing. In these tests, Parylene-C coatings significantly extended the lifetime to first failure on the leaded devices. Further, vias (through-hole interconnects) that were unfilled, but coated with Parylene-C , did not experience any failures in either test series. (There were 582 Parylene-C coated vias in each test.) Vias that were solder filled did not fail. Unfilled, uncoated vias that experienced failure, did not fail again once they were solder filled. [There were 1164 non-Parylene-C coated vias in each test sequence; none were initially solder filled, but all were subsequently solder filled when failures (at about 450 cycles) started showing up.]

For very high-g shock environments, we recommend our designers use the Leadless Chip Carrier, installed using a fat-filet concept. For more benign environments, leaded designs provide greater extended time to failure (cycles). For primarily real-estate utilization on the PWB, we recommend the J-lead package over the flat-pack design.

Further correlation of failures, comparisons to the amount of oxygen and nitrogen the solder joints were exposed to, plus the mode of test (cycle vs. shock) need to be done. Since the start of these tests, there has been industry data presented that show that solder joints exposed to 100% nitrogen fail more quickly than those in an oxygen environment. We have documented the amount of nitrogen in the thermal shock chambers, which has a liquid nitrogen direct injection cooling system for the cold cycle, and found that the amount of oxygen in our chamber not only varies over time, but is actually much higher than expected.

Contents

Introduction

Surface-mounted devices have provided the electronics industry with a higher circuit density capability and often higher frequency operational characteristics than the former, through-hole, all-leaded device technologies. Leaded, hybrid, microcircuitry packages (flat-packs) have been used for years, in our applications, typically with a 45° to 65° bend in the leads to mitigate stresses that are created as a result of the to thermal mismatch between the microcircuit alumina substrate ($4 - 6 \times 10^{-6}$ in./in./°C) and a printed wiring board (PWB) ($16 - 18 \times 10^{-6}$ in./in./°C). (Note: In this article, PWB and MLB for multilayer boards are synonymous and used interchangeably.) The lead bends required for these hybrids uses a lot of valuable real estate. This is critical in today's designs that are requiring ever more efforts to miniaturize physical sizes. Subsequent industry efforts led to the Leadless Chip Carrier (LCC), which was mounted directly on the printed wiring board without any lead at all. The solder joint was used to absorb the thermal stresses created and this technology worked fairly well for small (<1/2 in.) devices. Larger devices, placed in temperature cycling environments, experienced early interconnect (solder joint) failures in well under 100 cycles of -65 to +125°C.

The low-profile LCC was almost mandatory, in our applications, for extremely high-g environments such as artillery shells and earth penetrators. This led to our development of process-controlled, soldering technologies at Sandia/California that minimized voids in the solder fillets and provided a fat, bulbous solder fillet for printed wiring board installations of LCCs. This fat-fillet concept was proven to repeatedly provide thermal stress reliability's exceeding 100 thermal stress cycles (-65 to +125°C) for LCCs up to 3/4-in. square. This assembly process is more expensive to apply than the standard solder paste and reflow assembly operations typically used in industry, and while reported and in use for some high-reliability applications, it has not been incorporated in any large scale operations we are aware of.

Industry then came out with the "J" leaded device to replace the LCC designs. This style of lead virtually used the same footprint as the heralded LCC, but provided the necessary mechanical separation (height) from the board surface to allow for stress absorption in the lead. Although conceptually this appeared to be the long-awaited remedy for early thermal stress cycle failure, it initially didn't prove to work as well as expected. As a result the early J-leaded packages received some bad press. Many of the solder joint cracking and early separation anomalies observed turned out to be primarily a result of lead material and design. New designs use a fairly malleable lead (which must be handled carefully) compared to the rigid Kovar of some of the initial designs, and today's designs achieve much more lead flexibility. Requirements for extensive use of some form of hybrid package for Sandia-unique designs and a need to minimize the real estate required for component mounting on a board assembly, spawned the solder interconnect test sequence and processes that are the subject of this article.

The need to minimize physical space and maximize the amount of electronics in that space with long-term reliability requirements was a driver to not only use J-leaded devices, but to evaluate how these devices faired in long-term, temperature cycling environments compared to the well-known, flat-pack characteristics. The tests were only slightly expanded to include some LCCs in order to establish a peg-point for comparing other (previous) LCC temperature cycling data to these new tests.

Test Environments

Figures 1 through 3 depict the environment the loaded board assemblies were subjected to during the tests.

Temperature Cycle Profile

Each cycle of the temperature cycling profile required 3 hours to complete. Figure 1 shows four separate traces that are actual data taken from thermocouples on four of the assemblies, equally spaced, in the test chamber.

The assemblies in thermal cycle were stationary, suspended in the chamber, and the airflow circulation was baffled (diffused) to minimize the variation of temperature change on any single assembly.

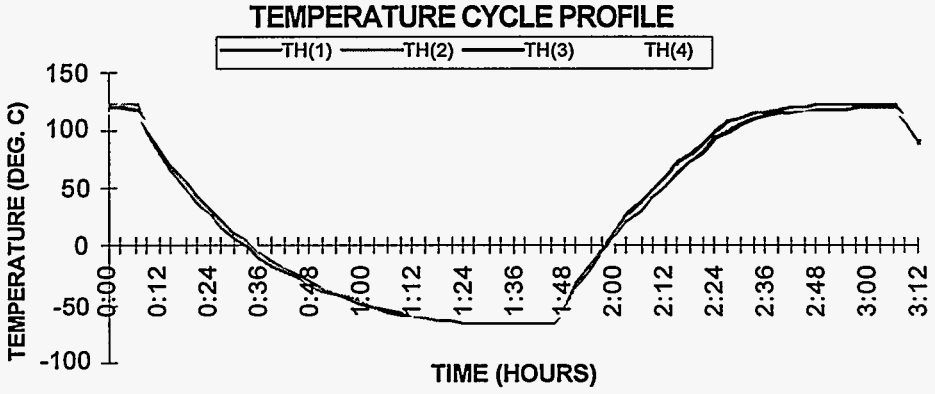


FIG. 1

Thermal Shock Profile

Assemblies exposed to thermal shock cycling were suspended in a vertically movable chamber that quickly transitioned between a hot cell (+125°C) and a cold cell (-65°C). This transition time was on the order of three seconds and the assemblies were allowed to dwell there until the *assembly* temperature had stabilized for at least 9 minutes (see Figure 2). Typical exposure time for these assemblies was approximately 21 minutes at each extreme (about 43 minutes per cycle). Baffles were also used here to minimize the airflow directly hitting the assemblies in test and to better equalize the cooling and heating in the chambers. Note that there are still some wide separations in the thermocouple data, especially during heatup times. This is primarily attributed to the geometries of the test chamber and the differing methods of heating and cooling. Heating was accomplished with air moving over electrical heating coils and being blown into the chamber. Cooling was accomplished by direct injection of liquid nitrogen, which was converted into a cold gas before being injected into the chamber, as needed, to maintain temperature.

Oxygen Levels

We measured and recorded the oxygen levels in the thermal shock chamber. This was to evaluate the differences in environment on expected variations in test results between the two test methods. The temperature cycling assemblies were exposed to atmospheric conditions (approximately 20% oxygen) throughout the testing. Thermal shock testing exposed the assemblies to variations in the oxygen content during test. One would expected that the nitrogen, injection-type cooling would create a nitrogen rich test environment throughout the test cycling. This was not the case however, as shown in Figure 3.

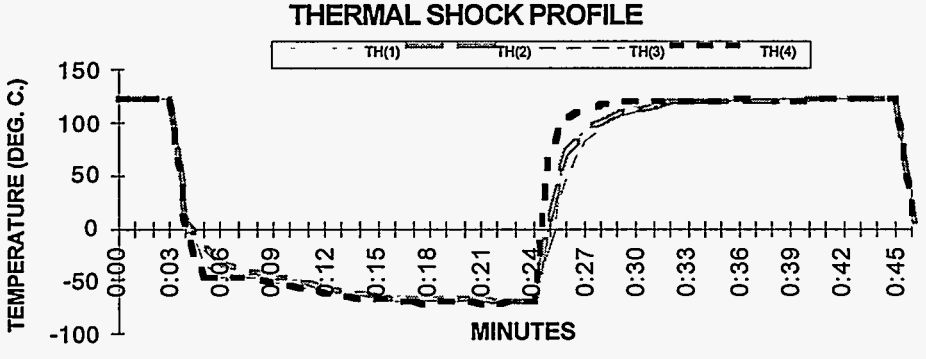


FIG. 2

Note that the oxygen level during the cold cycle is quite low, as expected, ranging from 1 to 6%. This is due to injecting nitrogen directly into the chamber for cooling. The oxygen level rises however once the chamber moves into the heat compartment, and is well above 10% during much of the high temperature portion of the cycle. This suggests that the heat compartment is not as well sealed as expected and the circulation fan may even draw in some outside air during its operation. The effects of this variable are still to be analyzed. But based on other, recently

reported data where test specimens cycled in a pure nitrogen environment had failed more quickly than like specimens cycled in an atmospheric environment, we expect to see differences.

Test Parameters

Components Tested

Table 1 lists the components (hybrid microcircuit packages) and lead configurations used in this series of tests.

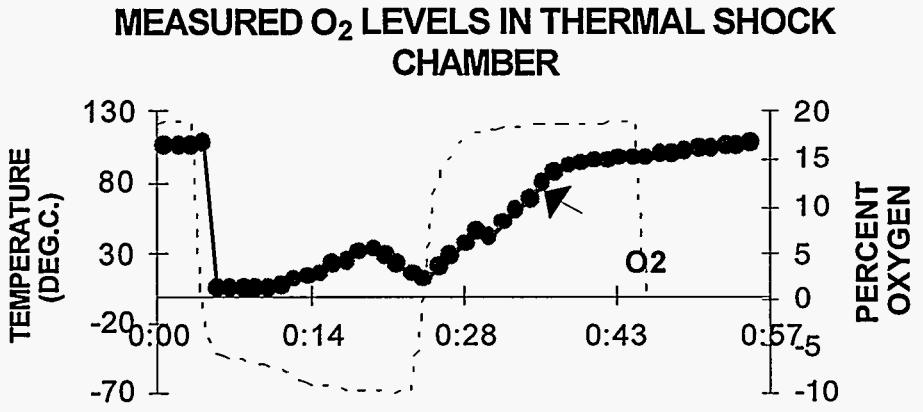


FIG. 3

Table 1. Components and lead configurations used in the tests

Component		Leads[a]				Package resistance[b] (ohm)	PWB[c] footprint width (in.)
Type	Size (in.)	No. of leads	h (in.)	th (in.)	w (in.)		
LC64	0.70 × 0.70	64	0.005	NA	NA	6.6 – 8.1	0.785
LC68	0.96 × 0.96	68	0.005	NA	NA	13.5 – 14.7	1.05
JL44	0.65 × 0.65	44	0.046	0.009	0.018	5.8 – 7.8	0.775
JL68	0.95 × 0.95	68	0.046	0.009	0.019	9.8 – 12.2	1.05
FP64	0.90 × 0.90	64	0.042	0.010	0.018	11.0 – 11.9	1.30
FP84	1.15 × 1.15	84	0.076	0.006	0.010	15.4 – 16.8	1.625

[a]Lead height (h) is the flexible height of an unsoldered lead, or for the LCCs (LC64 & LC68), the height above the PWB. Th is thickness and "w" is width of the nickel-iron alloy leads.

[b]The resistances vary considerably between packages due the highly resistive, long run, thick-film conductors used in the package manufacture. Thick-film conductor runs of over 0.25 in. are typical for all but the two smallest package sizes. Resistance variations within a given package type appear to be variations in these same conductors as multiple gold wire jumpers were placed on the pad attach points, inside the packages, to create a series circuit within the packages.

[c]These are the typical board space(s) required to install the various package styles used in these tests. The measurements shown are across a square footprint pattern

Test Assembly

Layout

We prepared each microcircuit package by adding two gold jumpers (1 mil diameter) across every other set of internal lead connection pads. (See Figure 4.) The associated leads were then jumpered externally with copper jumpers on the remaining alternate lead sets to create a series set of interconnects for each lead solder attachment.

One of each type microcircuit package (six packages total) was pretinned and soldered onto a multilayer printed wiring board (MLB) assembly for test using Sn62 solder. Duplicate assemblies were tested in thermal shock and temperature cycling, with the exception of one later experiment using Sandia-developed,[1] epoxide-type, conformal coating that was only exposed to thermal shock testing. Additionally, we made two special assemblies, one for thermal shock test and one for thermal cycle testing. Each assembly only contained one of each of the LCC packages (two LCCs per assembly) with industry standard solder fillet sizes (referred to in this article as "shallow fillets" and LC68SHLW and LC64SHLW in the charts). The LCCs were primarily included in these tests for comparison purposes and to relate the leaded devices to an extensive data base already on hand for LCC testing. Each microcircuit package had alternate internal and external jumpering to effect a single, serpentine circuit through every soldered interconnect of each package.

Figure 4 is not to scale and is shown without the sealed lid for clarification of the interconnect concept. Wide variations in device resistance were observed (Table 1) primarily the result of the variations in length and density of the package thick-film conductors extending from the solder joint, or external lead, into the package (the dark black traces of Figure 4). By comparison, internal resistances were milli-ohms due to the 1-mil diameter gold jumper wires bonded onto nickel-gold plated internal pads of the package. Likewise the external jumpers were in the milli-ohm range because of nominal 0.025 in. wide copper conductor traces, 0.0015 to 0.002 in. thick on the printed wiring boards. Not all external, MLB jumpers were made on the surface as shown. Some were deliberately positioned inside the MLB assemblies and interconnected with the use of plated-through vias (holes drilled through the board, then electroplated with copper to complete the electrical interconnect). There were 291 plated-through vias on each board assembly in the test.

The packages were located on each assembly as shown in Figure 5 and interconnected in series as mentioned above. This configuration allowed 100% monitoring of every solder joint, on each assembly, with a single set of electrical leads. In reality, a set of leads is made up of four separate wires, two for power (or current to the assembly) and two to monitor the voltage across the assembly. An external, current-viewing resistor was interconnected such that the instantaneous current flowing through the assembly

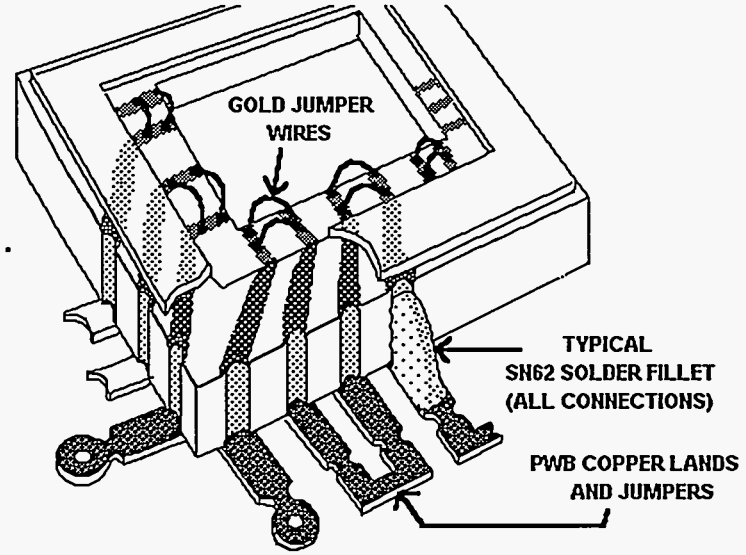
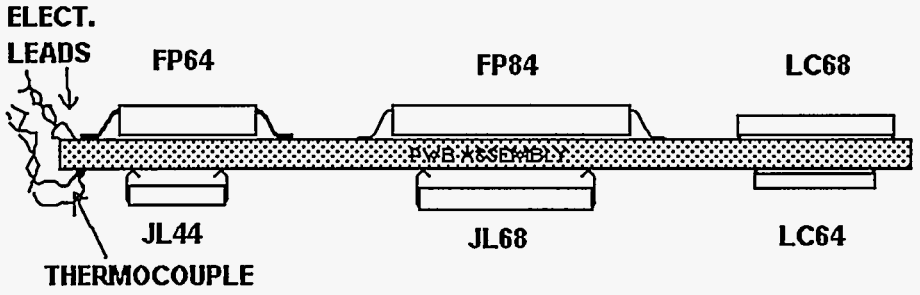


ILLUSTRATION OF SERPENTINE INTERCONNECT METHOD USED

FIG. 4

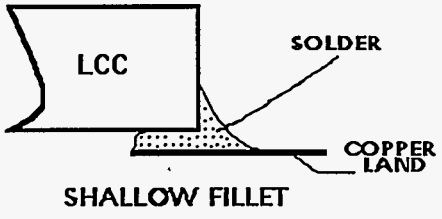


COMPONENT ORIENTATION
FIG. 5

was also recorded. This four-wire method of monitoring allows for very precise calculation of the resistance of the assembly at any given time and reduces the errors of lead resistance change, in the powering leads.

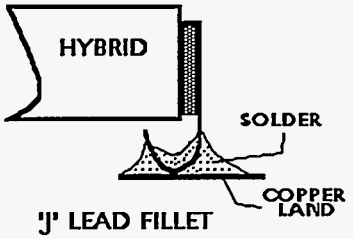
Solder Fillet Control

Experience has shown that the type of solder used and the attention given to the solder fillet formation itself plays a significant role in long-term reliability of PWB-to-component interconnects exposed to wide variations in temperatures. Figure 6 depicts the component lead types and solder interconnects evaluated in this series of tests (the via interconnect is explained above and is not shown).



SHALLOW FILLET

FIG. 6a

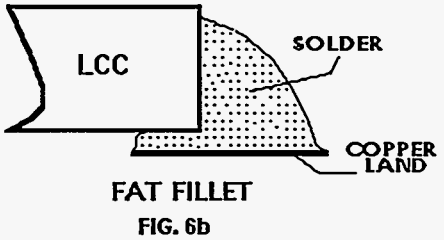


'J' LEAD FILLET

FIG. 6c

Figure 6 shows the typical, industry-standard solder fillet and is referred to in this article as a "shallow" fillet (Figure 6a). This reference is simply due to our typical use of a process-controlled, "fat" or bulbous fillet (Figure 6b) on all high-reliability applications involving soldering of LCCs since the early 1980s. (Appendix A gives the process steps for achieving fat fillets with minimized voids.) It was found at that time that this fat fillet would repeatedly provide LCC solder interconnection reliability sufficient for our applications, especially in high-g environments. The standard or "shallow" fillet was included in this series of tests only as a reference point for data taken during extensive, previous testing of the shallow and fat fillets (using Sn62 solder) for LCC applications.

The J-leaded packages, or hybrid cases, used in these tests were of a type shown in Figure 6c. The conductor was attached to the side of the package, as shown, which allowed the lead to flex from the package downward during thermal excursions of the assembly. The lead-height, discussed in Table 1,



FAT FILLET

FIG. 6b

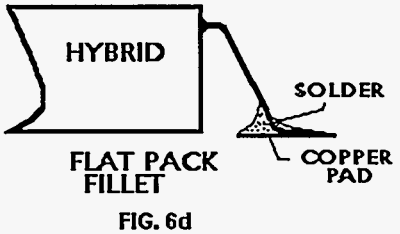


FIG. 6d

then is the unrestrained height from where the lead exits the package to the MLB (for both the J-lead and flat-pack). The flat-pack hybrid cases (Figure 6d) had the leads formed at a nominal angle of 60° and with nominal 0.010-in. radius bends. Currently, this is often referred to as a "gull wing attachment." The flat area on the copper pad was 0.050 in. minimum, and

the lead was not allowed to extend beyond the edge of the mounting pad (skew). All solder fillets (Sn62) were deliberately made to be on the "fat" side, that is, no skimping of solder, but not excessive Previous testing has shown that flat-pack leads soldered with this fat inner fillet have survived temperature cycling longer than those soldered with minimal fillets. We assumed that this was probably a good starting assumption for the J-leaded devices as well, and their solder fillets were made fat also.

Results

Figure 7 displays the test data resulting from this series of tests. Each data set is discussed in turn. This first graph is very busy (crowded) but shows at a glance the comparison of first failure to last failure for each type of interconnect, plus a direct comparison of time to failure for each device type can be quickly made. Failure for these data is a 10% increase in resistance or an electrical open in the circuit. (Appendix B shows all the failure data.)

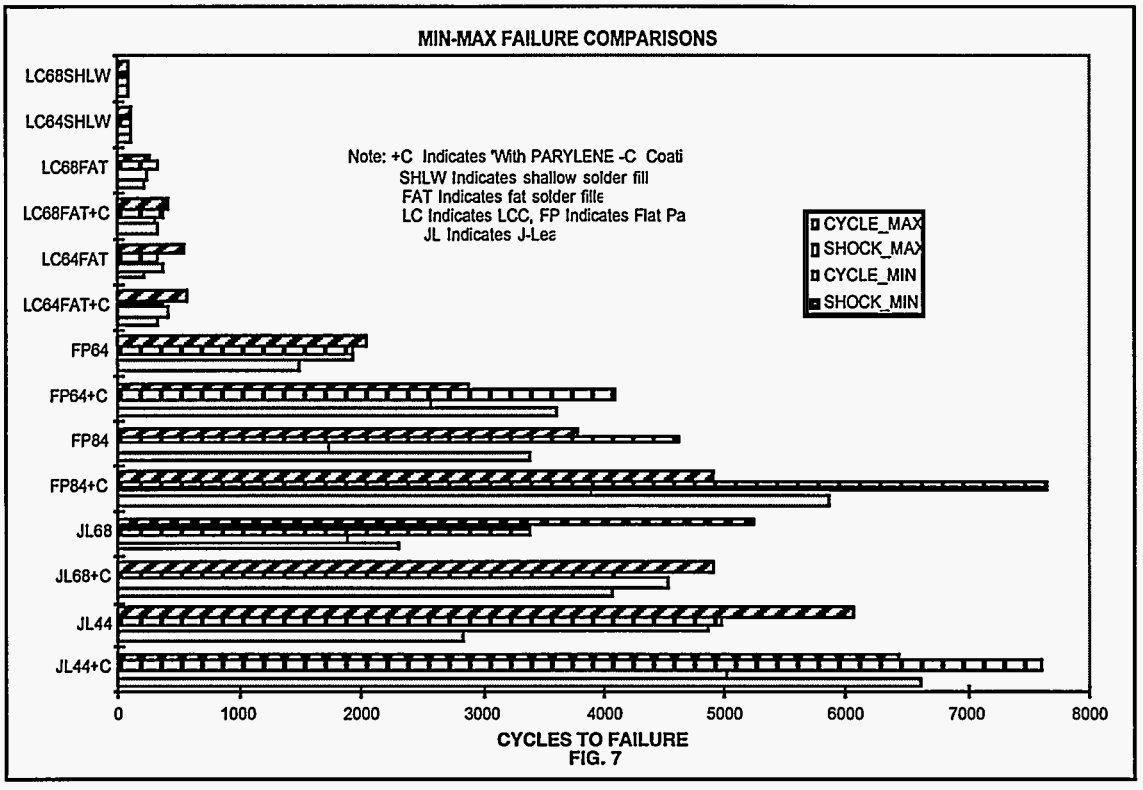


FIG. 7

Solders Used

Sn62 (Sn62/Ag2/Pb36) solder was used exclusively for this test series, with the exception of the PWB solder coating, Sn63 (Sn63/Pb37), as supplied on the copper traces. All preforms and pretinning operations were Sn62 solder. Sn62 has been shown[2] to reduce the migration of the lead and tin in the solder, creating lead rich areas that appear to promote cracking sites, during temperature cycling tests. Both the LCCs and J-Lead packages were installed onto the assemblies using vapor phase reflow (225° C inert atmosphere) technologies and the flat-pack devices were added afterward using resistance soldering techniques. The resistance soldering technique required individual soldering of each lead to the PWB assembly.

For many of our applications, a survival of at least 100 temperature cycles or shock cycles, using the previously stated temperature range, has become a minimum acceptable level of performance. For other applications, especially where thermal cycling is expected to occur, in the field, over many years, these data will prove useful in determining the package of choice.

The "+C" in the labels of Figure 7 depict data for Parylene-C coated samples. One can quickly observe the beneficial effects of the conformal coating used here. These data, concerning conformal coatings, will be covered later in the discussion. "FAT" as used in Figure 7 labels, refers to the previously mentioned fat, or bulbous, solder fillet used on LCC installations.

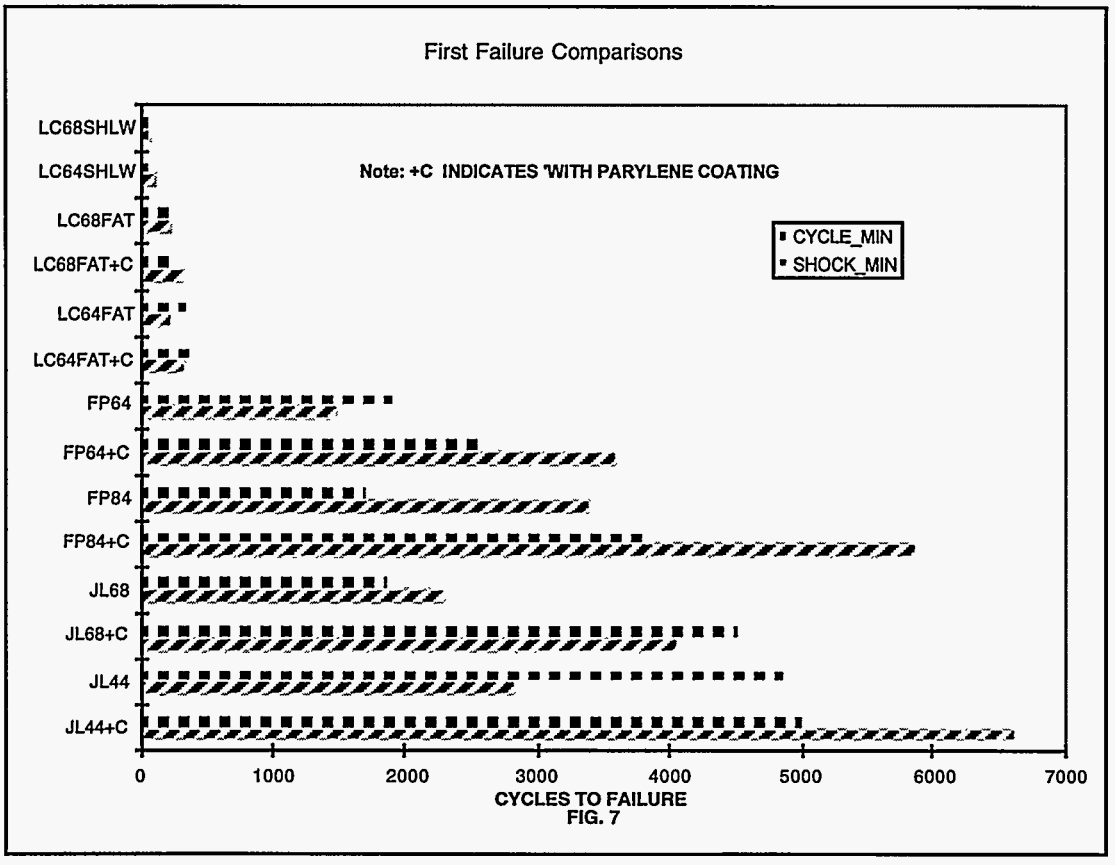


FIG. 7

For most of the designs we deal with here at Sandia, the reliability based on time to *first* failure is most important. These data are shown in Figure 8. Here, comparisons of the observed effects of temperature cycling tests as opposed to thermal shock testing are shown. Not all of the first failure points appear to make sense (based on package size and interconnect type) at first. Some of these differences will be explained later in the section(s) covering the type of interconnect, and some analysis, such as the effect of Oxygen and Nitrogen at temperature need much more analysis. It is our desire to discuss uncovered material more thoroughly in a final report.

Note in Figure 8 that the fat fillet used on the LCC installations all meet the 100-thermal-cycle criterion discussed previously. These are often the packages of choice for telemetries used in artillery shells and penetrators. We have re-used telemetries in 155-mm artillery shells, using LCCs with fat fillet interconnects, up to five times without failure. The devices in those tests experienced over 18,000-g during setback in firing and were simply soldered onto standard FR4 (glass epoxy) PWBs. All leaded hybrid packages we initially tested in these same environments experienced multiple modes of failure.

It is important to note that in *all* cases the Parylene-C conformal coatings extended the observed number of cycles to first failure. This too is discussed in more detail under the conformal coatings topic later. Variation anomalies observed in the flat-pack data (where it appears that the larger, the 84-lead package survives better than the smaller 64-lead flat-pack) are shown to be a function of lead geometries and the data are explained later under the Coatings section.

Leadless Chip Carrier Data

Leadless chip carrier (LCC) type hybrids have played a significant role in supporting our harsh environment telemetry development programs. Determining the cause of early failure modes, caused by premature cracking of the solder fillets, and establishing a reliable method of making solder interconnects onto glass epoxy MLBs has allowed the use of this technology for these programs. There are always tradeoffs of course. The difficulty of cleaning under LCCs—a nearly impossible task of inspection for entrapped material under the packages and the extra cost of using special installation processes—are the obvious down side considerations. The mere fact that these were the only type of hybrid device packaging that would repeatedly withstand the type of g-forces discussed above made them invaluable to some programs. These devices were only included in this series of tests as a peg-point for comparison of much existing data on LCC solder joint reliability to the

temperature cycling data on leaded devices used in these tests. Also this was the first time we have had the opportunity to compare thermal shock effects directly with temperature cycling effects. Any qualitative results of this last comparison, other than the graphic depiction of the data, are beyond the scope of this article.

Figure 5 depicts the component orientation on each assembly. Figures 6a and 6b illustrate the shallow (industry standard) and "fat" fillet formation discussed in this article. Table 1 provides the physical data for each LCC, including the general package size, footprint on the assembly, resistance, and lead data.

It is important to document that prior testing of 64-lead LCCs, installed with fat fillet technologies, also included installations where up to 50% of the mounting pads on the printed wiring assembly were removed prior to assembly (thus only 1/2 the normal "hold-down" capability). Additionally one full assembly received 100 thermal shock cycles (all leads, on all devices, attached) and then both assemblies were flown in the above, high-g environment. Neither worst-case test failed . This data is included only to provide some insight into a known and tested operational envelope for future application of the technology.

It is clear from Figure 9 that the fat fillet concept is advantageous for leadless chip carrier applications. Parylene-C coating provided some improvement, but not as significantly as can be observed for leaded devices. One can envision that the larger fillet transfers more stress into the underlying pad and results in some stress relief through exercising the elastic modulus of the buttercoat resin of the printed wiring board. Likewise, some have stated the obvious, that any crack must propagate further before a failure is observed. Whatever the cumulative mechanism, it works, and the goal of achieving 100-thermal-shock cycles before has been repeatedly met.

J-Lead Data

There is great interest, for our Sandia applications, in the J-lead package design. The footprint (real estate required for mounting) is very similar to the LCC, but the design allows for easier cleaning and inspection of the entire solder joint compared to an LCC package installation. This intrinsic feature of easy cleaning and inspection is extremely desirable for high reliability designs where an assembly must remain in the field for tens of years and still function. The flexibility of the leads suggests that the component should also withstand environmental thermal cycles very well. The need to evaluate this concept and compare the data to the flat-pack hybrid packages we have used at Sandia for years was the primary purpose of this series of tests. All the lead attachments (solder joints) were made with rather fat fillets as depicted in Figure 6c. This fat fillet, especially at the heel of the attachment to the substrate (printed wiring board), has proven to be a key element in flat-pack survival over extended periods of thermal cycling in our environments. For this reason this concept was adopted for all our leaded attachments in this series of tests.

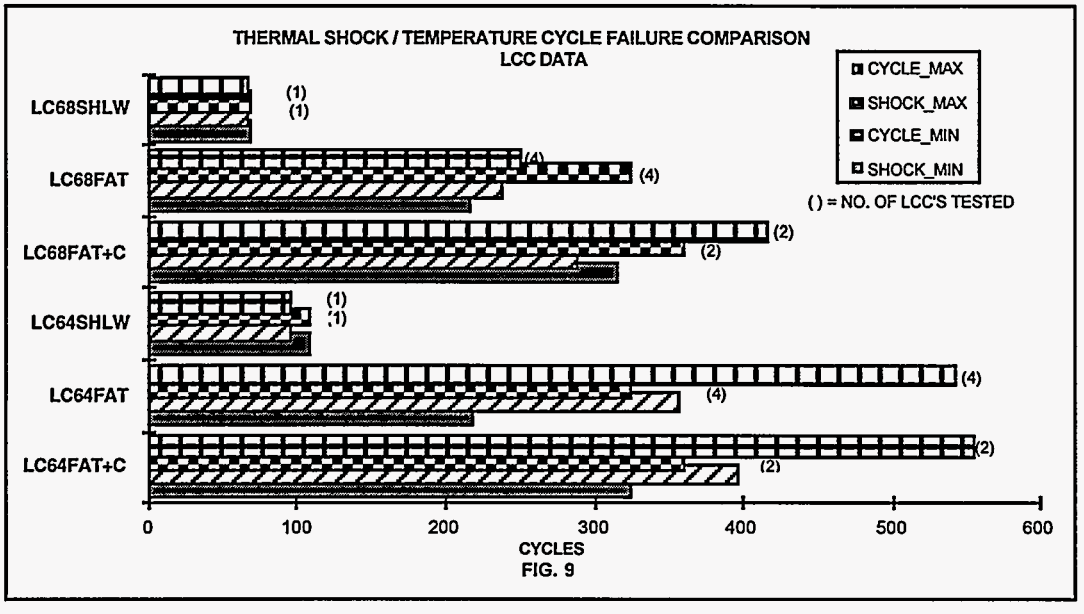


FIG. 9

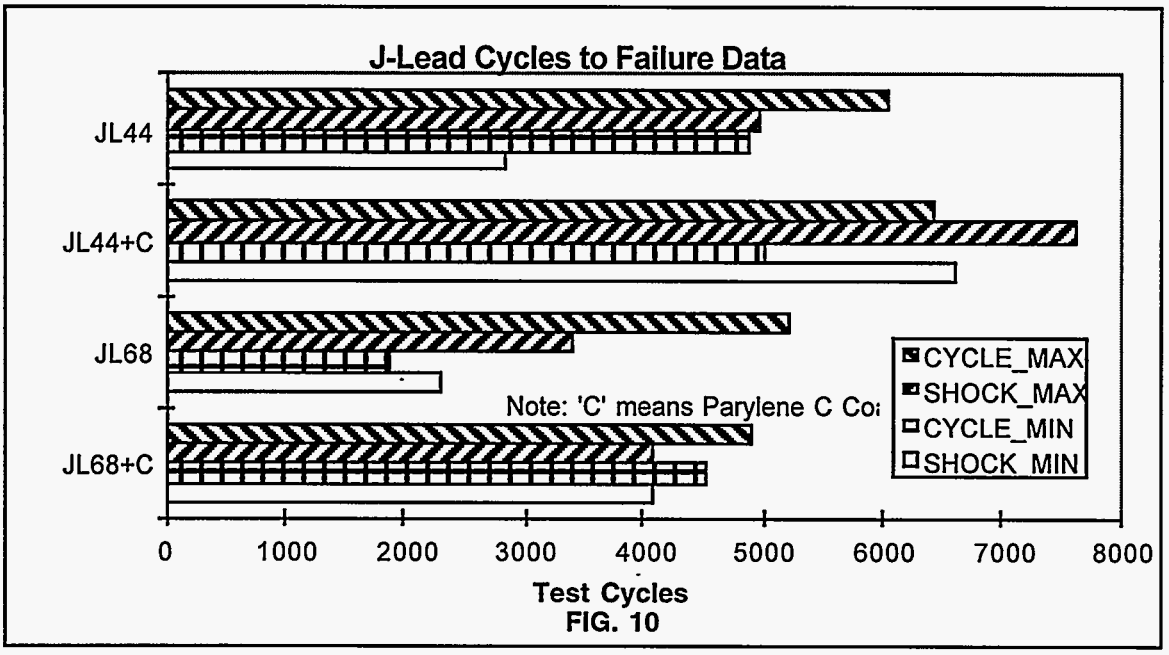


FIG. 10

Figure 5 depicts the component orientation on each assembly. Table 1 provides the physical data for each J-lead device including the general package size, footprint on the assembly, resistance and lead data.

Figure 10 depicts the resultant data for the J-leaded devices used in these tests.

For our purposes, the Shock Min and Cycle Min data are considered the most important. These are the first failure points for each device under test. For each test method (temperature cycling and thermal shock), there were two devices of each lead type under test that were Parylene-C coated and four of each lead type that had no conformal coating applied. The number of cycles to final failure (Max indications) are included to indicate the spread from first to last failure . Note that "Max" means the "first" failure of the last device of the series under test. The Parylene-C coating, application details and thickness are discussed later and will not be covered here. It is important to note that the Parylene-C coating increased the times to "first failure" in *every* case, often significantly.

Figure 11 is a Weibull plot of observed failures of the J-lead devices during thermal shock cycling. Note that for each device type (44 lead and 68 lead) there is a significant increase in time to failure of the Parylene-C coated parts. One is not overly enthusiastic on projections made from only two data points, but the consistency of the trend cannot be ignored. The improvement in time to failure has also been shown independently by others since the start of these tests.

Note that the spread of failure data (Parylene-C coated vs. non-coated) is not as great for the parts in temperature cycling. The time to first failures is still

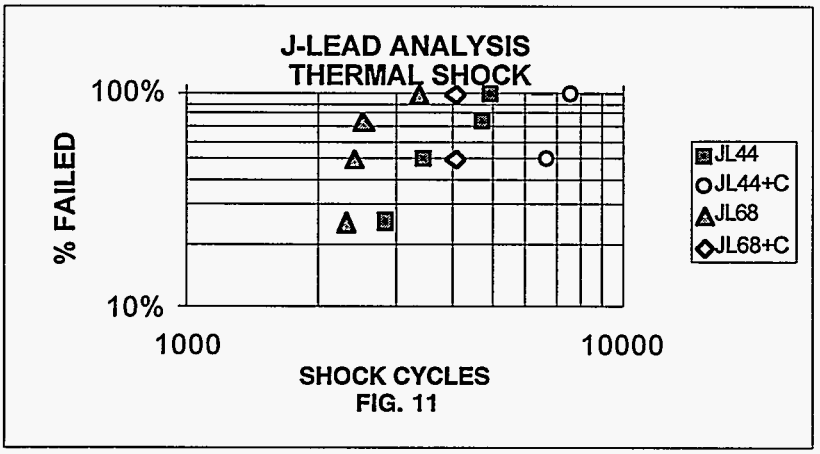


FIG. 11

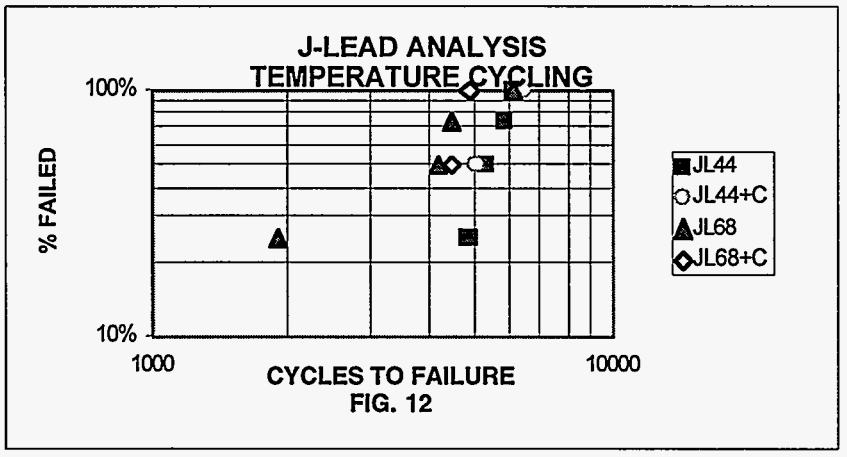


FIG. 12

extended when using the Parylene-C coating. It is felt that aging and working of the solder joints plays a significant role in the observed difference. Assemblies exposed to 3000 cycles of thermal shock have seen 2250 hours of environmental change, whereas those exposed to 3000 cycles of temperature cycling have seen 9000 hours of environmental change! Observed aging effects of the solder joints after 2850 thermal shock cycles, are very dramatic and are discussed under conformal coatings later in this article. Overall, the J-lead type interconnects are considered to have performed very well in these tests.

The comparison of J-lead data and Flat-pack data are illustrated further in the next section.

Flat-pack Data

Flat-pack type hybrid microcircuits have been used for years, mounted on glass-epoxy printed wiring boards, in our Sandia designs. They have performed extremely well and reliably using strict assembly criterion. A key factor in installing the flat-packs for our applications is control of the angle allowed for the bend of the leads. We require that the leads be bent to an angle of 45° to 65°, with a preferred angle of 60°. The bend radius is approximately 10 mils (0.010 inch) and a fat, solder fillet at the heel is mandatory. Figure 6d depicts the lead forming and solder attachment used for these tests. Figure 5 depicts the component orientation on each assembly. Table 1 provides the physical data for each flat-pack used, including the general package size, footprint on the assembly, resistance and lead data.

The flat-pack requires a significant amount of real estate on the printed wiring board for mounting, as shown in Table 1. In today's drive for ever smaller packaging of electronics, this becomes a serious limitation. The need for a microcircuit package, with a smaller footprint on the assembly, yet with the reliability of the flat-pack, is an ever present problem. The J-lead package appeared to potentially fit this need, but the interconnect reliability compared to that known for the flat-pack needed to be tested. The test data for the flat-pack hybrids used in these tests are shown in Figure 13.

Figure 13 shows the data for both thermal shock and temperature cycle testing. For each method of testing (temperature cycling and thermal shock), there were two devices of each type in the "coated" category (+C) and four of each in the uncoated category tested. The +C indicates assemblies with the Parylene-C coatings. Note that the coating extended the time to failure in every case. "Max" depicts the spread of first interconnect failure, of each device type. (For example, there would be four failure data points for FP84.) It is interesting to note that the smaller, 64-lead device typically failed earlier than the very large 84-lead device. This is primarily due to the shorter and much fatter leads on the 64-lead device. The longer, spindly (by comparison) leads of the 84-lead device were much more compliant and appear to stress the solder interconnects less. Again, the aging of the solder, depicted later under Conformal Coatings, has to play a part in the failures when one starts achieving several thousand cycles (or hours) of tests.

Figure 14 is a Weibull plot of the flat-pack failures observed during thermal shock. Note the decided increase in time to failure of the Parylene-C coated interconnects. The consistent, early failure of the short, thicker leads of the 64-lead flatpack is also obvious. Failure analysis of the leads as a function of lead length and cross-sectional area are consistent with beam flexure models for these data taken up to 3000 hours of test, but inconsistancies appear after that point. It is felt that aging and other mechanisms within the solder fillet play a greater role after this time. The visual effects are obvious and are shown in Figures 16 and 17. (Micrographic, cross-section data are not available for this article.)

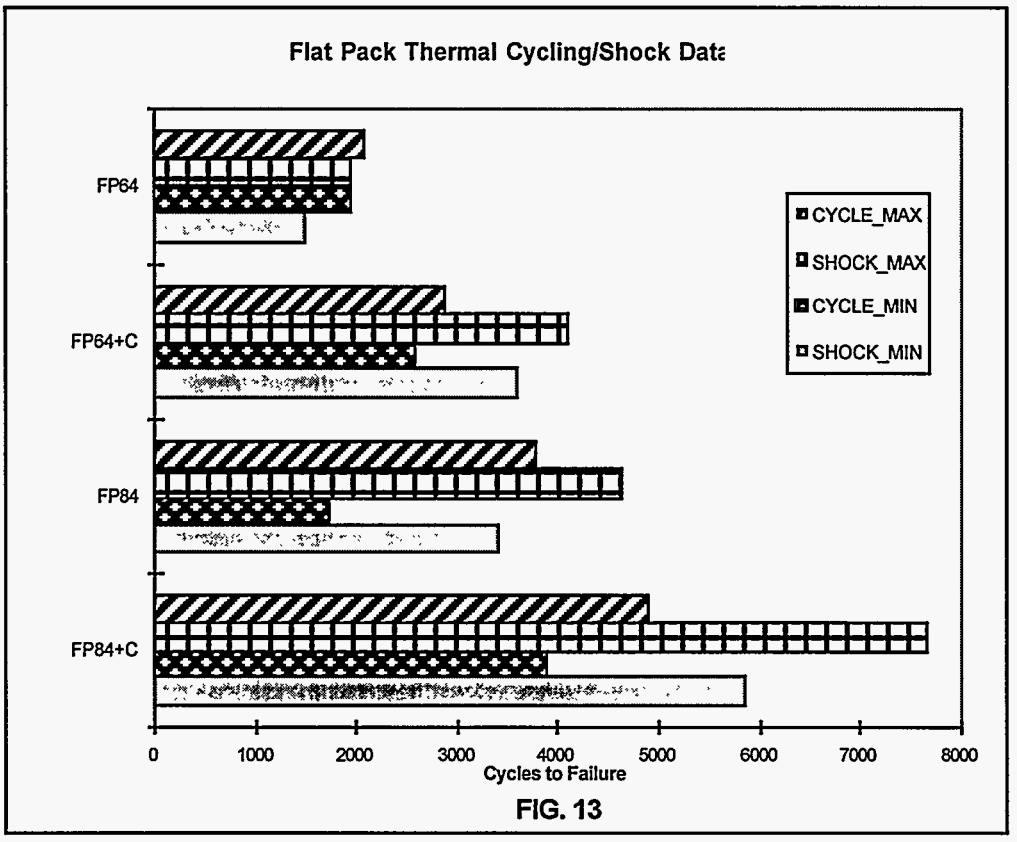


FIG. 13

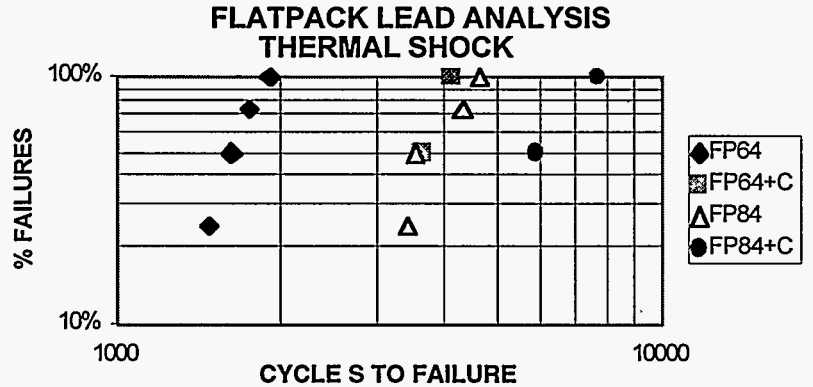


FIG. 14

Figure 15 is a Weibull plot of the flat-pack failures observed during temperature cycling. Here we observe more scatter in the uncoated assemblies, but the increase in cycles to failure of the coated assemblies is still significant and apparent.

Figure 7 quite clearly shows the favorable comparison between the flat-pack and J-lead device interconnects for both the temperature cycling and thermal shock testing. Both quite clearly are desirable for applications other than high stress or high-g environments. The much smaller footprint requirement, ease of cleaning and inspection of the interconnects tend to makes the J-lead a very desirable alternative to the flat-pack for most of our applications.

Via (Through-hole) Interconnects

Observations of via failures in these tests were so striking that they must be mentioned. As stated in the Layout section, there were 291 vias in each 6-layer multilayer printed wiring board assembly. As a result, we had 582 vias with only Parylene-C coatings in each type of test and 1164 vias, uncoated in each type of test (thermal shock and temperature

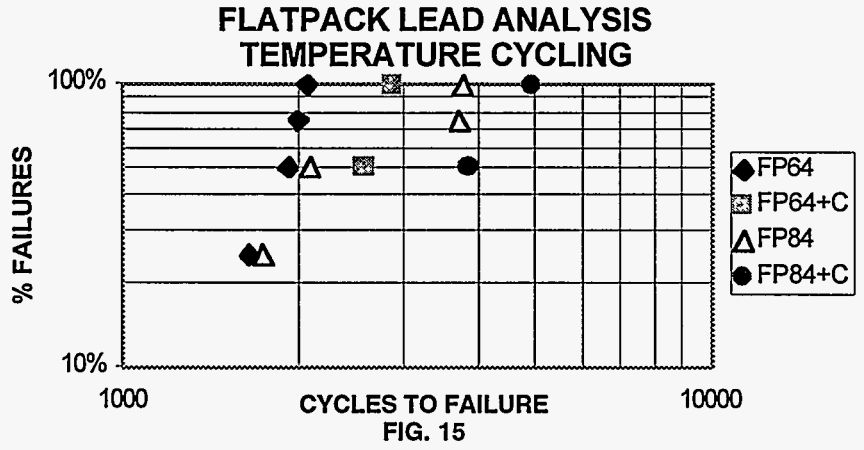


FIG. 15

cycling). There were *no* observed failures in any of the Parylene-C coated vias during the entire test. Failures in uncoated vias were observed. One failure was observed at cycle 364 (one via in one assembly in temperature cycling, 1092 hours of test), and two failures at cycle 442 in thermal shock (one via each on two different assemblies, 317 hours of test). After the failure was observed in the temperature cycling test, all the uncoated assemblies were removed from the test, all the vias were solder filled and the assemblies returned to test. *No* further via failures were observed over the remaining life of the test, which amounted to thousands of additional cycles. All vias in the epoxide coated board were solder filled prior to coating and no failures were observed throughout the 4864 thermal shock cycles the assembly was exposed to.

Post-test analysis (cross-section measurements), of the PWB vias, verified that all copper plating thicknesses, etchback etc. met the requirements of MIL-P-55110D. Since all the boards were of the same lot, no obvious variations were expected, or observed.

Another striking observation was documented at thermal shock cycle 2,850, when the assemblies were removed for a routine visual examination. The solder coatings and fillets on the non-Parylene-C coated assemblies appear checked and very granular (Figure 16). The same coatings and fillets on the Parylene-C coated assemblies looked as bright and shiny as the day they were made (Figure 17). This obvious difference in aging effects of the solder is credited with the absence of any via failures in the coated assemblies used in these tests.

Conformal Coatings

Two types of conformal coatings were used during these tests. Parylene-C , approximately 1/2 to 1 mil (0.001 inch) in thickness was used on those indicated assemblies throughout the testing. The results speak for themselves. There appears to be a clear benefit to the soldered interconnects treated with this coating.

We also used an Epoxide coating, developed at Sandia Albuquerque, on one assembly. All the vias on this assembly were solder filled prior to coating. (This coating is sprayed on and UV cured.) This one extra assembly was introduced late into the test sequence in the thermal shock environment. Comparative failure data, using one of our typical conformal coatings, were desired as a comparison to the extended lifetimes we were observing with the use of Parylene-C. The comparative data are shown in Figure 18.

In figure 18, the Parylene 1st and Parylene 2nd notations refer to the failures of specific devices on their respective assembly. There were two Parylene-C coated assemblies in thermal shock testing, but only one assembly with the epoxide coating. The failures of the first assembly and second assembly devices are included only to show the spread observed in the time (cycles) to failure One can then visually quickly compare the performance of the two coatings. The spread of failures of the uncoated assemblies are not included here to keep the clutter down on this chart, but can be seen in Figure 7. It is apparent that the

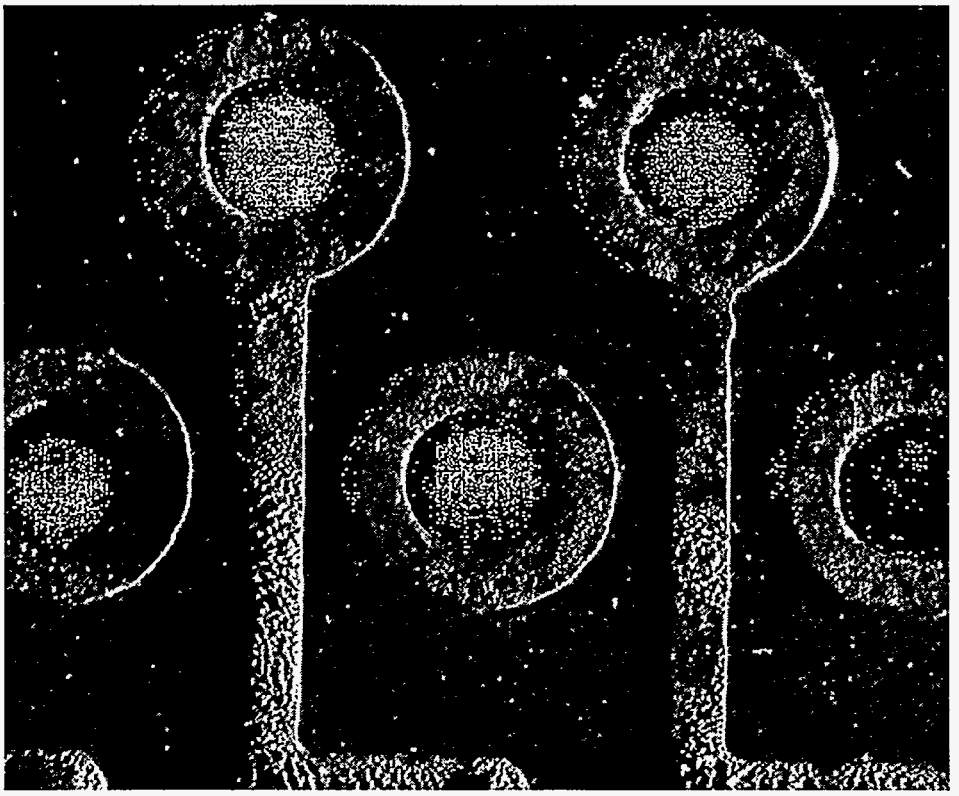


Figure 16. Solder on Non Parylene-C Coated Conductors

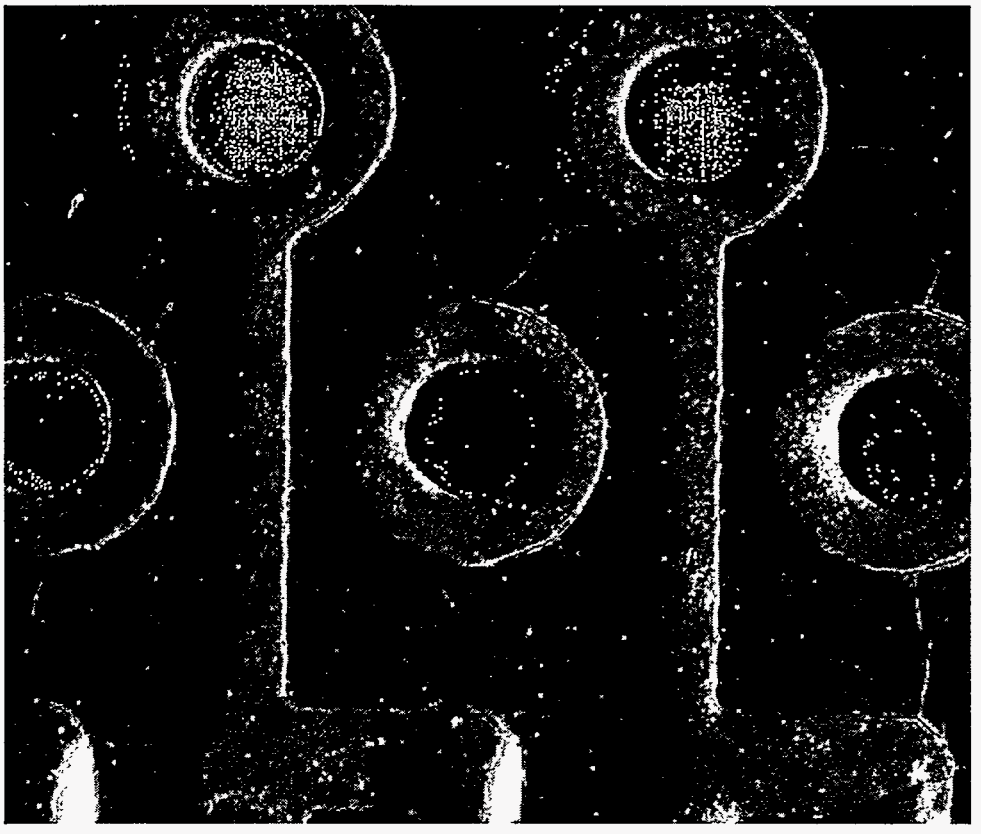


Figure 17. Solder coatings under Parylene-C coated Assemblies

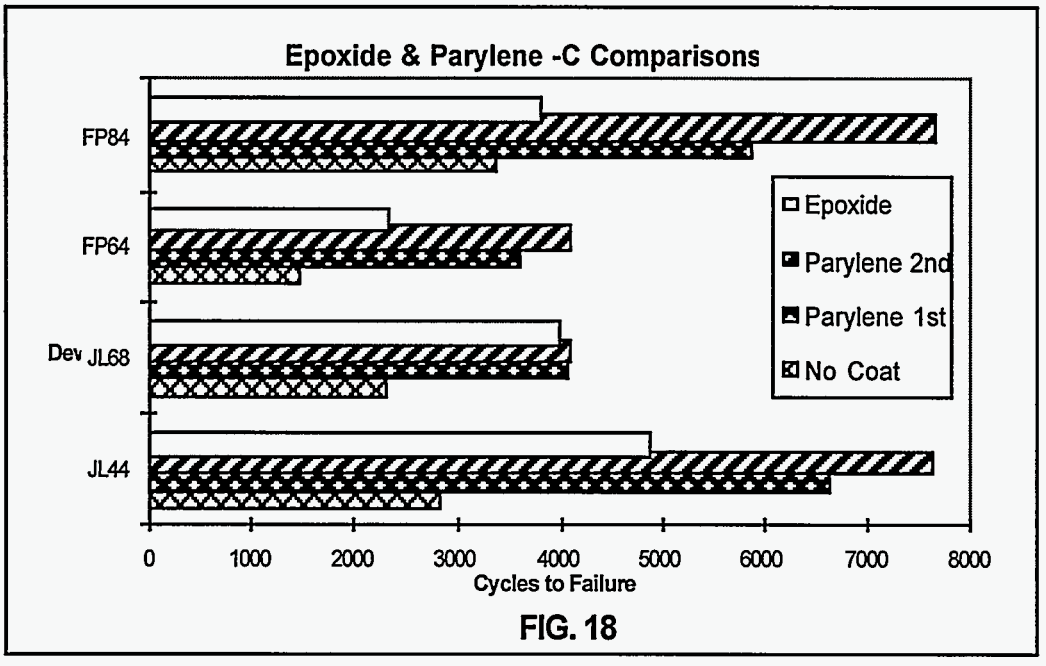


FIG. 18

epoxide coating was also beneficial in extending the times to first failure, but the Parylene-C performed better. The epoxide coating is easier to apply and does not require the rigor of sealing and masking protected areas compared to the Parylene-C process. Rework is much easier as the epoxide coating can be simply burned (melted) away with a hot soldering iron tip. Rework of solder joints coated with Parylene-C is a slow and generally tedious process to remove the Parylene-C . Abrasive methods appear to work the best for removing this coating.

Summary

We evaluated the comparative reliability of solder interconnections used for Leadless Chip Carriers (LCCs), J-leaded, and flat-pack hybrid microcircuits mounted on FR-4 glass epoxy printed wiring boards (PWBs). The board assemblies, with solder attached microcircuits, were repeatedly thermal cycled from -65 to +125°C. We recognize that this temperature range far exceeds most testing of assemblies. The purpose of these tests was to evaluate worst-case conditions and to obtain comparative information. Identical PWB assemblies using these three component types were subjected to both thermal shock testing (1 cycle every 42 minutes) and temperature cycle testing (1 cycle every 3 hours). The double testing evaluated the differences in stress application and evaluated the potential of replacing slow transition, expensive temperature cycle testing (which has been an industry standard for years) with the much more rapid thermal shock testing. In these tests, Parylene-C coatings significantly extended the lifetime to first failure on the leaded devices. Further, vias (through-hole interconnects) that were unfilled, but coated with Parylene-C , did not experience any failures in either test series. (There were 582 Parylene-C coated vias in each test.) Vias that were solder filled did not fail. Unfilled, uncoated vias that experienced failure, did not fail again once they were solder filled. [There were 1164 non-Parylene-C coated vias in each test sequence; none were initially solder filled, but all were subsequently solder filled when failures (at about 450 cycles) started showing up.] As a result, we recommend that all unused vias, on our high reliability application, assemblies be solder filled.

For very high-g shock or severe vibrational environments, we recommend our designers use the Leadless Chip Carrier, installed using a fat-fillet concept. For more benign environments, leaded designs provide greater extended time to failure (cycles).

We recommend our designers use the J-leaded package as the package of choice for new designs, primarily because of the saving in real estate on the board. Both J-leaded and flat-pack designs exhibited acceptable, long-term reliability. (None experienced a first failure in less than 1400 cycles, and both the coated 44-lead J-lead device and the coated 84-lead

flat-pack exceeded 5,800 cycles to first failure.) Much has been learned about what to check for in lead geometry of both devices. For example the smaller 64-lead flat-pack failed much earlier than the larger 84-lead device. This failure was a function of the massive, shorter leads on the smaller chip. The short, massive (rigid) lead transfers more thermal mismatch stress into a solder joint than does the longer, more flexible leads on the 84-lead device, even with the greater x and y vector motion of the larger package. LCCs can be used reliably for high-g environments provided that the process-controlled, fat fillet criteria is met. LCCs with these fat solder fillets survived more than two times longer than those with shallow (small) solder fillets. They are not as reliable, in general, for long-term, extensive, thermal extreme, cycling applications as the leaded devices, on glass-epoxy printed wiring boards.

The J-leaded devices used in these tests had the lead bonded to the side of the package from the exit to where the "J" portion of the lead extended past the package. This meant that the only flexible portion of the lead was from the bottom of the package downward. We believe that an even greater longevity would be observed if we used J-lead packages that do not have this side-bonding characteristic, and thus, allow stresses on the lead to make use of the elasticity of the higher portion of the lead.

Correlation of failures, comparisons to the amount of oxygen and nitrogen the solder joints were exposed to, plus the mode of test (cycle vs. shock) need to be done. Since the start of these tests, there has been industry data presented that show that solder joints exposed to 100% nitrogen fail more quickly than those in an oxygen environment. We have documented the amount of nitrogen in the thermal shock chambers (dual chamber), which has a liquid nitrogen direct injection cooling system for the cold chamber and heaters in the heat chamber. We found that the amount of oxygen in our hot chamber varies over time.

We will continue to use the thermal shock testing for quick-look evaluation to determine early failure mechanisms or assembly weaknesses under temperature induced stresses. The correlation of thermal shock and temperature cycling for the first few hundred cycles of test appear to correlate adequately. For long-term information, however, it really appears that one needs to test an actual assembly in a temperature environment that approximates the use environment as closely as possible. Extrapolations of thermal shock data into a temperature cycling environment may only provide ball park numbers at best.

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2. Joseph Hoyt, "The Influence Of Leg-Shaped, Solder-Joint Metallurgy On Surface Mount Solder Joint Strength," AMP Inc., Harrisburg, PA (from Proc. *NWCTP6789*, Naval Warfare Center, China Lake, CA, 1984).

3. Matthew Bevan, "The Effect of Conformal Coating on the Reliability of LCCC Soder Joints Exposed to Thermal Cycling," Fairchild Space Co., Germantown, MD.

Appendix A
Installing LCCs on Printed Wiring Boards with Vapor Phase Soldering

The following procedure is used to minimize void formation in solder joints and provide a fat bulbous fillet during the installation of LCCs onto assemblies. Other mechanisms have potential do provide the same results, but this is the procedure used during assembly of test parts discussed in this article. (Note: The instructions in this appendix are paraphrased from "LCC Preparation, SNL/CA Process," by V. C. Barr and J. Treml (2/29/88).

LCC Preparation

The preparation of LCCs, prior to installation, is critical to obtaining good solder joints. To insure good tinning of pads, the following procedures are used.

1. All pads of each LCC are cleaned using a fiberglass brush. When cleaning LCCs that are static sensitive, this cleaning must be performed at a Static Protected Work Station with air flow across the components from an ionizer.

2. The LCC is placed in an aluminum (metal or conductive) tray and cleaned with alcohol. It is then blow dried using an ionizing nozzle and oil-free air, placed in an aluminum tray, then put in a vacuum chamber. A vacuum is drawn to 1000 to 2000 microns (usually within 3-4 minutes from the start) and then the pressure is slowly returned to normal using dry nitrogen to backfill. (Authors note: The vacuum is used to extract any moisture, solvent or other volatiles that may be in open pinholes in the thick-film conductors of the LCC.)

3. Flux is poured (added) into the tray sufficient to cover the edges of the conductors. The tray now goes into the vacuum chamber and a vacuum is drawn (1000 to 2000 microns). the chamber pressure is now returned to normal using dry nitrogen to backfill. (Authors note: The vacuum is held until the flux boiling action slows significantly. We use a rosin, mildly activated flux during our installations. When the boiling action has slowed, at least 80% of any moisture and most volatiles have been removed. When the nitrogen is introduced, the flux helps seal surface openings to slow re-absorption or diffusion of moisture back into the conductor crevices. The nitrogen is also key in slowing this re-absorption or diffusion process.)

4. The LCC is tinned in a solder pot using Sn62 solder. This process should occur within 1/2 hour of removal from the nitrogen backfill (step 3). Dip the LCC, one side at a time, into solder (Authors Note: 480 to 500 degrees F., solder pot for our applications) at approximately a 45 degree angle, three times per edge. (Authors note: The three dips removes most excess gold and minimized gold intermetallic formation.)

5. Each LCC is now washed in flux remover, blow dried and placed in a vacuum until assembly.

Board Preparation

1. Wash the board (substrate) in alcohol. If a ceramic board is used, the conductors must be burnished slightly with a fiberglass brush and then washed. The board is blow dried and placed in the vacuum chamber. A vacuum is drawn (1000 to 2000 microns), then the pressure is returned to normal using dry nitrogen to backfill. (Authors note: Ceramic boards with thick film conductors usually have a glassy coating on the conductors, this must be removed, if other pretreatment has not done so, to fully expose the conductor surface. The vacuum then helps remove surface moisture and volatiles from the conductors.)

2. Flux is brushed (or coated) on the pads (rather than on the whole assembly). (This minimized post-soldering cleanup.) The board is placed in the vacuum chamber. A vacuum is drawn (300 to 1000 microns) without a dwell time, then the pressure is returned to normal using dry nitrogen to backfill.

3. Solder is manually added to each land (or pad) using a soldering iron. (Authors note: This is to attain sufficient solder (pre-form) to attain the fat fillet later) A trained technician can get a

uniform amount of solder buildup on each pad for fat fillets.

4. The board is washed in flux remover, blow dried and placed in a vacuum chamber. The board is now ready for assembly and can remain in the vacuum until such time. (Min. of 1000 - 2000 microns vacuum.)

Assembly

1. Apply flux to all pads (board and LCCs).

2. Draw vacuum (300 - 1000 microns) on board and LCC. Return pressure to normal, backfilling with dry nitrogen.

3. Place LCC(s) on the board and if necessary tack solder in two places (usually opposite corners to hold positioning) with a small soldering iron.

4. Put the board in a carrier and place it into the vapor phase soldering tank. [We use a 110-120 Degree C. small capacity (volume) system.] When the solder melts, it turns from a dull to shiny silver color. After the solder starts to melt, remain in position (in the reflow medium) for about 305 seconds to allow even solder flow. (The board usually stays in the primary vapor zone about 10-15 seconds for a pre-heat.) Remove the carrier carefully and slowly from the tank or system, keeping vibrations to a minimum. (The total time in our system is about 30 - 45 seconds.)

5. The carrier is then allowed to cool in a vibration free place.

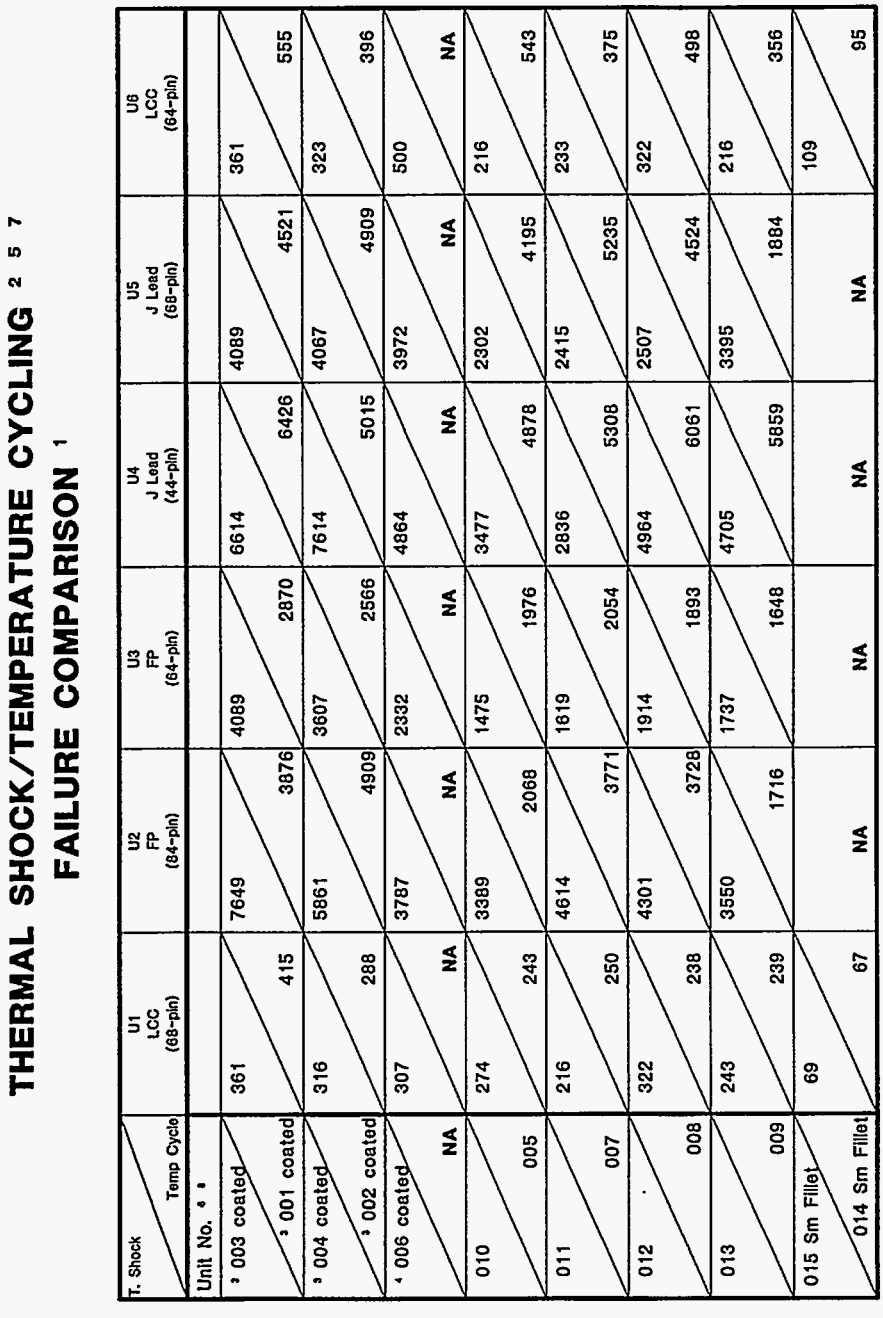
6. Wash the board in flux remover and (vacuum optional) dry.

7. All solder joints must be inspected for possible solder bridging and for good (adequately fat) solder fillets.

8. If touch up is required, the solder interconnect to be reworked should be fluxed and one must completely reflow the solder (add if necessary etc.) with a small iron. (Authors note: We have found that any reworked solder joint on an LCC must be completely melted (solder reflowed) or the interconnect is very prone to early failure. We do not see this failure tendency if the interconnect is remelted fully.)

9. Clean board and dry (we vacuum dry our assemblies and nitrogen backfill afterwards.)

Appendix B
Thermal Shock/Temperature Cycling
Failure Comparison



THERMAL SHOCK/TEMPERATURE CYCLING [2 5 7]
FAILURE COMPARISON [1]

T. Shock / Temp Cycle	U1 LCC (68-pin)	U2 FP (84-pin)	U3 FP (64-pin)	U4 J Lead (44-pin)	U5 J Lead (68-pin)	U6 LCC (64-pin)
Unit No. [4 6]						
[3] 003 coated	361	7649	4089	6614	4089	361
[3] 001 coated	415	3876	2870	6426	4521	555
[3] 004 coated	316	5861	3607	7614	4067	323
[3] 002 coated	288	4909	2566	5015	4909	396
[4] 006 coated	307	3787	2332	4864	3972	500
NA	NA	NA	NA	NA	NA	NA
010	274	3389	1475	3477	2302	216
005	243	2068	1976	4878	4195	543
011	216	4614	1619	2836	2415	233
007	250	3771	2054	5308	5235	375
012	322	4301	1914	4964	2507	322
008	238	3728	1893	6061	4524	498
013	243	3550	1737	4705	3395	216
009	239	1716	1648	5859	1884	356
015 Sm Fillet	69					109
014 Sm Fillet	67	NA	NA	NA	NA	95

[1] Cycles Completed (Tr. Shock/Temp. Cycle) 7649/6428 Unit #008 @ 4864 cycles
[2] Temp. Range -65C to 125C
[3] Parylene-c conformal coating
NA Not Applicable
[4] Base material epoxy/glass (FR-4) 6-layer MLB
[5] SNL/NM developed Epoxide conformal coating
[6] Cycle Time a)Tr. Shock 42 Min. b)Temp. Cycle 3 Hrs.
[7] numbers 001 thru 015 represent assembly serial numbers
[8] Thermocouples attached to: TS 003,010,012,015 TC 001,005,008,014