Wafer Level Thin-Film Solder Bonding of a Hybrid Sensor for Interfacial Force Microscopy

C. M. Matzke and J. E. Houston
Sandia National Laboratories
Albuquerque, NM 87185-1413

ABSTRACT

We discuss the design, fabrication and performance of a hybrid force sensor for Interfacial Force Microscopy which features a new wafer-level, thin-film soldering technique.

1. INTRODUCTION

Scanning probe techniques have shown dramatic growth recently and are presently making significant impact on surface and interfacial problems in material science. The Interfacial Force Microscope (IFM) is a scanning force-probe technique similar to the atomic force microscope (AFM) but distinguished by its use of a self balancing, differential-capacitance force sensor. This sensor eliminates the mechanical instability found in the displacement sensors used in the AFM and greatly expands the IFM's range of applicability. However, IFM sensors presently in use consist of chemically milled metal sheets epoxied to insulating substrates and are individually assembled, a process which is tedious, time consuming and unreliable. The hybrid design is necessitated by the need to have reasonably large capacitance values and low compliance on the moveable components. In addition, the deflection detection is done by an RF bridge circuit which makes semiconductor-based designs difficult. Thus, the hybrid scheme avoids the release of features with severe aspect ratios and the deposition of thick films which are difficult in the normal microelectronics-type fabrication. In order to correct difficulties with the present design, we have developed a process which includes a multi-sensor, wafer-level layout and a newly developed In thin-film solder assembly technique. In this paper, we discuss the details of our fabrication process and demonstrate its viability by showing actual IFM results obtained with the new sensors.

2. THE IFM SENSOR DESIGN

Figure 1 shows a schematic of the basic IFM sensor design (1). It consists of a capacitor common plate (teeter totter) suspended above two individual capacitor pads by torsion bars. A probe tip is mounted on one end of

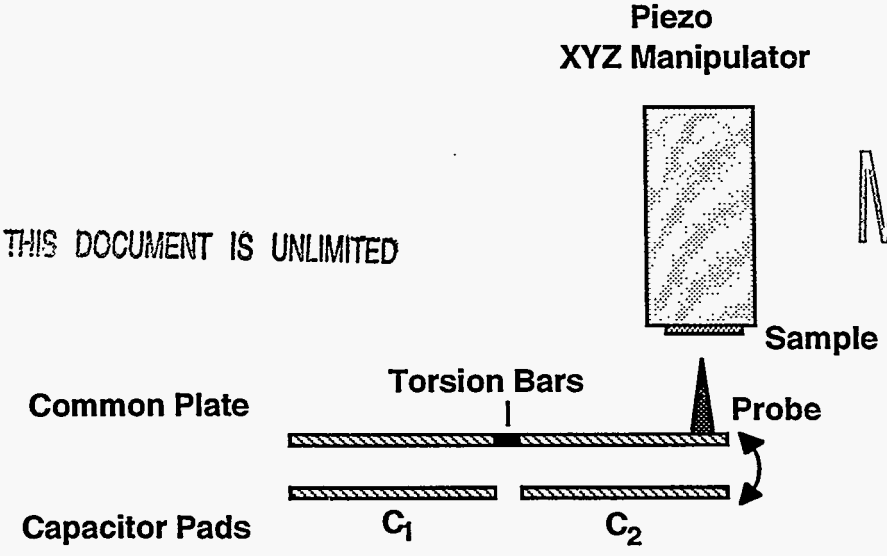


Figure 1 A schematic of the IFM differential capacitor force sensor and sample assembly.

the common plate which can interact with a sample mounted on a piezo tube scanner for xyz positioning and scanning. An interaction force between the tip and sample rotates the teeter totter changing the capacitance

differentially and this change is detected by an RF bridge circuit (1 Mhz). The sensor is, then, electrostatically rebalanced by a feedback controller which places the proper dc (or low frequency) voltages on the individual capacitors.

3. THE FABRICATION PROCESS

The steps required to implement this sensor design are schematically illustrated in Fig. 2, and consist of two separate levels of piece-part fabrication. The hybrid design was necessitated principally by the use of the RF-bridge displacement detection scheme, which requires highly insulating materials to isolate the capacitance pads and common plate. The top level, containing the torsion bars and capacitor common plate, has been fabricated both by chemical milling of a thin BeCu sheet and by a deep-etching process on a Si wafer (in the remaining discussion we will only cover the Si-based fabrication). The substrate, containing the capacitor gap well, the capacitor electrodes, leads and bonding pads, is fabricated from either quartz or glass. After fabrication, the two levels are then bonded by the thin-film soldering technique.

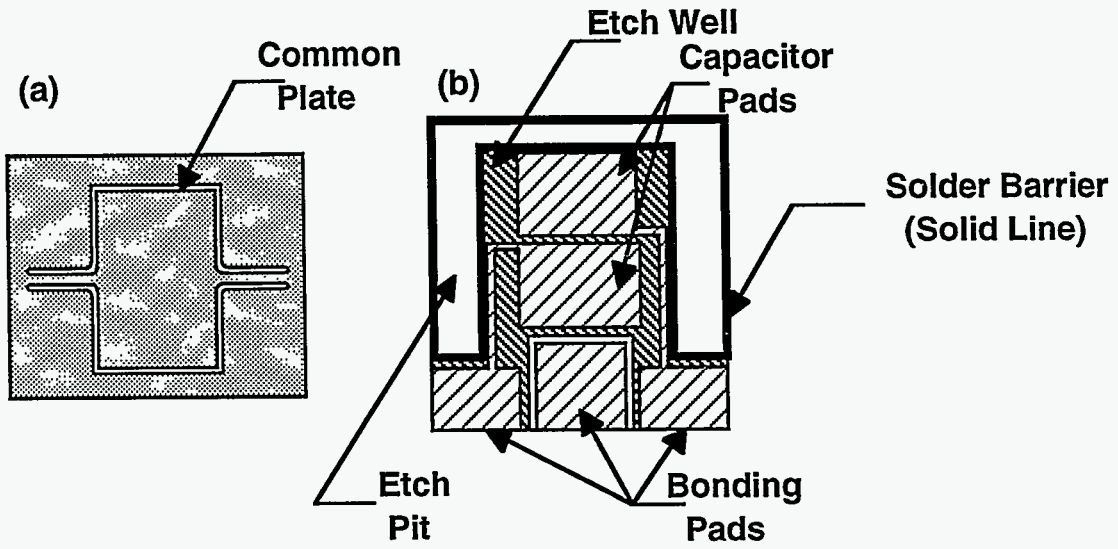


Figure 2. A schematic illustrating the two-level fabrication necessary for the hybrid IFM sensor. (a) shows the basic configuration of the capacitor common plate while (b) shows the substrate configuration

The initial step in the fabrication process is the preparation of the substrate, which involves etching the substrate, deposition and patterning the metal electrodes in the well, and deposition and patterning the solder film. Except for a nickel plating process (used as the deep Si etch mask) and a deep silicon etch described below, conventional microelectronics equipment was used for all processing. Since our features are large compared to microelectronics circuitry, metal film thicknesses and patterned photoresist dimensions are not critical and processes, that were characterized for microelectronics, perform well for our hybrid materials. Also, some of the same process-step sequences such as, for example, photoresist descum after development, were used. (These details are not mentioned further in the process description below.) Since the majority of the processing involves wet chemical etches, the process sequence was determined mainly by chemical selectivity issues.

The initial development work on thin film soldering was aimed at bonding Si to Si (2) and we have expanded this application to include bonding of other materials as required in the development of the hybrid IFM sensor. Advantages of the thin film solder-bonding process include the low bonding temperatures for soldering metals and alloys (in the 100 C to 300 C range for In and its alloys) and the malleable characteristics of these materials. This latter property gives the solder a forgiving nature, making it possible to bond rougher non-mirror surfaces with somewhat mismatched thermal expansion coefficients. In addition, this fabrication approach, like

wafer bonding, avoids the integrated processing problems associated with release of features with severe aspect ratios and depositions of rather thick materials in the micron range, which are unusual in microelectronics fabrication.

3.1 Glass Substrate Processing

The substrate starting material for the Si sensor is a 3 in Corning Pyrex® wafer with a thermal expansion coefficient of 3.2 μin/in F (3) compared to the Si thermal expansion coefficient of 2.8 μin/in F (4), and the first mask level involves etching both the well and pit in this glass. The etching configuration is shown schematically in Fig. 3. Since the solder film thickness partly determined the dielectric gap for the metal sensors, and the solder flows during bonding, we found that capacitance varied as much as 40% for an older substrate configuration. As shown in the drawing of Fig. 3, with a solder pit the glass barrier wall between the well and pit functions as the height determinant for the Si common plate. In testing this design, the capacitance varied less than 5%. The well etch forms a recessed area for the dielectric air space, the channel for the interconnection of the electrode pads to the soldering pads and an area for the soldering pads outside the capacitor, which are hard wired to the microscope. The pit etch forms only the recessed area for the In solder material

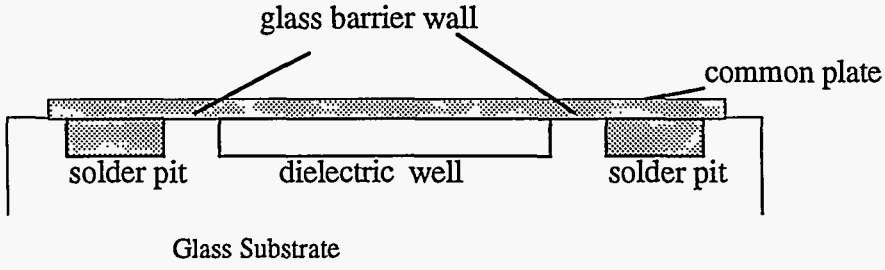


Figure 3. A cross section schematic illustrating the configuration of the glass barrier wall.

For these simultaneous etches, the glass wafer is ion milled with argon to remove the more porous top layer and prevent undercutting of the etchant, followed by deposition of a Cr-Au etching mask by e-beam evaporation. (Cr-Au is deposited sequentially to depths of 500 and 2000 Å, respectively.) After patterning the metal with photoresist using standard photolithography, the Au is etched in a KI-I_2 solution and the Cr in a commercial Cr etchant to form the glass etchant windows in the metal mask. Finally, the glass is etched to a nominal depth of 4 μm with hydrofluoric acid to form the well and pit.

The second mask level is used to deposit the Cr-Au film in the well and pit. In the air well, the patterned Cr-Au functions as capacitor pads, bonding pads and interconnecting leads. Cr-Au in the pit serves as a wetting surface for the subsequently deposited solder material. To process this level, the metals are simply e-beam deposited, patterned with photoresist using the second mask (which is appropriate for the described configuration) and then etched in the same solutions as stated above for the mask function.

The next process step is metalization of the substrate backside. Initial tests indicated inconsistent bonding due to nonuniform heating. We found that backside metalization improved the thermal contact to heating surfaces and the bonding uniformity was greatly enhanced.

The third mask level involves protecting the Cr-Au in the well areas from the subsequently deposited solder film. A standard photolithography process is used to mask the well area with one of the thicker photoresists, that can withstand temperatures in the soldering range of 160 to 170 C. After preparing the wafer with photoresist, the solder, pure In, is e-beam deposited to a thickness determined by (and the same as) the depth of the pit, which is presently 4 μm. Following In deposition, a thin 100 Å film of Au is deposited to minimize formation of In oxide, which is a detrimental In diffusion barrier and requires higher temperatures to ensure adequate bonding. Using the fourth mask with the well-protect photoresist in place, the In is patterned using standard photolithography and etched

in a hydrochloric acid-peroxide solution leaving In in the pit recess. Finally, all photoresist including the well-protect resist is removed in acetone, leaving the substrate fully prepared for solder bonding.

3.2 Silicon Common-Plate Processing

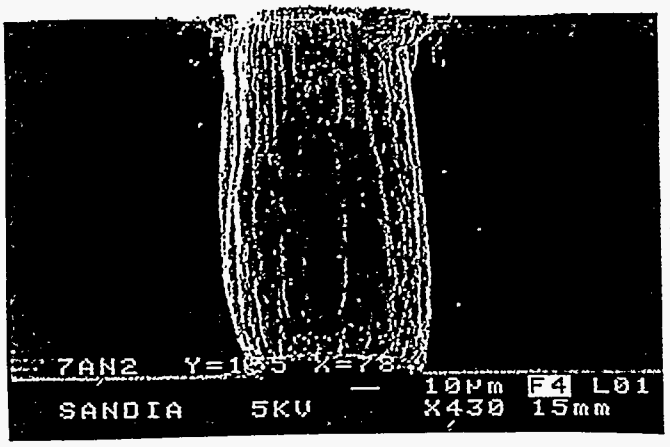
The second major process sequence involves producing the Si common plate by etching through a thin 125 μm Si wafer. First, the insulating film (a blanket oxide) is deposited using chemical vapor deposition (CVD), followed by Cr-Au metalization. The Cr-Au film functions as a seed layer for subsequent Ni plating, and later on for the device, it serves an electrical conduction path for the probe. In the next processing step using the common plate mask, photoresist is patterned on the Cr-Au film to expose some of the seed film for Ni plating while insulating the remaining areas from the plating solution. The prepared wafer is Ni plated in a commercial sulfa-solution bath contained in a customized configuration to accommodate smaller microelectronics size samples. The Ni, which is a resilient material, is plated to a 2 μm thickness that adequately masks the Si from the subsequent deep plasma etch process. To further prepare the wafer, after removing the photoresist, the Ni plated film also serves as an etchant mask and the Cr-Au seed layer, along with the oxide film, are cleared in the open areas that are to be plasma etched.

A cleaner plasma etch results if the backside of the wafer is also mask and the Si is etched half way through from one side, then flipped over and etched the rest of the way to avoid difficult etching next to the platen. For this mask, photoresist is first patterned on the backside using a mirror image common plate mask and backside aligner equipment. Cr-Pt-Au rather than Cr-Au is then deposited on the prepared wafer backside for the following reasons. A thin Au film of only 100 Å thickness functions as a seed layer for Ni plating by inhibiting oxidation of Pt that would form upon venting the bell jar. The more robust Pt layer insures a continuous conductive film for the common plate capacitor. The readily forms amalgam with the solder. From initial testing, we found that the amalgam diffuses rapidly out on a continuous gold film beyond the actual bonding area and depletes the solder material. Therefore, the common-plate Au film is minimized, since it is not patterned like that of the pit-etch side of the bonding area.

After deposition, the metal sandwich film is patterned with photoresist, which again acts as a mask for the Ni plating process. This time the photoresist is aligned to the photoresist beneath the metal film, which was backside aligned to the front side features. Following the plating process to the same thickness, the wafer is soaked in acetone to remove all the photoresist. This results in lifting the metal film that is not mask with Ni. The wafer at this point contains the Ni mask on both sides of the wafer and is ready for the deep plasma etch.

The Si etch is accomplished using a high density 500 W inductively coupled plasma (ICP) process run at 250 W RF power. (5) The sample, which is mounted to a platen with clips, is cooled to -40 C and evacuated to 5 mT, then etched in an SF_6, argon and oxygen plasma for a total time of 90 minutes to clear the unmasked areas of Si.

Figure 4. An SEM micrograph of via hole deep etched through a 155 μm Si wafer illustrating the minimum degree of lateral etching.

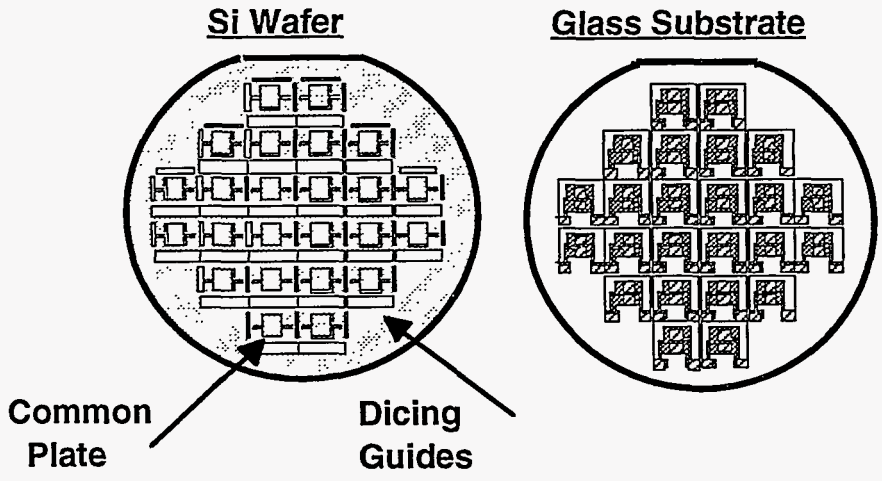


Etching parameters have been characterized so that the etched profile is quite vertical and undercutting the mask is minimized, as shown in Fig. 4. In the final processing step, the Ni etch mask is removed by soaking the wafer in a dilute nitric acid solution, leaving the exposed Au surfaces for solder bonding.

3.3 Bonding

The preprocessed glass and Si wafers, shown schematically in Fig. 5, are bonded together in an evacuated system equipped with heating elements, plates and weights stacked in the configuration illustrated in Fig. 6. Starting at the bottom of the drawing, with the first insulating ring and heating plate in place, the sample is aligned on the first flat plate under a microscope. After placing the aligned wafers and flat plate on the heater plate at the bottom, the rest of the stack is carefully placed to avoid misaligning the wafers.

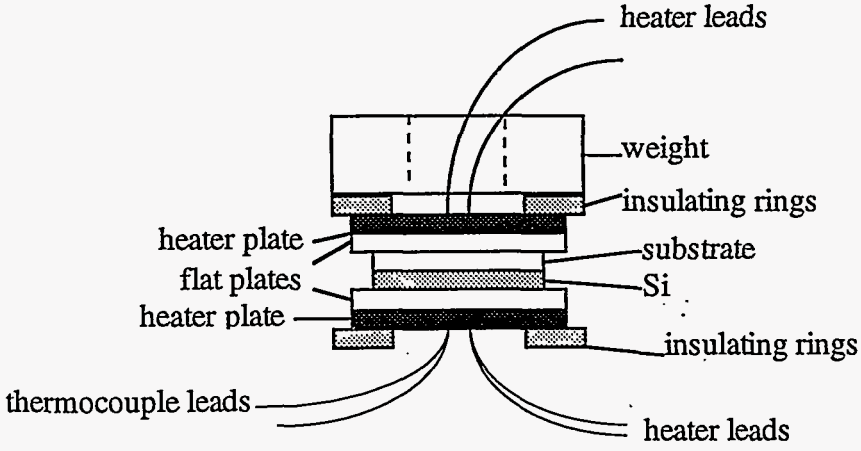
Figure 5. A schematic illustrating the die layout at the wafer level for both the Si and Glass wafers.



Through testing, each of the parts in the assembly were added, and heating elements were placed on either side of the sample assembly to enhance heating uniformity. The aluminum flat plates adjacent to the sample were milled and polished to within one μm flatness across four inches to enhance contact uniformity. Finally, weights were added to further enhance contact. Items essential for successful bonding that are not shown in the figure, are the deposited wafer backside metalization film for contact and the thin Au film, which was deposited on the In to minimize In oxide. We found that capping the In with Au was a fundamental solution to the bonding diffusion barrier problem, which caused persistent bonding non-uniformity and higher temperature requirements in the 180 to 200 C range to achieve maximum bonding.

With the established arrangement, the sample assembly is first evacuated to the low 10^{-6} range before heating to the target temperature of 162 C. Due to the large assembly mass, the last few degrees are approached slowly and the temperature is held at 160 to 165 C for 15 to 20 minutes.

Figure 6. A schematic of the thin-film solder bonding hardware assembly.



3.4 Separation of Die

The final step is to separate individual die by sawing the wafer assembly apart. Since solder is a relatively soft material, forces that may stress or deform the bond were minimized by using a multiple pass procedure. First parallel cuts of only the Si material are made on either side of subsequent glass cuts using high blade rpm and low cutting speeds. The final glass cuts are made between the Si cuts without exerting any force on the thin film solder bond, producing individual sensors which are ready for electrical testing as explained next.

4. Sensor Performance

IFM sensors fabricated as described above are capable of detecting forces on the attached probe of a few nN and can image surface morphology in both attractive and repulsive modes. The compliance of the sensor (i.e., the sensor displacement under the influence of a probe force) is extremely small and the frequency response is in excess of 5 kHz. Sensors of this type have been used to measure the behavior of the adhesive force between differing end-group combinations on self-assembling molecular monolayers adsorbed on a Au probe and Au sample surfaces (6) and for determining the nanomechanical properties of Au surfaces using a W probe as a very small-scale indentor (7).

To illustrate this latter application, we show in Fig. 7 a repulsive-force image (similar to those obtained by a commercial AFM) of a carefully prepared Au(111) single-crystal surface (8). As can be seen, the surface is very flat showing both single and double atomic steps (a single step has a height of about 0.3 nm) intersecting at angles controlled by the crystalline structure of the underlying lattice. The probe tip in this case had a radius of curvature of only about 25 nm. In the graph of Fig. 8 we show the result of a loading curve (i.e., the repulsive force on the probe vs. the relative displacement of the tip) as we approach, deform and withdraw from the surface. The initial rise in force just after surface contact follows a 3/2 behavior with respect to deformation, as indicated by the solid line. This is the classic Hertzian behavior which results from the fact that the contact area changes as the surface is deformed. Hertzian deformation indicates that the deformation is elastic or nonpermanent. However at a load of about 44 μN, the behavior deviates from Hertzian and, upon withdrawal, the loading curve shows a broad hysteresis loop. This indicates that the surface has been permanently deformed. The point at which the behavior deviates from Hertzian represents the threshold for plastic deformation, i.e., the initial yield point for the material. At this level of indentation, there are no existing dislocation under the probe and the plastic threshold represents the point at which dislocations are initially nucleated.

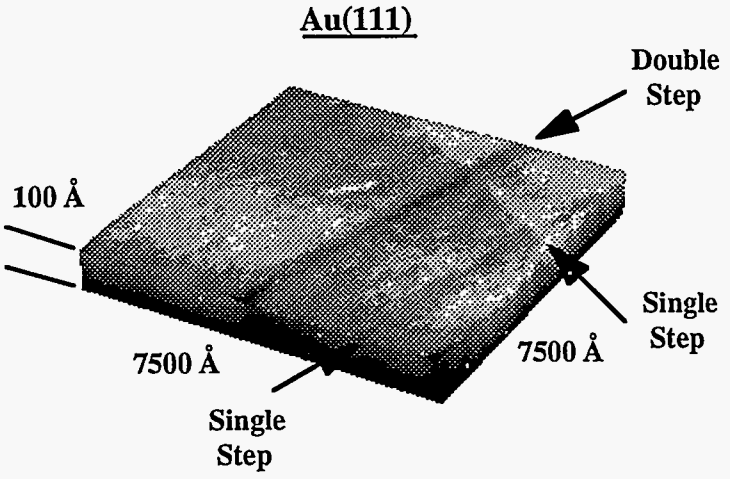


Figure 7. A repulsive-force image of a Au(111) surface.

The result of the loading curve of Fig. 8 is shown in the image of Fig. 8 in the region marked by the symbol "1". As can be seen, the plastic behavior shows up as a dent, which is about 40 nm in diameter and about 6 nm deep. The study that produced this data (8) was aimed at observing the effect of the subtle surface defects, represented by the steps, on the mechanical behavior. Therefore, loading curves like that of Fig. 8 were taken at various positions relative to the step edges shown in Fig. 7, as indicated by the numbered arrows in Fig. 8. The conclusions from this study were that, indeed, these subtle surface defects cause large variations in the effective hardness of the Au surface. For example, the yield stress for the dent that straddles a step edge (#2) is almost a factor of two smaller than for the dent out on the flat terrace shown as dent #3. This type of work provides important information concerning the fundamental aspects material yield and is necessary in order to be able to eventually tailor material properties for specific applications. These results are a tribute to the stability, low compliance and controllability of the IFM sensors.

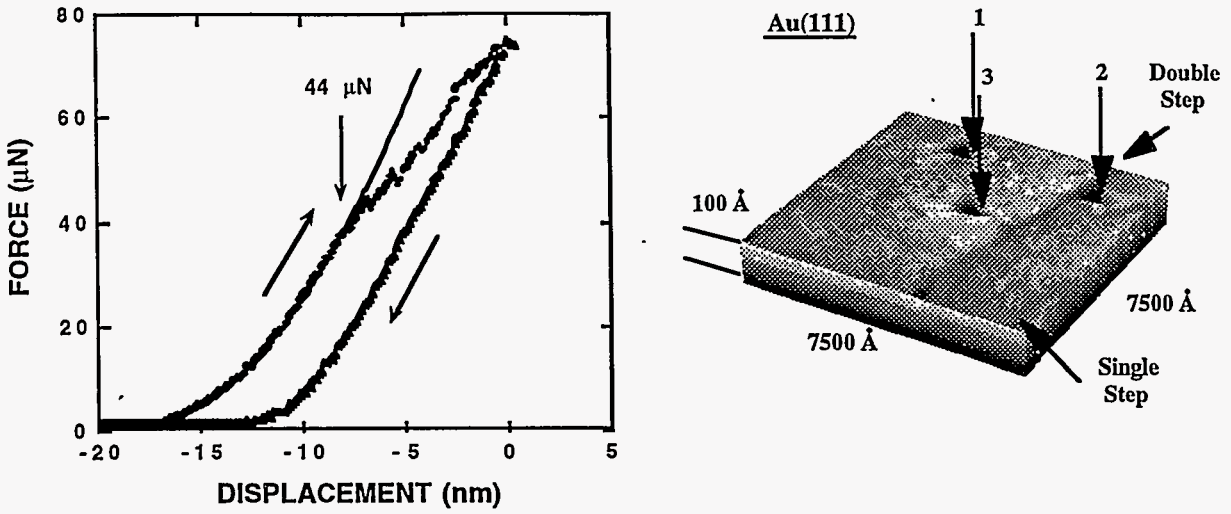


Figure 8. The left-hand graph represents the loading curve (force vs. relative displacement) for a W probe indenting the Au surface. The solid line is the Hertzian relation indicating an elastic deformation, while the hysteresis loop signals a permanent deformation. The right-hand image shows the surface of Fig. 7 after loadings in three different locations.

5. SUMMARY

The IFM is a relatively new technique for studying interfacial bonding and mechanical properties at the nm level. The unique aspect of this technique is its use of a differential-capacitor force sensor which is electrostatically self balancing. The sensitivity, reliability and overall response of this hybrid sensor depends critically on the fabrication process; one which produces consistently small capacitor gaps and strong bonding between the hybrid parts. We have recently established a fabrication process for these sensors which allows them to be reliably produced at the multi-unit, wafer level with hybrid-part bonding by a newly developed In thin-film soldering technique. The individual sensors consistently have capacitance values near 10 pF and force sensitivities of a few nN--a considerable improvement over the present hand assembled, epoxy bonded prototype units. These increased capabilities are clearly illustrated in Figs. 7 and 8 by our ability to image single atomic steps on a well prepared single-crystal Au(111) surface. This fabrication process is particularly important for the growth of application of the IFM technique since sensor can now be mass produced by standard semiconductor-related commercial foundry.

ACKNOWLEDGEMENTS

Work on this sensor fabrication was made possible through the use of the facilities at Sandia's Compound Semiconductor Research Laboratory. The authors would like to thank P. T. Vianco for many helpful discussions concerning the thin-film soldering process. This work was supported by the U. S. Department of Energy under Contract DE-AC04-94AL85000. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the U. S. Department of Energy.

REFERENCES

1. S. A. Joyce and J. E. Houston, Rev. Sci. Instr. **62**, 710 (1991).
2. P. T. Vianco, G. Kohler and S. Kravitz, *Ultrminiatuare resonator accelerometer,* Sandia Internal Report No. SAND96-0971 (April, 1996). Sandia National Laboratories, Albuquerque, NM.
3. Value obtained from specification information furnished by Corning Glass, Corning, NY, 14831.
4. *Handbook of tables for Applied Engineering Science*, 2nd edition (1976), CRC Press, p.117

5. R. J. Shul and P. Glarborg, Sandia National Laboratories, Albuquerque, N. M; private communication.

6. R. C. Thomas, J. E. Houston, R. M. Crooks, T. Kim and T. A. Michalske, J. Amer. Chem. Soc. **117**, 3830 (1995).

7. P. Tangyunyong, R. C. Thomas, J. E. Houston, T. A. Michalske, R. M. Crooks and A. J. Howard, Phys. Rev. Lett. **71**, 3319 (1993).

8. R. Q. Hwange, J. D. Kiely and J. E. Houston (In Preparation).