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Nonvolatile Field Effect Transistors Based on Protons and $Si/SiO_2/Si$ Structures

W.L. Warren, K. Vanheusden, D.M. Fleetwood, J.R. Schwank,
P.S. Winokur, and M.G. Knoll
Sandia National Laboratories,
Albuquerque, New Mexico 87185-1349

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R. A. B. Devine
France Télécom/CNET,
BP 98, 38243 Meylan, FRANCE

35-word Abstract

A novel nonvolatile memory effect involving H^+ motion in SiO_2 is illustrated in bulk Si and SOI MOS devices. The technology is compatible with standard Si processing and potentially radiation tolerant.

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DISCLAIMER

I. INTRODUCTION

It has been known for quite some time that hydrogen plays an important role in the electrical and radiation response of MOS devices. The effects can be beneficial, for example, as in the case of the passivation of process-induced interface traps [1,2]. They can also be detrimental as in the case of post-irradiation interface trap density buildup [3-5].

Recently, we have demonstrated that annealing Si/SiO_2/Si structures in a hydrogen containing ambient introduces mobile H^+ ions into the buried SiO_2 layer [6]. Changes in the H^+ spatial distribution within the SiO_2 layer were electrically monitored by current-voltage (*I-V*) measurements.

The ability to directly probe reversible protonic motion in Si/SiO_2/Si structures makes this an exemplar system to explore the physics and chemistry of hydrogen in the technologically relevant Si/SiO_2 structure. In this work, we illustrate that this effect can be used as the basis for a programmable nonvolatile field effect transistor (NVFET) memory that may compete with other Si-based memory devices. The power of this novel device is its simplicity; it is based upon standard Si/SiO_2/Si technology and forming gas annealing, a common treatment used in integrated circuit processing. We also briefly discuss the effects of radiation on its retention properties.

II. EXPERIMENTAL DETAILS

Three different types of SOI materials were investigated: separation by the implantation of oxygen (SIMOX), zone-melt-recrystallization (ZMR), and Unibond®. We also studied a standard thermal SiO_2 (40-nm thick) oxide capped with a nominally undoped chemical-vapor-deposited amorphous Si layer which crystallized when the structure was annealed at 1200°C for 2 h in Ar + 1% O_2. After etching test patterns in the top Si layer, wafers were annealed in either forming gas (FG) [N_2:H_2; 95:5 or N_2:D_2; 95:5 (by volume, 99.999% pure)] or nitrogen for 30 min. The top Si layer was etched to allow lateral diffusion of hydrogen into the buried oxide during the forming gas anneal. This lateral diffusion is crucial because the amount of hydrogen diffusing through the top Si strips into the buried oxide is negligible, due to the very low solubility of hydrogen in Si.

For the capacitance-voltage (*C-V*) measurements, the Si strips were etched off using KOH. *C-V* measurements on the SiO_2/Si structures, exposed during the KOH etch, were made at 1 MHz with a mercury probe. Small Al gates were deposited by evaporation after the FG anneal and KOH etch on a limited number of samples. Current-voltage (*I-V*) measurements on the Si/SiO_2/Si structures were performed using the point-contact Ψ-MOSFET technique [7]. The buried oxide plays the role of the gate oxide and the top Si layer represents the transistor body. Two tips of a standard four point probe are placed on the top Si layer to form the source and drain point contacts, while the gate voltage is applied to the back of the Si substrate. Some capacitors were irradiated with 100 keV x-rays.

III. RESULTS AND DISCUSSION

Figure 1 (a) shows the hysteretic behavior of the *I-V* curves on SIMOX after it received a 550°C FG anneal. Similar features were observed upon annealing between 500 - 800°C in FG. Curve 1 was recorded with a *decreasing* gate (substrate) bias (from positive to negative) after the bias was kept constant at the initial value (+ 40 V) for 5 min. Curve 2 was subsequently recorded using the *opposite* gate voltage sweep direction (from negative to positive) after holding the gate bias at the initial value (- 70 V) for 5 min. The hysteretic behavior is noted as the original *I-V* curve (curve 1) was not retraced by reversing the voltage sweep direction (curve 2). Curve 3 was recorded after curve 2 using the same procedure described for curve 1, showing the reversibility of the process.

The negative voltage shift ΔV in the *I-V* plots is caused by positive charges in the buried SiO_2 (areal density $\approx 2 \times 10^{12}$ cm^{-2}). We suggest at this time that the observed hysteretic behavior is the result of an electric field induced migration of the charged ionic species from one Si/SiO_2 interface to the other. This type of behavior was not observed after annealing in N_2, showing that the presence of hydrogen in the anneal ambient triggers the hysteretic behavior.

Figure 1 (b) shows the hysteretic behavior of the *C-V* curves on SIMOX buried oxide after it received a 550 °C FG anneal. Following the FG anneal the top Si was removed in KOH solution, and a metal gate was formed on the exposed oxide. The 3 curves were measured using the same sequences used in Fig. 1 (a). Again, the negative voltage shift, ΔV, in the *C-V* plot is caused by positive charges in the buried SiO_2. However, since the semiconductor body is now the substrate Si (as illustrated in the insets), ΔV will now be maximum if the positive charges are located near the SiO_2/substrate-Si interface, i.e., the opposite interface as compared to the *I-V* measurements. Unlike in the $Si/SiO_2/Si$ device structure, reversing the gate bias polarity in the Si/SiO_2/metal-gate capacitor does not show a repeatable-loop behavior, but leads to a permanent change.

The difference in behavior between the Ψ-MOSFET and MOS capacitor can be explained by assuming that the charged species can escape the SiO_2 dielectric through the metal gate [8], but are unable to exit through the Si substrate or top Si layer. It follows from the sequence in Fig 1. (b) that escape occurs through the metal gate under a negative gate bias, which proves that the mobile species involved are positively charged. The crucial role of the hydrogen anneal step to trigger the hysteretic effect, the much higher solubility of hydrogen in metals such as Al or Hg as compared to Si [9], and the relatively rapid motion of this positive charge at room temperature as compared to Na^+ motion [10] collectively suggest that the mobile charge is H^+.

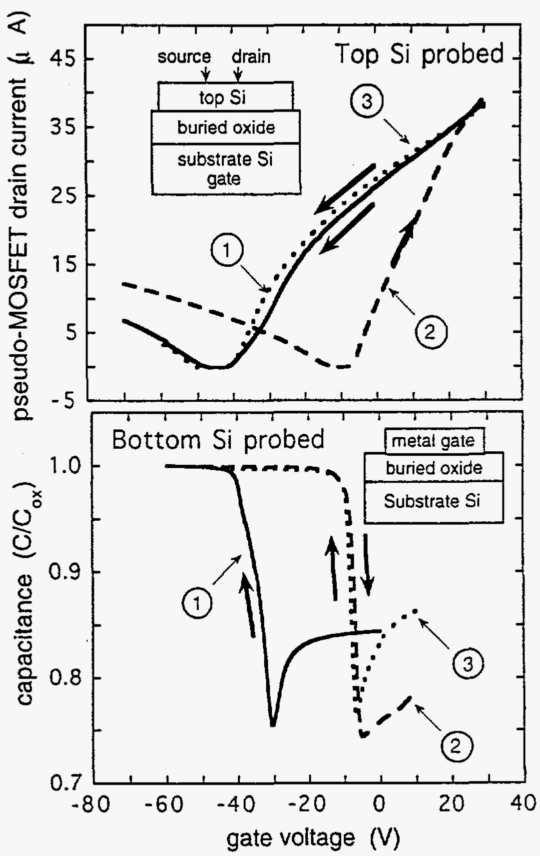

Figure 1:
Hysteretic behavior of *I-V* (a) and *C-V* (b) curves on SIMOX after it received a 550 °C FG anneal. *I-V* curves were measured using a Ψ-MOSFET, and *C-V* curves using a MOS capacitor as shown in the insets. The insets show a schematic of the devices used to measure the curves.

At the conference, we will also discuss that hysteresis loops are observed in the NVFET via typical ferroelectric hysteresis measurements. In this case, the "polarization" charge measured results from protonic motion in the buried oxide.

The transient behavior of the field induced charge migration from an accumulated interfacial layer into the bulk of the buried SiO_2 layer was analyzed earlier [6] as a function of different gate voltages (V_G) and different temperatures. As discussed in the full paper, the activation energy for motion of both the H or D related species is estimated to be ~ 0.8 eV, identical to that reported for H^+ diffusion in SiO_2 [3,5]. Our data and previous work on post-irradiation interface state density buildup [3-5] suggest that H^+ and D^+ transports through the SiO_2 film by a process involving the formation and dissociation of bonds with bridging network oxygens. It is suggested that the defects so formed are positively charged and that the conduction proceeds by simple hopping of H ions from one bridging O bond site to another.

The mechanism can be exploited in the design of a nonvolatile field effect transistor (NVFET). For instance, an n-channel transistor can be changed to "normally on" or "normally off" by applying a positive or negative gate (substrate) bias which will drift the protons to the top Si/SiO_2 or substrate Si/SiO_2 interface, respectively. For a memory device this can be interpreted as writing the device to a bit state "1" or "0", respectively. To read the device, the zero bias drain current I_0 is simply measured (high current then corresponds to logic state "1", low current to "0"), as visualized in Fig. 1 (a).

For memory devices, a short write time is often desired. Figure 2 shows the IV characteristics of poly-Si/40 nm thermal oxide/Si structures. The oxides received a high temperature inert anneal to create a large density of oxygen vacancies to act as H_2 cracking sites as will be discussed later. The response time is approximately 30 msec. Since the protons move via a space charge limited current flow as illustrated in the full paper, proton motion speeds up dramatically in thinner oxides. That is, the speed of the proton transport, and hence the switching speed, is proportional to d^{-3}, where d is the oxide thickness. For devices fabricated using a poly-Si-capped 10-nm thermal oxide substrate, a write time of about 1 ms is anticipated at room temperature. These results demonstrate that NVFET-based memories can be fabricated using standard thermal oxides with poly-Si capping layers, so both bulk-Si and fully depleted SOI based nonvolatile memories are achievable in this technology. Further details of the two types of implementations will be discussed in the full paper.

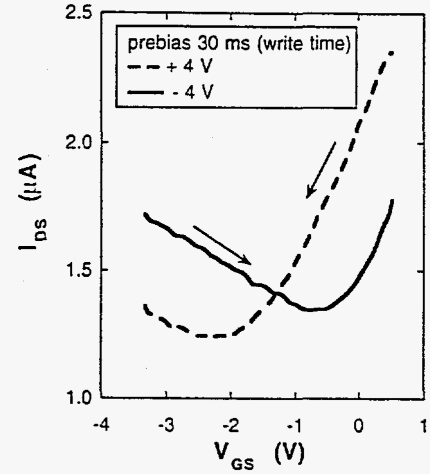

Figure 2: IV Hysteretic behavior of poly-Si/40 nm thermal oxide/Si structures after receiving a 550°C FG anneal.

Figure 3 shows the radiation response of the NVFET following a 100 krad (SiO_2) irradiation at 0V bias, typical operating conditions for a SOI-based NVFET memory. Note that the "window" between the two states of the memory is virtually unchanged by radiation exposure at 0 V bias. Thus, SOI-based NVFET's has the potential to show excellent radiation response.

We now discuss a possible mechanism underlying the incorporation of mobile H^+ ions in a $Si/SiO_2/Si$ structure. It is known that a high-temperature inert anneal step creates neutral O vacancies (Si-Si bonds) in the buried oxide via O out-diffusion from the SiO_2 into the top and substrate Si layers [11]. These O vacancies are preferentially located near both of the Si/SiO_2 interfaces. Because these strained Si-Si bonds can act as H_2 cracking sites [12] in the buried SiO_2, they are catalyst sites for the generation of atomic hydrogen. When this H^0 reaches the top or bottom interface, its electron may be liberated to the Si conduction band, resulting in H^+. So the two buried-SiO_2/Si interfaces act as "proton generators". Since the solubility of H species in Si is low, once formed, the H^+ is largely "imprisoned" in the buried SiO_2 layer, sandwiched between the two encapsulating *c*-Si layers, i.e., the interfaces form a diffusion barrier for H_2. Mobile H^+ ions are not typically observed in H-annealed thermally-oxidized Si wafers since the Si-Si bond densities (cracking sites) are significantly less numerous, and H diffusion barriers at the SiO_2/gate (or ambient) interface are usually small. The radiation tolerance of this structure apparently results from the unexpectedly small cross-section for the protons to capture radiation-induced electrons [13].

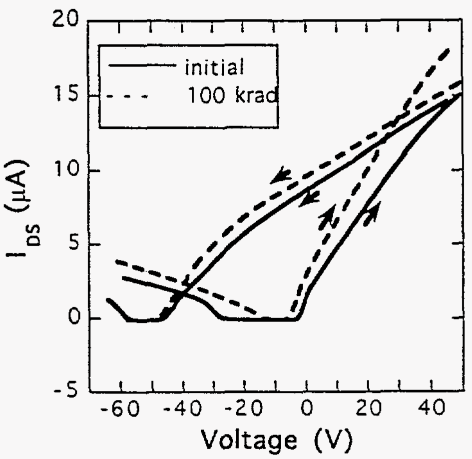

Figure 3: IV curves of a SIMOX NVFET following before and after unbiased 100 krad (SiO_2) irradiation.

IV CONCLUSIONS

From a fundamental view, the ability to create protons via a forming gas anneal allows one to directly probe protonic motion in the Si/SiO_2 system. This makes it possible to investigate hydrogen chemistry and physics in the Si/SiO_2 system in a fairly simple and straightforward manner. From an applied point of view protons in SiO_2 structures have great potential for application in the design of a new generation of non-volatile memories. This device is simple, completely compatible with bulk-Si and SOI MOS processing, and potentially radiation-tolerant.

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