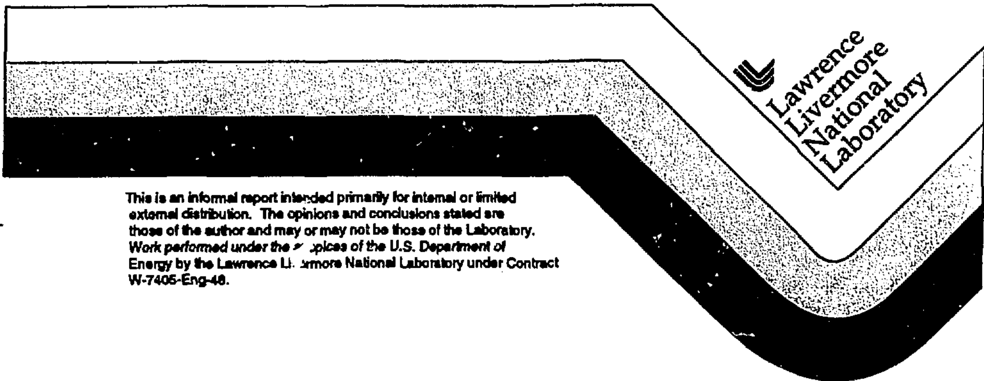
12/5-1-95 JS (1)

UCRL-ID-114325

Single Event and TREE Latchup Mitigation for a Star Tracker Sensor: An Innovative Approach to System Level Latchup Mitigation

J. R. Kimbrough, N.J. Colella, R.W. Davis
D.B. Breuner, P.G. Coakley, S.W. Lutjens and C.E. Mallon

August, 1994



This is an informal report intended primarily for internal or limited external distribution. The opinions and conclusions stated are those of the author and may or may not be those of the Laboratory.
Work performed under the auspices of the U.S. Department of Energy by the Lawrence Livermore National Laboratory under Contract W-7405-Eng-48.

DISCLAIMER

This document was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor the University of California nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial products, process, or service by trade name, trademark, manufacturer, or otherwise, does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or the University of California. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or the University of California, and shall not be used for advertising or product endorsement purposes.

This report has been reproduced
directly from the best available copy.

Available *to DOE and DOE contractors from the*
Office of Scientific and Technical Information
P.O. Box 62, Oak Ridge, TN 37831
Prices available from (615) 576-8401, FTS 626-8401

Available to the public from the
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Rd.,
Springfield, VA 22161

Single Event and TREE Latchup Mitigation for a Star Tracker Sensor: An Innovative Approach to System Level Latchup Mitigation

J. R. Kimbrough, N. J. Colella, and R. W. Davis
Lawrence Livermore National Laboratory*
Livermore, CA 94550

D. B. Breuner, P. G. Coakley, S. W. Lutjens, and C. E. Mallon
JAYCOR
San Diego, CA 92121

ABSTRACT

This paper presents an innovative "blink" approach rather than the typical "operate through" approach to achieve system level latchup mitigation on a prototype star tracker camera. Included are circuit designs, flash x-ray test data, and heavy ion data demonstrating latchup mitigation protecting micro-electronics from current latchup and burnout due to Single Event Latchup (SEL) and Transient Radiation Effects on Electronics (TREE).

INTRODUCTION

Electronic packages designed for spacecraft should be fault-tolerant and operate without ground control intervention through extremes in the space radiation environment. If designed for military use, the electronics must survive and function in a nuclear radiation environment. Radiation reliability requirements are met by the use of hardened electronic parts and circumvention circuits for protection against a radiation pulse. However, hardened parts are expensive and lag the performance of commercial parts. Commercial parts can provide a significant increase in satellite

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

MASTER

DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

computational and imaging performance without accompanying increases in cost, mass and power. System level latchup mitigation and fault-tolerant computing technologies address concerns of Single Event Upsets (SEU) and destructive Single Event Phenomena (SEP), due to cosmic ray particles or weapon generated prompt ionization pulses [1,2,3]. Mitigating the latchup current effects at the system level rather then the part level removes the restriction that all parts must be latchup immune.

Destructive Single Event Phenomena (SEP) due to cosmic rays are Single Event Latchup (SEL), Single Event Burnout (SEB), and Single Event Gate Rupture (SEGR). A cosmic ray creates a high density current path in the device resulting in overheating and local melting in the metalization or dielectric layers. In CMOS devices the ion creates a parasitic 4 layer p-n-p-n Silicon Controlled Rectifier (SCR) resulting in SEL. After 440 μs the high density current in the SCR can destroy the device [4].

SEB occurs in n channel MOSFETs depending upon the device operating voltages. The ion's ionization path creates a current density sufficient to turn on the parasitic npn bipolar transistor which then goes into current avalanche mode. Device burnout occurs within tens to hundreds of microseconds depending upon the drain to source voltage, and current density [5, 6].

SEGR is due to an ion creating a high conductivity path through the gate dielectric and rupturing the gate dielectric. Sufficient energy must be stored in the gate's electric field to melt the dielectric and the metalization layers. Power MOSFETs and EEPROMs are susceptible to SEGR due to high electric fields across insulators in the devices. In the case of EEPROMs the high electric field is only present during erase or write operations [6, 7, 8].

Our innovative "blink" approach addresses current latchup at the system, subsystem or package level of integration. Detection of either an external high flux event or internal excess current flow causes the system to "blink." Within microseconds power is disconnected, and the stored energy dumped to ground before semiconductor damage occurs. System level mitigation is analogous to a person blinking at a bright flash of light.

This work represents a first for: (a) self-contained sensing for latchup, (b) fast power removal to protect latched components, and (c) autonomous recovery for transparent operation to other system elements. Our approach detects a latchup and removes power (called power dump) in less than 2 microseconds from all susceptible devices before damage can occur. This paper discusses the circuitry, heavy ion test results, and flash x-ray (FXR) test results that demonstrate the effectiveness of the approach in a high performance star tracker camera system designed by

Lawrence Livermore National Laboratory (LLNL).

CAMERA CIRCUIT DESIGN

The primary radiation hardening emphasis is survival in natural space radiation environments, with the additional capability to survive a prompt radiation pulse associated with a nuclear event. The major design features are:

-Selection of semiconductor devices with an acceptable radiation response.

-Using a radiation tolerant power supply to provide noise immunity and ease system integration.

-Single event and prompt pulse latchup mitigation including event detection, power dump, and energy limiting measures with autonomous recovery.

-Addition of a dark line compensation circuit to remove radiation induced dark lines caused by radiation striking the CCD dark reference cells. High performance cameras use these dark cells to establish a noise floor and provide noise compensation.

Figure 1 shows the block diagram of the star tracker electronics. Excluding the DC-DC converter the star tracker consists of commercial non radiation hardened components. The Star Tracker is based upon the Thomson TH7883 Charge Coupled Device (CCD) and the Thomson TH7990 Drive Clock Sequencer and & Synchronization integrated circuit. TH7883 is a NMOS technology single field area image sensor consisting of 576 by 384 pixels. Each pixel size is 23 μm x 23 μm. The TH7883's light sensitivity and low noise makes it attractive for star tracker applications. The TH7990 Drive Clock Sequencer & Synchronization device (CCD controller) requires +5 VDC and provides all the synchronization and drive signals required to operate the TH7883 CCD.

The radiation assessment of the components indicated that several components required total dose tests. In addition the TH7883 CCD and TH7990 controller required SEU and SEL tests. Piece part total dose tests confirmed operation up to 15 krad(Si). A small 15 watt radiation hardened DC-to-DC converter mounted on the circuit board converts the standard spacecraft 28 VDC power to ±15 VDC and ±5 VDC required for camera operation. In addition the converter isolates the camera from other electrical noise sources in the spacecraft. The isolation minimizes the Electromagnetic Interference and Electromagnetic Coupling (EMI/EMC) effects. Minimization of

the EMI/EMC allows using the camera in a wide range of applications.

All camera operating voltages are derived from the DC-DC converter with the exception of the ionizing radiation pulse detector, which requires external uninterrupted power. Current limiting resistors and minimization of circuit capacitance reduce the current and stored charge available for semiconductor burnout. In addition, latchup mitigation circuitry shown in figure 2 protects the camera electronics from potential damage due to prompt photocurrents and integrated circuit latchup. The circuit senses and responds to either transient ionizing radiation or a transient current on the +5 V bus caused by single event latchup. The mitigation circuit includes the DC-DC converter, ionizing radiation pulse detector, power MOSFET switches, dual function linear integrated circuits and driver transistors.

When latchup current transients occur on the +5 VDC line amplifier U2B amplifies the voltage increase across a 0.1 ohm sense resistor due to the increased current and U2A compares the voltage to a preset threshold. If the sense voltage exceeds the comparator threshold, the comparator drives the self test input of the ionizing radiation pulse detector HIGH initiating a power dump. The DC to DC converter output voltages are disabled and crowbars (labeled CB+ and CB-) shunt each regulated output voltage to ground. Autonomous recovery occurs upon time out of the radiation pulse detector with the restoration of power and initialization of the camera control logic.

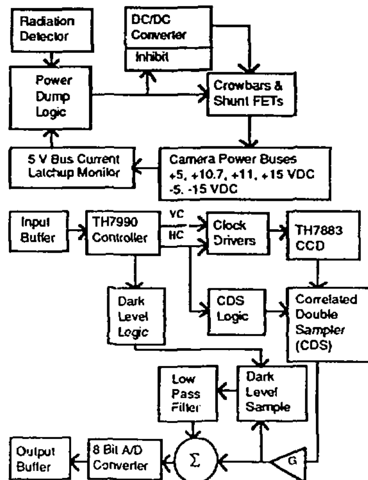


Figure 1. Block Diagram of the star tracker. VC are vertical clocks and HC are Horizontal clocks.

Figure 2. Power dump circuit with DC-DC converter.

SETUP FOR SEL TESTS

SEL tests and FXR dose rate effect tests were performed at system and component levels. SEL tests consisted of heavy ion and strobe light induced latchup in delidded controllers. Heavy ion SEL tests performed at the 88 inch cyclotron at Lawrence Berkeley Laboratory used the Aerospace Corporation target and diagnostic chamber. Aerospace Corporation monitored ion flux and energy. Table 1 shows the ions, Linear Energy Transfer (LET), and angle between the beam and the normal to the device surface.

TH7990 controller SEL tests consisted of operating delidded ceramic versions of the plastic device and monitoring the +5 VDC for latchup current during ion exposure. Monitoring one phase of the four phase "CCD readout register clock" and the "composite blanking pulse" output lines verified device operation. Operating the camera while exposing the TH7990 controller to the beam allowed system level latchup mitigation tests. TH7883 SEL tests and system level latchup mitigation tests used the same ions as the TH7990 SEL device tests but only at zero degree rotation.

A strobe pulse of approximately 2 µs FWHM from a General Radio Model 1538-A Strobotac caused latchup in a de-lidded TH7990 controller chip. This allowed bench top testing of

the latchup mitigation circuit while monitoring the camera bias voltages and TH7990 control signals.

Heavy Ion and Strobe Light Test Results

During the ion TH7990 controller SEL tests the part latched with 100 to 140 mA increase in current. Figure 3 shows latchup cross section for a delidded TH7990 controller. The onset of latchup occurred at an LET of 14.5 (MeV/mg/cm^2) and the saturated cross section is 1.7×10^{-3} cm^2.

Figure 4 shows outage times and recovery of the +15, +11, +10.7 and +5 V sources. An arbitrary power dump period of 5 ms removes power long enough to quench any latchup, yet short enough to minimize system impact. Following power-up, the camera comes up in an undefined state and requires a re-initialization to restore the correct operating mode. The TH7990 wave forms show operational recovery indicative of an automatic mode reset (MDCNTL and INIT set internal TH7990 mode control registers). At this point a computer can reset the camera logic in response to a fast interrupt. The bottom trace shows one clock output from the TH7990.

Table 1. Characteristics of Ions Used in SEP Tests

Ion	Energy (MeV)	Rotation (deg)	LET (MeV/ (mg/cm^2))
^{20}Ne	89	0	5.5
^{20}Ne	89	60	11
^{40}Ar	175	0	14.5
^{40}Ar	175	48	21.7
^{65}Cu	283	0	28.8
^{86}Kr	366	0	38.8
^{86}Kr	366	60	77.6
^{136}Xe	603	0	63.3
^{136}Xe	603	60	126.6

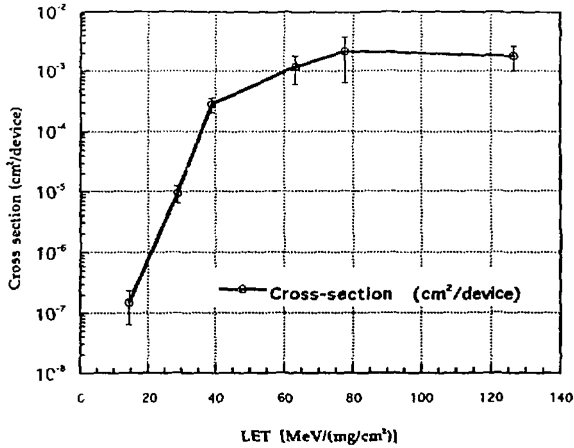


Figure 3. Latchup cross section for TH7990 controller

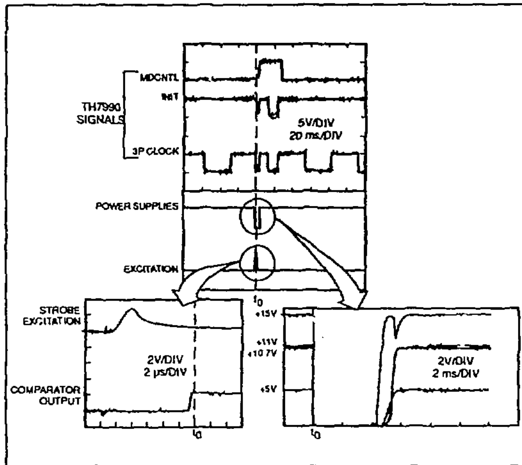


Figure 4. Time sequence in laboratory tests, showing strobe output, latchup sense output,

SETUP FOR FXR DOSE RATE TESTS

Two power dump circuits with simulated loads for the camera electronics were tested at the Physics International 1150 flash x-ray facility. Both circuits shunted the power supply output voltages to ground and disconnected the simulated camera electronics from the power supply. However, one circuit used discrete series MOSFETs to disconnect the DC to DC converter output voltages from the simulated camera electronics and shunt MOSFETs. The other circuit that is in the star tracker used the built-in output disable feature of the DC to DC converter. This later circuit has few parts and provides EMI/EMC isolation.

Table 2. Simulated star tracker electrical circuit loads

Voltage (VDC)	+15	+11	+10.7	+5	-5	-15
Resistance (ohms)	360	750	750	33	200	750
Capacitance (μF)	22	10	4.7	22	2.2	22

Physics International 1150 facility's 6 inch diameter cathode pulsed 3.8 MeV radiation source gave spatially uniform dose rates up to of 1.1×10^{11} rad(Si)/s over the area of the power dump circuit. Radiation diagnostics included an array of LiF TLDs (Thermoluminescent Dosimeters), provided and measured by Physics International, and two PIN diodes. TLD measurements provided the total dose and the PIN diodes the Full Width Half Max (FWHM) pulse width of 45 ns. The 0.87 in dose rate equation 1 converts the LiF total dose to rad(Si).

$$\text{Rad(Si)/s} = \frac{\text{Total Dose}*0.87}{\text{FWHM}} \qquad (1)$$

FXR test data were recorded on HP transient wave form digitizers. All input and output voltages were monitored by resistive voltage probes, and transient current measurements were made on the +28 and +5 power buses with Pearson Model 110 A current probes.

FXR POWER DUMP TEST RESULTS.

The FXR tests characterized the DC-DC converter power dump circuit used in the star tracker and the series switch power dump circuit. The following measurements were made: (a) power supply voltages fall time during radiation exposure, (b) recovery time of regulated voltages,

and (c) DC-DC converter input current. Recorded pre- and post-shot DC power levels provided a simple diagnostic of abnormal circuit behavior. Triggering the self test power strobe function of the ionizing radiation pulse detector provided baseline power dump data prior to radiation exposures.

Figures 5 and 6 show the fall times of the positive and negative camera bias voltages for the DC-DC converter power dump circuit. All the voltages fall to less than one volt within 2 to 3 μs, which is sufficient to preclude latchup induced burnout in integrated circuits. Comparison between the fall times for the ± 15 VDC lines before and during an exposure of 7.6×10^{10} rad(Si/s) shown in figures 7 and 8 indicate no significant dose rate effects.

The transient ringing during the radiation exposure is radiation induced cable current. Since the current injection occurs after the 2k ohm signal pick-off resistor and before the 50 ohm resistor in the 2k to 50 ohm voltage probe the transient voltage must be scaled. After scaling the estimated *transient ringing is less than 0.2 volts*

Figures 9 and 10 show the recovery of the positive and negative voltages of the DC-DC converter power dump circuit following an exposure of 7.6×10^{10} rad(Si/s). Recovery occurs within 4 ms of the exposure with 2 ms due to the time out period of the ionizing radiation pulse detector. The remaining recovery time is the RC time constant for removing the gate voltage due to gate capacitance and the 10k ohm resistor between the MOSFET gate and ground. Decreasing the 10k ohm gate resistor allows faster recovery times. The half volt overshoots on the ± 15 VDC and +5 VDC lines is coincident with the one amp surge on the 28 VDC input to the DC-DC converter. The current surge recharges and stabilizes the DC-DC converter output capacitance and the simulated load capacitance.

The second power dump circuit used series MOSFETs (IRFD9024) to disconnect the power supply voltages from shunt MOSFETs and simulated camera electrical loads. Removing the DC to DC converter output capacitance from the shunt MOSFETs results in twice as fast fall times as shown in figures 11 and 12. The fast power dump circuit of series and shunt MOSFETs is a general purpose circuit that can be used to isolate power supplies or capacitance from the sensitive electronics and dump power before damage occurs.

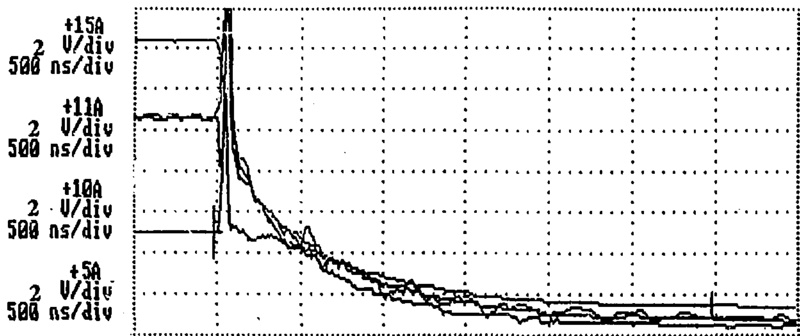


Figure 5. Fall times for the +5 VDC, +10.7 VDC, +11 VDC, and +15 VDC at a dose rate of 7.6×10^{10} rad(Si)/sec.

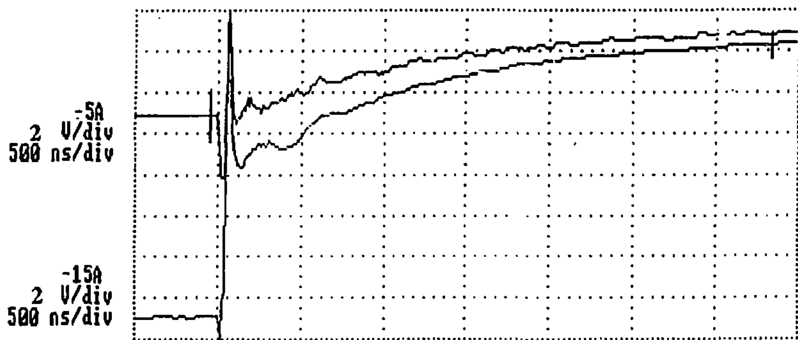


Figure 6. Fall times for -5 VDC and -15 VDC at a dose rate of 7.6×10^{10} rad(Si)/sec.

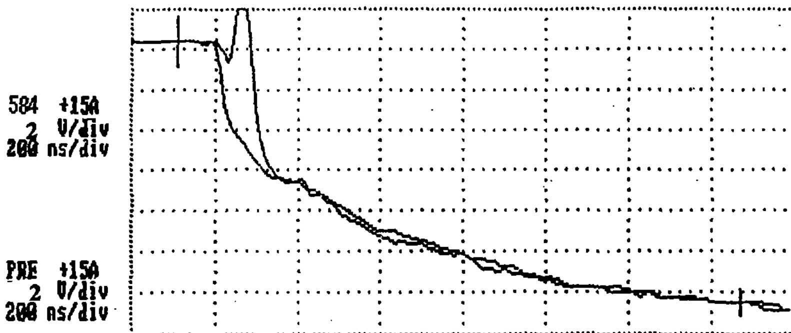


Figure 7. Comparison of the +15 VDC fall time pre shot and during exposure to $7.6x10^{10}$ rad(Si)/sec.

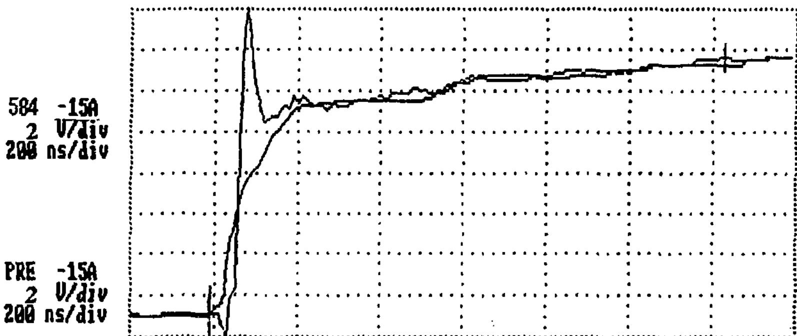


Figure 8. Comparison of the -15 VDC fall time pre shot and during exposure to $7.6x10^{10}$ rad(Si)/sec.

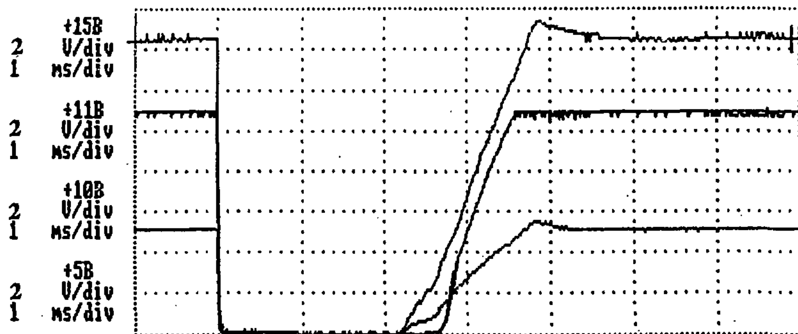


Figure 9. Recovery times for the +5 VDC, +10.7 VDC, +11 VDC and +15 VDC at a dose rate of $7.6x10^{10}$ rad(Si)/sec.

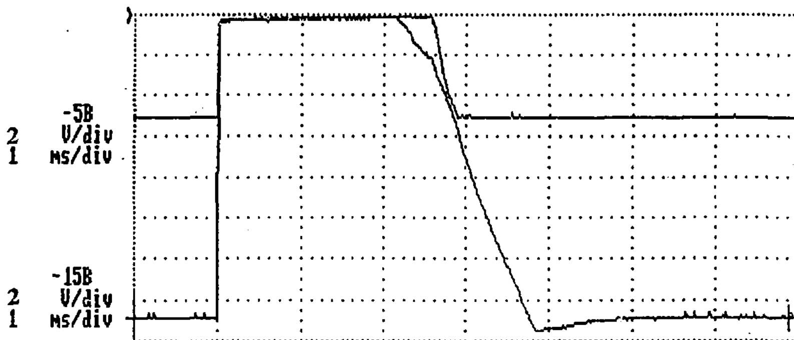


Figure 10. Recovery times for -5 VDC and -15 VDC at a dose rate of $7.6x10^{10}$ rad(Si)/sec.

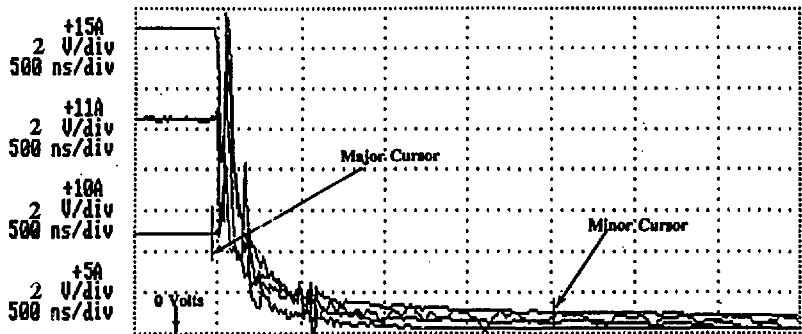


Figure 11. Fall times for the +5 VDC, +10.7 VDC, +11 VDC and +15 VDC power dump and series MOSFETs at a dose rate of 9.9×10^{10} rad(Si)/sec.

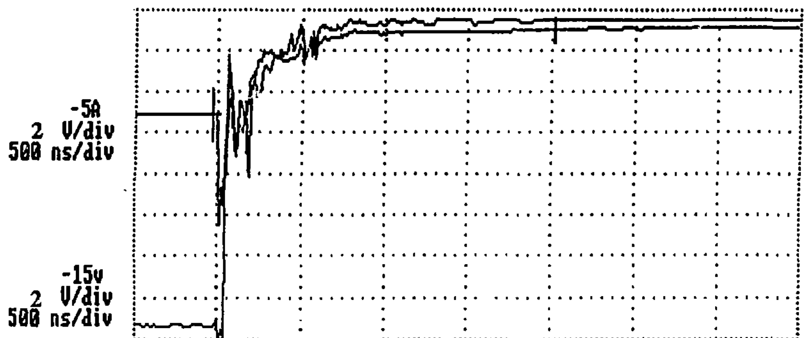


Figure 12. Fall times for -5 VDC and -15 VDC power dump and series MOSFETs at a dose rate of 9.9×10^{10} rad(Si)/sec.

CONCLUSION

The "blink" approach was developed and incorporated into a prototype star tracker for handling single event and transient radiation latchup. Laboratory and radiation effect tests confirm autonomous system level latchup detection and mitigation before permanent semiconductor burnout occurs. Heavy ion SEL and FXR dose rate radiation tests demonstrate that fast acting, low on resistance MOSFETs can quickly dump power to electronic packages and prevent device burnout. The blink approach allows the use of high performance commercial parts without the cost and performance degradation of systems based entirely on hardened parts.

REFERENCES

[1] D. A. Renee's, "Architectures for Fault-Tolerant Spacecraft Computers," Proceedings of the IEEE, Vol. 66, No. 10, pp 1255-1268, October 1978.

[2] D. P. Siewiorek, "Architecture of Fault-Tolerant Computers: An Historical Perspective", Proc. of the IEEE, Vol. 79, No. 12, December 1991

[3] J. L. Kaschmitter, D. L. Shaeffer, N. J. Colella, C. L. McKnett and P. G. Coakley, "Operation of Commercial R3000 Processors in the Low Earth Orbit (LEO) Space Environment", IEEE Trans. on Nucl. Sci., Vol 38, No. 6, December 1991

[4] F. N. Coppage D. C. Evans, "Characteristics of Destruction From Latch-up in CMOS," IEEE Tran. on Nucl. Sci., Vol. NS-24, No. 6, pp. 2226-2229, Dec. 1977.

[5] A. E. Waskiewicz, I. W. Groninger, V. H. Strahan, D. M. Long, "Burnout of Power MOS Transistors with heavy Ions of Californium-252," IEEE Tran. on Nucl. Sci., Vol . NS-33, No. 6, pp. 1710-1713, Dec. 1986.

[6] T. A. Fischer, "Heavy-Ion, Gate-Rupture in Power MOSFETs," IEEE Tran. on Nucl. Sci., Vol . NS-34, No. 6, pp. 1786-1791, Dec. 1987.

[7] J. C. Pickel, J. T. Blandford, Jr., A. E. Waskiewicz, V. H. Strahan, Jr., "Heavy Ion Induced Permanent Damage in MNOS Gate Insulators," IEEE Tran. on Nucl. Sci., Vol . NS-32, No. 6, pp. 4176-4179, Dec. 1985.

[8] T. F. Wrobel, " On Heavy Ion Induced Hard-Errors in Dielectric Structures," IEEE Tran. on Nucl. Sci., Vol . NS-34, No. 6, pp. 1262-1268, Dec. 1987.