A New Pulse Arrival-Time Recording System[1]

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ABSTRACT

We describe a new pulse arrival-time recording system that is being developed at Los Alamos. The new PATRM/PCI (Pulse Arrival-Time Recording Module/Peripheral Component Interconnect) has had several features added. These features enhance our time-correlation-measurement capabilities. By applying the latest advances in electronics and computer technology we are able to increase capability over existing instrumentation while lowering the per channel cost. The modular design approach taken allows easy configuration of both small and large systems.

Introduction

We developed the PATRM (Pulse Arrival-Time Recording Module) [1] at Los Alamos approximately 5 years ago. It is being primarily used on systems involved in neutron coincidence and neutron multiplicity studies. This dual-width, CAMAC module essentially records the arrival-time of signals applied to any of its inputs. These arrival-times are stored sequentially into the PATRM's on-board memory. The recording of raw arrival-time data allows different algorithms to be performed on the same data. This module has proven to be very useful for time-correlation measurements and has provided an effective diagnostic tool . One disadvantage of recording raw-arrival-time data is that it requires a large amount of high-speed memory. The original PATRM has static memory

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modules that are much more expensive then the conventional dynamic memory modules used in today's PCs. The PATRM can store up to 4 million 32bit events with the finest time resolution of 100ns. We are currently developing two types of systems that require time-correlation measurements; large multi-channel waste-assay and interrogation systems, and small low-cost monitoring systems. Our previous acquisition systems required several different types of modules to perform the complete data acquisition. Our goal is to replace a rack of hardware with essentially a small expansion chassis or with a single card and at the same time provide increased capability and lower cost. The new PATRM/PCI will perserve all the functionality of the original module with several features added. Some of the new features are: (1. Channel ID tagging, (2. finer time resolution in order to permit gamma/neutron time correlation studies, (3. virtually unlimited data storage, (4. programmable channel selection, (5. programmable channel delay gating and, (6. on board scalers, i.e., counters for every channel.

PATRM/PCI System Description

The PATRM/PCI uses the PCI(Peripheral Component Interconnect) bus standard. The PCI standard is a high-performance I/O bus architecture developed mainly by Intel Corp.[2]. The PCI bus is processor independent and has been adopted by all major computer manufacturers. The 32-bit, 33Mhz, version of the PCI bus has a theoretical bandwidth of 132 Mbytes/sec. The PATRM/PCI is a single card that accepts 16 differential ECL(emitter-coupled-logic) signals and provides the necessary high-speed circuitry to time-tag and channel-tag incoming signal events. The events are then stored into main memory or memory residing on a PCI memory card . A small system implementation would consist of at least one PATRM/PCI card plugged into a standard

PCI motherboard with CPU. For large system with several input channels one can use a bus expansion chassis. Current motherboards have up to 6 PCI slots and there are passive backplanes with up to18 PCI slots available. The majority of the PATRM/PCI design is implemented by one 20,000 gate, FPGA(field-programmable-gate-array).

PCI Bus Versus Other Busses

Why develop a system based on the PCI bus standard and not VME, VXI or even CAMAC? The main reason is cost versus performance obtained with the PCI Bus. The PCI bus standard allows very fast, high level designs without expensive hardware and system software. The PCI bus standard allows any card on the bus to be a bus-master. Thus affording high-speed data transfers to and from either main memory or a memory card on the PCI bus without CPU intervention. Another performance feature is true plug and play. Because PCI standard incorporates all board setting in its configuration space, that is, all board parameters can be set under software control. Because the PCI bus is designed primarily for the PC market, the price of implementing a PCI card is relatively inexpensive. Several PCI controller ICs are available from different manufactures. These ICs are advanced, single chip solutions which are quite inexpensive. Although the PCI cards lack the industrial-strength aspect of the VME or VXI, there are emerging form factor boards that address this issue. The Compact PCI [3] form factor seems to be one implementation that shows great promise of industry acceptance. The Compact PCI standard is designed around a passive backplane using low-capacitance connectors. The standard configuration allows up to 7 boards per PCI bridge. The board size is the 3U or 6U Eurocard standard, the same form factor as used in VME. A design that is developed on a standard PCI card can be easily ported to a Compact PCI module, because the

interface controller is the same. The initial prototype of the PATRM/PCI is being developed in a standard PCI backplane with a future version most likely ported to Compact PCI.

PATRM/PCI Card Description

In the normal mode of operation, the PATRM/PCI board is first configured under software control and the inputs are enabled. Up to 16 ECL(emitter coupled logic)signals, (which originate at detectors), are fed into the standard ECL I/O connector located on the PATRM/PCI (see Fig. 1). Once the input pulses are synchronized they are processed in a pipeline-fashion at the programmable clock rate. We plan to use the higher speed-grade FPGAs when they become available. This will allow use to achieve a clock rate of 100Mhz or a time resolution of 10ns. The output of the synchronizer is loaded into the Programmable Delay Shift Register(PDSR). This register allows synchronization with external events. When a non-zero,16 bit value, is shift out of the PDSR, i.e. the hit detector output goes high enabling the High Speed FIFO (HSF) to store the event. The following parameters are stored into the HSF: 1) the Time Mark Counter (TMC) which is a 32 bit real time counter that is incremented at the programmable clock rate. 2) The output of the PDSR, which contains the 16 bit channel information, allowing multiple hit information to be stored in the same clock cycle, and 3) 16 bits from the status and control register, information provided such as External Gate, Veto, etc. The HSF is used to de-couple the potential high instantaneous rate from the lower readout rate of the PCI controller. The State Machine (SM) which is implement in the FPGA is used to read the FIFO, decode and compresses data, and control the PCI bus controller. The PCI controller is a commercially available PCI 2.1 [4] compliant bus mastering single-chip ASIC from

AMCC [5]. The PATRM/PCI utilizes several features of the PCI controller. This controller interfaces directly to the PCI bus with a single chip solution. It contains three physical address spaces, memory, I/O, and configuration. The input signals are also sent to 16 scalers which can be read and/or reset concurrently with the pulse arrival time recording operation.

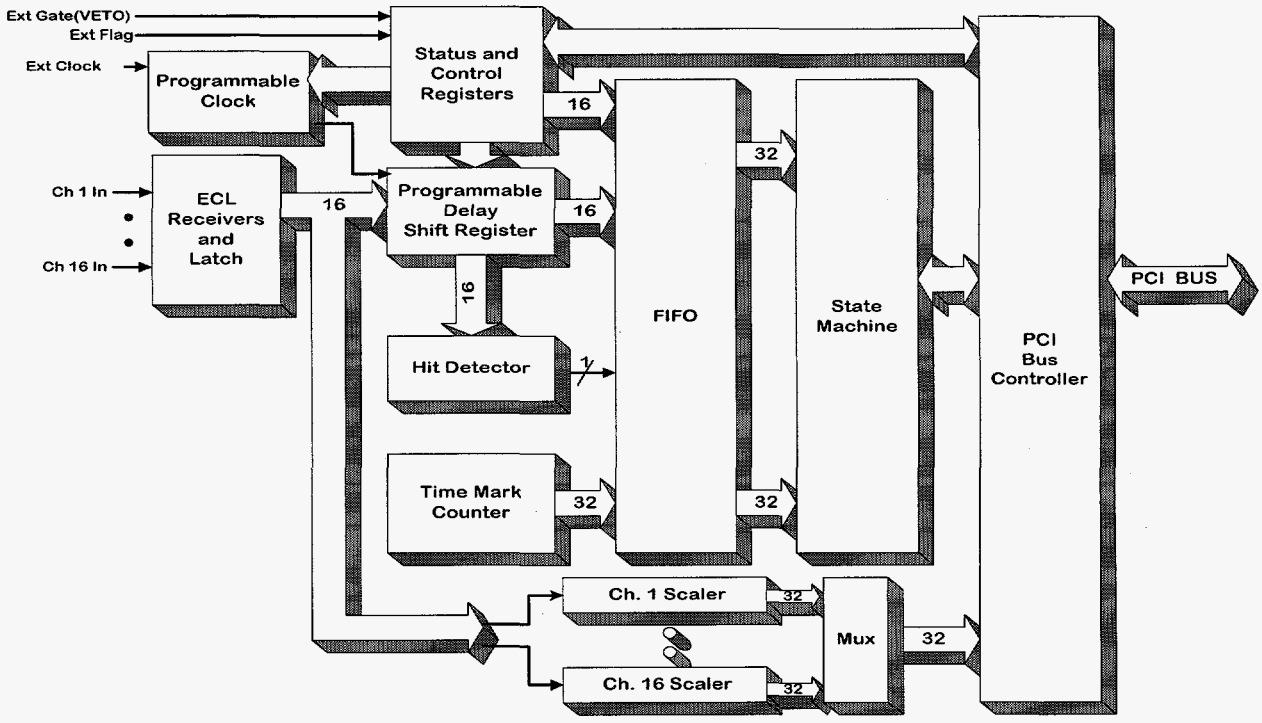

Fig. 1 PATRM/PCI Block Diagram

Status

Currently the majority of the design has been completed and critical portions have been computer simulated. A prototype board has been built and PCI controller has been tested.

Due to the delays in receiving qualified versions of the FPGA that was chosen post-route simulation have only been done. Currently the 20,000 gate, FPGA, houses the majority of the design including the high-speed FIFO and state machine. The other parts of the design are implemented in ECL and the single PCI controller chip.

Acknowledgments

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[1] G.J. Arnone, et al., "A Pulse Arrival-Time Recording Module for Analyzing Neutron Multiplicity's", Los Alamos National Laboratory document LA-UR-92-3460, presented at the 1992 IEEE NSS Conference.

[2] Intel Corporation, Santa Clara, Ca.

[3] Compact PCI Specification, IEEE 1101.11.

[4] PCI Specification, Rev. 2.1, PCI Special Interest Group, P.O.Box 14070, Portland, Or.

[5]AMCC, 6195 Lusk Blvd., San Diego, Ca.