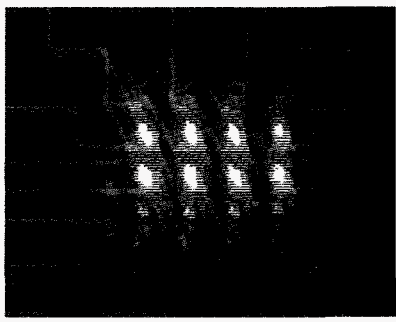
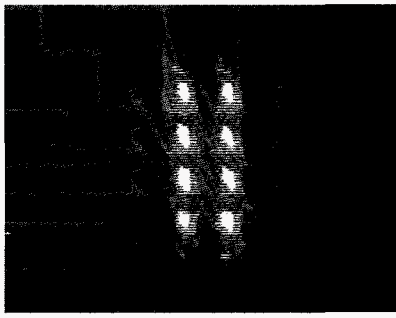


NCAICM

National Center for Advanced Information Components Manufacturing



Program Summary Report

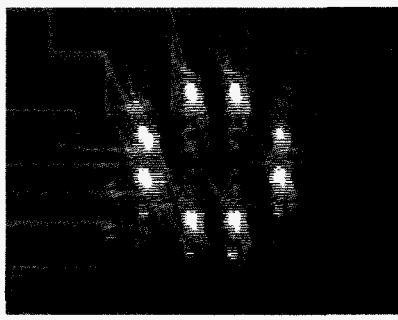
Volume II

October 1996

Defense Advanced Research Projects Agency

Department of Defense

Department of Energy



Cover Photos:
Sixteen element red vertical-cavity surface-emitting laser array (670 nanometer)

NCAICM
National Center for Advanced Information Components Manufacturing

Program Summary Report

Volume II
October 1996

Abstract

The National Center for Advanced Information Components Manufacturing focused on manufacturing research and development for flat panel displays, advanced lithography, microelectronics, and optoelectronics. This report provides an overview of the program, program history, summaries of the technical projects, and key program accomplishments.

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The National Center for Advanced Information Components Manufacturing (NCAICM) Program Summary Report is presented in two volumes. Volume I provides an overall summary of the Program. Volume II provides details of the program history and individual projects.

Figures

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PROGRAM HISTORY

The National Center for Advanced Information Components Manufacturing (NCAICM) program was initiated in October 1992 by the 1993 Defense Appropriations Bill, which appropriated funds to the Defense Advanced Research Projects Agency (DARPA) for establishing the program. The NCAICM program office was established at Sandia in February 1993, and a kick-off workshop was held in Albuquerque, NM, in March 1993. The workshop had broad industry participation together with the three Department of Energy (DOE) weapons laboratories: Sandia, which had overall responsibility for organizing the workshop, Los Alamos, and Lawrence Livermore. Key program inputs and suggestions from industry were obtained at the workshop. These inputs shaped both the Phase I and Phase II project areas.

The Project Advisory Board (PAB) was formed and members selected in April 1993. The PAB was composed of representatives from industry, DARPA, and the three DOE Laboratories. Proposals for the Phase I projects were submitted to the PAB by the laboratories during the June - July 1993 time frame. In parallel, proposals for Phase II projects were submitted to DARPA by industry in partnership with one or more laboratories. The PAB selected the Phase I projects and gave formal approval to the projects at the September 1993 meeting.

The Phase II projects were selected by DARPA during the September 1993 through February 1994 time frame and work on the projects was begun as soon as contracts could be established with the industrial participants. Although some contracts for the Phase II projects took an extended period of up to 12 to 18 months to establish, most were in place and work underway by mid-1994. The Phase I projects were underway by the end of October 1993.

A mid-program information exchange meeting was held in Albuquerque, NM, in December 1994 to ensure a free flow of nonproprietary information among projects, and a Program Status Report was published in February 1995. A number of projects were completed by the end of Fiscal Year (FY)95 (end of September 1995), while some continued into FY96, primarily because of delays in negotiating contracts. The NCAICM program office at Sandia was closed in mid-1996. Figure 1 gives a chronological list of the key activities for the NCAICM program.

October 1992	NCAICM established and funded through DARPA in the 1993 Defense Appropriations Bill.
January 1993	NCAICM formally established at Sandia National Laboratories.
February 1993	NCAICM program office established at Sandia.
February 1993	Sandia Commerce Business Daily announcement for the NCAICM Kick-off Workshop.
March 1993	DARPA Broad Agency Announcement 9322 issued for NCAICM.
March 1993	NCAICM Kick-off Workshop in Albuquerque.
April 1993	Project Advisory Board selected.
April 1993	Phase II white paper proposals due to DARPA.
May 1993	DARPA selected white papers for full proposals.
June 1993	Project Advisory Board made tentative Phase I project selections.
June 1993–July 1993	Phase II full proposals due to DARPA.
September 1993	Five Phase I projects formally approved by Project Advisory Board.
September 1993–Feb. 1994	DARPA made 21 Phase II project selections.
December 1994	Technical Information Exchange Workshop.
February 1995	Program Status Report published.
October 1995–June 1997	Window of completion dates for Phase I and PhaseII projects.

Figure 1. Key programmatic dates.

PROGRAM STRUCTURE

The NCAICM program had the following characteristics:

- Industry-driven, competition-selected projects.
- Two types of projects: pre-competitive projects done at the Center, and joint industry and national lab projects where intellectual property rights were protected.
- Teaming of industry and national lab resources, both personnel and facilities.
- Manufacturing focus: flat panel displays, advanced lithography, microelectronics, and optoelectronics.
- Flexible program management.
- Flexible project funding arrangements (see Project Funding section).
- 100% government-funded projects.
- Cooperative program between DARPA and DOE.
- Projects coordinated with and complementary to other DOE, DoD, university, and national laboratory efforts.
- Flexible project areas because of the technical breadth and depth of the national labs.
- Center located at Sandia with access to Los Alamos and Lawrence Livermore.

This program model was very flexible in terms of the technical project areas, funding mechanisms, cooperative arrangements, and project management.

PROGRAM INITIATION AND WORKSHOP

A workshop was chosen as the method to inform potential industry partners of the NCAICM program and to define how they could participate. After the appropriate Commerce Business Daily notice and Broad Agency Announcement (BAA), the kick-off workshop was held March 30-31, 1993. Two types of projects were defined at the workshop—Phase I: pre-competitive projects performed at the Center at Sandia that were to be staffed by Sandia, Los Alamos, and Lawrence Livermore personnel but might have industry participants; and Phase II: industry-defined and industry-led joint, competitively-selected projects conducted in partnership with the three national labs.

The goals of the workshop were to:

- Define the technical areas considered in this program.
- Inform the attendees of participation requirements.
- Solicit industry input for the pre-competitive (Phase I) projects.
- Inform industry of the national labs' capabilities in the program technical areas.

The workshop had approximately 400 attendees representing nearly 200 private sector companies and approximately 30 universities and government agencies.

PROJECT SELECTION

Phase I

Immediately after the kick-off workshop, a Project Advisory Board (PAB) was formed for the purpose of Phase I project selection and general NCAICM oversight.

Gene Feit	SEMATECH
Roger Johnson	Science Applications International Corp.
Bob Pinnel	U.S. Display Consortium
Steve McBurnett	DARPA
Charles Fowler	DOE
Ray Bair	Sandia
David Watkins	Los Alamos
Tony Bernhardt	Lawrence Livermore
Jim Jorgensen	Chairperson, NCAICM Program Office

Figure 2. Project Advisory Board.

Using the industry input from the workshop as a guideline, short proposals for Phase I projects were solicited. From the 24 proposals received, the PAB recommended several changes and consolidation to five projects, which were tentatively selected in June 1993. The project teams were requested to provide complete project plans incorporating the PAB guidance by September 1993. The PAB approved five projects for full funding beginning October 1993.

Phase II

Potential Phase II project teams had 30 days following the workshop to submit a short white paper proposal to DARPA. The proposal had to be industry-led, and the industrial partner (or lead industrial partner when more than one was involved) submitted the proposal. Approximately 140 short proposals were received. The cognizant DARPA program managers reviewed the short proposals and recommended approximately 60 for full proposals, due 30 days after white paper selection notification.

As the full proposals were received at DARPA, selection teams were formed for final project selection. Twenty-one projects were selected by DARPA, and the notifications to the project teams occurred between September 1993 and February 1994. The Phase I and Phase II projects ran concurrently.

PROJECT FUNDING

The NCAICM funding of $60M from DARPA established the Center and funded five Phase I projects and twenty-one Phase II projects. The Center funding, which included the Phase I projects, was 20% of the total funding, and the Phase II projects received 80% of the total.

The Center funding from DARPA covered three main elements: the Center program office operations, the Phase I projects, and partial funds (Sandia supplied joint funds) to move two key Sandia facilities outside the restricted "technical area": the Microelectronics Development Laboratory (MDL) and the Advanced Manufacturing Processes Laboratory (AMPL). These two Sandia facilities are major information components manufacturing R&D facilities; the MDL contains a silicon wafer fab and the AMPL contains the large area processing capability needed for flat panel displays. Another facility, the Compound Semiconductor Research Laboratory (CSRL), which contains the III-V materials processing capability, was already outside the restricted "technical area." The Phase I projects used these laboratory facilities, and many Phase II projects also used these facilities. The NCAICM program office was located in the AMPL.

Since minimizing development time was a critical issue with nearly all of the Phase II projects, it was necessary to have the most time-efficient funding methodology available. Each of the Phase II proposals was submitted by the lead industrial partner, but the proposals were written such that the Industry and Laboratory tasks and funding were readily separable. The model shown in Figure 3 was used to distribute the funds and establish the required agreements among the participating agencies and partners.

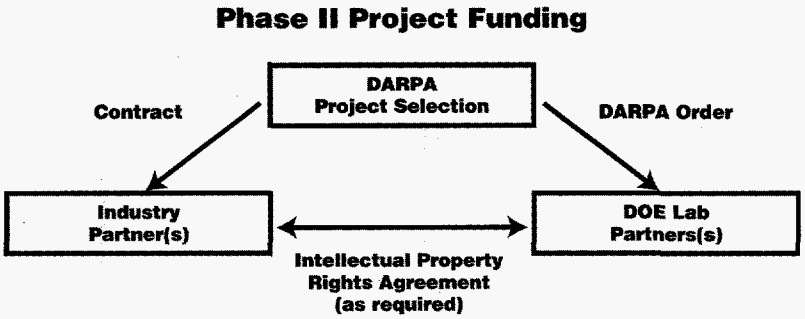

Figure 3. Project funding model.

DARPA, utilizing the BAA, directly contracted with the lead industry partner for the industry part of the project through DARPA's most efficient means. A standard interagency funding agreement was used to transfer funds to the DOE lab partners. Each of the laboratories submitted their part of the project proposal to DOE for approval through normal processes and, thereby, received their funding directly from DARPA. The only agreement required between the industry partner(s) and the lab partner(s) was an intellectual property rights agreement.

PROJECT MANAGEMENT

A small, permanent staff resided at the Center at Sandia for the purposes of general program administration and project management. This staff served as a resource for the PAB, provided program management for the Phase I projects, and was the primary contact for program administration for DOE. The Center staff also assisted the DARPA program managers as required in the Phase II project management. The NCAICM program office staff had representatives from each of the three Laboratories to facilitate the flow of program and project information among the Laboratories.

A mid-program review of all NCAICM projects was held in early December 1994 to provide a forum for cross-project interaction. The PAB reviewed the Phase I projects on a quarterly basis, and the cognizant DARPA program managers also reviewed their projects on a quarterly basis. Other forums, such as the DARPA High Definition Systems review for flat panel displays, were also used for project information dissemination and cross-program coordination.

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Of the twenty-six projects, twenty-one had follow-on activities of some type. A total of forty-four follow-on or spin-off activities came from the twenty-one projects having such activities. The funding sources for the forty-four follow-on or spin-off activities are as follows:

- Industry 21
- Government 17
- National laboratory 6

Figure 4 summarizes the follow-on activities of the NCAICM projects. Twenty-five of the twenty-six projects produced results likely to be used in manufacturing by industry, and eight projects produced results sufficiently mature to be used directly by the industrial partner.

ORIGINAL PROJECTS		POTENTIAL FOLLOW-ON
Flat Panel Display Projects		
Phase I	Phosphor Characterization Facility	PCF operation expected under CRADA funding. DARPA provided follow-on funding for FY96.
Phase I	Electron Emission Characterization Facility	DARPA provided follow-on funding for FY96 with an option for FY97. Other potential projects include work with DOE Basic Energy Sciences.
Phase I	Flat Panel Display Cost Modeling	Follow-on is the U.S. Display Consortium Factory Simulation project. NCAICM will support incorporation the FCM into the USDC simulation tool.
9322-040	Low-Cost, Large Area, Field Emission Display Development Program	DOE-funded related activities with SVC at LLNL. SVC provided significant funds to LLNL, as well as equipment donations. SVC received TRP funding.
9322-068	High-Performance Manufacturing Technology for FED Based FPDs	The automated vacuum probe station, designed and built under this program, has been commercialized and is available for purchase.
9322-127	Diamond Cold Cathode Technology for Field Emissions Display Manufacturing	SIDT continues development of diamond-based flat panel displays and continues to invest in display development.
9322-136	Field Emitter Array Patterning for Large Flat Panel Displays	Interest expressed by industry to initiate a follow-on program to develop a commercial tool for manufacturing field emission displays. Presently, there are no funds for this activity.
9322-014	Advanced Development of Large Area Full-Color Electroluminescent Flat Panel Display	The development work of this project is being continued through seven follow-on projects under the TRP, TTI, and STTR programs. Planar and Los Alamos are continuing their joint-project activities.
9322-041	Novel, Blue Light-Emitting Polymer Diodes for Color FPDs	Continued development is being funded through five projects, which fall under internal lab funding, the TTI program, and a joint LANL-University of California project.

Figure 4. Summary of follow-on activities.

ORIGINAL PROJECTS		POTENTIAL FOLLOW-ON
Flat Panel Display Projects (Continued)		
9322-002	Precision Thick Film Technology for 100% Yield of Large Area High-Resolution Color AC-PDPs	Photonics plans to introduce the processes developed in this project into production.
9322-003	Improved Emissive Coatings for Super-High-Efficiency Color AC-PDPs	This project will continue though FY96. At present, no follow-on is anticipated.
9322-009	Low-Cost Maskless Electrode Fabrication Process for HDS Color FPDs	Photonics will continue work to introduce electroplating of conductor patterns into production. DARPA approved funding for continued Sandia support in FY96.
9322-052	Advanced Lithography Tool for Large Area FPD Manufacturing	Polyscan intends to include Sandia in follow-on proposal to DARPA. Phase II of this project is scheduled to start in mid-1996.
9322-135	Glass Panel Alignment and Sealing for FPDs	DARPA provided follow-on funding for FY96 and FY97 activities. USDC Vacuum Sealing project planned for 1996-97. Other potential activities include CRADA and User Facility applications.
Advanced Lithography Projects		
Phase I	Automatic System Identification	No direct follow-on proposed.
9322-026	An Automatic System Identification Workbench for Active Structure Control	The Workbench project will continue through funding from General Motors. Some interest expressed by three other companies. Metron will continue to use and develop the software.
9322-088	Active Vibration and Motion Control for Advanced Lithography	Sandia made software available through a Small Business CRADA. The small business is developing a commercial version of the Maglev system.
Microelectronic Projects		
Phase I	Sensors and Metrology	The Metrology Lab is incorporated into a Sandia User Facility. Sensor work is being continued via DOE and other funding sources.

Figure 4. (continued)

ORIGINAL PROJECTS		POTENTIAL FOLLOW-ON
Microelectronic Projects (continued)		
9322-001	Chemical Vapor Cleaning for Advanced Contamination-Free Manufacturing	Program will be continued unilaterally at Air Products. SEMATECH's Surface Preparation Group is following project with interest.
9322-027	In-Situ Particle Monitoring in Microelectronics Manufacturing Processes	Insitec anticipates commercializing the HiVol instrumentation to sell to wafer fabrication tool manufacturers.
9322-022	The Development of High-Density Ferroelectric Memory	Micron is continuing development of the ferroelectric technology with internal funding. Discussions for a follow-on with Sandia have been conducted, but no definite proposal is in place.
9322-080	Manufacturing Technology for a One-Megabyte Ferroelectric PZT Nonvolatile Memory	Sandia follow-on activities are proposed or underway: two with Phillips Lab; three with Texas Instruments. Interest areas are rad-hard nonvolatile memories, ferroelectric processing, and pyroelectric IR detectors.
9322-044	Advanced Single Wafer Metallization	Equipment and process development activities will continue at CVC with the goal of commercializing the technology.
Optoelectronic Projects		
9322-015	Development of an Automated Packaging Machine for Optoelectronic Components	Follow-ons include potential participation in Air Force MANTECH program, DARPA fiber optic gyro manufacturing program, and NIST automated packaging program.
9322-020	Advanced Information Component Manufacturing: Optoelectronics Shared-Memory Massively Parallel Processor	Internal laboratory program to develop optically interconnected processors approved. DARPA, DoD services, and intelligence community funding appears likely.
9322-023	Red Vertical-Cavity Surface-Emitting Devices for Printing and Data Communications	Xerox will continue with VCSEL development via internal funding. Honeywell will continue to evaluate the manufacture and market issues.

Figure 4. (concluded)

The following companies, national laboratories, and universities were directly involved in NCAICM projects either as a prime contractor, member of a consortium, or team member. As indicated in the map (Figure 5), the projects were dispersed across a wide geographic area.

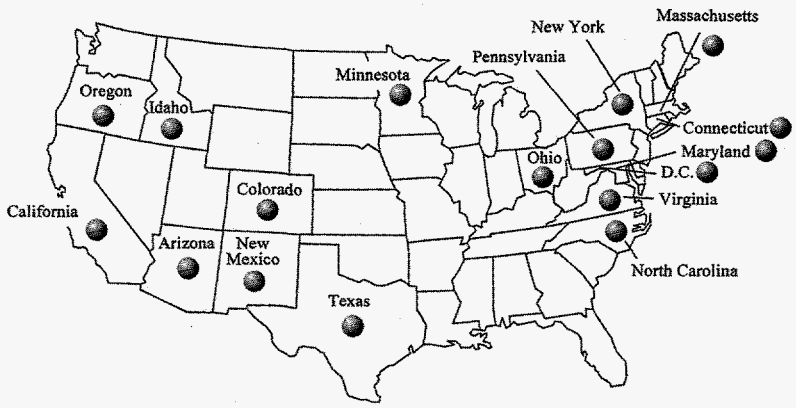

Figure 5. NCAICM participants.

Johns Hopkins University

University of Arizona

Lehigh University

University of California at Santa Barbara

Massachusetts Institute of Technology

University of New Mexico

North Carolina State University

Virginia Polytechnic Institute

Stanford University

Figure 6. Universities.

Sandia National Laboratories

Los Alamos National Laboratory

Lawrence Livermore National Laboratory

Figure 7. National Laboratories.

Air Products and Chemical Corporation
AT&T (now Lucent Technologies)
AT&T Bell Laboratories (now Lucent Technologies)
Bellcore
Coloray Display Corporation
CVC Products, Inc.
David Sarnoff Research Center
EG&G
Emcore
FED Corporation
Hewlett-Packard Company
High Density Circuits, Inc.
Honeywell, Inc.
IBM
Insitec Measurement Systems
Martin Marietta Laboratories (now Lockheed Martin)
Metron, Inc.
Micron Display Technologies, Inc.
Micron Semiconductor, Inc.
Microprobe
National Semiconductor Corporation
Naval Research Laboratory
Newport Corporation
Ortel Corporation
Photon Dynamics
Photonics Imaging, Inc.
Planar America, Inc.
Plasmaco, Inc.
Polyscan, Inc. (now Etec Polyscan)
Radiant Technologies, Inc.
Raytheon Company
Schumacher Company
Science Applications International Corporation
Shipley Company, Inc.
SI Diamond Technology, Inc.
Silicon Video Corporation
Superior Vacuum Technology
Symetrix Corporation
UNIAX Corporation
United Technologies Photonics (now Uniphase Telecommunications)
Xerox Corporation
Zenith Corporation

Figure 8. Companies.

The following projects have patent activities as noted:

FLAT PANEL DISPLAY PROJECTS

Low-Cost Large Area Field Emission Display Development Program

Project 9322-040

More than a dozen patent applications by Lawrence Livermore, or by Silicon Video and Lawrence Livermore jointly, are in process. Titles not available.

Diamond Cold Cathode Technology for Field Emissions Display Manufacturing

Project 9322-127

More than a dozen field emission display development and several diamond cold cathode technology patents were filed. Titles not available.

Advanced Development of Large Area, Full-Color Electroluminescent Flat Panel Displays

Project 9322-014

Patent Application: "Blue Light Emitting Thiogallate Phosphor," R. C. Dye, D. C. Smith (Los Alamos National Lab); C. N. King, R. T. Tuenge (Planar), October 1994.

ADVANCED LITHOGRAPHY PROJECTS

Active Vibration and Motion Control for Lithography

Project 9322-088

Two patent applications in process. Titles not available.

MICROELECTRONIC PROJECTS

Sensors and Metrology

Phase I

Patent Application: N-Methyl-2-Pyrollidinone Sensing Using Surface Acoustic Wave Technology, K. B. Pfeifer, A. E. Hoyt, G. C. Frye (Sandia National Labs), December 1995.

In-Situ Particle Monitoring in Microelectronic Manufacturing Processes

Project 9322-027

Patent search underway in anticipation of patenting the HiVol instrument.

Manufacturing Technology for a One Megabit Ferroelectric PZT Nonvolatile Memory

Project 9322-080

Patent Application: "Ferroelectric Capacitor with Reduced Imprint," J. T. Evans (Radiant); W. L. Warren, B. A. Tuttle, D. Dimos, G. E. Pike (Sandia National Labs).

OPTOELECTRONIC PROJECTS

Optically Interconnected Computing Cluster

Project 9322-020

One patent application in process. Title not available.

Red Vertical-Cavity Surface-Emitting Devices for Printing and Data Communication

Project 9322-023

Patent: "Electrically Injected Visible Vertical-Cavity Surface-Emitting Laser Diodes," R. P. Schneider and J. A. Lott Crawford (Sandia National Labs), U.S. Patent No. 5,351,256.

Patent Application: "AlGaInP/AlGaAs Heterostructure Red Laser Diodes Using Carbon as the Sole P-Type Dopant and Method for Fabrication," R. P. Schneider, Jr., M. Hagerott Crawford (Sandia National Labs), May 19, 1995.

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T. E. Felter, A. A. Talin, M. E. Malinowski, A. G. Chakhovskoi, L. Shea, B. E. Russ, J. McKittrick, J. Talbot, "Characterization of $ZnGa_2O_4$ and YAG:Cr Phosphors for Field Emission Displays," Society for Information Display International Symposium, Vol. XXVI, May 23-25, 1995, Orlando, FL.

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J. Baxter, T. Bomber, D. Lauben, "A Factory Cost Model for the Flat Panel Display Industry," Display Works '96, Semiconductor Equipment and Materials International, February 1996, San Jose, CA.

T. Bomber, J. Campbell, K. Boom, "Cost of Ownership Evaluations for Cluster Tools," *Applied Cost Modeling Newsletter*, published by Wright, Williams, and Kelley, Inc., 1996.

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"Factory Cost Model for Flat Panel Display Manufacturing" (User's Guide - Version 1.02), NCAICM, March 18, 1996.

HIGH-PERFORMANCE MANUFACTURING TECHNOLOGY FOR FED BASED FLAT PANEL DISPLAYS

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ADVANCED DEVELOPMENT OF LARGE AREA, FULL-COLOR ELECTROLUMINESCENT FLAT PANEL DISPLAYS

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"Avoiding the Pitfalls in the Use of Surface Analysis in the IC Industry," presented at the Sixth Annual IEEE/SEMI Advanced Semiconductor Manufacturing Conference, Boston.

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OPTOELECTRONIC PROJECTS

RED VERTICAL-CAVITY SURFACE-EMITTING DEVICES FOR PRINTING AND DATA COMMUNICATION

K. D. Choquette, R. P. Schneider, Jr., M. H. Crawford, K. M. Geib, J. J. Figiel, "Continuous Wave Selectively Oxidized AlGaInP Vertical-Cavity Lasers," *Electron. Lett.* 31, 1145 (1995).

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Research facilities at the three National Laboratories were actively used in the conduct of NCAICM-sponsored research and development (Figure 9). The facilities are described by the major physical plant structure with a short statement of the overall facility capability followed by a list of specific NCAICM project activities.

Advanced Manufacturing Process Laboratory, SNL/NM

Microelectronics Development Laboratory, SNL/NM

Compound Semiconductor Research Laboratory, SNL/NM

Materials Research Building, SNL/CA

Target Fabrication Facility, LANL

Electronic Materials Laboratory, LANL

Ion Beam Materials Laboratory, LANL

Electron Cyclotron Resonance Chamber, LANL

Stealth Designer's Workbench and Computing Capability, LANL

Central Computing Facility, LANL, LLNL, SNL

Center for Microelectronics and Optoelectronics, LLNL

Photonics and Advanced Telecommunications Laboratories, LLNL

Advanced Microtechnology Facilities, LLNL

Figure 9. National Laboratory Facilities.

ADVANCED MANUFACTURING PROCESS LABORATORY (AMPL)

Light laboratory with capabilities including hybrid micro-circuits, thin and thick film large area processing, materials characterization, etc.

- Phosphor Characterization Facility: State-of-the-art equipment is available to measure cathodoluminescence, photoluminescence, and electroluminescence for flat panel display phospors.

- Active Vibration and Motion Control Testbed: An existing active structures testbed and newly acquired lithography tool were used to develop an improved maglev stage incorporating structural control. The testbed was used to perform automated identification of the structural dynamics of lithography tools and subsystems.

- Flat Panel Display Cost Modeling: This project developed economic models for large area flat panel display manufacturing processes. The modeling effort included a Cost-of-Ownership tool for equipment evaluations and a static Factory Cost Model for manufacturing facility analysis.

- Glass Panel Alignment and Sealing System: A prototype system was developed to investigate alignment and sealing of flat panel plates including direct laser sealing.

- Large Area Processing Systems: Available equipment was used for developing low-cost electrode fabrication processes and precision thick film technology for flat panel displays.

MICROELECTRONICS DEVELOPMENT LABORATORY (MDL)

Heavy and light laboratory facility with more than 30,000 square feet of clean room space for processing wafers up to 150 millimeters in diameter.

- User Metrology Laboratory: The existing metrology capabilities in the MDL were augmented by a field emission scanning electron microscope computer coupled to an optical wafer scanner for patterned substrates. The User Metrology Lab provides state-of-the-art surface and gas analysis and serves as a test and analysis platform for new sensor development.

- Particle Monitoring Development: A prototype laser-based particle counter, sizer, velocimeter instrument was used in an existing MDL plasma reactor to test particle detection and measurement capabilities.

- Ferroelectric Nonvolatile Memories: The existing MDL equipment capabilities were used for process development, materials characterization, and testing of high-density ferroelectric memories.

- Cluster Tool Development: An advanced single-wafer metallization cluster tool will be installed in the MDL for process development and characterization.

COMPOUND SEMICONDUCTOR RESEARCH LABORATORY (CSRL)

This facility is used to develop compound semiconductor-based technologies for high-performance microelectronic and integrated optoelectronic components. The CSRL materials synthesis facilities provide capabilities for epitaxial growth in nearly every compound semiconducting alloy system.

- Red Vertical-Cavity Surface-Emitting Laser (VCSEL) Development: The CSRL facility was used in this effort to employ red VCSEL technology for high-performance laser printing and plastic optical fiber data communication applications.

MATERIALS RESEARCH BUILDING (MRB)

Light laboratory with small clean room, electron microscopes, scanning auger microprobes, and other materials characterization and deposition facilities.

- Electron Emission Characterization Facility (EECF): Specialized vacuum systems and electron emission microscopes are available to measure and modify electron emission from cold cathode materials and structures and to determine their compatibility with phosphors.
- Diamond Materials Development Laboratory: Existing equipment was used to develop diamond cold cathode deposition processes. The EECF is available to evaluate the field emission properties of diamond films.

TARGET FABRICATION FACILITY (TFF)

Originally built for the development and fabrication of inertial confinement fusion (ICF) targets, this facility is now being used for a variety of additional projects including NCAICM. Capabilities in the facility that were used in the NCAICM project include the following: a variety of physical vapor deposition and chemical vapor deposition capabilities; a variety of analytical tools such as scanning electron microscope, scanning auger spectroscopy, special apparatus for secondary electron yield measurements, metallurgical lab, etc.; electro- and electro-less plating capabilities; precision machining and micro-assembly at submillimeter-scale capability.

- Phosphor Development: Existing equipment and capabilities of the TFF were used to select and develop critical manufacturing processes for blue and white phosphors. The new materials and processes are directed at transitioning electroluminescent displays from multicolor to full-color capability.
- Improved Emissive Coatings: The TFF was used for the development and testing of new emissive thin film magnesium oxide dielectric coatings to improve both the efficiency and operational characteristics of plasma displays.

ELECTRONIC MATERIALS LABORATORY

Capabilities in this facility include: ultra-fast photoconductivity, Raman spectroscopy, X-ray diffraction, electroabsorption spectroscopy, internal photoemission, Hall effect and other electrical probes, photothermal deflection spectroscopy, inert atmosphere processing facilities, thermal and e-beam evaporators and other thin film deposition techniques.

- Polymer Diode Development: A multidisciplinary team used existing facilities in the Electronic Materials Laboratory to develop a new blue-light source based on electroluminescence from conjugated polymers. The effort integrated expertise and equipment required for organic synthesis, polymer processing, device physics, semiconductor manufacturing, and device modeling.

ION BEAM MATERIALS RESEARCH LABORATORY

Used in the Phosphor Development project to determine overall material composition, dopant concentration and distribution, and interface integrity.

ELECTRON CYCLOTRON RESONANCE CHAMBER

This major piece of equipment was used to determine the erosion rate of magnesium oxide films exposed to plasmas. The facility was used in the Improved Emissive Coatings project.

STEALTH DESIGNERS WORKBENCH AND COMPUTING CAPABILITY

Although not a facility per se, this capability has been developed in previous projects and represents a significant investment in time and equipment. This capability provided a computational foundation for the Control Designer's Workbench for Active Structural Control project. The Designer's Workbench was modified and improved as a result of the NCAICM project.

CENTRAL COMPUTING FACILITY (CCF):

The central computing facilities of the DOE laboratories are among the most powerful in the world. The System Identification project used the CCF capabilities in the development of computational algorithms and system control design.

CENTER FOR MICROELECTRONICS AND OPTOELECTRONICS (CMO)

Cross-cutting capabilities in materials development, characterization and modeling of fundamental material properties, and in thin-film processing and microfabrication technologies are integrated to address challenges in the semiconductor processing, electronic packaging, and flat panel display industries.

- Field Emission Manufacturing Development: Existing equipment and capabilities were used to develop aerogels or xerogels as spacers for large area displays, to reduce the operating voltage of emitter tips, and to provide a method to test field emission baseplates prior to sealing.

- Nano-Scale Field Emitter Development: Unique equipment was used in a non-photolithographic process to pattern 0.1-micron scale gated field emitters.

PHOTONICS AND ADVANCED TELECOMMUNICATIONS LABORATORIES

Light laboratories with capabilities including microwave probe station and machine vision coupled with robotics allowing submicron positioning for optoelectronics packaging. The optically connected computing cluster project benefited from capabilities including high-speed bit error rate testing for optical interconnects and networks, and optoelectronic measurements in femtosecond, picosecond temporal responses, and spectral diagnostics.

- Optoelectronic Packaging Prototype: A modular, cost-effective manufacturing prototype was developed to provide the capability to align and attach optical fiber to a variety of optoelectronic components. The system employs machine vision and automated robotics.

- Optically Interconnected Computing Cluster: A field trial used existing workstations with optical link/bus interfaces to demonstrate the feasibility of an optically interconnected distributed computing cluster.

ADVANCED MICROTECHNOLOGY FACILITIES

Three exposure facilities scaled to support the display size requirements for head-mounted displays, laptop displays, and large television displays were used to support the Optical Interference Lithography project. These facilities expose photosensitive resist applied to the surface of glass plates, resulting in very small dot patterning for fabricated field emission devices.

- Optical Interference Lithography: An optical interference lithography process was demonstrated, which can pattern and fabricate very small, high-density field emission structures over large areas. The process is simple, inexpensive, and robust, and offers the possibility of brighter, more efficient flat panel displays than conventional display technologies.

Detailed project descriptions and DARPA Quad charts for the 26 NCAICM projects are provided. The projects are presented by technology area.

FLAT PANEL DISPLAYS page 37

CHARACTERIZATION FACILITIES

Phosphor Characterization Facility

Electron Emission Characterization Facility

FPD COST MODELING

Flat Panel Display Factory Cost Modeling

FIELD EMISSION TECHNOLOGY

Low-Cost, Large Area Field Emission Display Development Program

High-Performance Manufacturing Technology for Field Emission Based Flat Panel Displays

Diamond Cold Cathode Technology for Field Emission Display Manufacturing

Field Emitter Array Patterning Using Laser Interference for Flat Panel Displays

ELECTROLUMINESCENT TECHNOLOGY

Advanced Development of Large Area, Full-Color Electroluminescent Flat Panel Displays

Novel, Blue Light-Emitting Polymer Diodes for Color Flat Panel Displays

PLASMA DISPLAY TECHNOLOGY

Precision Thick Film Technology for 100% Yield of Large Area High-Resolution Color AC-PDPs

Improved Emissive Coatings for Super-High-Efficiency Color AC-PDPs

Low-Cost Electrode Fabrication Process for HDS Color FPDs

FPD EQUIPMENT DEVELOPMENT

Advanced Lithography Tool for Large Area Flat Panel Display Manufacturing

Glass Panel Alignment and Sealing for Flat Panel Displays

Flat Panel Displays

CHARACTERIZATION FACILITIES

PHOSPHOR CHARACTERIZATION FACILITY

Phase I Project

Team: **Sandia National Laboratories**

Description:

The Phosphor Characterization Facility (PCF) was originally designed to provide several types of phosphor excitation. Cathodoluminescence (CL), ultraviolet (UV) and vacuum ultraviolet (VUV) phosphor screens and powders can be tested in this system. The system includes a vacuum system, plasma chamber and electron chamber, gauge and instrument control bay, and data acquisition computer.

A commercial hot-filament electron gun covers the 5 to 1000 eV range for low-voltage cathodoluminescent excitation, and a second gun covers the 500 to 10,000 eV range for higher-voltage and higher-power studies. A glow-discharge plasma gun was installed to provide a high current density source of very-low-energy (0-5 eV) electrons. Since noble gasses and gas mixtures are used to generate the glow-discharge, this source is used for plasma display phosphor investigations. It has the advantage of producing ions and electrons just as in a plasma display. This feature allows for a differential analysis between VUV excitation/degradation and that caused by electrons, ions, and high-energy neutrals.

A high-resolution/sensitivity quadrupole mass spectrometer monitors the cleanliness of the vacuum environment and provides real-time information about decomposition products from phosphor screens and powders during excitation. Inexpensive mass spectrometers are installed, which if contaminated or damaged by ablation products can be readily replaced.

The PCF system incorporates optical instrumentation that is used to measure phosphor emission spectra as a function of excitation intensity and time, photoluminescence response for wavelengths greater than 200 nanometers, screen reflectivity properties and screen emission uniformity, and life test parameters. A commercial VUV excitation source/monochrometer system provides information on low-energy electron and VUV excitation properties of display phosphors. Non-optical instrumentation includes voltage-source/pico-ammeters to measure screen and/or powder electrical properties.

The PCF vacuum chamber contains three separate test chambers to accommodate samples up to six inches in diameter. Eight small powder samples can be loaded into the powder sample chamber, and four 1 inch × 1 inch screen samples can be loaded into the electron gun and plasma source sample chambers at one time.

Project Impact:

The PCF is used to characterize and understand the operation of phosphors made by industrial, university, and other NCAICM partners. The PCF effort is coordinated with the Army Research Laboratory at Fort Monmouth and with the Phosphor Technology Center of Excellence at the Georgia Institute of Technology.

Accomplishments:

- The PCF was fully operational as of the first quarter of FY95.
- System calibrations are traceable to the National Institute of Standards and Technology.
- Phosphor characterization has been performed for seven organizations.
- The facility is a designated User Facility.

PHOSPHOR CHARACTERIZATION FACILITY

Paul Royer, Robert Mays, and Bob Walko, Sandia National Laboratories

Objectives

- Provide a facility to support the investigation, control, and science-based understanding of physical and other scientific emission processes (chemical, thermal, etc.) and materials (quantum – macroscale).
- Provide state-of-the-art equipment and technical expertise to support different types (acoustic, EM, ferromag-, atomic, etc.) of emissive display and device/information science and technology.
- Provide analytical capability to determine and/or characterize critical/key technology integration factors.

Approach

- Use available equipment to construct a characterization facility.
- Purchase minimal equipment to extend the systems' range of capabilities to leading-edge status in science and technology development.

Status

- Facility operational.
- Commercial, internal Laboratory, and other external (including foreign) – developed emissive materials are being tested on a routine basis.
- Characterization/development efforts span the micrometer through nano-meter-scale regimes (atoms through supramolecular structures) and include thin films, aerogel/sol-gel formulations, powders, and other novel light/charge/ion/neutral atom/phosphor/etc. emitters.

Schedule/Tasks

- Excitation sources constantly being tested and/or upgraded to ensure adequacy of physical capabilities against device/applications objectives covering energy/wavelength spectrum from sub-VUV through long IR and beyond.
- Sample preparation and test procedures in constant and dynamic optimization, along with systems calibrations and traceabilities.
- Additional materials can and will be accepted over the near-term on a regular basis.

ELECTRON EMISSION CHARACTERIZATION FACILITY

Phase I Project

Team: **Sandia National Laboratories**

Description:

The Electron Emission Characterization Facility (EECF) contains specialized equipment for the investigation of field emission from gated field emitter structures, continuous films, chemical vapor deposited diamond, and related materials. Two electron emission microscopes (EEM) and two point probe scanners (PPS) were designed and built.

Each EEM and PPS is housed in its own ultra-high-vacuum system and contains a load-lock mechanism so that samples may be changed without venting to atmosphere. The load locks speed analysis by eliminating the bakeout step that would otherwise be required for each sample. Samples may be heated (with temperature monitoring) before, during, and after analysis.

Both EEMs contain objective and projective electron optics and resolve at a fraction of a micron with magnification adjustable from 10 to 200X. Typical fields of view accommodate an entire pixel, 250 microns in diameter. One EEM uses a three-element immersion lens, which produces a low field at the surface of the sample. This is ideal for gated structures. The other EEM employs a two-element objective, which places a high field on the sample. This design has produced excellent results with gated emitters and is expected to yield results with new ungated emitter films.

The PPSs are optimized for different measurements. PPS1 scans relatively large areas, typically 3 millimeters. Large samples can be accommodated and heating, with temperature measurement, is available. PPS2 is attached to a scanning auger microprobe. This instrument permits direct scanning electron microscopy of the sample as the emission current is measured. In addition, Auger maps of the surface can be made and chemical analysis of emission sites can be performed.

The PPSs produce emission maps containing typically 128 × 128 elements. Resolution is sensitive to the gap between probe and sample as well as to the radius of curvature of the probe. Current resolution is on the order of a few microns, but sub-micron resolution is expected with PPS2 since smaller tip radii and distances should be easier to use. The PPSs also measure turn-on voltage vs. gap distance, which can help elucidate the emission mechanism.

Project Impact:

The EECF is used to characterize and understand the operation of field emission devices made by industrial, university, and other NCAICM partners. The test results provided by this facility are critical to the successful manufacture of field emission-based flat panel displays in the U.S.

Accomplishments:

- Established a world class laboratory for the investigation of cold cathode structure and materials for vacuum microelectronics.
- Completed construction of unique instruments such as Electron Emission Microscopes and Point Probe Scanners.
- Constructed emission maps on gated and ungated emitters for eight organizations. More than 200 samples investigated.
- Improved understanding of emission process.
- Reported results at national and international conferences.
- Established partnerships with industry and universities.

ELECTRON EMISSION CHARACTERIZATION FACILITY

Tom Felter, Mike Malinowski, and Alec Talin,
Sandia National Laboratories

Objectives

- Measure electron emission in field emitter display cathodes.
- Improve FED performance.
- Address compatibility and life-time issues.

Approach

- One-on-one collaborative basis with industrial and university partners.
- Samples and results proprietary.
- Research oriented.
- Publication desirable.

Status

- Published and presented work at national meetings.
- Continuing sample analysis under way with EEM and scanner. More than 200 samples investigated.
- Auger microprobe refurbished and coupled to scanner.

Schedule/Tasks

- Electron Emission Microscopes and Point Probe Scanners fully operational.
- Fast I-V System—May 96.
- Gas Handling System—July 96.
- Close-out report—Sept. 96.

FPD Cost Modeling

FLAT PANEL DISPLAY FACTORY COST MODELING

Phase I Project

Team:

Sandia National Laboratories
Lawrence Livermore National Laboratory

Description:

The Flat Panel Display Cost Models project developed economic models of large area FPD manufacturing processes. Four key technologies (active matrix liquid crystal, plasma, inorganic electroluminescent, and field emission) are the subject of the models. Model requirements were coordinated with the U.S. Display Consortium (USDC) and its member companies. Two models were developed.

The Cost-of-Ownership model (CoO) is a comparative analysis tool used for evaluation of FPD manufacturing equipment and provides relative ranking of equipment cost contributors. The CoO employs an activity-based approach to life cycle costing of equipment.

The Factory Cost Model (FCM) is a static economic model of an actual or planned FPD manufacturing facility. The FCM design allows users to customize factory process flows unique to their operation. The model consists of individual calculators for capacity, resources, and product cost. It is capable of simultaneous tracking of a user-defined number of distinct products, and allows for the sharing of equipment between multiple process steps.

Project Impact:

The goal of the project was to provide industry standard models for the economic evaluation of FPD manufacturing equipment and processes. Use of standard models is anticipated to result in improved equipment selection and lower factory costs. The models may also see use as evaluation tools in justifying capital expenditures and attracting investment capital to new display technologies.

Accomplishments:

- The CoO model is currently being used by the USDC for project evaluation.
- More than 275 copies of the CoO were distributed to USDC members and the SEMI/North American Flat Panel Display Division.
- The FCM was Beta tested with industry and licensed for use.
- The FCM will be incorporated in the USDC flat panel factory simulation tool.
- The CoO and FCM models were transitioned to commercial companies.

Flat Panel Display Factory Cost Modeling

Tom Bomber and Dave Lauben, Sandia National Laboratories;
Kris Boom, Lawrence Livermore National Laboratory

Objectives

- Develop economic models for display manufacturing that can be adapted for four flat panel technologies:
  - Plasma display.
  - Inorganic electroluminescent.
  - Field emission.
  - Active matrix liquid crystal.
- Two models were developed that are capable of evaluating each technology:
  - Cost-of-Ownership (CoO) for equipment.
  - Factory Cost Model (FCM) for plant.

Approach

- Site visits were made to FPD companies to determine generic process steps for the four technologies and receive feedback on model requirements and company needs.
- The CoO is based on the SEMATECH model that was developed for the microelectronics industry. The CoO uses Microsoft Excel as the computation platform.
- The FCM is based on requirements developed from industry input. The computation platform is Microsoft FoxPro.
- Both the FCM and the CoO are designed to run on IBM-compatible personal computer platforms.
- The CoO and FCM models were revised based on feedback from users. The models will be turned over to a commercial company for long-term maintenance.

Status

- Site visits have been conducted at 10 FPD companies that are manufacturing or developing FPDs in one of the four technologies.
- The final version of Cost-of-Ownership model, which is based on the SEMATECH CoO, has been distributed. The model uses Microsoft Excel as the computation platform. More than 275 copies of the CoO have been distributed.
- FCM was developed. Microsoft FoxPro was selected as the computation platform. The FCM Version 1.01 was distributed. Training classes were held for the user community.

Schedule/Tasks

- Site visits completed—July 94.
- First version of CoO completed and distributed—Aug. 94.
- FCM beta site distribution—Jan. 95.
- Version 1.01 of FCM distributed—Jan. 96.
- Training classes on FCM offered—March–May 96.
- Hand-off CoO and FCM to commercial firms—Sept. 96.

FIELD EMISSION TECHNOLOGY

LOW-COST, LARGE AREA FIELD EMISSION DISPLAY DEVELOPMENT PROGRAM

Project 9322-040

Team:

Silicon Video Corporation
Lawrence Livermore National Laboratories

Description:

This project developed the technology and manufacturing techniques for fabricating large flat panel displays based on field emission cathodes. The effort has two major objectives:

- Reduce the size of the field emission structure to approximately 0.1 micron.
- Fabricate the structure using a low-cost, high-throughput lithography technique that does not require expensive step-and-repeat lithography.

The smaller cathode feature size lowers the voltage that is necessary for emission to occur. This in turn, lowers the power loss due to column address switching, facilitates focusing, and allows the use of lower-voltage, lower-cost drivers.

Project Impact:

A nano-scale field emission cathode structure will enable a low-cost, field emission display that can effectively compete with active matrix liquid crystal displays for a full range of military and commercial applications.

Accomplishments:

- Lawrence Livermore National Lab (LLNL) and Silicon Video Corporation (SVC) personnel created a 3" cathode prototype line at LLNL, which developed and refined all of the processes required for large area manufacturing of field emission cathodes.
- SVC successfully demonstrated operation of fully functional, sealed 3" color display, incorporating the SVC/LLNL cathode technology.
- All of the process technology, optimized using Design of Experiments methodology, was formally transferred to SVC manufacturing personnel for use in their new manufacturing line in San Jose in January 1995.
- SVC and the Department of Energy have funded continuing follow-on work at LLNL.
- The LLNL project managers of the LLNL-SVC collaboration received the 1996 Federal Laboratory Consortium Award for Excellence in Technology Transfer.
- More than a dozen patent applications filed by LLNL, or by SVC and LLNL jointly, are in process.

Low-Cost, Large Area, Field Emission Display Development Program

Marco Slusarczuk, Silicon Video Corporation;
Anthony Bernhardt, Lawrence Livermore National Laboratory

Objectives

- Develop low-cost techniques for fabricating 0.1-micron scale gated field emitters.
- Integrate new techniques to produce nominally 3-inch-diagonal addressable field emitter arrays for use in flat panel displays.
- Scale up 3-inch FEC technology to 10" size.

Approach

- Use non-photolithographic techniques for patterning 0.1-micron scale gated field emitters.
- Use unique LLNL equipment and expertise to demonstrate feasibility of individual process steps.
- Conduct joint LLNL/SVC process development.
- Use disciplined documentation program to ensure transferable technology.
- Scale-up new FEC technology at SVC.

Status

- Demonstrated <20-volt switching of 0.15-micron emitters to get display current requirements.
- Demonstrated 3-inch prototype.
- Added DOE and SVC resources to program.
- 10-inch scale-up to be done by SVC with LLNL support.

Schedule/Tasks

- Bed of nails—Feb. 94.
- Gated emitter—July 94.
- 40-pixel test—Dec. 94.
- 3-inch FEC test—March 95.
- 3-inch display (color)—July 95.

HIGH-PERFORMANCE MANUFACTURING TECHNOLOGY FOR FIELD EMISSION BASED FLAT PANEL DISPLAYS

Project 9322-068

Team:

Micron Display Technology, Inc.
Lawrence Livermore National Laboratory

Description:

This project is developing technology for enhancing the manufacture of Field Emission Displays (FED). The three major areas include (1) development of spacers for large area displays, (2) development of a process to reduce the operating voltage of emitter tips, and (3) development of processes and equipment for testing FED baseplates before sealing of the display.

- The spacers are to be made of aerogels or xerogels. These materials can be molded or etched, and they may provide a low-cost, manufacturable spacer technology.
- The operating voltage of the grid of an FED is reduced by processes compatible with display manufacturing.
- The testing procedures, processes, and hardware for the vacuum automated testing of FED baseplates will be developed. Testing will be performed prior to sealing the display.

Project Impact:

The project was expected to provide a low-cost, manufacturable spacer for large area FEDs. Another objective was to provide a manufacturing compatible process for reducing the grid operating voltage. This reduction would lower power consumption and improve manufacturability. Finally, a method of testing baseplates before sealing was to be developed. This testing would decrease cost by eliminating packaging of defective baseplates and provide early feedback on baseplate processing.

Accomplishments:

Spacers

- Spacers with high-aspect ratio and small feature sizes have been molded using xerogels.
- Vacuum compatibility and electrical standoff capability have been demonstrated.

Reduced operating voltage

- Work function measurement techniques have been demonstrated for silicon substrates.
- The work function of silicon substrates has been reduced by > 0.5 eV.

Baseplate testing

- An automated Vacuum Probe Station has been built.
- A vacuum compatible probe card technology has been developed and probe cards are commercially available.
- FED baseplates have been tested for functionality in the probe station.
- Testing of single pixel functionality has been demonstrated but not optimized.
- The probe station was advertised in *Semiconductor Fabtech*, Issue No. 2, pg. 236, 1995, as a commercially available product.

High-Performance Manufacturing Technology for Field Emission Based Flat Panel Displays

Jim Browning, Micron Display Technology;
Anthony Bernhardt, Lawrence Livermore National Laboratory

Objectives

- Develop large area FED spacer with manufacturing compatible process.
- Develop process to reduce emitter tip operating voltage. Make process compatible with display manufacturing.
- Develop technology for testing FED baseplates in vacuum prior to packaging. Process must be high throughput and low cost.

Approach

- Use xerogels to make spacers. The material has good etch and mold properties and is vacuum compatible.
- Reduce work function of emitter tips.
- Design and build an automated vacuum probe station. Develop algorithms and hardware for display testing. Develop a probe card. Develop a baseplate-cleaning process to reduce burn-in time.

Status

- Spacers fabricated with high-aspect ratio at appropriate geometries. Vacuum and electrical compatibility confirmed.
- Work function measured on silicon samples. New process tested on bare silicon.
- Probe station operational; substrates tested; testing technique functional but not optimized on prober.

Schedule/Tasks

- Develop spacer process—May 96.
- Reduce grid operating voltage (1st phase)—July 96.
- Design and build probe station—March 95.
- Integrate spacers and sealed displays—Dec. 96.
- Reduce grid operating voltage (2nd phase)—July 97.
- Demonstrate fully automated baseplate testing—Dec. 97.

Diamond Cold Cathode Technology for Field Emission Display Manufacturing

Project 9322-127

Team:

SI Diamond Technology, Inc.
Sandia National Laboratory, CA
Lawrence Livermore National Laboratory
David Sarnoff Research Center

Description:

Develop diamond cold cathode materials to a point where they can be used for cost-effective manufacturing of high-performance field emission displays. The project tasks included:

- Improve the laser ablation Amorphic Diamond™ deposition process.
- Evaluate field emission properties of other types of diamond thin films.
- Study other wide bandgap materials.
- Examine microstructural materials.
- Study manufacturing issues.

Project Impact:

Provide material that will emit electrons at low electric fields uniformly across the cathode for high-performance and low-cost flat panel displays.

Accomplishments:

- The updated emission test chambers are operational.
- An Auger microprobe with scanning point emission imaging capabilities is on-line at SI Diamond (SIDT).
- A higher-resolution field emission map of an Amorphic Diamond™ surface was made at Sandia showing more detail of the emission sites over a broad area on the cathode.
- More than 100 externally supplied samples from 25 external sources have been received and tested at SIDT.
- The emission properties of GaN and AlN films provided by Superior Vacuum Technology Associates have been measured.
- Analysis was completed of diamond samples grown at Lawrence Livermore using a copper vapor laser. These samples were grown to test the effect of power density on emission properties.
- Amorphic Diamond™ has been optimized to yield >50,000 emission sites/cm^2 at 50 volts/micron.
- An investigation has been conducted analyzing emission from single crystal diamond.
- Emission maps have been taken of a new, internally produced, chemical vapor deposited diamond film that has a low "turn-on" field and a high-emission site density.
- Using Amorphic Diamond™, SIDT demonstrated a matrix-addressed monochrome 5"-diagonal display.

Diamond Cold Cathode Technology for Field Emission Display Manufacturing

Donald E. Patterson and Nalin Kumar, SI Diamond Technology, Inc.;
Tom Felter, Sandia National Laboratories;
Bill McLean, Lawrence Livermore National Laboratory;
Bawa Singh, David Sarnoff Research Center

Objectives

- Develop diamond cold cathode material to a point where it can be used for cost-effective manufacturing of high-performance field emission displays.
- Improve the laser ablation Amorphic Diamond™ deposition process.
- Evaluate field emission properties of other types of diamond thin films.
- Study other wide bandgap materials.
- Examine microstructural materials.
- Study manufacturing issues.

Approach

- Grow samples in-house and acquire samples from other research groups.
- Evaluate material properties at SIDT and SNL.
  - Multiprobe ball tester (FED 1.4/1.5) to measure emission field and uniformity.
  - Scanning emission auger microprobe (SEAM) to study distinct emission sites.
  - Broad area tester (BAT 4) to measure emission site density.
  - FE microscope at SNL for basic field emission physics.

Status

- All testing equipment operational.
- AD™ films improved to 50,000 emission sites/cm^2 at 50V/μm.
- Hundreds of alternative internal cathode materials tested and evaluated.
- More than 100 cathode materials from 25 external suppliers have been tested and evaluated.
- Several potential nitride and carbide cathodes evaluated.
- Sarnoff investigation of diamond/graphite composites completed for mechanism elucidation.

Schedule/Tasks

- Diamond testing and evaluation—Sept. 96.
- Amorphic diamond cold cathode optimization—Dec. 95.
- Understanding field emission from diamond cold cathodes—Sept. 96.
- Evaluation of other large bandgap materials—Sept. 96.
- Manufacturing issues—Sept. 96.

Field Emitter Array Patterning using Laser Interference for Flat Panel Displays

Project 9322-136

Team:

FED Corporation
Lawrence Livermore National Laboratory
Zenith Corporation

Description:

This project united earlier work on laser interference lithography done by Lawrence Livermore National Laboratory (LLNL) with improved high-resolution resist materials and processing techniques to develop and characterize a new high-resolution patterning process. The process produced features as small as 0.15 micron on 0.3-micron centers and was used to fabricate field emitter arrays.

Project implementation proceeded in three overlapping activities:
LLNL reassembled the original interference system and tested its functionality.
FED Corporation and LLNL jointly worked on the development of the high-resolution lithographic process. FED Corporation fabricated and evaluated test arrays. As a final test, FED Corporation combined phosphor plates from Zenith Corporation with the test arrays to demonstrate monochrome display arrays.

Project Impact:

High-resolution flat panel displays in all sizes are of strategic importance to the military and represent a critical new domestic business opportunity. Field emitter array-based flat panel displays promise numerous performance advantages over virtually every other flat panel technology. Arrays fabricated using this new process and exposure system should have significantly lower operating voltages and much higher densities. The former is important in reducing driver costs, reducing beam spread (lower lateral potential), and improving yield. The latter greatly improves current densities and extends display resolution capabilities in small head-mounted display configurations.

Accomplishments:

- Produced resist patterns as small as 0.15 micron on 0.3-micron centers.
- Demonstrated the exposure and formation of large area dot arrays over pre-existing address line topographies.
- Demonstrated the large area capability of interference lithography by exposing a 20" × 20" plate to create 10^{11} - 10^{12} dots in approximately four minutes.
- Produced functional field emitter arrays with laser interference exposure that operated at 17 volts.
- Produced functional 512 × 512-pixel field emitter display arrays using laser interference exposure that demonstrated both improved uniformity and addressability.

Field Emitter Array Patterning using Laser Interference for Flat Panel Displays

Steven M. Zimmerman, FED Corporation;
Andrew M. Hawryluk, Lawrence Livermore National Laboratory

Objectives

- Develop UV laser interference patterning system.
- Develop higher-resolution lithography using near-4V and high-contrast resists.
- Fabricate and test high-density field emitter arrays with ultra-small (0.1 μm) gate opening and 5V operation.
- Demonstrate 512 × 512 monochrome display arrays using small-grid-opening high-density field emitters.

Approach

- Reconstruct interference exposure system at Lawrence Livermore National Laboratory.
- Develop and characterize high-resolution UV lithographic process using exposure system.
- Use exposure system and optimal lithographic process to fabricate dense field emitter arrays.
- Characterize array structure and performance.
- Demonstrate monochrome display using fabricated arrays.

Status

- All tasks have been completed.
- Key accomplishments:
  - Arrays as small as 0.15 μm dots on 0.3 μm centers made.
  - Patterning over topography demonstrated.
  - Large area exposure demonstrated (20" × 20" plate, 10^{11}-10^{12} dots, ~4 minutes exposure).
  - 17-volt array operation demonstrated.
  - Addressable 512 × 512 display array with improved uniformity demonstrated.

Schedule/Tasks

- Reconstruct interference system—Aug. 94.
- Pre-process test devices—Feb. 95.
- Develop photoprocess—Feb. 95.
- Process test devices—May 95.
- Evaluate test devices—July 95.
- Final report—Aug. 95.

ELECTROLUMINESCENT TECHNOLOGY

ADVANCED DEVELOPMENT OF LARGE AREA, FULL-COLOR ELECTROLUMINESCENT FLAT PANEL DISPLAYS

Project 9322-014

Team:

Planar America, Inc.
Los Alamos National Laboratory
Sandia National Laboratories

Description:

This project focused on the development of blue and white electroluminescent (EL) phosphors, which would allow the transition of EL flat panel technology from multicolor to full-color capability. Metal-organic chemical vapor deposition (MOCVD) and multisource sputtering were investigated to reduce the cost and improve the performance of blue phosphors. Atomic layer epitaxy and multisource sputtering were investigated to develop a broad band "white" EL emission.

Project Impact:

This project will provide the blue phosphor manufacturing technology needed to commercialize a full-color 320 × 256 line EL flat panel display for portable test and measurement, medical monitors, and vehicle displays. High-resolution, full-color 640 × 480 head-mounted displays for both military and commercial applications will be realized as a result of the white phosphor manufacturing development.

Accomplishments:

- Developed a relatively high-luminance crystalline-as-deposited MOCVD process for the thiogallate blue phosphor at temperatures compatible with standard flat panel display glass substrates.
- Scale-up of MOCVD blue phosphor process continued under Technology Reinvestment Program.
- Developed a sputter deposition process with high luminance for $SrS:CeF_3$ blue-green phosphor.
- Atomic layer epitaxy (ALE) reactor fabricated and installed for white phosphor deposition. ALE precursor preparation facility established at Planar.
- ALE white phosphor deposition process with high luminance optimized for deposition on active matrix EL wafers.
- Load-locked multisource sputtering system with H_2S gas capability fabricated and tested for multilayer white phosphor deposition.
- Developed a multisource sputter process for $(ZnS:Mn/SrS:Ce)_n$ multilayer white phosphor using H_2S gas.
- Selected ALE white phosphor process for color active matrix EL manufacturing.

Advanced Development of Large Area, Full-Color Electroluminescent Flat Panel Displays

Richard T. Tuenge, Planar America;
Robert Dye, Los Alamos National Laboratory

Objectives

- Develop a higher brightness, lower-cost blue TFEL phosphor manufacturing process.
- Develop a white phosphor manufacturing process for AMEL head-mounted displays.

Approach

- Metal-organic chemical vapor deposition (MOCVD) process for the thiogallate blue phosphor developed by Los Alamos National Laboratory.
- Multisource sputtering process for blue phosphors developed at Planar.
- Sputtering process for multilayer white phosphor developed by Sandia National Laboratories.
- Atomic layer epitaxy (ALE) process for the white AMEL phosphor developed at Planar.

Status

- An MOCVD process has been developed for crystalline-as-deposited thiogallate blue phosphor at LANL.
- Completed investigation of crystalline-as-deposited blue phosphor films by sputtering.
- An ALE white phosphor process has been established and implemented for AMEL head-mounted displays.
- A sputtered multilayer white phosphor process has been developed and characterized at Sandia.
- Project completed in March 1996.

Schedule/Tasks

- Complete MOCVD blue phosphor process optimization—April 95.
- Establish baseline process for multilayer white phosphor—Sept. 95.
- Deliver blue and white phosphor test samples—Oct. 95.
- Establish ALE white phosphor process for AMEL displays—Dec. 95.
- Deliver white AMEL display—March 96.
- Project completed—March 96.

Novel, Blue Light-Emitting Polymer Diodes for Color Flat Panel Displays

Project 9322-041

Team:

UNIAX Corporation
Los Alamos National Laboratory
Hewlett-Packard Company
Department of Chemistry, University of California Santa Barbara

Description:

This project explored the development of a new blue light source based on electroluminescence from conjugated polymers. It is part of a larger program to develop commercially viable polymer electroluminescent devices for use in a variety of emissive flat panel displays. The multidisciplinary project team combined scientists with expertise in organic synthesis, polymer processing, device physics, semiconductor manufacturing, and device modeling. The principal goal of the DARPA-sponsored research was to produce robust, efficient, blue light-emitting prototype devices suitable for use in low-information-content displays.

Project Impact:

Polymer electroluminescent devices are an emerging technology in a very early stage of development. Because the technical barriers to their commercial exploitation are still being identified, work in this area remains high risk. The prospect of developing an alternative emissive flat panel display technology balances this risk with the promise of a new, low-cost display technology with advantages over the well-known existing display technologies.

Accomplishments:

- Several new electroluminescent polymers were designed, synthesized, and tested.
- Techniques were developed for systematic lowering of operating voltages through the use of "roughened" polyaniline electrode layers.
- Blue polymer light-emitting diodes with external quantum efficiency greater than 2% were demonstrated.

Novel, Blue Light-Emitting Polymer Diodes for Color Flat Panel Displays

Alan Heeger, UNIAX Corporation;
Darryl Smith, Los Alamos National Laboratory;
Ron Moon, Hewlett-Packard Company

Objective

- Develop efficient, blue light sources based on thin polymer electroluminescent layers.

Approach

- Failure analysis of existing device structures.
- Systematic variation and testing of alternative device architectures.
- Variation of active layer characteristics through organic synthesis of alternative conjugated polymers.
- Development of polymer processing techniques to optimize polymer/electrode interfaces.

Status

- Several new electroluminescent polymers have been designed, synthesized, and tested.
- Techniques have been developed for the systematic lowering of operating voltages through the use of "roughened" polyaniline electrode layers.
- Blue polymer LEDs with external quantum efficiency >2% have been demonstrated.
- Preliminary encapsulation techniques have been developed, and examination of degradation during storage has been initiated.

Schedule/Tasks

- Continue program of new macromolecule design and synthesis.
- Further reduce operation voltage of prototype devices to promote longer operating life.
- Develop effective fabrication and encapsulation techniques to enable long-term storage without degradation.
- Perform Hall effect and transport measurements.
- Begin microscopic device modeling under conditions of strong injection.

PLASMA DISPLAY TECHNOLOGY

PRECISION THICK FILM TECHNOLOGY FOR 100% YIELD OF LARGE AREA HIGH-RESOLUTION COLOR AC-PDPS

Project 9322-002

Team:

Photonics Imaging, Inc.
Sandia National Laboratories
Los Alamos National Laboratory

Description:

A key problem in printing large area inorganic glass dielectric film is that there is no noncontact method to measure either the film thickness or uniformity prior to firing the part. Thus, there was no in-process control to dynamically adjust the screen printer for each substrate's characteristics in order to achieve yield. The objective of this project was to develop a low-cost, precision thick film screen printing manufacturing process capable of producing high-resolution, full-color plasma displays with a yield of 100%.

Project Impact:

This project developed new production equipment, novel sensors and innovative software for in-process quality feedback control in the thick film process loop manufacturing cluster.

Accomplishments:

- Developed a measurement machine with electronic feedback to measure the flatness of the glass substrate and the uniformity of the fired dielectric.
- Developed a reproducible technique to measure average thickness of the "green" dielectric.
- Characterized the screen printing process variables and evaluated their effect on dielectric layer uniformity. Fabricated screen printed glass plates and developed specifications for a new generation production screen printer.
- Developed noncontact thickness measurement sensors (optical or X-ray) to measure the thickness uniformity of the "green" dielectric layer.
- Developed integrated FPD manufacturing model software for the thick in-process loop manufacturing cluster.
- Developed a production measuring machine for large panels to make noncontact thickness measurements at several points on the panel, determine thickness variation, and provide rapid feedback to the printing equipment.

Precision Thick Film Technology for 100% Yield of Large Area High-Resolution Color AC-PDPs

Peter S. Friedman, Photonics Imaging, Inc.;
Walter Worobey, Sandia National Laboratories;
Marion Scott, Los Alamos National Laboratories

Objective

- Develop low-cost, precision thick film screen printing manufacturing process capable of producing high-resolution, full-color AC-PDPs with a yield of 100%.

Approach

- Develop noncontact sensors to measure film thickness and uniformity of "green" dielectric.
- Characterize printing process variables and evaluate their effect on uniformity of dielectric layer.
- Develop production machine for noncontact thickness measurement of large area panels.
- Develop FPD manufacturing model software for the thick film process loop manufacturing cluster.
- Integrate thick film feedback loop with screen printing operation.

Status

- Contract signed September 26, 1994.
- Equipment to measure glass flatness and fired dielectric thickness was received and implemented.
- Equipment to measure thickness and uniformity of "green" dielectric was ordered.
- Equipment to integrate thick film feedback loop with screen printing operation was ordered. Software for the feedback loop was developed.

Schedule/Tasks

- Precision screen printed glass plates were fabricated to identify critical parameters and process instructions for optimization of thick film uniformity.
- Noncontact thickness measurement sensors for green dielectric were developed.
- Production measuring machine for noncontact green was designed and ordered.
- Integrated FPD manufacturing model software for thick film manufacturing cluster was delivered.

IMPROVED EMISSIVE COATINGS FOR SUPER-HIGH-EFFICIENCY COLOR AC-PDPS

Project 9322-003

Team:

Photonics Imaging, Inc.
Los Alamos National Laboratory
Sandia National Laboratories

Description:

This project focused on attaining color plasma displays with higher efficiency and longer lifetime. The improved efficiency was to be achieved by one or more methods of increasing the secondary electron production of the top thin film, dielectric, emissive layer used in plasma displays. The methods employed in this investigation were ion-beam deposition processes to alter film microstructure, doping to introduce band-bending effects, surface modification to lower the work function, and replacing or blending MgO with other emissive oxides.

Project Impact:

The potential impact is the development of new emissive thin film dielectric coatings to improve both the efficiency and operational characteristics of color plasma displays. Theory suggests that the secondary electron emissivity can be improved substantially.

Accomplishments:

- Produced MgO-coated test panels via novel deposition techniques.
- Evaluated effectiveness of ion beam sputtered MgO films versus e-beam deposited MgO films in operating plasma panels.
- Evaluated BeO as an overcoat material relative to MgO.

Improved Emissive Coatings for Super-High-Efficiency Color AC-PDPs

James F. Nolan, Photonics Imaging, Inc.;
Marion Scott, Los Alamos National Laboratory;
Walter Worobey, Sandia National Laboratories

Objective

- To increase efficiency and lifetime by improving the material properties of the emissive/protective thin film, top dielectric layer in color AC-PDPs. Additional improvements in VUV transmission and reduced ion-erosion rates (for enhanced lifetime) will be sought for the modified top thin film, emissive, dielectric coating.

Approach

Phase I:

- Calibrate surface structure and emissivity of present MgO coating used in color AC-PDPs.

Phase II:

- Develop improved emissive coating through selective MgO crystal orientation, surface modification, doping and/or blending, and material substitution.

Phase III:

- Design improved production thin film emissive coating deposition chamber.

Status

- Ion beam sputtered MgO evaluated in operating panels.
- BeO films evaluated in panels.
- Effect of substrate temperature on e-beam deposited MgO films evaluated.
- Alkali-doped MgO films in progress.
- Alkali-doped/blended films in progress.
- Effect of oxygen and materials contamination being evaluated.

Schedule/Tasks

- E-beam MgO coating—April 95.
- Ion-sputtered MgO—May 95.
- Ion-beam flow-thru MgO—June 95.
- Ion-assist MgO—July 95.
- BeO coating—July 95.
- Cs surface modification—Feb. 96.
- P-type doping—1Q-2Q 96.
- Project complete—2Q 96.

Low-Cost Electrode Fabrication Process for HDS Color FPDs

Project 9322-009

Team:

Photonics Imaging, Inc.
Los Alamos National Laboratory
Sandia National Laboratories

Description:

This program developed an electrode fabrication process consisting of large area, pattern aqueous plating of a composite metallization system, such as Cu/Ni/Au, with a preliminary thin layer providing a glass bonding conductive "seed" coating from which pattern electroplating can proceed. For example, with copper as the primary conductive layer, the nickel flash coating provides an interdiffusion barrier (between the copper and the gold), and the top gold flash layer provides a corrosion-resistant surface as well as a non-oxidizable surface for electrical bonding (e.g., flip chip on glass).

Project Impact:

The process improvements could lead to electrodes with better uniformity, improved conductivity, reduced undercut, less material usage, and lower cost. The end result will be larger area, lower cost, and higher resolution plasma displays.

Accomplishments:

- Accomplished large area selective plating of metallizations on thin vacuum deposited seed layers.
- Evaluated metallization using high-temperature plasma display processes.
- Investigated substrate electroless seed layer deposition. After evaluation, the vacuum-deposited seed layers process was selected.

Low-Cost Electrode Fabrication Process for HDS Color FPDs

Peter S. Friedman, Photonics Imaging, Inc.;
Walter Worobey, Sandia National Laboratories;
Marion Scott, Los Alamos National Laboratories

Objective

- Develop low-cost, high-resolution electrode fabrication process based on selective electroplating and/or electroless deposition utilizing electroless or vacuum-deposited seed layer. The developed metallization process is to be compatible with chip-on-glass/ flip-chip-on-glass packaging technology.

Approach

Phase I:

- Develop vacuum-deposited and electroless high-resolution seed layers.

Phase II:

- Develop selective electroplating and electroless metallization system, including compatible photoresist and stripping processes.

Phase III:

- Develop selective electroplating metallization system and optimize process parameters for 21-inch-substrates at Photonics Imaging.

Status

- Contract signed September 26, 1994.
- Selective electroplating metallization system/process demonstrated on 5-inch substrates.
- Selective electroplating metallization system with optimized process parameters demonstrated at SNL on 10.4-inch-diagonal substrates.

Schedule/Tasks

- Phase I completed.
- Phase II completed. (Electroless metallization system eliminated from further consideration.)
- Phase III to be completed by 3Q 96.

FPD MANUFACTURING EQUIPMENT DEVELOPMENT

ADVANCED LITHOGRAPHY TOOL FOR LARGE AREA FLAT PANEL DISPLAY MANUFACTURING

Project 9322-052

Team:

Etec Polyscan, Inc.
Sandia National Laboratories

Description:

Polyscan is developing an advanced laser direct write machine for the exposure of large area masks and for maskless imaging of large area flat panels displays. The following key technologies are being developed:

- Higher-resolution, high-throughput scan lenses to resolve features as small as 5 microns over very large fields.
- Multichannel modulators capable of sustained printing rates in the several GHz range.
- Higher performance continuous velocity translation stages.
- Adaptive warping engine to permit real-time, nonlinear scaling of the image database.

Sandia Laboratories and Etec Polyscan, Inc. will conduct a joint development effort. Polyscan will design and build the machine. Sandia Laboratories will investigate photoresist materials most suitable for the laser direct write process for variety of applications.

Project Impact:

The system developed in this program will enable industry to image fine lines over 24" × 24" areas at rates comparable to current large area steppers without the need for photomasks. In addition, adaptive imaging will permit industry to use less expensive substrates, perhaps even plastic substrates, without regard to distortion of prior layers.

Accomplishments:

- Phase 1 design completed and all parts fabricated.
- Phase 1 system integration restarted after delay due to facility flooding.
- Phase 1 to be completed using Etec Polyscan resources by mid-96.

Advanced Lithography Tool for Large Area Flat Panel Display Manufacturing

Shi-kay Yao, Etec Polyscan, Inc.;
John Zich, Sandia National Laboratories

Objectives

- To develop large format multimedia laser imaging system for mask generation and maskless laser direct writing of 24" x 24" flat panel display substrates.
- To prove the lower cost-of-ownership of the laser direct write manufacturing tool for applications ranging from quick-turn prototypes to mass-production volumes.
- To develop and prove a novel method to image onto deformed prior layers (adaptive imaging) to permit the use of low-cost substrates.

Approach

- Upgrade existing PCB laser direct imager from 25-μm features to 10-μm features and eventually 5-μm features.
- Increase printing speed from 80 x 10^6 to 160 x 10^6 to 2.5 x 10^9 pixels per second.
- Develop on-line method to extract prior-layer substrate deformation data in real-time to permit dynamic registration of current layer (adaptive imaging).
- Develop advanced Raster Image Processor to permit real-time generation of warped image grid (adaptive imaging).
- Build the machine in phases so that Phase I will result in a useful Laser Mask Generator, while Phase II will result in a high-resolution, high-speed Laser Direct Write Tool, culminating in Phase III with the ultimate Adaptive Laser Imaging Tool.

Status

- Program started in July 94.
- Phase I design completed.
- All parts fabricated.
- Phase I Laser Mask Generator System Integration in process, delayed by natural disaster.
- Program restarted in new facility in January 96 and will be completed using company resources by July 96.

Schedule/Tasks

- Program started in July 94.
- Phase I design completed in Dec. 94.
- Phase I Laser Mask Generator complete by July 96.
- Phase II 5-μm Laser Direct Imaging Tool complete by June 97.
- Phase II Machine Installed at SNL—to be determined.
- Phase III Adaptive Imaging Module retrofitted onto Phase II machine—to be determined.

GLASS PANEL ALIGNMENT AND SEALING FOR FLAT PANEL DISPLAYS

Project 9322-135

Team:

FED Corporation
Coloray Display Corporation
Plasmaco, Incorporated
SI Diamond Technology, Incorporated
Sandia National Laboratories

Description:

The goal of this project was to develop a new alignment and sealing system that greatly improves sealing characteristics, design flexibility, cost, and yield in the manufacture of reduced pressure flat panel displays. The project was a joint effort between Sandia National Laboratories and a consortium of display companies headed by FED Corporation and including Coloray Display Corporation, Plasmaco Incorporated, and SI Diamond Technology Incorporated.

The project consisted of the following three activities, which concurrently and interactively shared results: Sandia investigated both thermal and laser sealing of several materials of interest to the commercial companies in the consortium including soda lime and Corning 7059. Several different types of laser-heated seals including frit, fiber, and direct plate melting, were attempted. Finite-element analysis was used to evaluate seal designs and minimize stress.

Sandia designed and fabricated an integrated alignment and sealing system. The specifications for the system were jointly developed by both Sandia and the consortia. This system provided thermal-panel sealing as well as vacuum-thermal-panel cleaning and outgassing.

The consortium members, in addition to advising Sandia and reviewing results, each fabricated prototype display sealing test vehicles. Near the end of the project, Sandia will work with each of the consortium members, using the new alignment and sealing system with the best known processing conditions to seal their prototypes. Each consortium member will evaluate their sealed prototypes and share the results with the group.

Project Impact:

Flat panel displays are both a strategic military component and a critical new domestic business opportunity. Reduced-pressure flat panel technologies promise many of the simplest implementations and the best ultimate performance for these displays. Improved alignment and sealing methods will be required for high-resolution display manufacture across the entire spectrum of display sizes and will represent an important competitive advantage.

Accomplishments:

- The thermal-sealing prototype tool with automatic alignment is complete.
- Thermal seals using the prototype tool with full dynamic alignment during sealing were made with both frit rods, screened frit, and glass rods.
- A unique coupling of thermal and stress modeling was achieved for the first time and was used to evaluate sealing structures.
- Experimental seals requiring no vertical movement between the plates were demonstrated using both thermal and laser heating.
- Through panel ND:YAG laser seal heating was experimentally demonstrated.
- CO_2-laser panel melting and between-panel seal heating was experimentally demonstrated.

Glass Panel Alignment and Sealing for Flat Panel Displays

Steven M. Zimmerman, FED Corporation;
Larry Kovacic, Sandia National Laboratories

Objectives

- Experimentally evaluate the use of laser heating at elevated bias temperatures, for frit sealing, fiber sealing, and direct plate-melt sealing.
- Develop a prototype flat panel tool that integrates both the panel-to-panel alignment and sealing operations and includes a laser for laser-sealing experiments.
- Demonstrate conventional thermal sealing with alignment and laser sealing to the extent available.
- Evaluate the sealing tool by consortium members using their own prototype displays.

Approach

Sandia:

- Use existing laser facilities to evaluate laser sealing with soda lime and Corning 7059 glasses.
- Design and fabricate an alignment and sealing system with both thermal and thermally biased laser sealing capabilities.
- Use finite-element analysis to model seal stress.

Consortium members:

- Jointly advise on design and review experimental work.
- Fabricate material and prototype display samples.
- Test seal samples with Sandia and evaluate results.

Status

Program effective date: 1/12/94.

- Consortium agreement and contracts (Members: FED, Coloray, Plasmaco, SI Diamond). Complete.
- System specifications. Complete.
- System design. Complete.
- System construction:
  - Phase I—Complete.
  - Phase II—Canceled.
- Thermal- and laser-sealing experiments—in progress.
- Materials and prototype fabrication—in progress.
- Thermal and stress analysis—complete.

Schedule/Tasks

- Schedule specifications—April 94.
- System design and construction—March 95.
  - Phase I (alignment and thermal sealing)—Nov. 95.
  - Phase II (vacuum chamber)—Canceled.
- Process definitions (extended)—March 95.
- System laser capability—June 95.
- Material and prototype fabrication—Aug. 95.
- Laser-sealing experiments (extended)—Sept. 95.
- FEA analysis (extended)—Sept. 95.
- Prototype sealing and evaluation—Dec. 95.
- Final report—May 96.

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Advanced Lithography

AUTOMATED SYSTEM IDENTIFICATION

Phase I Project

Team: **Sandia National Laboratories**
Los Alamos National Laboratory

Description:

The goal of this project was to develop the capability to perform automated identification of structural dynamic models of lithography machines and subsystems. Automated model evaluation is a key element required in implementing precision control of fine motion machinery. Existing control design approaches were reviewed to determine the requirements they place on system identification algorithms. The inputs to the control design process are both a nominally accurate structural dynamic model and an estimate of the accuracy of the math model or a model of the system noise. This project proposed to develop the capability to assess system models and uncertainties using artificially generated excitation and system-identification technology. The automated identification approaches were to be validated using both numerical and experimental test beds of varying complexity.

The project team successfully applied the Canonical Variate Analysis (CVA) algorithm to the simulated lithography stage dataset. The algorithm was initially available in Matrix X and later in MATLAB. Working with Wallace Larimore, Adaptx, Inc., the team helped debug the MATLAB version and learned how to use the algorithm with noisy data. The team demonstrated that CVA gives very accurate answers with minimal data and is generally considerably more efficient than the Eigensystem Realization Algorithm (ERA) for the datasets tested. CVA has definite potential as an algorithm for extracting modal parameters, in addition to its application in the system identification task in this project. The downside of CVA is its availability only as a commercial compiled code, although the user can readily call most portions of the code as MATLAB subroutines.

Project Impact:

The project culminated with selected aspects of the technology being implemented in the vibration control of an operational lithography machine under the NCAICM Phase II lithography project, Active Vibration and Motion Control for Lithography, Project 9322-088.

Accomplishments:

- A wide variety of algorithms were reviewed for their application to automated system identification. The ERA and CVA algorithms were selected.
- Coding and documentation of ERA code and accuracy indicators were completed.
- The initial coding of the CVA algorithm was completed.
- A simulation model of a magnetically levitated lithography stage was constructed to test the identification algorithms. The model was incorporated into a SIMULINK environment.
- A test matrix was defined to compare the performance of the ERA and CVA algorithms. The results of the comparison were formally documented.

AUTOMATED SYSTEM IDENTIFICATION

Stew Kohler, Pat Barney, Jeff Dohner, Robert Kipp, Jim Lauffer, Gordon Parker, Ron Rodeman, Sandia National Laboratories; Norm Hunter, Los Alamos National Laboratory

Objectives

- Develop technology to perform automated identification of structural dynamic models of precision machines and subsystems.
- Apply this technology to microchip lithography machines, where these identified models will be used by controllers to re-position workpieces rapidly while minimizing settling time, thus maximizing throughput rates.

Approach

- Survey control design approaches, determine requirements.
- Identify possible automated system ID algorithm techniques, evaluate for this and similar applications.
- Develop, code, and debug algorithms of the types selected for their appropriateness.
- Develop numerical simulator and hardware test bed to evaluate algorithm performance.
- Perform code development and numerical testing in a computing environment that is compatible with the environment being used by the Phase II participants to facilitate integration into the Phase II lithography control system.

Status

- Two algorithm approaches, Eigensystem Realization Algorithm and Canonical Variate Analysis, were identified, developed, and coded.
- Initial code versions were delivered to the Phase II participants.
- Numerical simulation environment was developed.
- Detailed numerical test plan was developed.

Schedule/Tasks

- Initial coding of two algorithms complete—Sept. 94.
- Numerical simulation environment development complete—Aug. 94.
- Numerical test plan developed and approved—Nov. 94.
- Numerical evaluation complete—March 95.
- Hardware test bed developed—May 95.
- Auto system ID demonstrated on hardware—Sept. 95.

Control Designer's Workbench for Active Structural Control

Project 9322-026

Team:

Metron, Inc.
Los Alamos National Laboratory
Naval Research Laboratory

Description:

The project goal was the construction of a Control Designer's Workbench for structural modeling, analysis, and design of active vibration control systems. The effort provided the following seamlessly integrated capabilities to enable the successful design of commercially feasible active vibration control systems:

- State-of-the-art finite-element analysis techniques for structural modeling of existing and next-generation information component manufacturing machines.
- Dynamics analysis and visualization capabilities enabling the identification of the contributing factors to unwanted disturbances in flat panel and integrated circuit (IC) component manufacturing processes and determining means for controlling them.
- Analysis and simulation capabilities to be used in designing active vibration control systems for flat panel and IC component manufacturing processes.
- Design, analysis, and simulation capabilities for performing on-line system identification for the above active vibration control systems.

Key capabilities include software modules allowing:

- Identification of physical nature of unwanted disturbance.
- Identification of optimal location of actuators to control unwanted disturbance.
- Identification of optimal location of sensors to detect desired actuator/disturbance interaction.
- Insight into attainable levels of control system performance.

Project Impact:

Dramatic reduction in the time and effort required to design and build active (or passive) vibration reduction systems for use in high-precision manufacturing environments.

Accomplishments:

- Finite-element modeling, active structure control, input/output data, systems identification, controller, simulation, visualization, and remote computing toolboxes completed and integrated into Khoros backplane.
- Modeling and controls analysis completed for two-piece platen-mirror and monolithic platen-mirror maglev fine-stage and XLS Corporation stepper base/bridge assemblies and reticle components.
- Documentor and on-line Help file structure infrastructure completed.
- Active control software released for use.

CONTROL DESIGNER'S WORKBENCH FOR ACTIVE STRUCTURAL CONTROL

Albert Jenab, Metron, Inc.;
Janine Fales, Los Alamos National Laboratory;
David Armoza, Naval Research Laboratory

Objectives

- Construction of a Control Designer's Workbench for structural modeling, analysis, and design of active-vibration-control systems. The proposed effort will provide the following seamlessly integrated capabilities to enable the successful design of commercially feasible active-vibration-control systems:
  - State-of-the-art finite-element analysis techniques for structural modeling of existing and next-generation information component manufacturing machines.
  - Dynamics analysis and visualization capabilities enabling the identification of the contributing factors to unwanted disturbances in flat panel and IC component manufacturing processes and determining means for controlling them.
  - Analysis and simulation capabilities to be used in designing active-vibration-control systems for flat panel and IC component manufacturing processes.
  - Design, analysis, and simulation capabilities for performing on-line system identification for the above active-vibration-control systems.

Approach

- Leverage from existing capabilities of DARPA-sponsored Stealth Designer's Workbench.
- Survey available FEM, CAD/CAM, controls analysis, and visualization software tools.
- Select core set of software/hardware tools spanning desired capabilities.
- Construct prototype FEM, Active Structural Control, Visualization, and Remote Computing Toolboxes and supporting analysis routines.
- Integrate prototype Toolboxes into Khoros-based workbench environment.
- Utilize prototype Toolboxes to provide modeling and analysis support to ongoing Phase I and II NCAICM active-control projects.
- Incorporate photolithography machine component models and related analysis into tutorials and educational materials.
- Distribute beta-version software to NCAICM Phase I and II active-control projects. Revise and upgrade capabilities as appropriate.
- Release Version 1.0 to interested parties.

Status

- FEM, Active Structure Control, I/O Data, Systems Identification, Controller, Simulation, Visualization, and Remote Computing Toolboxes completed and integrated into Khoros backplane.
- Modeling and controls analysis completed for two-piece platen-mirror and monolithic platen-mirror maglev fine-stage and XLS base/bridge assemblies and reticle components.
- Documentor and on-line Help file structure infrastructure completed.
- Release 1 of Phase I and II NCAICM active-control software in March 1996.

Schedule/Tasks

- Release I with documentation completed March 1996.

ACTIVE VIBRATION AND MOTION CONTROL FOR LITHOGRAPHY

Project 9322-088

Team:

Lucent Technologies, Advanced Technology Systems
Sandia National Laboratories

Description:

This project applied active vibration and motion control to advanced lithography. The project was divided into two main parts:

Real Time Through-the-Lens Alignment - Lucent Technologies developed a prototype system to actively control reticle position and motion during the lithographic exposure based on through-the-lens alignment signals. The alignment system uses the stepper exposure (actinic) wavelength to detect the position of the reticle (mask) relative to the position of the wafer (target). Advanced optical and digital signal processing are used to extract the low-level alignment signal from the noise. Active control processing is used to drive an actuated reticle stage to track the motions of the wafer stage as it settles following a step.

Magnetically Levitated Stage - Sandia Labs developed an improved version of their maglev stage, which incorporates structural control and improved hardware and software. The improved stage system incorporates auxiliary piezoelectric (PZT) actuators and sensors embedded in the platen and adds the processing to permit active structural control of the platen. This structural control reduces modal vibrations in the platen and permit extremely rapid (high bandwidth) motion control of the stage to improve alignment and wafer throughput.

Project Impact:

Improve stepper overlay performance by eliminating errors associated with current off-axis alignment systems. Improve stepper throughput by increasing wafer step speed and allowing a "shoot-while-settle" operation. These improvements will provide substantial cost benefits to semiconductor manufacturers by increasing both chip yield per wafer and wafer throughput.

Accomplishments:

Alignment System - Bench-top testing of the optical-detection scheme showed robust and well-behaved alignment signals under several process coatings (resists). System testing on an XLS stepper showed good alignment performance (< 8 nanometers (nm)) and fast settling time (<20 milliseconds (msec)) under ideal conditions using internal metrics.

Stage System - This project produced several improvements in the maglev wafer positioning stage system. By use of assembly code, built-in digital signal processor (DSP) digital filters, and input/output boards with their own DSPs, the sample rate was increased from 2500 Hz — the sample rate at project start — to 8000 Hz and the controller bandwidth from 30 Hz to 90 Hz. This represents a 67% reduction in the step-and-settle time. The high-frequency position noise for the 90-Hz controller is 5 nm peak-to-peak. Further increase in bandwidth to 150 Hz (6 msec settling time) resulted in excitation of platen resonances. Positioning noise was 250 nm, about 20 times greater than acceptable. With active structural control, the maglev controller bandwidth was increased to 150 Hz with the high-frequency position noise at 5 nm peak-to-peak. The step and settle time was reduced by 40% below that of the 90-Hz controller. The software and hardware improvements to the maglev system are being transferred to Integrated Solutions, Inc.

Active Vibration and Motion Control for Lithography

Nick Matich, Lucent Technologies;
Doug Jordan, Sandia National Laboratories

Objectives

- Maximize wafer throughput in a production lithography stepper.
- Reduce alignment and overlay errors to permit 0.1 μm critical dimension.

Approach

- Design a real-time, through-the-lens alignment system using the exposure wavelength for alignment.
- Dynamically control reticle with respect to wafer during exposure.
- Incorporate structural sensor and actuators into existing maglev stage to control modal vibrations and permit increased positioning bandwidth (speed). Also, improve system hardware and software.

Status

- Installed alignment system on XLS stepper.
- Initial testing shows good results (<8 nm) based on internal metrics.
- Exposure and actual overlay testing pending.
- Maglev fine stage step-and-settle for a 1-μm step decreased from 30 msec to 10 msec without active structural control (ASC) and to 6 msec with ASC.
- Positioning noise of 150-Hz controller decreased from 250 nm p-p to 5 nm p-p with ASC.

Schedule/Tasks

- Initial alignment testing completed—Dec. 95.
- Improve maglev system performance via use of ASC actuators in a self-sensing mode—March 96.
- Transfer maglev system software improvements to Integrated Solutions, Inc.—Ongoing.

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Microelectronics

CONTAMINATION-FREE MANUFACTURING

SENSORS AND METROLOGY

Phase I Project

Team:

Sandia National Laboratories
University of New Mexico
University of Arizona

Description:

Advanced metrology and the development of high-sensitivity, *in-situ*, real-time, process sensors is implemented through three primary objectives: (1) to improve state-of-the-art of gas phase metrology by developing precise calibration equipment and techniques for parts-per-billion (ppb) and parts-per-trillion (ppt) gas sensors, (2) develop real-time, in-situ sensors for contamination, process, and process endpoint control for advanced microelectronics fabrication, and (3) provide the microelectronics industry with a world-class user metrology laboratory for unparalleled surface and gas analysis capabilities while establishing a test and analysis platform for new sensor development. Advanced baseline metrology, calibration, and state-of-the-art analytical capabilities were developed along with ultra-sensitive, *in-situ*, *real-time* gas and surface sensors. High-resolution scatterometry equipment was designed and developed as a process endpoint tool for photolithography and etch processes. Volatile organic compounds (VOC) and catalytic gate sensors with sensitivities from ppb to ppt were developed for determining the purity of process gases at the inlet, in the process chamber, and at the exhaust of gas process tools. The state-of-the-art of gas phase metrology was enhanced by developing novel instrument calibration for ppb down to ppt impurity concentrations, and by creating computer models for simulating gas impurity and particle transport in gas handling equipment and tools.

Project Impact:

Semiconductor and flat panel display manufacturing will benefit from improved baseline metrology, novel high-sensitivity *in-situ*, real-time sensors and process control monitors, and access to advanced state-of-the-art analytical capabilities.

Accomplishments:

- A state-of-the-art surface metrology User Facility was established. A field emission scanning electron microscope in tandem with an optical wafer scanner is capable of measuring defects on bare or patterned substrates. Determination of defect type and chemical composition is possible.
- Scatterometery has demonstrated the required exposure and focus sensitivity to be viable as a process control and endpoint monitor for photolithographic processes for photomasks, wafers, and field emission arrays.
- A unique calibration system, accurate and precise down to 0.5 ppb was designed, fabricated, and tested. A second-generation system providing precise mixtures in the low ppt range is currently under development.
- Designed, built, and tested a vertical furnace system equipped with on-line, *in-situ* probes for studying impurity transport in a process tool.
- Delivered two different Surface Acoustic Wave-based (SAW) technologies for monitoring nonvolatile materials found in advanced manufacturing environments. Example: Sensor developed for 1-Methyl-2-pyrrolidinone (NMP), a primary constituent of widely used photoresist strippers, along with several novel films for NMP detection (Initial sensitivity $\approx$ 300 ppb).
- Demonstrated SAW-based sensor technology in a semiconductor fabrication environment (Sandia Microelectronics Development Laboratory).

SENSORS AND METROLOGY

Bob Blewer, Bob Donovan, Sandia National Laboratories;
Bob McNeil, University of New Mexico;
Farhang Shadman, University of Arizona

Objectives

- Advance the state-of-the-art of gas phase metrology by developing precise calibration equipment and methodologies for ppb and ppt calibration.
- Provide the ability to map contaminant transport and impurity profiles in a process tool.
- Develop real-time, in-situ sensors for contamination, process, and process endpoint control with the sensitivities required for advanced microelectronics fabrication.
- Provide the microelectronics industry with a world-class user metrology laboratory for state-of-the-art surface and gas analyses, and to serve as a test and analysis platform for new sensor development.

Approach

- Develop a precision mixing system for preparing calibration gases with ppt resolution using advanced analytical equipment (e.g., Atmospheric Pressure Ionization Mass Spectrometer, APIMS).
- Select a standard process tool and equip it with in-situ sensors. Sampling the impurity concentration at specific points, develop a model to predict the concentration throughout the tool.
- Develop surface acoustic wave (SAW) sensors for microelectronic manufacturing.
- Enhance the present metrology capabilities at SNL by acquiring a field emission scanning electron microscope (FESEM) computer coupled to an optical wafer scanner for patterned substrates.

Status

- Preliminary measurements of NMP vapors using polyvinylacetate-coated SAW sensors completed. Initial response of the sensor to transient NMP pulses in a flow of nitrogen is rapid (≈2 min) with a sensitivity of approximately 100 Hz/ppm of NMP (≈300 ppb).
- At the University of Arizona, the new in-situ probe installed in the vertical furnace was tested, and transport model development was more than 50% complete. The preliminary mixing and calibration system was completed and tested. Results show a linear calibration response of APIMS, thereby confirming consistent gas mixing.
- The University of New Mexico demonstrated the viability of scatterometry as an endpoint detection tool for photolithography, and is continuing to develop the technique.

Schedule/Tasks

- Catalytic-gate hydrogen sensor fabricated and tested—Jan. 94.
- Preliminary (ppb) gas mixing system completed—July 94.
- Trace analysis system completed—Aug. 94.
- Scatterometry viability study completed—Aug. 94.
- Contaminant transport model testing and enhancement—Sept. 94.
- NMP sensor developed and installed in the MDL—Nov. 94.
- FESEM and wafer scanner delivered and installation begun—Nov. 94.
- Advanced (ppt) gas mixing system — Jan. 95.
- Deliverables—Oct. 96.
  1. Comprehensive gas metrology package including ppt calibration methodologies, contaminant transport models, and contaminant profile monitoring system.
  2. SAW sensors for microelectronic manufacturing environment.
  3. Scatterometry technology for control of photolithography and etch processes.
  4. Advanced state-of-the-art User Metrology Laboratory.

CHEMICAL VAPOR CLEANING FOR ADVANCED CONTAMINATION-FREE MANUFACTURING

Project 9322-001

Team:

Air Products and Chemicals, Inc.
Schumacher Company (a unit of Air Products)
Lehigh University
Sandia National Laboratories

Description:

Chemical Vapor Cleaning (CVC) is a cutting-edge program designed to fully explore the issues of gas phase processes for surface metal contaminant removal utilizing nonstandard methods.

Chemical Vapor Cleaning uses gas phase ligand processing to remove metal contamination by basically reversing the CVD deposition process. Carefully selected ligand systems have been shown to bind with surface metal forming a metal complex, which is subsequently desorbed and removed as a volatile species. No etching of, or damage to, the substrate is expected or observed. The CVC process tends to use low to moderate temperatures (≤300°C).

Project Impact:

The results generated from this program will directly support the realization of commercial low-temperature gas-phase cleaning technologies. The information on reaction conditions and removal rates will provide a useful starting point for a commercial equipment or semiconductor manufacturer. The handling and mass-flow delivery methods and materials compatibility data required to achieve effective cleaning will also be of direct benefit to commercial tool developers.

Accomplishments:

- Determined full mechanisms for copper and iron removal from oxide by CVC process. High purity sources of CVC reagents have been generated. Completed purification efforts for Hhfac at Schumacher.
- Completed round-robin comparison of TXRF analytical services versus SIMS, TOF-SIMS, and HIBS. All methods correlate well.
- From 3×10^{15} atoms/cm^2 initial contamination, have reduced iron and copper to 2×10^{11} cm^2 and 1.6×10^{10} cm^2, respectively (by TXRF and SIMS).
- Copper reduction by five orders of magnitude in ≤5 minute processing time. Iron reduction by four orders of magnitude, although at longer times.
- First silicon has been processed at Lehigh University.
- Sodium reduction has been shown by Hhfac CVC from ≈ 2 atomic % to ≤ 0.01 atomic % on SiO_2 surfaces (by XPS).
- Determined viscosity and vapor pressure of Hhfac.

CHEMICAL VAPOR CLEANING FOR ADVANCED CONTAMINATION-FREE MANUFACTURING

David Bohling, Scott Beck, Mark George, Kristine Young, Alfred Badowski, and Daniel Moniot – Air Products; David Roberts, Ray Vrtis, George Voloshin – Schumacher; Dennis Hess and Satish Bedge – Lehigh University; Bob Blewer, Bob Donovan – Sandia National Laboratories

Objectives

- Develop Chemical Vapor Cleaning (CVC) for the removal of trace metal contamination from silicon wafer surfaces.
- Determine the limitation of CVC for Fe, Cu, Na, and post-RIE Al residue to $\leq 10^{10}$ cm^{-2}.
- Determine physical parameters of CVC cleans: activation energies, kinetics, mechanisms.
- Develop best CVC process methodologies for the removal of Fe, Cu, Na, and Al.
- Explore and define alternative CVC reagents beyond those currently used.
- Develop purification methods for CVC reagents to levels appropriate for cleaning.

Approach

- Perform CVC experiments under controlled conditions and with well-characterized surfaces.
- Determine and use controlled contamination methods.
- Define the best analytical methods for characterizing large numbers of samples.
- Fabricate electrical test structures to ascertain the effects of contamination and cleaning efficiency. Correlate with cleaning limits.
- Clean post-RIE etch residues using featureless surfaces, serpentine structures, and examine hardened resist degradation/removal.
- Use XPS and trapping to determine the mechanisms for Na cleaning using NH_3/HMDS process.

Status

- Completed round-robin test on various TXRF vendors, comparing to SIMS and HIBS. All methods correlated well.
- Have fully defined mechanisms for Cu and Fe removal from oxide. Have begun mechanistic evaluation of Na cleans.
- Current cleaning results have reached 1.6×10^{10} atoms/cm^2 for Cu and 2×10^{11} atoms/cm^2 for Fe.
- Three orders of magnitude metal removal have been accomplished in ≤5-minute process at 300°C, 10 torr.
- Purification methods for Hhfac have been developed.

Schedule/Tasks

- Initiate Na cleans in commercial scale tool—Apr. 96.
- Show ≤1E10 feasibility for Fe and Cu—March 96.
- Show ≤1E10 feasibility for Na—June 96.
- First silicon test structures from Lehigh—Jan. 96.
- Determine Na removal mechanisms—March 96.
- Post-RIE residue cleans initiated—March 96.
- First silicon device structure from Sandia—March 96.
- Compare dry clean in parallel with best effort wet cleans in split lot type experiments—Sept. 96.
- Demonstrate compatibility with line process—Sept. 96.

In-Situ Particle Monitoring in Microelectronic Manufacturing Processes

Project 9322-027

Team:

Insitec Measurement Systems
Sandia National Laboratories

Description:

The objective of the project was to improve particle detection and measurement capabilities during wafer fabrication directly in the plasma tool. The initial work focused on application of an Insitec PCSV (Particle Counter, Sizer, Velocimeter) laser-based instrument to an operating plasma chamber. These studies provided preliminary estimates of the spatial distribution of particulate in the plasma tool as a function of both particle size, velocity, and number density.

Following the effort, a prototype High-Volume (HiVol) single-particle counter was reconfigured to interface to the plasma tool. This instrument, originally developed under a Phase I/II grant from DARPA, has the potential to measure particle flux rates to the wafer surface directly, in real-time. This effort represents the first evaluation of the HiVol prototype in an operating plasma. Particle sensing capability as a function of test conditions was investigated. Chamber test conditions include particles formed by nucleation, particles introduced through seeding, and various plasmas chemistries to assess possible interference from the plasma on the light scattering measurement.

Project Impact:

On-line, in situ sensors of particle size and concentration have the potential to enhance yields through improved local process control at the site of particle contamination. The only currently available particle detection technology for use in microelectronic manufacturing processes is installed in the plasma reactor pump lines. These sensors, while providing useful information describing particle fluxes in the gas flow, do not necessarily correlate with particle deposition at or on the wafer surface. Thus, an instrument is required having the capability to measured the particle concentration directly at the wafer surface.

Accomplishments:

- Initial PCSV measurements were made and particle velocity and size data were collected.
- An appropriate optical interface for HiVol was defined and a new HiVol instrument was fabricated. The new system is fiber coupled to an 70 mW, air cooled Argon-Ion laser system. The instrument incorporates an extensive light-blocking and filtering system to improve the signal-to-noise ratio to light rejection ratios of 10^6 to 1. The capability to locate the detector at multiple-angle back-scatter and side scatter locations was also incorporated into the new design.
- A new electronics system was also designed, fabricated, and tested. The new electronics replace a multiboard signal processor with a compact, single-board design suitable for multipoint installation in a manufacturing environment.
- We determined that the plasma does not significantly impact the light-scattering measurement.
- HiVol particle-detection capability was documented, in plasma, in an operational research reactor, to 0.4-micron particle diameter. Modifications to the signal-detection and processing scheme are currently underway to augment detection capability to 0.2 microns.
- We determined that scattering signature can be used to measure particle speed.

In-Situ Particle Monitoring in Microelectronic Manufacturing Processes

Michel Bonin, Donald Holve, Insitec Measurement Systems;
Daniel Rader, Sandia National Laboratories

Objectives

- Measure particle velocity, size, and number density of particles in a research plasma reactor using commercially available (Insitec PCSV), optically based single-particle-counting technology.
- Evaluate the performance of an in-chamber, High Volume (HiVol), optically based, single-particle counter to determine particle flux to the wafer surface. The new diagnostic will provide:
  - measurements immediately above wafer surface.
  - real-time, temporally resolved particle flux data.
  - new information characterizing particle deposition on wafers.
  - capability for measurements in other locations such as load-locks.

Approach

Task 1:

- Modify research plasma chamber for PCSV access.
- Incorporate a particle generation to the research plasma chamber.
- Assess impact of plasma (if any) on the light scattering measurement.
- Implement experimental test matrix to investigate particle response to plasma and gas flows under various test conditions for both nucleated and seeded particle distributions.

Task 2:

- Design an appropriate optical interface between the plasma chamber and the HiVol instrument.
- Using the DARPA SBIR Phase I/II HiVol as a base instrument, design and build a HiVol system appropriate for the research plasma chamber.
- Investigate the effect of plasma radiation on the HiVol measurement.
- Complete an experimental test matrix similar to Task 1 to evaluate HiVol performance and document minimum particle size detectability.

Status

Task 1:

- Initial PCSV measurements have been made. Preliminary particle velocity and size data have been collected.
- Have found that plasma does not impact the light-scattering measurement.
- Challenges associated with particle seeding identified. Solutions currently being implemented.

Task 2:

- Optical interface between HiVol and Sandia's research reactor has been identified.
- The new HiVol design is complete and has been fabricated.
- The new signal processor is complete.
- The new design has been evaluated in-plasma in a Sandia research reactor. Current size sensitivity is 0.4 micrometers. Anticipate 0.2 micrometers with improved signal processing.
- Have also demonstrated capability to determine particle speed from scattered signature.

Schedule/Tasks

- Project inception—May 94.
- First PCSV measurements—July 94.
- HiVol interface defined—July 94.
- Prototype design complete—June 95.
- HiVol prototype first tests—Oct. 95.
- First in-plasma particle detection—Dec. 95.
- Evaluation and completion of test matrix—March-April 95.
- Project complete, final report submitted—April 95.

FERROELECTRIC DEVELOPMENT

DEVELOPMENT OF HIGH-DENSITY FERROELECTRIC MEMORY

Project 9322-022

Team:

Micron Semiconductor, Inc.
Sandia National Laboratories
Symetrix Corporation

Description:

The purpose of this project was to develop a ferroelectric nonvolatile memory and manufacturing process with the potential to produce a commercially viable, high-density (1mB and above) ferroelectric integrated circuit.

Project Impact:

Provide a robust ferroelectric memory cell that is scaleable to higher densities than is currently possible by placing the bottom capacitor electrode directly above and in contact with the transistor drain.

Accomplishments:

- Ferroelectric memory chip was designed and processed, and proper operation of CMOS periphery circuitry was verified.
- An improved method to synthesize the MOD spin-on solution for ferroelectric deposition was developed.
- An accurate, gravimetric analytical technique was developed to determine the composition of MOD solution precursors and final crystalline films.
- A precise, rapid analytical technique was developed and is used routinely to monitor final ferroelectric film composition.
- Acceptable processes were developed for etching platinum electrodes and ferroelectric films. Reproducible ferroelectric properties were achieved on $2 \times 2\ \mu m^2$ capacitors.
- The effect of chemical composition on film microstructure, and consequent ferroelectric properties, was determined. X-ray diffraction revealed details of the solid state transformations into the desired ferroelectric phase and undesirable other phases.
- Processes were developed for planarization of the ferroelectric capacitor structure.
- A number of ILD (Inter-Level Dielectric) and passivation films were investigated, and an acceptable ILD process was implemented.
- Several different barrier metal schemes were investigated.

Development of High-Density Ferroelectric Memory

Wayne Kinney, Micron Semiconductor, Inc.,
Gordon Pike, Sandia National Laboratories

Objectives

Develop a ferroelectric-based high-density nonvolatile memory technology.

Approach

- Develop ferroelectric capacitor process.
- Full process integration using high-density memory.

Status

- MOD spin-on process optimized and reproducible.
- Good ferroelectric performance on 2 x 2-μm capacitors.
- Etches developed for electrodes and ferroelectric.
- High-density nonvolatile memory designed.
- First high-density devices produced.
- Inadequate barrier metal prevents full device operation.
- Peripheral logic circuitry operates correctly on wafers with ferroelectric capacitors.
- Post-capacitor processing degrades ferroelectric.

Schedule/Tasks

- Y1 process transfer complete—Feb. 94.
- Barrier and interlevel dielectric process development.
- Full process integration.
- First silicon on memory device—Sept. 95.

MANUFACTURING TECHNOLOGY FOR A ONE-MEGABIT FERROELECTRIC PZT NONVOLATILE MEMORY

Project 9322-080

Team:

Radiant Technologies. Inc.
Sandia National Laboratories
Virginia Polytechnic Institute
Bellcore
Raytheon Company
High Density Circuits, Inc.

Description:

The project objective was to develop crucial technical process and design elements necessary for the future manufacture of reliable 1-Mbit ferroelectric nonvolatile memories. A top-down product development approach was used to force realistic product requirements and specifications. The design of a 1-Mbit memory data path, up to but not including full layout, was completed to identify the necessary design rules required for the process and electrical parameters in production.

Project Impact:

Develop U.S. ability to fabricate ferroelectric based nonvolatile memory; for high-density memory and specialty low-density products.

Accomplishments:

- The cause of two reliability-limiting mechanisms in ferroelectric memories, fatigue and imprint, were identified. A solution to this problem was found.
- Fully integrated discrete capacitors were built that demonstrate desired fatigue and imprint properties.
- An interlayer dielectric process that preserves capacitor properties was demonstrated.

Manufacturing Technology for a One-Megabit Ferroelectric PZT Non-Volatile Memory

Joe Evans, Radiant Technologies, Inc.;
Gordon Pike, Sandia National Laboratories

Objective

- Develop the crucial technical process and design elements necessary for the manufacture of reliable 1-Mbit ferroelectric memories.

Approach

- Design and simulate the data path for a 1-Mbit DRO ferroelectric memory.
- Develop and test CVD, dry etch, and ILD process steps.
- Build and test 256-bit DRO IC memories to unify process with design.

Status

- Fabricating 256-bit memory.
- Demonstrated excellent capacitor properties.
- PZT CVD and PZT dry etch in development.

Schedule/Tasks

- Contract start—March 94.
- Design review—Feb. 94.
- Initial process development—Aug. 94.
- Design review—Dec. 94.
- Initial IC fab and test—June 95.
- Design review—July 95.
- Final IC fab and test—Oct. 95.
- Final design review—Nov. 95.
- Final report—Jan. 96.

MICROELECTRONIC EQUIPMENT DEVELOPMENT

ADVANCED SINGLE-WAFER METALLIZATION CLUSTER TOOL

Project 9322-044

Team:

CVC Products, Inc.
MIT Lincoln Laboratories

Description:

This project involves the development of advanced metallization/silicidation processes and equipment for 0.25-micron and 0.18-micron technology nodes. The project addresses contact silicide, interconnect, and self-aligned silicide requirements. These processes are developed using a Modular Equipment Standards Committee (MESC) compatible cluster tool consisting of four advanced single-wafer process modules:

1. Cleaning module: uses inductively coupled plasma source (ICP) to clean contact and via holes.
2. Collimated plasma vapor deposition (PVD) module: deposits collimated refractory metals.
3. Metal-organic chemical vapor deposition (MOCVD) module: deposits copper and titanium nitride.
4. Rapid thermal process (RTP) module: used for all thermal processing applications.

A cobalt silicide cluster tool with an integrated ICP/PVD module and an RTP module will be delivered to MIT Lincoln Laboratories.

Project Impact:

Provide process solutions for contact and interconnect metallization requirements for 0.25-micron and 0.18-micron technologies using single-wafer MESC cluster tool technology. Demonstrate technological and economical impacts of cluster tool processing for cobalt silicide and Cu/TiN CVD applications.

Accomplishments:

- Universal reactor design completed. The universal reactor design was successfully applied to the fabrication of the RTP module.
- Design and fabrication of the first RTP tool completed. Temperature uniformity of better than ±3°C was obtained.
- Design of the key parts of the ICP and MOCVD modules were completed.
- Central wafer handler was fabricated and docked onto the RTP tool.

ADVANCED SINGLE-WAFER METALLIZATION CLUSTER TOOL

Yong Jin Lee, CVC Products, Inc.; MIT Lincoln Laboratories

Objectives

- Develop and fabricate a cluster tool for 0.18-μm silicide and interconnect applications.
- Develop equipment and process for contact and via cleaning using inductively coupled plasma.
- Develop equipment and process for refractory metal PVD.
- Develop equipment and process for MOCVD Cu, TiN.
- Develop equipment and process for silicidation using RTP.

Approach

- Reactor designs based on universal single-wafer modules allowing maximum reusability of designs.
- Advanced RTP incorporating multizone lamp source, multizone showerhead, emissivity correction, ultraclean rotation, and model-based multizone temperature control.
- Advanced MOCVD design featuring advanced gas-flow control, liquid delivery system, and temperature-controlled surfaces.
- Cleaning module featuring inductively coupled plasma (ICP).
- PVD module for sputter deposition of refractory metals.
- Integrated silicide cluster tool allowing pre-clean, metal deposition, and rapid thermal anneal in a vacuum integrated environment.

Status

- Universal reactor design is complete. The universal reactor design has been successfully applied to the fabrication of the RTP module.
- Design and fabrication of the first RTP tool is complete. Temperature uniformity better than ±3°C, 3σ has been achieved.
- Design of the key parts of the ICP, PVD, MOCVD have been completed.
- Central Wafer Handler has been fabricated.

Schedule/Tasks

- Completion of full process characterization on RTP—March 96.
- Completion of MOCVD—July 96.
- Completion of ICP—Aug. 96.
- Completion of PVD—June 96.
- Delivery of integrated silicide cluster tool to MIT Lincoln Lab—Sept. 96.

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Optoelectronics

DEVELOPMENT OF AN AUTOMATED PACKAGING MACHINE FOR OPTOELECTRONIC COMPONENTS

Project 9322-015

Team:

Uniphase Telecommunications Products
Lawrence Livermore National Laboratory
MIT Manufacturing Institute
Ortel Corporation
Newport Corporation

Description:

This project sought to substantially reduce the costs associated with packaging optoelectronic (OE) components by developing a modular, cost-effective manufacturing station for automated attachment of optical fibers to a variety of OE components. This automated manufacturing station for aligning and attaching optical fiber to OE components will be versatile and user friendly, low cost (<$100K production cost target for a single attachment station), and sufficiently modular and generic to find widespread application throughout the field of OE manufacturing.

A synergistic team of optoelectronic component manufacturers, optical equipment manufactures, and experts in automation, manufacturing, packaging, and machine vision was assembled to address the goals of this project. The team specified, designed, built, tested, and integrated into production a modular cost-effective station for automated attachment of optical fibers to OE components. The pigtailing station consists of two functional sub-systems or modules that perform coarse/fine alignment, fiber attachment, parts handling, and feeding.

Project Impact:

By enabling low-cost, high-throughput packaging of optoelectronic components, the automated pigtailing station has significantly reduced manufacturing costs for optoelectronic components. In addition, the technology developed under this project was transferred to an equipment manufacturer and is being used in a commercial pigtailing station.

Accomplishments:

- Completed specification, detailed design, and fabrication of an automated optical fiber pigtailing machine.
- Vision based coarse and fine alignment with active feed back, design completed, fabricated, and tested.
- One hour unattended operation achieved.
- Better than 0.1-micron alignment capability achieved.
- Machine automation software code written and debugged.

Development of an Automated Packaging Machine for Optoelectronic Components

V. Rodino, Uniphase Telcom Products;
Mark Lowry, T. Strand, Lawrence Livermore National Laboratory;
A. Sharon, MIT Manufacturing Institute

Objective

- Substantially reduce the cost of pigtailing optoelectronic (OE) components by developing a modular, cost-effective manufacturing station for automated attachment of optical fibers to a variety of OE components.

Approach

- Technology development.
  - Design and construction of an automated manufacturing station for OE pigtailing.
  - Modules include coarse-fine alignment and attachment, parts handling, and fiber prep.
- Manufacturing implementation.
  - Production demonstrations.
- Technology transfer.

Status

- 24-month program launched March 15, 1994.
- Specification and preliminary design of the automated fiber-pigtailing station are complete.
  - Machine will be compatible with high-throughput manufacturing processes (>20 pigtails per hour).

Schedule/Tasks

- Specification completed—June 94.
- PDR held—Nov. 94.
- CDR—Feb. 95.
- Build prototypes—June 95.
- Interface to production lines—Nov. 95.
- Production demo—Dec. 95.
- Final design revisions/technology transfer—March 96.

OPTICALLY INTERCONNECTED COMPUTING CLUSTER

Project 9322-020

Team:

Martin Marietta (now Lockheed Martin)
Lawrence Livermore National Laboratory
AT&T (now Lucent Technologies)
Honeywell
IBM

Description:

This project performed a field trial of parallel optical interconnect buses developed by the Optoelectronics Technology Consortium (OETC). The field trial consisted of:

- The OETC members (Lockheed Martin, Lucent Technologies, Honeywell, IBM) built optical buses, which consist of a 32-channel transmitter and receiver pair, plus a 32-fiber ribbon cable.
- Approximately half of the buses were used at LLNL in a Optically Interconnected Computing Cluster testbed. The testbed was built in collaboration with computer architects at major U.S. computer companies. Demonstrations of capability were held to develop the interest of user companies.
- The remaining buses were used in collaborative evaluations between the OETC companies and user companies who are developing product applications.

Project Impact:

The project will potentially leverage several new system applications at U.S. computer, telecommunications, and military systems companies. These applications will provide an initial market for makers of components including laser diode arrays, fiber ribbon cables and connectors, and packaged subsystems.

Accomplishments:

- Prototype buses were demonstrated and performed beyond the project goals of 500 Mbytes/second per channel over 100-m-long cables.
- The computing cluster interface architecture was completed.
- Assembled receiver and transmitter modules for the 32-channel transmitter/receiver links. These units underwent high-speed test at IBM. The modules were assembled into links, tested, and delivered to LLNL.
- Delivered buses to LLNL for test bed applications; additional buses will be used by OETC II team for test bed applications.
- Completed studies of system insertion opportunities for optically interconnected computing technology.

Optically Interconnected Computing Cluster

Kelly Wypych, Lockheed Martin, Inc.;
Mark Lowry, Lawrence Livermore National Laboratory

Objectives

- Develop a quantity of 50-75 working 32 x 1 500-Mb/s per channel optoelectronic buses using the OETC modules.
- Develop an optically interconnected computing cluster using 20-30 of the OETC buses.
- Demonstrate the cluster to US computer companies with interests in applying the optical interconnect technology.
- Supply a quantity of the OETC buses to user testbeds for system applications development. Gain feedback from the users on future requirements.

Approach

- Use the module designs developed under the DARPA OETC program as a starting point.
- Incorporate changes desired by users, e.g., CMOS compatibility vs. ECL.
- Bring up Honeywell's MOCVD process for VCSELs to handle the larger quantities of this program.
- Transfer module assembly from the AT&T lab to the prototype production environment at AT&T Merimac Valley.

Status

- First vertical-cavity surface-emitting laser (VCSEL) arrays delivered from Honeywell to AT&T. Initial modules using the new VCSELs perform beyond the specification.
- Design changes incorporated in TX and RX modules to allow for differential CMOS compatibility.
- Initial architecture of computing cluster defined.

Schedule/Tasks

- Prototype modules delivered to LLNL—Nov. 94.
- 1st of deliverable modules to LLNL—Feb. 96.
- Complete LLNL delivery—March 96.
- User demonstrations—June 96.
- User evaluation results—June 96.

RED VERTICAL-CAVITY SURFACE-EMITTING DEVICES FOR PRINTING AND DATA COMMUNICATION

Project 9322-023

Team:

Xerox Corporation
Honeywell Incorporated
Sandia National Laboratories

Description:

This project involved the development of red vertical-cavity surface-emitting laser (VCSEL) technology for commercialization. Sandia's fundamental and pioneering developments in this technology were evaluated with a focus on insertion into two key markets: high-performance laser printing using laser arrays and data communications using plastic optical fiber. The following areas were addressed:

- System and Prototyping - VCSEL device performance specifications appropriate for the printing and datacomm markets were developed. Appropriate packaging strategies for single elements and arrays were identified.
- Device Development - Specific VCSEL device performance issues were addressed, directed towards reaching the red VCSEL device performance specifications required based on the System and Prototyping effort. Opportunities for building architectural similarities into the datacomm and printhead device structures were exploited whenever possible. The packaging strategies identified in the System and Prototyping effort were implemented.
- Prototype Demonstration - The output of the device development effort was used to build prototype devices for insertion into print array and datacomm systems. Relevant system performance parameters were measured on the prototype devices to evaluate the level of performance obtained.

Project Impact:

Create a commercial use for a technology that has the potential to result in a stronger domestic position in these areas. Evaluation of the systems advantages of using red VCSELs in the applications will result in an earlier and higher quality decision on the strategic importance of this technology.

Accomplishments:

- Performance specifications for printhead and datacomm were defined.
- A number of significant red VCSEL performance milestones were achieved:
  - Continuous wave (CW) lasing in red VCSELs up to 8-mW output power.
  - Power conversion efficiencies for CW red VCSELs up to 11%.
  - Single transverse mode operation of CW red VCSELs in excess of 2-mW. CW lasing of red VCSELs achieved up to 60°C.
  - Lasing emission from CW red VCSELs over 642-690-nm range.
  - 1600 hour CW red VCSEL operation (1 mW) with no degradation. Successful demonstration of oxide-confined red VCSEL devices.
  - Sub-milliamp threshold currents and low threshold voltages (<150-mV above the photon energy).
- The VCSEL fabrication process was successfully transferred from Sandia to an industrial partner.
- Red VCSEL arrays for printing were successfully fabricated by an industrial partner.
- Preliminary evaluation of a red VCSEL in a data communications link was performed by an industrial partner.
- Modeling software was developed for more efficient design of red VCSEL structures.
- Red VCSEL materials growth capability was established by an industrial partner.

RED VERTICAL-CAVITY SURFACE-EMITTING LASERS FOR PRINTING AND DATA COMMUNICATION

Robert Thornton, Xerox Corporation;
Mary Hibbs-Brenner, Honeywell Technology Center
Adelbert Owyoung, Sandia National Laboratories,

Objective

- Develop Red VCSEL devices to meet the performance specifications defined by the key markets of data communications using plastic optical fiber and high-performance laser printing.

Approach

- Leverage leading edge work performed at Sandia National Labs.
- Create a cooperative effort between systems developers for the two key markets.
- Enlist the early-on involvement of production/manufacturing organizations.
- Focus on device performance advances needed to enable target systems.

Status

Start Date: 12/28/93
Program Duration: 24 Months

- One year extension obtained on time to complete.
- Preliminary device performance specs for data communication and printing established.
- VCSEL discrete device performance level advanced (5mW CW RT).
- Transfer of Red VCSEL processing technology to Xerox complete. VCSEL printhead arrays prototypes fabricated, packaged, and delivered.
- Red VCSEL structures grown at Honeywell. Initial fiber data communication with Red VCSELs demonstrated.

Schedule/Tasks

- Establish system performance specs—June 94.
- Base-level device performance established—Aug. 95.
- Array design latitudes established—April 95.
- Prototype devices fabricated—May 96.
- Prototype test and evaluation complete—July 96.

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AC	Alternating Current (AC-plasma displays)
ALE	Atomic Layer Epitaxy
AMEL	Active Matrix Electroluminescent
AMPL	Advanced Manufacturing Processes Laboratory, SNL/NM Facility
BAA	Broad Agency Announcement
CCF	Central Computing Facility
CFM	Contamination-Free Manufacturing
CMO	Center for Microelectronics and Optoelectronics, LLNL Facility
CMOS	Complementary Metal Oxide Semiconductor
CoO	Cost-of-Ownership
c-PVD	Collimated - Plasma Vapor Deposition
CSRL	Compound Semiconductor Research Laboratory, SNL/NM Facility
CVC	Chemical Vapor Cleaning
CVD	Chemical Vapor Deposition
CW	Continuous Wave
DARPA	Defense Advanced Research Projects Agency
DoD	Department of Defense
DOE	Department of Energy
EECF	Electron Emission Characterization Facility, SNL/CA Facility
EEM	Electron Emission Microscope
EL	Electroluminescent (Displays)
ETO	Electronic Technology Office (DARPA)
FCM	Factory Cost Model
FED	Field Emission Display
FPD	Flat Panel Display
HDS	High Definition Systems
Hhfac	Hexafluoro-2,4 Pentanedione
HIBS	Heavy Ion Backscattering
ICF	Inertial Confinement Fusion
ILD	Inter-Level Dielectric
LANL	Los Alamos National Laboratory
LCD	Liquid Crystal Display
LLNL	Lawrence Livermore National Laboratory
MDL	Microelectronics Development Laboratory, SNL/NM Facility

MESC	Modular Equipment Standards Committee
MOCVD	Metal-Organic Chemical Vapor Deposition
MRB	Materials Research Building, SNL/CA Facility
NCAICM	National Center for Advanced Information Components Manufacturing
Nd:YAG	Neodymium:yttrium aluminum garnet (laser)
NMP	1-Methyl-2-pyrrolidinone
OETC	Optoelectronics Technology Consortium
PAB	Project Advisory Board
PCSV	Particle Counter, Sizer, Velocimeter
PDP	Plasma Display Panels
Phase I	Pre-competitive projects
Phase II	Industry-defined, industry-led, competitively-selected joint projects with the National Labs
POI	Parallel Optical Interconnects
PPS	Point Probe Scanner
PVD	Plasma Vapor Deposition
PZT	Lead zirconate titanate
R&D	Research and Development
RIE	Reactive Ion Etch
RTP	Rapid Thermal Processing
SAECS	Surface Analysis and Emission Characterization System
SCI	Scaleable Coherent Interface
SEMATEC	A consortium of semiconductor companies
SEMI	Semiconductor Equipment and Materials International
Si	Silicon
SIDT	SI Diamond Technologies, Inc.
SIMS	Secondary Ion Mass Spectroscopy
SNL	Sandia National Laboratories
STTR	Small Business Technology Transfer Program
SVC	Silicon Video Corporation
TRP	Technology Reinvestment Program
TTF	Target Fabrication Facility, LANL Facility
TTI	Technology Transfer Initiative
TTO	Tactical Technology Office (DARPA)
TXRF	Total External Reflectance X-ray Fluorescence
UHV	Ultra-High Vacuum
USDC	U.S. Display Consortium
VCSEL	Vertical-Cavity Surface-Emitting Laser
XPS	X-ray Photoelectron Spectroscopy

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