ASSESSMENT OF CIRCUIT BOARD SURFACE FINISHES FOR ELECTRONIC ASSEMBLY WITH LEAD-FREE SOLDERS

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Abstract

The suitability of various metallic printed wiring board surface finishes was assessed for new technology applications that incorporate assembly with Lead-free solders. The manufacture of a lead-free product necessitates elimination of lead (Pb) from the solder, the circuit board as well as the component lead termination. It is critical however for the selected interconnect Pb-free solder and the corresponding printed wiring board (PWB) and component lead finishes to be mutually compatible. Baseline compatibility of 'select' Pb-free solders with Pb containing PWB surface finish and components was assessed. This was followed by examining the compatibility of the commercially available CASTIN™ (SnAgCuSb) Pb-free solder with a series of PWB metallic finishes: Ni/Au, Ni/Pd, and Pd/Cu. The compatibility was assessed with respect to assembly performance, solder joint integrity and long term attachment reliability. Solder joint integrity and mechanical behavior of representative 50 mil pitch 20I/O SOICs was determined before and after thermal stress. Mechanical pull test studies demonstrated that the strength of SnAgCuSb solder interconnections is notably greater than that of SnPb interconnections. With the exception of electroless Pd surface finishes, Pb-free solder interconnections to peripheral leaded packages survived 5000 temperature cycles of 0°C to 100°C. Metallurgical cross-sections were used to examine the structure of the joints made to Ni/Au, Ni/Pd, and Pd surface finishes. For the Ni/Pd finishes, intermetallic compounds were found floating neat the interface between these Pd-Ni compounds and the interface, correlating to lower pull strengths.

I. Introduction

The electronics industry is driven by both technological advances such as chip functionality and alternative packaging techniques, including environmental drivers, such as alternate cleaning processes and Pb-free solders. The development and assessment of Pb-free solders for electronics applications has intensified in recent years [1-10]. The majority of these studies involved using non-Pb bearing coatings for both circuit boards as well as the package I/Os (leads and terminations).

The electronics industry infrastructure is not ready to convert over to Pb-free circuit board finishes and component lead finishes. The alternate PWB finishes such as immersion gold over electroless nickel (Ni/Au) and electroless Pd over electroless Ni (Ni/Pd) are still in their infancy for mass production. Prior to converting over to a new solder technology (in this case a Pb-free solder), upfront evaluation of the compatibility of this solder both with the current and future and component lead terminations is necessary.

The compatibility of Pb-free solders with Pb-containing surface finishes has been addressed in detail elsewhere [11] and will be summarized in Section II. In Section III, results from the compatibility evaluations of Pb-free solder with Pb-free surface finishes will be discussed.

II. Baseline Compatibility with Pb-Free solder and Pb-containing PWB finishes

The solder selected for this study was a commercially available alloy, 96.2Sn-2.5Ag-0.8Cu-0.5Sb (wt.%) designated by the trade name, CASTIN™ (A.I.M. Corp.) based on previous manufacturability studies. The goal was to quantify the effects of Pb contamination on the performance of solder joints made with CASTIN™ alloy. The following combinations for PWB surface finish and component lead surface finish were used:

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DISCLAIMER

PWB finish	Component lead finish
HASL	SnPb
Imidazole	SnPb
Imidazole	Sn

A. Experimental: Circuit Board Prototypes

The devices used to evaluate the integrity of the circuit board solder joints were 20 I/O Small Outline Integrated Circuit (SOIC) packages. The package material was plastic. The leads were copper, having the gull wing configuration . The lead pitch was 0.050 in. The lead finishes were either electroplated 63Sn-37Pb solder (which provided the Pb contamination) or hot dipped 100Sn coatings.

The 20 I/O SOIC packages were assembled onto a double-sided, epoxy-glass multifunctional laminate circuit boards with a nominal 0.062 in. thickness. The glass transition temperature of the laminate was between 150°C and 200°C.

The solders were printed onto the circuit boards as a paste comprised of 89-91 wt.% type 3 metal powder and an RMA flux vehicle. Solder reflow of the test vehicles was performed in an infrared/natural convection furnace under flowing nitrogen (<100ppm O_2). The nominal furnace parameters were determined in a previous study [12]. The circuit boards were visually inspected after assembly for general defects as well as those that would directly impact the reliability data. Defects of either category were not observed for either of the solders.

Thermal cycling of selected test vehicles was performed in air. The cycle parameters were: (1) limits, 0°C and 100°C; (2) 5 min. holds at the limit temperatures; and (3) 20°C/min. ramp rates in wither direction. CASTIN™ solder containing specimens were exposed to 0, 2980, 5671, or 10037 cycles.

The microstructure of the SOIC solder joints and their failure morphology were documented by cross section/metallographic techniques and scanning electron microscopy (SEM), respectively. The mechanical integrity of the gull wing joints was assessed by a pull test procedure. First, the plastic package was cut from the leads. Then, each lead was secured into a small group fixture that was attached to the cross head of a mechanical test frame. The lead was pulled from the circuit board in a direction perpendicular to the surface. The pull direction, coupled with the gull wing geometry, constituted a *peel-type* mechanical test on the solder joint. The cross head speed of the test frame was 0.35 in./min. Twenty (20) leads were pulled per test; the data were represented as the mean and $\pm$ one standard deviation of those multiple data.

B. Results: SOIC Solder Joint Performance

The as-fabricated solder joint exhibited minimal manufacturing defects. The observation corroborated the results of previous manufacturing trial with the CASTIN™ and Sn-Ag-Bi solders [11]. Generally, better wetting was observed for the Sn-Pb coated surfaces as opposed to the imidazole and 100Sn coatings in the case of the CASTIN™ solder; however, the differences were not significantly great so as to affect the solder joint mechanical properties in the fabricated condition, or cause premature degradation during thermal cycling.

Metallographic cross sections were made of four solder joints per each of the solder/printed wiring board (PWB) finish/lead finish systems. The microstructure of the as-fabricated joints confirmed good wetting of the leads and circuit board copper features. Plastic deformation, in the form of grain boundary displacement or cracks, was not observed in the solder microstructure of the fillet regions nor in the gap between the underside of the lead and the circuit board. All indications were that the Sn-Pb surface finishes had readily dissolved into the solder during the assembly process.

Similar metallographic cross sections were made of the corresponding specimens subjected to the nominal 10,000 thermal cycles. Some plastic deformation was observed in the solder microstructure, but it was restricted to the fillet regions of the joint (either the heel fillet or the smaller toe fillet at the end of the gull wing lead). The extent of such damage was limited to surface shear bands and the formation of small cracks at the base of the fillet near the circuit board. The magnitude of the observed deformation was not considered consequential to the integrity (mechanical or electrical) of the solder joints. This point was later supported by the mechanical test results.

The pull strength data for the SOIC leads is presented in Table 1. The strength of as-fabricated joints made with the CASTIN™ solder was not sensitive to the circuit board or lead finishes. The strengths were statistically the same, whether the circuit board and lead finishes were: (1) both Sn-Pb (5.43 ± 0.32 lb.), (2) imidazole and Sn-Pb, respectively (5.47 ± 0.53 lb.); or imidazole and pure Sn, respectively (5.81 ± 0.59 lb.).

The fracture morphologies of the CASTIN™ solder joints were sensitive to the coating composition. Shown in Fig. 1 is a scanning electron micrograph of the failure morphology of the circuit board pad from an as-fabricated test vehicle having the imidazole coating; the lead had a Sn-Pb coating. The contour of the failure path followed that of the lead. A similar morphology was observed when the lead finish was changed to pure Sn. However,

the fracture path of the joints made with Sn-Pb on both the lead *and* the circuit board pad progressed along the solder/copper pad interface (Fig. 2). This result suggests that the HASL coating caused failure to preferentially occur there. Irrespective of the difference in the failure mode, the pull strength of the CASTIN™/HASL/Sn-Pb joints was not significantly different from that of the other joint materials combinations.

Table 1: Pull strength data

Thermal Cycles	CASTIN™		
	HASL/Sn-Pb (lb.)	Imid. / Sn-Pb (lb.)	Imid. / Sn (lb.)
0	5.42 ± 0.32	5.47 ± 0.53	5.81 ± 0.59
2602	4.79 ± 0.97	5.57 ± 0.52	4.22 ± 0.55
5068	4.77 ± 0.82	4.71 ± 0.38	4.05 ± 0.99
10,106	4.24 ± 0.43	4.91 ± 0.68	4.56 ± 0.67

Test configuration is an important variable, when all else is equal (i.e., materials and joint processing), because it can determine the stress state in the joint (bulk solder and interfaces) and therefore, where failure occurs. For example, the interface strength will appear greater when tested under shear, such as in the ring-in-plug test format, than when tested with a tensile component, such as in the SOIC lead pull test. Therefore, in the former case, the joint strengths will more closely represent the bulk solder properties. In this latter case, failure is more likely to occur at the interface, reflecting the generally weaker strength of the interface under tension.

Estimates of the Sn-Pb concentration in the joints were based on typical joint geometries observed in the metallographic cross sections. It was also assumed that the Sn-Pb coating layer of the lead had a thickness of 0.0003 in. The results of the computations showed that in the first case of complete interdiffusion, the expected Sn-Pb contamination would be approximately 10 wt.%. In the second scenario of localized Sn-Pb contamination build-up, the Sn-Pb concentration in the joint gap was calculated to be about 18 wt.%

The impact which thermal cycling had on the pull strength of the CASTIN™ solder joints was dependent upon the particular circuit board/lead finish (Table 1). In the case of a Sn-Pb finish on both the circuit board (HASL) and on the leads, the post-thermal cycle pull strengths were lower than the baseline (zero cycles) value of 5.42±0.32 lb.; however, the decrease became significant only after 10,106 thermal cycles (4.24±0.43 lb.). The fracture morphology did not differ from that of the as-fabricated pull test specimens. The microstructural damage observable in the thermally cycled parts, did not appear to have a strong role in the failure modes of the solder joints. Therefore, the source of lower strengths for the thermally cycled joints were smaller scale changes to the microstructure of the solder that remained unobservable.

The pull strength of the CASTIN™/imidazole/Sn-Pb joints decreased slightly with thermal cycling; however, the lower strengths were not significantly different from the baseline value following any of the exposure conditions. The fracture morphology likewise remained unchanged from that of the as-fabricated units.

The CASTIN™/imidazole/Sn solder joints, on the other hand, exhibited strength drops that were significant in all cases of thermal cycling. From a baseline value of 5.81±0.59 lb., the pull strength decreased to 4.22±0.55 lb., 4.05±0.99 lb., and 4.56±0.67 lb. after 2602, 5058, and 10,106 thermal cycles, respectively. When these data were compared with those from the other two test categories, the values were similar. That is, a large extent of the apparent strength loss was due to a relatively high as-fabricated (initial) strength (again, relative to the other data).

It was noted from metallographic cross sections that the drop in strength accompanying the Sn-Pb additions was not caused by large-scale damage that could potentially jeopardize the *electrical* performance of the joint. Also, thermal cycling did not alter the fracture morphology of the solder joints. Finally, the strength levels of the Sn-Pb contaminated CASTIN™ solder joints were more than adequate to provide the mechanical integrity of the package.

The test results from the CASTIN™ solder joints indicated that there was no significant trend to pull strength versus Sn-Pb contamination level after thermal cycling. That is, Sn-Pb contamination did not consistently accelerate, nor retard, the extent of pull strength loss in the SOIC solder joints caused by thermal cycling. Based upon the earlier estimates of the Sn-Pb contamination levels to be expected in the gull wing joints (which would be further increased in the PCB HASL finish specimens), and the fact that at those levels, 63Sn-37Pb compositional phases would certainly form in the solder (as determined from earlier DSC data), then the presence of those regions did not deteriorate the as-fabricated pull strength, nor did they cause an adverse effect on joint strength and integrity under the thermal aging conditions which accompanied the thermal cycling tests. Therefore, it may be Inferred that the 63Sn-37Pb regions, which form in CASTIN™ solder with excess (<2%) Sn-Pb contamination, are

relatively stable under *general* elevated temperature environments, and are not likely to pose a threat to joint reliability under extended service conditions.

III. Compatibility with Pb-Free PWB Finishes

The past few years have seen the emergence of thin metallic films for large volume circuit board applications, especially in fast growing segments such as the cellular terminals. Recent studies show that Ni/Au and Ni/Pd coatings provide enhanced solder wettability [13, 14]. The current electroless Ni/immersion Au and electroless Ni/electroless Pd processes deposit a thin (5-10 µin), dense noble metal layer over an ~ 150 µin Ni-Phosphorus barrier layer. The purpose of the gold or palladium coating is to prevent the oxidation of the underlying nickel layer, thereby enhancing solderability. An alternative process involves the deposition of a ~20 µin Pd layer directly over the copper substrate, thereby eliminating the electroless Ni chemistry.

The objective of this portion of the study was to determine the viability and the range of applicability of the new immersion/electroless metallic finishes, with special emphasis toward their compatibility with Pb-free solders.

A. Experimental: Circuit Board Prototypes

Prototype assembly was conducted using a National Center for Manufacturing Sciences (NCMS) solderability test vehicle (STV). This test vehicle is a double sided epoxy glass board, designed with a broad variety of typical through hole and surface mount components. Most of the components are daisy chained, thus allowing their solder joints to be electrically monitored during any functional or environmental testing.

The test vehicle assembly consist of the following components:

Component	Quantity
1206 chip capacitors (20 top/20 bottom)	40
SOT-23 (8 top/8 bottom)	16
SOIC 20	7
LCCC 44	1
PLCC 44	1
PLCC 84	1
132 QFP (0.025" pitch)	1
208 QFP (0.5mm pitch)	1
256 QFP (0.4mm pitch)	1
20 pin ceramic DIP	2
20 pin plastic DIP	3
68 pin PGA	1
Axial resistors	65

The SM assembly was performed on a Fuji system using the Pb-free solder paste. The solder paste was constituted with 89-91% (by weight) type 3 metal powder and conventional RMA based flux vehicle. The reflow profile was adjusted to accommodate the slightly higher melting point of the Pb-free solder. Wave soldering was performed with a no clean flux and nitrogen inerted atmosphere.

B. Results:

PWB solder interconnection integrity/reliability

A general concern with noble metal surface finishes is joint embrittlement due to incomplete dissolution of the Au or Pd layers into the solder matrix [13]. Small concentrations of Au or Pd at the solder/substrate interface can lead to the formation of brittle SnAu or SnPd intermetallic compound phases. The role of Pd concentration on solder joint embrittlement is discussed elsewhere [15].

The mechanical integrity of solder interconnections was measured by pull testing leads of surface mount packages soldered on STVs. The body of the surface mount packages were excised using a low speed diamond saw. Individual leads were grasped with a stainless steel clamp mounted on a motorized microtensile tester. The leads were vertically pulled at a rate of 0.4 inches per minute: failure strength was recorded as the maximum load observed during the test. A decision was made to pull test leads from three package styles:

- 256 I/O 0.4 mm Pitch PQFP Gull Wing Leads
- 84 I/O 50 mil Pitch PLCC J-Leads
- 20 I/O 50 mil Pitch SOIC Gull Wing Leads

The PLCCs are representative of standard surface mount packages and the 0.4 mm pitch PQFP represent fine pitch technology packages. While pull testing "as assembled" STVs provides an adequate representation of the mechanical integrity of solder interconnections, additional evaluations are required for assessment of the interconnection reliability. The following variations of stress testing were used to assess solder joint integrity.

- "As Assembled" (i.e., no accelerated aging)
- After 2500 temperature cycles of 0 °C to 100 °C (3 cycles per hour)
- After 5000 temperature cycles of 0 °C to 100 °C (3 cycles per hour)

Automatic electrical monitoring for open solder interconnections during temperature cycling was not

performed. However, upon completion of temperature cycling, manual electrical continuity measurements were made on all of the surface mount and through hole component solder interconnections. Temperature cycling did not create open solder interconnections on any of the peripheral leaded surface mount packages. Opens were detected on most of the 256 I/O ceramic BGAs after 5000 temperature cycles. All of the 44 I/O leadless ceramic chip carriers (LCCC) had open solder interconnections after 2500 temperature cycles and the LCCCs fell off the STVs after 5000 cycles. These thermal-fatigue induced open solder interconnections were observed to be a function of the package type rather than the surface finish.

A complete report describing the performance of metallic surface finishes with eutectic SuPb solder has been published elsewhere [16]. In this study, we have specifically focused in comparing the solder joint integrity of joints made with CASTIN™ solder. The results of the mechanical strength tests for the 256 I/O PQFP are presented in Figure 3. Approximately 100 leads from each PQFP were pull tested. The remainder of the leads were left intact for metallurgical cross sectioning and evaluations.

Prior to thermal cycling, the average pull strength for 0.4mm pitch PQFP leads was about 1 pound while the average for the bigger 50 mil pitch PLCC leads was over 3 pounds (data not shown). A fracture in the solder fillet near the peripheral lead was the typical mode of failure when the leads were pulled vertically. The solder fillet usually remained on the STV surface mount land. Although the craters formed when the leads separate form the solder fillets appear to indicate a lead/solder interface separation, examination of the leads and fillets show the separation to be a cohesive failure in the bulk solder. This was the case for the majority of the pull tests. For the case of Pd, there is preliminary indications of a "seeding" problem (i.e., adhesion of Pd to Cu).

A comparison of the PQFP pull strength frequency distribution before and after temperature cycling clearly indicates a non-ideal behavior of the Pd-based finishes. This trend is stronger with the CASTIN™ solder, where there is a significant decrease in the pull strengths after 2500 cycles. Current work in progress shows that this decrease continues after 5000 cycles (data not shown in this paper).

Figure 4 shows the mechanical pull test data from the 50 mil pitch SOICs, which clearly shows a lower pull strength for the electroless Pd finishes both before and after temperature cycling as compared to the other finishes. The differences in pull strength for the other surface finishes before and after thermal cycling is not statistically significant.

Metallurgical Cross-section

SOIC's from 2,500 and 5,000 thermal cycles boards prepared with different surface finishes were cross-sectioned to examine the interface metallurgy and the integrity of the solder joints. The cross-sectioning was done parallel to the shorter edge of the chip so that leads #1 and #20 could be exposed in the same mount. The samples were then examined using a scanning electron microscope.

Wetting of the Joints

The joints on all 4 surface finishes exhibited good solder wetting, and the imidazole finished joint after 500 cycles shown in Figure 5, is a typical example. Both toe and the heel of the leads were adequately formed, and the solder spread to completely cover the copper pad on the substrate. The wetting angles of the joint on the copper pad were between 20 to 25°. And the wetting angle along the lead is typically less than 10°.

Voids in the Joints

The joints with the electroless Pd finish had many voids along the interface of the copper pad, as evidenced by the micrograph (after 2500 cycles) in Figure 6. The size of the voids range from several μm to 100 μm in diameter. The large amount of the voids correlates with a low pull strength measured from joints made with this surface finish.

Some voids were also found in the joints with an immersion Ni/Au finish, as can be seen in Figure 7, but not nearly as many as in those with the Pd finish. The pull strength of the Ni/Au finish is slightly less than the imidazole and Ni/Pd joints ; the differences might not be statistically significant.

No voids can be seen in the cross-sections of any of the other joints. Therefore it can be concluded that the voids in the Pd and Au/Ni finished joints were not from the solder paste, since certainly some voids would have appeared in other surface-finished joints. The source of voiding may meet with entrapped contamines by in which the plating or immersion bath used in those particular processes may rest with entrapped contaminants.

Integrity of the joints

There were no significant cracks observed in any of the thermal cycled joints, from either the 2,500 or the 5,000 cycled samples. It indicates that the thermal cycling condition (0 to 100°C) has very little impact on the SOIC solder joint integrity up to 5,000 cycles. Some small, crack like, connections can be seen between voids in the

electroless Pd joints which may be attributed to the weak linkage between the voids.

Interface metallurgy

The metallurgy at the solder-substrate interface and in the solder joints is dependent, to a large measure, on the surface finishes. The joint made with an imidazole surface finish have the typical nodular-shaped Cu_6Sn_5 intermetallic compound at the interface between the solder and the copper substrate, as shown in Figure 8. The compound is about 3 to 4 μm thick. There are also some Cu_6Sn_5 compound floating in the solder, which may be the precipitate from the copper content in the solder, or from Cu dissolved in the solder from both the copper substrate on PWB and/or the copper lead of the SOIC. Silver in the solder appears as a Ag_3Sn precipitate, typically 1 μm or less in size. Antimony (Sb) remained largely in solid solution in the Sn-rich phase.

The joint made with the Pd finish have many $PdSn_4$ precipitates in the joint. Figure 9 is a magnified micrograph of the solder between the lead and the substrate in Figure 2. The voids in the joints are clearly visible. The voids are connected, possibly due to cracks generated during the thermal-cycle testing. The rectangular light-gray precipitate in the solder is $PdSn_4$ intermetallic compound, with Pd coming from the dissolution of the Pd surface finish. The intermetallic compound at the interface of solder and substrate appears to be Cu_6Sn_5, which is formed when the Pd dissolves and the solder contacts the Cu on the PWB directly.

For the electroless Ni/Pd surface finish, dark-gray particles are seen in the solder, which were found to be Cu_6Sn_5. There are also 3 to 4 μm size light-gray particles in the solder which have been detected as being $PdSn_4$, with Pd coming from the surface finish. The $PdSn_4$ particles appear in a band about 2 to 10 μm from the Ni layer and close to the (Cu,Ni)-Sn compounds. In addition, a high P content was detected in the Ni layer, believed to be coming from the plating bath.

A micrograph of the Ni/Au finished joint seen in Figure 10 shows a 5 μm-thick Ni layer, with a (Cu,Ni)-Sn compound on it. The (Cu,Ni)-Sn compound is a continuous sub-micron layer, but the morphology is different from the same compound above Pd/Ni finish joints which have large particles extending into the solder. There was no Au in evidence from viewing the micrograph. The Ag_3Sn precipitate in the solder are generally larger than those in the other surface finished joints. Pin-holes were often seen in the Ni layer, a typical example can be seen in the center of Figure 10. The hole is filled with Cu_6Sn_5 compound since there is a direct contact between the solder and the Cu substrate.

IV. Conclusions

The viability of various metallic printed wiring board surface finishes was assessed with new technology applications that incorporate assembly with lead-free solders.

Baseline compatibility of select Pb-free solders, CASTIN™, was established with Pb containing PWB surface finish and component leads. As-fabricated mechanical pull strengths of gull-wing components attached with the Pb-free solder were not sensitive to the presence of SnPb from the lead and/or circuit board SnPb coatings. Although strength drop was observed after thermal cycling, it was not sensitive to the SnPb in the finish. The post-thermal cycle strengths (and microstructural integrity) were adequate to meet attachment requirements.

Compatibility of CASTIN™ solder with noble metal PWB finishes (Ni/Au, Ni/Pd and Pd) was assessed.

Solder joints made with Pd coated boards show marked decrease of mechanical strength which can be attributed to the formation of $PdSn_4$ intermetallic. Solder interconnections to peripheral leaded packages for all other surface finishes exhibited excellent strength retention 5000 temperature cycles of 0°C to 100°C. For the Ni/Pd finishes, intermetallic compounds were found floating neat the interface between these Pd-Ni compounds and the interface, correlating to lower pull strengths.

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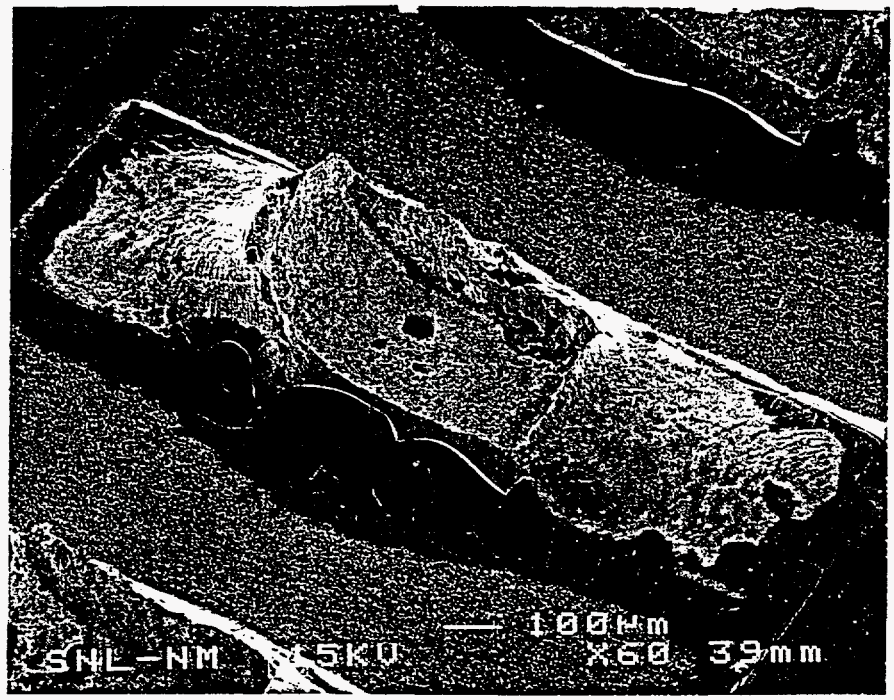


Figure 1. Scanning electron micrograph of the solder joint pull test failure (circuit board pad) for Castin solder, imidazole PCB finish and SnPb lead finish.

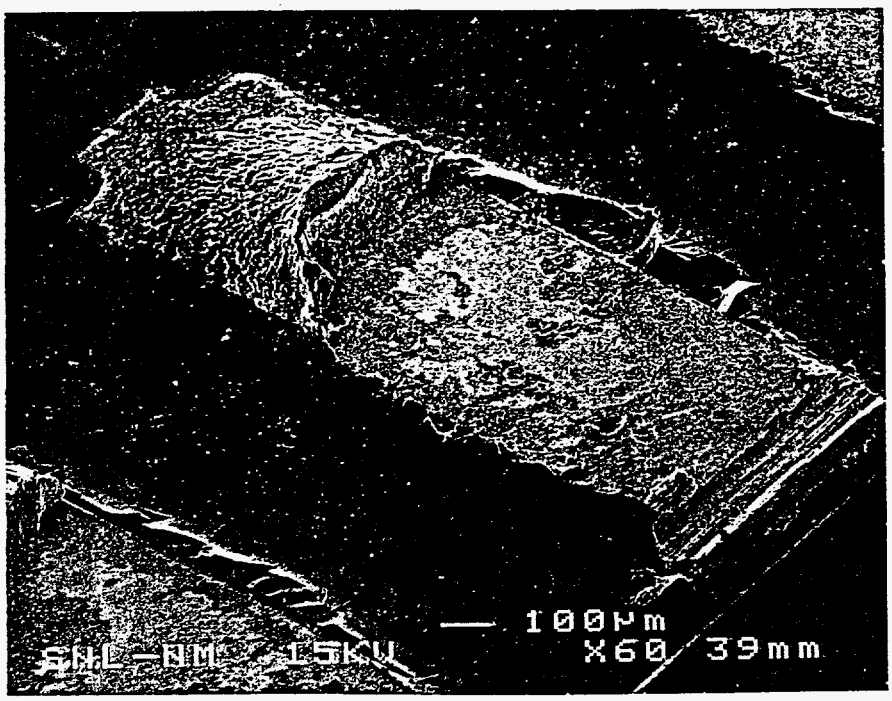
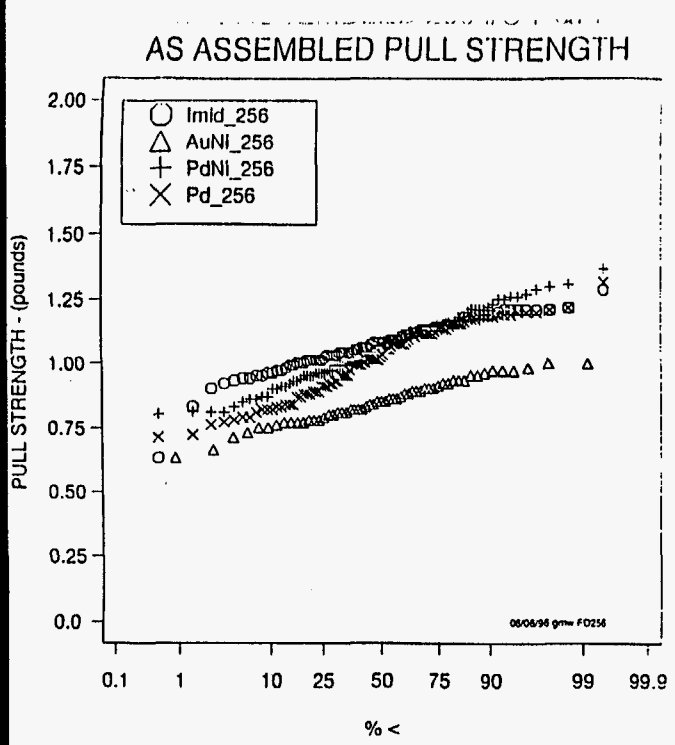
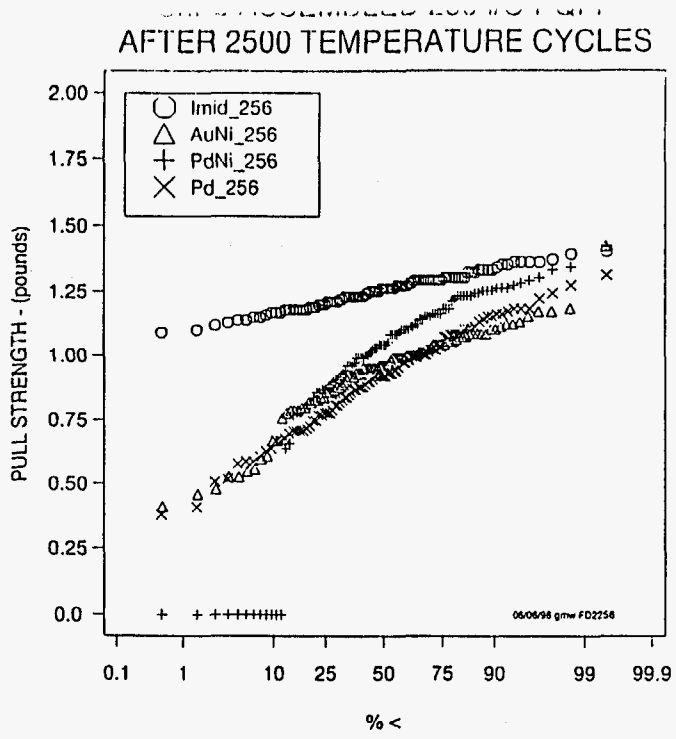


Figure 2. Scanning electron micrograph of the solder joint pull test failure (circuit board pad) for Castin solder, SnPb (HASL) PCB finish and SnPb lead finish.





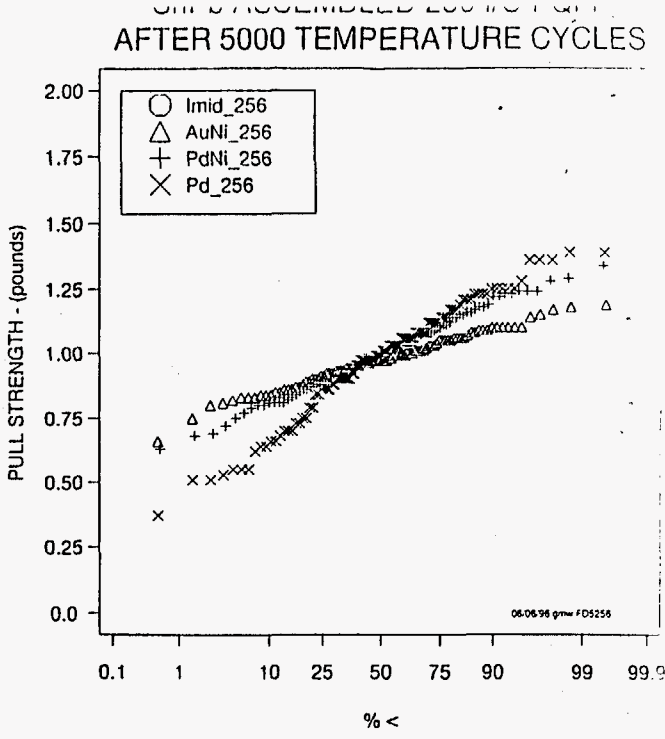
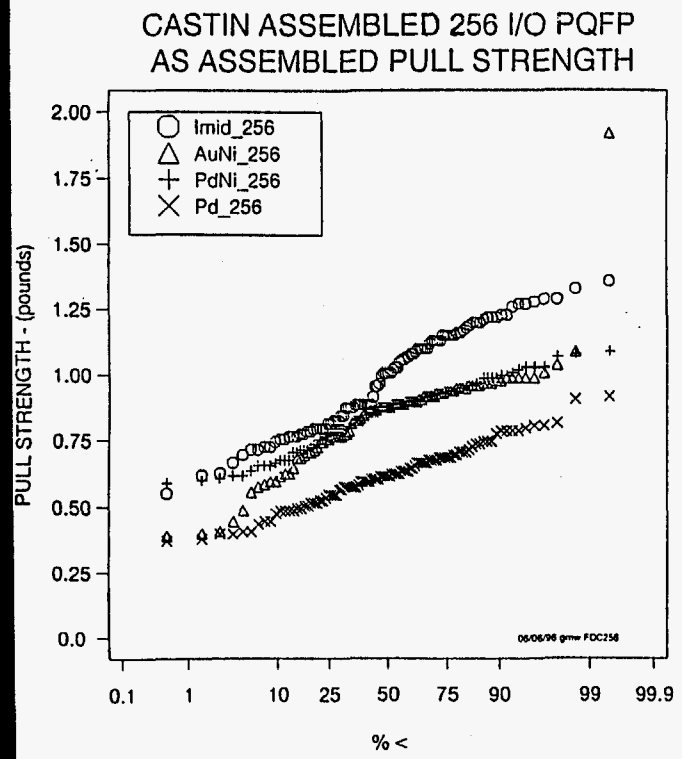
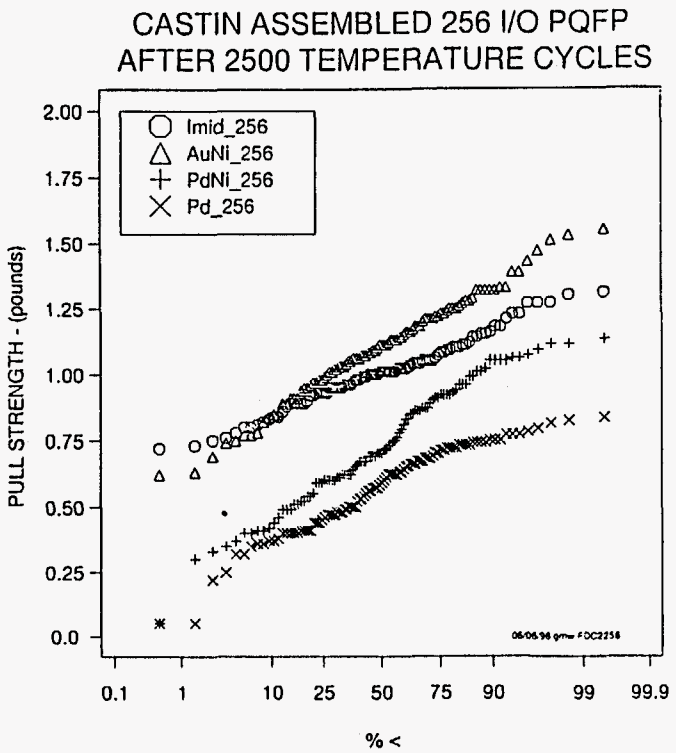
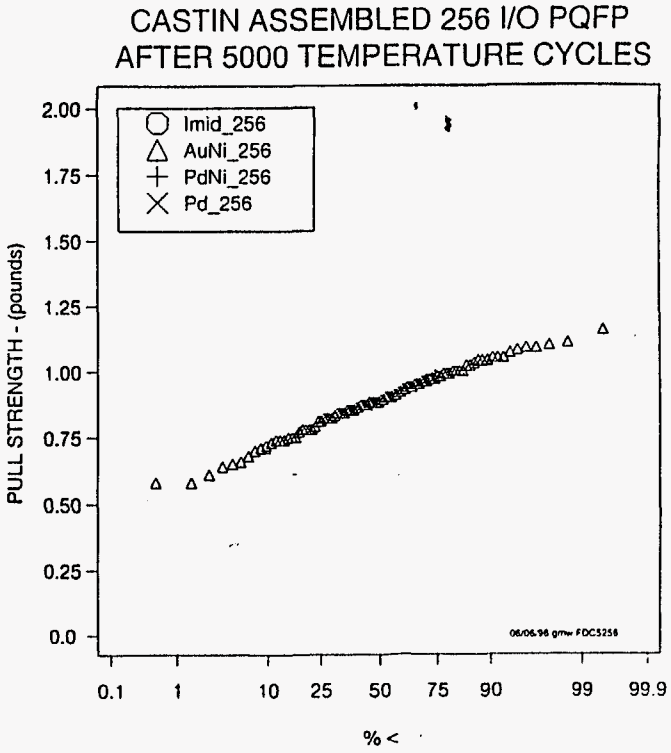


Figure 3: Mechanical pull test data for 256 I/O, 0.4 mm pitch PQFPs before and after thermal cycling







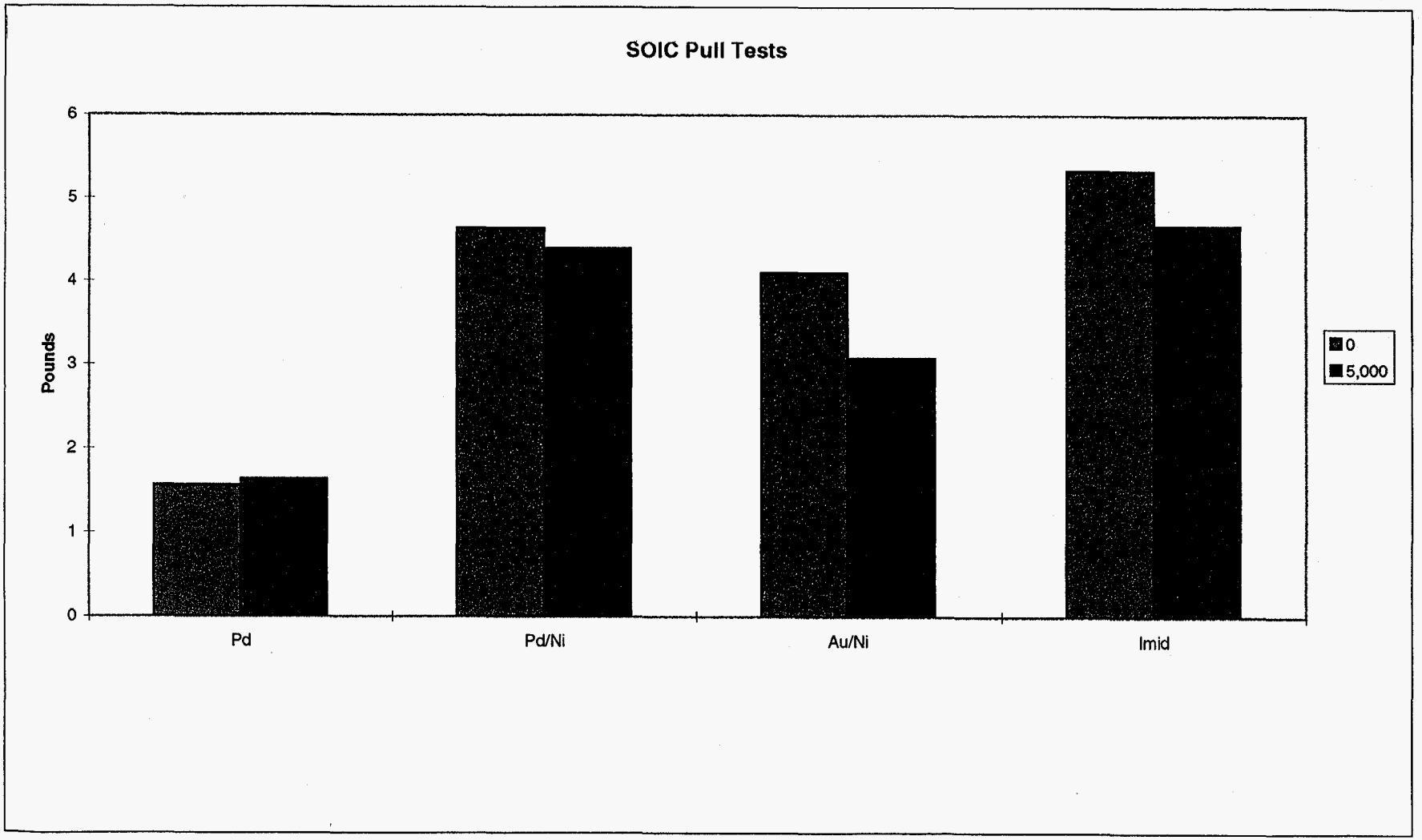


Figure 4: Mechanical pull test for 50 mil pitch SOICs before and after thermal cycling

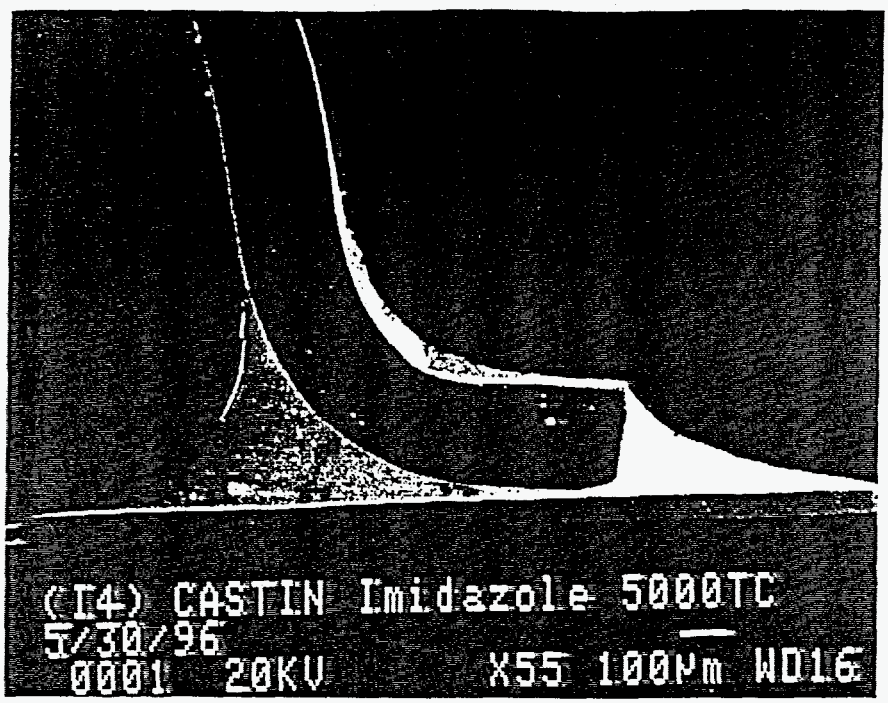


Figure 5. Scanning electron micrograph of the cross-section of a SOIC lead on a imidazole-finished PWB after 5000 thermal cycles.

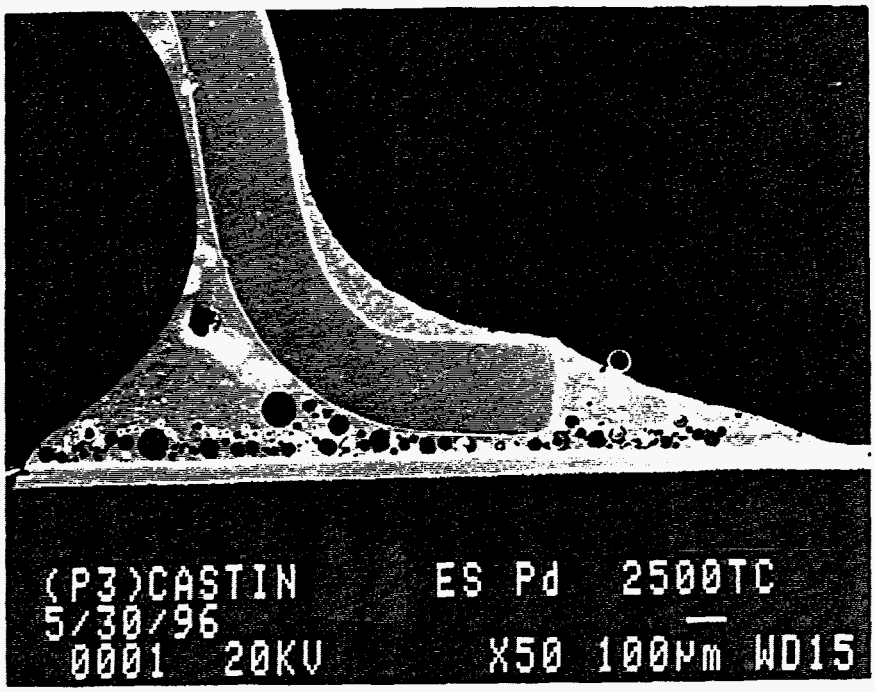


Figure 6. Scanning electron micrograph of the cross-section of a SOIC lead on a Pd-finished PWB after 2500 thermal cycles.

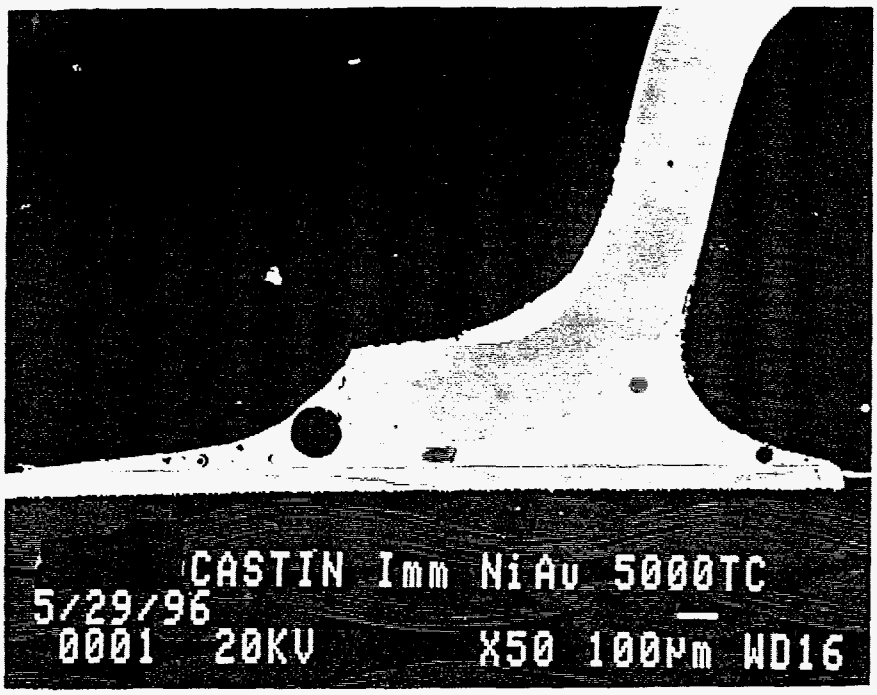


Figure 7. Scanning electron micrograph of the cross-section of a SOIC lead on a immersion Ni/Au-finished PWB after 5000 thermal cycles.

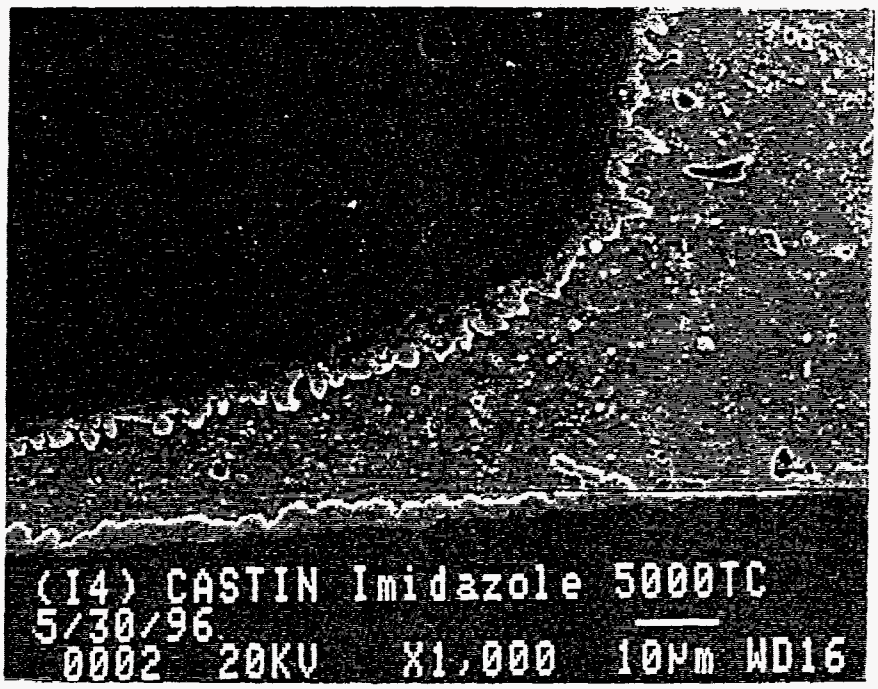


Figure 8. Secondary-electron micrograph of the cross-section of a solder joint between the SOIC lead and PWB on a imidazole-finished PWB after 5000 thermal cycles, magnified from Figure 5.

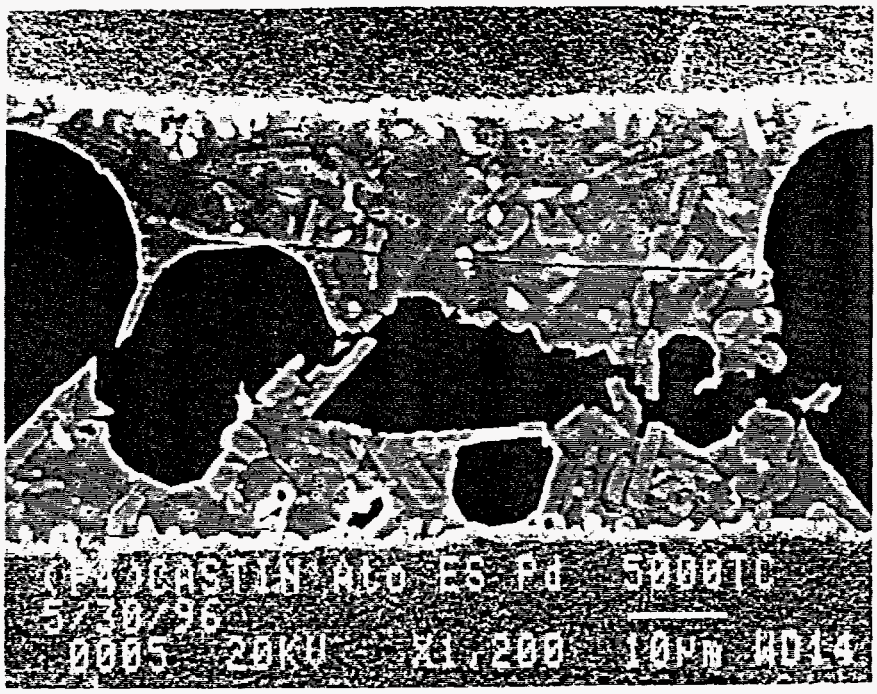


Figure 9. Secondary electron micrograph of the cross-section of a solder-joint between the SOIC lead and PWB on a Pd finished PWB after 2500 thermal cycles, magnified from figure 6.

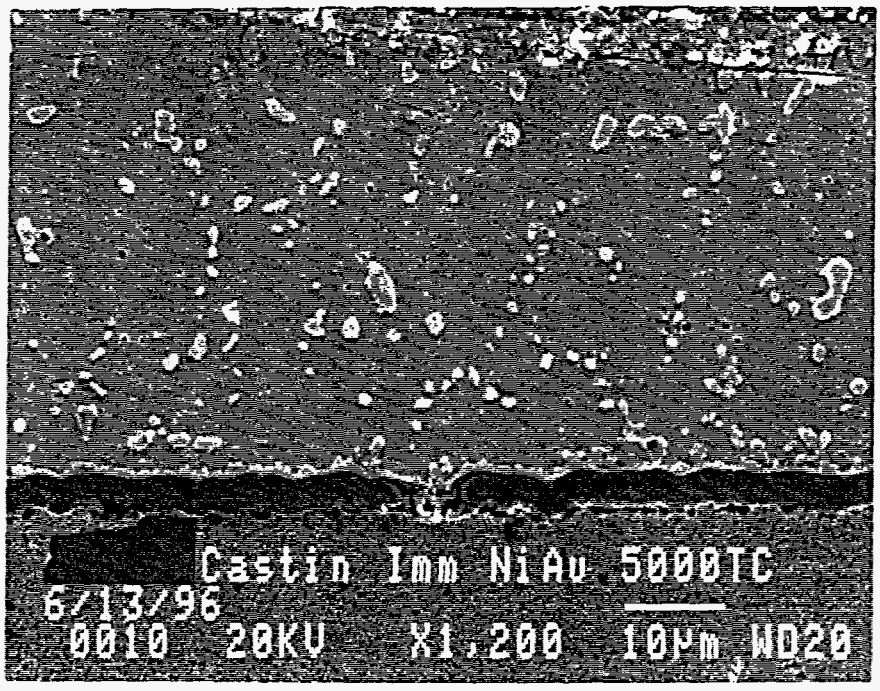


Figure 10. Secondary electron micrograph of the cross-section of a solder joint between the SOIC lead and PWB on an immersion NiAu-finished PWB after 5000 thermal cycles.