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DETERMINING TWO-PORT S-PARAMETERS FROM A ONE-PORT MEASUREMENT USING A NOVEL IMPEDANCE-STATE TEST CHIP

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Abstract- A novel custom high-speed test chip and data reduction technique that allows for the accurate determination of the two-port S-parameters of a passive network from a set of one-port measurements is presented. A typical application for this technique is high-speed integrated circuit package characterization where one-port is of a microelectronic size scale and inside the package. The test chip is designed to operate up to 20 GHz.

I. INTRODUCTION

The measurement of any passive two-port network where only one measurement port is readily accessible is a useful capability for many tasks. An ideal application of this technique and in fact the primary purpose of this work, is the determination of electrical parasitics of microelectronic packages. This need was identified based on Sandia's extensive experience in packaging test chips [1]. Measurement of package parasitics is important for high-speed integrated circuits including both analog and digital applications in both GaAs and Si technologies. In fact, in many high-speed designs, the package is part of the circuit.

Shown in Fig. 1 is a diagram of a hypothetical RF integrated circuit package. It is desired to accurately determine the two-port network extending from the Integrated Circuit (IC) bond pads to an external observation point (i.e. after a transition to a PC board as shown in Fig. 1). Ideally, this measurement should be performed in a configuration identical to actual use in order to properly account for all parasitics.

Packaging parasitics are commonly measured "direct" by using RF probes contacting points internal (with the package lid removed) and external [2]. Here, through the use of a special test chip and extraction technique, the two-port S-parameters can be accurately extracted with the package used in its intended configuration (full assembled with an IC).

This paper focuses exclusively on the problem of accurate extraction of two-port networks with non-ideal test terminations. It should be noted that in principle, the N-port problem could be similarly addressed with N/2 impedance state generators and a more generalized extraction technique similar to reference [3].

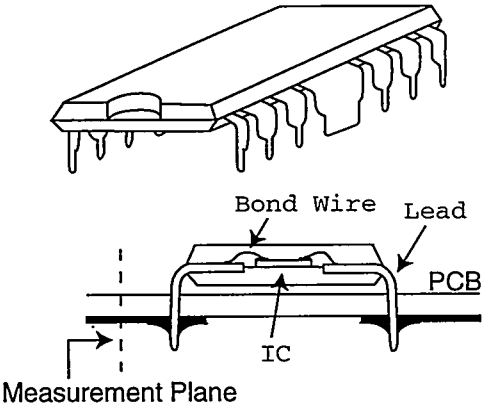

Fig. 1. Diagram of a hypothetical RF package.

II. THEORY

A block diagram of the measurement technique is shown in Fig. 2. Here, it is desired to uniquely determine the network parameters of the network, [S], by only observing the electrical reflection, Γ, at one of the network's ports. The

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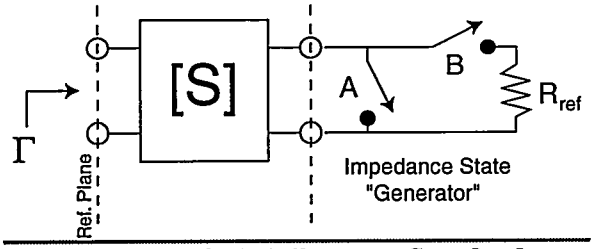
switch arrangement shown on the right of Fig. 2 represents the electrical function of the test chip. Appropriate control of the two electronic switches, presents three different impedance states to the second port of the network while measurements of Γ of the first port are performed. Since the network [S] is assumed linear, and passive, the forward and reverse transmission coefficients, S_{21} and S_{12}, are equal. Therefore, [S] is comprised of three complex unknowns and data measured with three appropriately selected standards, provides enough information to uniquely determine [S].



Switch A	Switch B	Standard
On	Off/On	"Short"
Off	Off	"Open"
Off	On	"Load"

Fig. 2. Block Diagram of the measurement technique.

The measured Γ_i with the i-th standard, $\Gamma_{s,i}$, connected to the network is:

$$\Gamma_i = S_{11} + \frac{\Gamma_{s,i} S_{21} S_{12}}{1 - S_{22}\Gamma_{s,i}} . \qquad (1)$$

Assuming three impedance states a, b, and c, with corresponding known reflection coefficients, $\Gamma_{s,a}$, $\Gamma_{s,b}$, and $\Gamma_{s,c}$, are applied successively to port 2 and the resulting port 1 reflection coefficients Γ_a, Γ_b, and Γ_c are then measured, Eq. 1 yields 3 equations with three unknowns. Solving for the network's S-parameters gives:

$$S_{11} = \frac{-\left(\Gamma_a\Gamma_b\Gamma_{s,c}\Delta_1 + \Gamma_b\Gamma_c\Gamma_{s,a}\Delta_2 + \Gamma_a\Gamma_c\Gamma_{s,b}\Delta_3\right)}{\Delta}, \qquad (2)$$

$$S_{22} = \frac{\Gamma_c\Delta_1 + \Gamma_a\Delta_2 + \Gamma_b\Delta_3}{\Delta}, \qquad (3)$$

and

$$S_{21}S_{12} = \frac{(\Gamma_a - \Gamma_b)(\Gamma_b - \Gamma_c)(\Gamma_c - \Gamma_a)\Delta_1\Delta_2\Delta_3}{\Delta^2}, \qquad (4)$$

in which

$$\Delta = \Gamma_c\Gamma_{s,c}\Delta_1 + \Gamma_a\Gamma_{s,a}\Delta_2 + \Gamma_b\Gamma_{s,b}\Delta_3, \qquad (5)$$

where

$$\Delta_1 = \Gamma_{s,a} - \Gamma_{s,b}, \qquad (6)$$

$$\Delta_2 = \Gamma_{s,b} - \Gamma_{s,c}, \qquad (7)$$

and

$$\Delta_3 = \Gamma_{s,c} - \Gamma_{s,a}. \qquad (8)$$

Inspection of Eq. 5 reveals that Δ approaches zero as any set of the port-2 impedances approach each other. Additionally, in Eqs. 2 – 4, the numerators also approach zero to allow for the correct limit of the given parameter. To avoid this singular point, the three impedance states must be spread out as far as possible in Γ-space. Thus, the standard short, open, and load conditions are targeted for the impedance-state-generator test chip. When using Eq. (4), the appropriate branch cut of the square-root function required to determine S_{21} ($= S_{12}$) must be selected to correctly determine the phase. Fortunately, in general the phase is known at DC and is a continuous function of frequency for the application explored here.

It should be noted that this technique along with the test chip discussed below is quite general. That is, it is not only applicable to packaging applications.

III. EXPERIMENT

Fig. 3 shows a microphotograph of the completed test chip fabricated with a GaAs MESFET foundry process. The control pads (0V, -3V operation) on the right-hand side of the photograph operate the switches which are comprised of depletion mode transistors (V_T=-2.2V). The ground-signal-ground RF port on the left-hand side of the photograph accesses the generated impedance states. Shown in Fig. 4 are

the measured (using on-wafer probes) Γ's with the test chip in its three impedance states ("short", "load" and "open") plotted from 0.05 to 10.05 GHz. The three states are seen to be far apart at any frequency in Γ-space for robust parameter extraction.

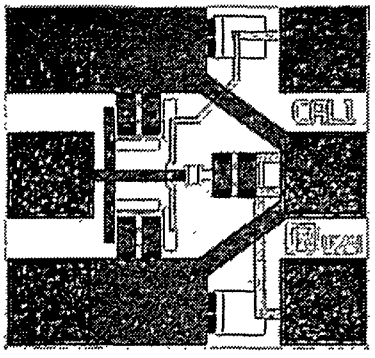


Fig. 3. Microphotograph of the impedance state generator test chip (approx. 18x16 mil^2).

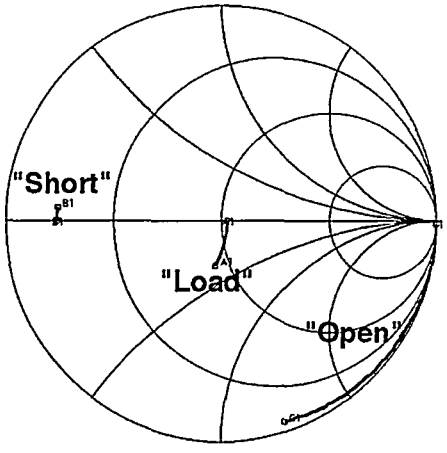


Fig. 4. Measured reflection coefficient (S_{11}) of the impedance-state generator test chip from 0.05 to 10.05 GHz.

To verify the technique, the test configuration shown in Fig. 5 was measured both "directly" and through the use of the technique described in this paper. The test configuration was selected to mimic a microelectronic package (although a rather large one). It was comprised of an RF probe, elbow adapter, and an HP85057 25 Ohm Mismatch Airline .

The S-parameters were measured directly at the 2.4-mm coaxial connections to either side of Fig. 5. An additional measurement was made for the cascade of two RF probes. The effect of one of the probes was then removed from the measurement. The resulting S-parameters accurately describe the network from the left-hand coaxial connector to the tip of the left-hand RF probe. This network is intended to be similar to a package transition from the microelectronic to real world.

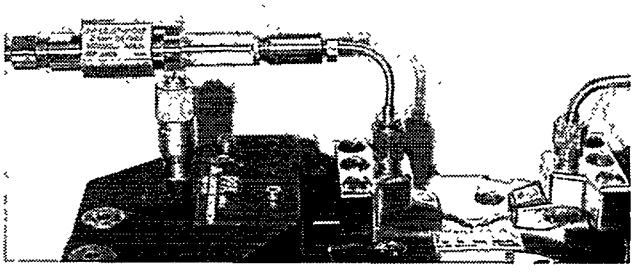


Fig. 5. Photograph of the test configuration, which simulates a packaging measurement.

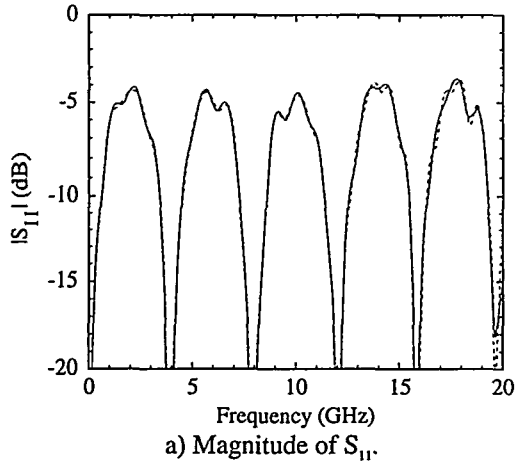
Data collection for the new technique was from the left-hand coaxial port with the impedance-state generator test chip contacted to the tips of the left-hand probe. DC probes (not shown) provided the control bias to the FET switches.

Shown in Fig. 6 and Fig. 7 are the directly measured S-parameters (dashed lines) and S-parameters measured using the technique describe here (solid lines). The data from the two techniques are for all practical purposes identical (except for some noise on the direct transmission measurement).

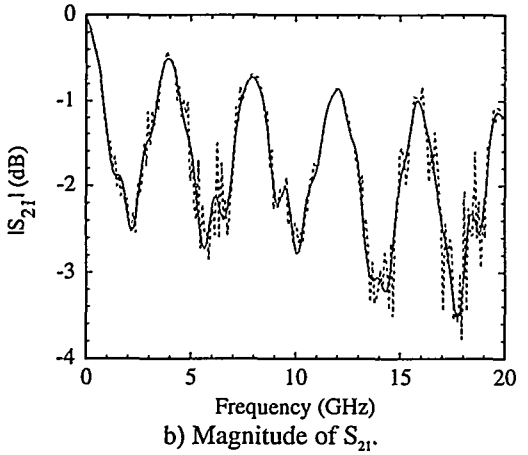
IV. CONCLUSIONS

A method for accurately determining the S-parameters of a linear, passive two-port network with access to only one-port of the network was presented. This measurement is achieved by using a special Sandia-designed test chip along with a special extraction technique. Data was presented to verify the technique. An ideal

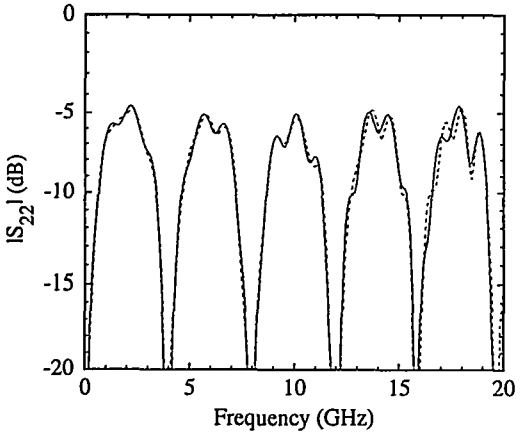
application for this approach is the measurement of parastic networks for microelectronic packages.



a) Magnitude of S_{11}.



b) Magnitude of S_{21}.



c) Magnitude of S_{22}.

Fig. 6. Comparison of the magnitudes of the S-parameters measured by a conventional (dashed lines) and new technique (solid).

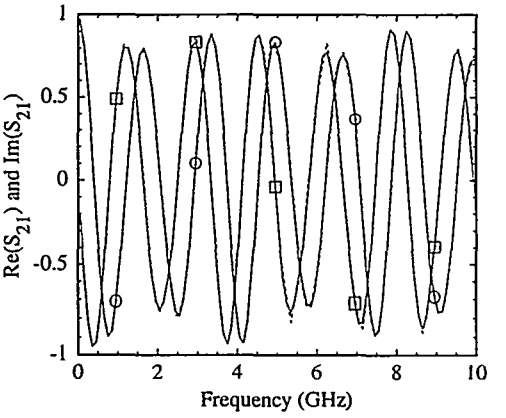


Fig. 7. Comparison of real (circles) and imaginary (squares) parts of S_{21} measured by a conventional (dashed line) and the new technique (solid line). This data demonstrates proper phase extraction.

V. ACKNOWLEDGEMENTS

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VI. REFERENCES

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