

## GaN Metal Oxide Semiconductor Field Effect Transistors

F. Ren, S. J. Pearton, C. R. Abernathy, A. Baca<sup>+</sup>, P. Cheng<sup>+</sup>, R. J. Shul<sup>+</sup>,  
S. N. G. Chu<sup>#</sup>, M. Hong<sup>#</sup>, J. R. Lothian<sup>\*</sup>, and M. J. Schurman<sup>\*\*</sup>

University of Florida, Gainesville, FL32606

<sup>+</sup>Sandia National Laboratories, Albuquerque, NM 87185

<sup>\*</sup>Bell Laboratories, Lucent Technologies, Murray Hill, NJ 07974

<sup>#</sup>Multiplex Inc., South Plainfield, NJ 87123

<sup>\*\*</sup>EMCORE Inc., Somerset, NJ 07061

RECEIVED

MAR 15 1999

OSTI

### ABSTRACT

A GaN based depletion mode metal oxide semiconductor field effect transistor (MOSFET) was demonstrated using  $\text{Ga}_2\text{O}_3(\text{Gd}_2\text{O}_3)$  as the gate dielectric. The MOS gate reverse breakdown voltage was  $> 35\text{V}$  which was significantly improved from  $17\text{V}$  of Pt Schottky gate on the same material. A maximum extrinsic transconductance of  $15\text{ mS/mm}$  was obtained at  $V_{ds} = 30\text{ V}$  and device performance was limited by the contact resistance. A unity current gain cut-off frequency,  $f_T$ , and maximum frequency of oscillation,  $f_{max}$  of  $3.1$  and  $10.3\text{ GHz}$ , respectively, were measured at  $V_{ds} = 25\text{ V}$  and  $V_{gs} = -20\text{ V}$ .

## **DISCLAIMER**

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, make any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

## **DISCLAIMER**

**Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.**

A number of GaN field effect transistors (FETs) and AlGaN/GaN heterostructure FETs have been reported showing excellent device breakdown characteristics<sup>1-5</sup>. The conventional low resistance n<sup>+</sup>-cap layer structure used to reduce parasitic resistances in GaAs technology is generally not applied in nitride devices as it is difficult to perform the gate recess step. This is due to the high chemical stability of GaN which makes wet etching very difficult except at high temperatures or under optical stimulation.<sup>6,7</sup> The drawback of dry etching for pattern transfer is the ion bombardment induced damage. This damage then causes a low gate breakdown voltage.<sup>8</sup>

These problems can be overcome by using a metal oxide semiconductor FET (MOSFET) approach of the type recently reported for GaAs and InGaAs.<sup>9,10</sup> The Ga<sub>2</sub>O<sub>3</sub>(Gd<sub>2</sub>O<sub>3</sub>) films were deposited on GaAs or InGaAs using e-beam evaporation from a single crystal of Ga<sub>2</sub>O<sub>3</sub>(Gd<sub>2</sub>O<sub>3</sub>) in an MBE chamber. As a result, both n- and p-type enhancement mode MOSFETs could be demonstrated. In this study, a similar approach has been applied to fabrication of Ga<sub>2</sub>O<sub>3</sub>(Gd<sub>2</sub>O<sub>3</sub>)/GaN devices resulting in the demonstration of the first GaN MOSFET.

The GaN layer structure was grown on c-Al<sub>2</sub>O<sub>3</sub> substrates prepared initially by HCl/HNO<sub>3</sub>/H<sub>2</sub>O cleaning and an in-situ H<sub>2</sub> bake at 1070 °C. A GaN buffer <300 Å thick was grown at 500 °C using trimethylgallium and ammonia and crystallized by ramping the temperature to 1040 °C. The same precursors were used again to grow ≥ 3 μm of undoped GaN (n < 10<sup>16</sup> cm<sup>-3</sup>) and an ~8000 Å Si-doped (n = ~3 x 10<sup>17</sup> cm<sup>-3</sup>) active layer.<sup>11</sup>

A cross-sectional view of the schematic GaN MOSFET is shown in Figure 1. Device fabrication started with isolation and achieved with Cl<sub>2</sub>/Ar dry etching in a Plasma Therm ICP system. An oxide of Ga<sub>2</sub>O<sub>3</sub>(Gd<sub>2</sub>O<sub>3</sub>) mixture was then deposited as a gate oxide using the technique similar to that previously reported for GaAs MOSFET.<sup>12</sup> Followed with oxide removal in the source and drained regions prior to the ohmic contact deposition with a HCl

solution and Ti/Al/Pt/Au was employed as the ohmic metallization. Then, the gate contact was defined with a standard photoresist lift-off process of Pt/Ti/Pt/Au.

A cross-sectional TEM of the Ga<sub>2</sub>O<sub>3</sub>(Gd<sub>2</sub>O<sub>3</sub>)/GaN is shown in Figure 2. A sharp Ga<sub>2</sub>O<sub>3</sub>(Gd<sub>2</sub>O<sub>3</sub>)/GaN interface was obtained which is consistent with our x-ray reflectivity data.<sup>13</sup> The Ga<sub>2</sub>O<sub>3</sub>(Gd<sub>2</sub>O<sub>3</sub>) is amorphous and there was no stress observed in the oxide layer. The dc characteristics of a 1.2 × 60 μm<sup>2</sup> gate dimension GaN MOSFET is shown in Figure 3. This is the first demonstration of GaN based MOSFET. A maximum extrinsic transconductance of 15 mS/mm was obtained at V<sub>ds</sub> = 30 V, which was limited by the parasitic resistance. The use of a thin and heavily doped channel (< 800 Å and > 10<sup>18</sup> cm<sup>-3</sup>) will improve both transconductance and reduce the contact resistance. The extrinsic RF characteristics of a typical GaN MOSFET is illustrated in Figure 4. The device was measured at drain and gate voltage of 25V and -20V, respectively. The unity gain cut-off frequency and maximum frequency of oscillation of 3.1 and 11.2 GHz, respectively, were achieved. The device rf performance was also limited by contact resistance and extrinsic capacitance.

In summary we have demonstrated GaN depletion mode MOSFETs and showed both dc and rf characteristics. The device performance can be improved by optimizing the layer structure using a thin and heavily doped channel layer which will reduce the contact resistance and enhance transconductance.

The authors gratefully acknowledge the U. S. Office of Naval Research under Contract No. N00014-98-1- (J. C. Zolper), and DARPA/EPRI under contract MDA972-98-1-0006 0204 (D. Ritter/J. Melcher) for support of this work. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed-Martin Company, for the U. S. Department of Energy under Contract DEAC04-95AL85000.

## References

1. P. M. Asbeck, E. T. Yu, S. S. Lau, G. J. Sullivan, J. Van Hove and J. M. Redwing, *Electron. Lett.* **33** 1230 (1997).
2. S. C. Binari, W. Kruppe, H. B. Dietrich, G. Kelner, A. E. Wickenden and J. A. Freitas, *Solid State Electron.* **41** 1549 (1997).
3. M. S. Shur, *Mat. Res. Soc. Symp. Proc.* **483** 15 (1998).
4. J. Burm, K. Chu, W. J. Schaff, L. F. Eastman, M. A. Khan, Q. Chen, J. W. Yang and M. S. Shur, *IEEE Electron. Dev. Lett.* **18** 141 (1997).
5. R. Gaska, Q. Chen, J. Yang, A. Osinsky, M. A. Khan and M. S. Shur, *IEEE Electron. Dev. Lett.* **18** 492 (1997).
6. M. S. Minsky, M. White and E. L. Hu, *Appl. Phys. Lett.*, **68** 1531 (1996).
7. C. Youtsey, I. Adesida and G. Bulman, *J. Elecgrton. Mater.* **27** 282 (1998).
8. F. Ren, J. R. Lothian, Y. K. Chen, R. Karlicek, L. Toan, M. Schurman, R. A. Stall, J. W. Lee and S. J. Pearton, *Solid State Electron.* **41** 1819 (1997).
9. F. Ren, M. Hong, J. M. Kuo, W. S. Hobson, J. R. Lothian, H. S. Tsai, J. Lin, J. P. Mannaerts, J. Kwo, S. N. G. Chu, Y. K. Chen and A. Y. Cho, 1997 IEEE GaAs IC Symposium, Anaheim, CA Oct. 12-15, 1997.
10. F. Ren, J. M. Kuo, M. Hong, W. S. Hobson, J. R. Lothian, J. Lin, H. S. Tsui, J. P. Mannaerts, J. Kwo, S. N. G. Chu, Y. K. Chen and A. Y. Cho, *IEEE Electron. Dev. Lett.* **19** 309 (1998).
11. M. J. Schurman, T. Salgaj, C. Tran, R. Karlicek, I. Ferguson, R. Stall and A. Thompson, *Mater. Sci. Eng. B*, **43** 222 (1997).
12. M. Hong, M. Passlack, J. P. Mannaerts, J. Kwo, S. N. G. Chu, N. Moriya, S. Y. Hou and V. J. Fratello, *J. Vac. Sci. Technol. B*, **14** 2297 (1996).

13. F. Ren, M. Hong, S. J. Pearton, C. R. Abernathy, J. R. Lothian, S. N. G. Chu, M. A. Marcus, M. J. Schurman, and A. Baca, App. Phys. Lett.(in press).

## Figure Captions

**Figure 1.** A cross-sectional view of GaN metal oxide semiconductor field effect transistor(MOSFET).

**Figure 2.** A cross sectional TEM of  $\text{Ga}_2\text{O}_3(\text{Gd}_2\text{O}_3)/\text{GaN}$  sample.

**Figure 3.** Drain I-V characteristics of an  $1.2 \times 60 \mu\text{m}^2$  gate dimensional GaN MOSFET.

**Figure 4.** Rf characteristics of an  $1.2 \times 60 \mu\text{m}^2$  gate dimensional GaN MOSFET measured at  $V_{ds} = 25 \text{ V}$  and  $V_{gs} = -20 \text{ V}$ .









