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Stability of Trapped Electrons in SiO_2

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Abstract

Thermally stimulated current and capacitance voltage methods are used to investigate the thermal stability of trapped electrons associated with radiation-induced trapped positive charge in metal-oxide-semiconductor capacitors. The density of deeply trapped electrons in radiation-hardened 45 nm oxides exceeds that of shallow electrons by a factor of ~ 3 after radiation exposure, and by up to a factor of 10 or more during biased annealing. Shallow electron traps anneal faster than deep traps, and seem to be at least qualitatively consistent with the model ofLelis et al. Deeper traps may be part of a fundamentally distinct dipole complex, and/or have shifted energy levels that inhibit charge exchange with the Si.

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Electron trapping near the Si/SiO_2 interface can strongly affect the response of metal-oxide-semiconductor (MOS) devices to ionizing radiation or high-field stress.[1-6] These electrons can be present at densities exceeding 10^{12} cm^{-2}, given similar amounts of trapped positive charge.[4,5] The nature of electron traps in the near-interfacial SiO_2 is unknown, although there is compelling evidence these defects are often intimately associated with trapped holes.[3-5,7,8] This relation is depicted most directly in the model of Lelis et al., which suggests trapped electrons and holes occupy opposite sides of a "compensated" E'_γ center in SiO_2.[3,8] Charge exchange between electron traps and the Si occurs over a wide range of time scales, depending on the trap energy and/or location relative to the Si/SiO_2 interface.[6,9,10]

Here we report a detailed study of the stability of trapped electrons in SiO_2. Capacitors with 45-nm oxides were irradiated with 10-keV x rays at ~ 20°C to 2.0 Mrad(SiO_2) at 1100 rad(SiO_2)/s and 10 V bias. Effective densities of shallow electron traps ΔN_{es} were estimated via high-frequency (1 MHz) capacitance-voltage (C-V) hysteresis measurements[5,11-13] at a ramp rate of ~ 0.5 V/s; all C-V data were taken at room temperature. Effective densities of more deeply trapped electrons ΔN_{ed} were estimated from thermally stimulated current (TSC) and high-frequency C-V measurements (swept from negative-to-positive bias to exclude the contribution of shallow trapped electrons[13]) via the expression:[4,10]

$$Aq\Delta N_{ed} = \Delta Q_p - C_{ox}\Delta V_{mg} . \qquad (1)$$

Here $\Delta Q_p = Aq\Delta N_p$ is the trapped positive charge obtained by integrating the TSC after correcting for parasitic leakage, $-q$ is the electronic charge, ΔN_p is the trapped positive charge density, C_{ox} is the oxide capacitance, A is the area, and ΔV_{mg} is the midgap voltage shift.[4,5] TSC measurements were performed at −12 V during a ~ 0.11°C/s ramp from ~ 20°C to 350°C.[14] To investigate the stability of the trapped charge, devices were annealed in two different ways between irradiation and TSC measurement. Isochronal anneals were performed on some devices for 0.25 h at temperatures from 20°C to 200°C.[13] Other devices were isothermally annealed for times ranging from 0.25 h to 744 h at 115°C.

Figure 1 shows ΔN_p, ΔN_{ed}, and ΔN_{es} for devices irradiated to 2 Mrad(SiO_2) and annealed at (a) 0 V or (b) –10 V for 0.25 h at temperatures ranging from 50 to 200°C before TSC measurements were performed. Data at different temperatures are for different capacitors, as each TSC measurement removed all radiation-induced charge from the devices.[14] The points at 20°C are controls for which no anneals were performed. After irradiation, the density of trapped positive charge (triangles) was 2.5 x 10^{12} cm^{-2}, the density of deeply trapped electrons (circles) was 1.3 x 10^{12} cm^{-2}, and the density of shallow trapped electrons (squares) was 0.4 x 10^{12} cm^{-2}. In Figs. 1(a) and 1(b), values of ΔN_p decrease with increasing anneal temperature as expected.[1,10] The density of shallow trapped electrons also decreases systematically with increasing temperature in each case. In contrast, in Fig. 1(a) the density of deeply trapped electrons increases by up to 13% for temperatures below 125°C, and decreases at higher temperatures. Even for negative bias anneals in Fig. 1(b), which might be expected to electrostatically expel electrons from the oxide, there is essentially no change in ΔN_{ed} until the temperature exceeds 100°C. The stability of the deeply trapped electrons during these negative bias anneals is significant and surprising.

Figure 2 investigates the stability of the trapped charge for (a) 0 V and (b) –10 V isothermal annealing at 115°C. Here the trapped positive charge (triangles) and the shallow trapped electron densities (squares) decrease with increasing anneal time at either bias. For the 0 V anneal in Fig. 2(a), the density of deeply trapped electrons (circles) increases for times less than 1.5 h, and decreases for longer times. For the –10 V anneal in Fig. 2(b), the value of ΔN_{ed} is unchanged for times up to 1.5 h, and decreases for longer annealing times. Note that longer annealing times at negative bias more efficiently remove deeply trapped electrons than annealing at 0 V (or positive[10,13]) bias. In Fig. 2(a), both ΔN_p and ΔN_{ed} are $\approx$ 0.7 x 10^{12} cm^{-2} after a 744 h (31 day) anneal at 0 V, but in Fig. 2(b) $\Delta N_p \approx 0.5$ x 10^{12} cm^{-2} and $\Delta N_{ed} \approx$ 0.15 x 10^{12} cm^{-2} after similar anneals at –10 V.

In Fig. 3 we compare the relative stability of shallow and deeply trapped electrons during (a) isochronal and (b) isothermal anneals. In each case, the data are normalized to postirradiation values. For the isochronal anneals in Fig. 3(a), the greatest stability is exhibited by deeply trapped electrons during 0 V

anneal (solid squares), with the next greatest by the deeply trapped electrons during –10 V anneal (open squares). The stability of the shallow electrons during –10 V (open circles) or 0 V (solid circles) anneals is similar, and less than the deeply trapped electrons in either case. At 100°C, for example, the values of ΔN_{ed} for 0 V and –10 V anneals in Fig. 3(a) are essentially equal to postirradiation levels. On the other hand, values of ΔN_{es} are ~ 30 % lower than postirradiation levels. The annealing response of the radiation induced defects in Fig. 3(a) may differ from that of the high-field-stress induced defects studied by Bhat and Saraswat,[11] who observed no temperature dependence of C-V hysteresis in their devices for measuring temperatures between 20°C and 200°C. (Recall that all C-V measurements are performed at room temperature here.) For the isothermal anneals in Fig. 3(b), the overall trends are similar to Fig. 3(a). The deeply trapped electrons at 0 V bias (solid squares) exhibit the greatest stability, and the shallow electrons at 0 V (solid circles) exhibit the least stability.

In previous studies the density of shallow trapped electrons estimated via C-V hysteresis has been observed to (1) increase logarithmically with increasing voltage ramp time,[12] (2) be relatively independent of measuring temperature,[11] and (3) exhibit a similar time-dependent buildup for postirradiation room-temperature storage similar to that of E'_{γ} centers.[15] These behaviors are consistent with expectations derived from the model of Lelis and co-workers, based on the reversible tunnel exchange of electrons between the Si and a shallow electron trap site on the Si atom opposing the Si that holds the trapped hole.[3,16] Hence, it is reasonable that the shallow trapped electrons are associated with defects that are at least qualitatively similar in nature to those envisioned by Lelis et al. This presumes that only an O vacancy separates the trapped positive and negative charge, and that the trapped electron is at a position and energy level that facilitates exchange with the Si on the time scale of the C-V measurements.

The more deeply trapped electrons are present after irradiation at densities that exceed those of the shallower traps in this study by a factor of ~ 3 after irradiation, and by as much as a factor of 10 or more during annealing. Looking at Figs. 1 and 2, the stability of these deeply trapped electrons is comparable to that of the trapped positive charge. Indeed, for the 0 V anneals in Figs. 1(a) and 2(a), it appears that

trapped positive and deeply trapped negative charge are removed at roughly the same rates at higher temperatures and/or longer annealing times. This suggests that a large percentage of the oxide-trap charge in these devices consists of dipole complexes that are highly stable at room temperature. Thus, the deeply trapped electrons appear to be associated with defect or impurity levels that do not communicate readily with either the Si or the trapped positive charge. An obvious candidate for an impurity related center that might serve as an electron trap is a hydrogen complex near the Si/SiO_2 interface.[17-20] Whatever the microstructure of this center, during negative bias TSC measurements it releases charge that transports across the oxide. So the positive side of the dipole is either simply a trapped hole, or else it is a defect that releases mobile positive charge when the device is baked to high temperature at large negative bias. The negative charge associated with this center returns to the Si only when the positive charge is released.

Because a border trap is defined as a near-interfacial oxide trap that exchanges charge with the Si,[10] it is clear that most compensating electrons in these devices are stably trapped electrons (at least at room temperature), and so do *not* lie in border traps. This contrasts with the shallow electron traps measured via C-V hysteresis, which have been identified as "slow" border traps in previous studies,[15,17] and with still faster border traps[7,9,10,12,17] that can be mistaken for interface traps. This emphasizes the wide range of time constants with which electrons can be exchanged with defects in the near-interfacial SiO_2 in the presence of trapped positive charge, and highlights the need to characterize the role of these defects in device performance and long-term reliability.

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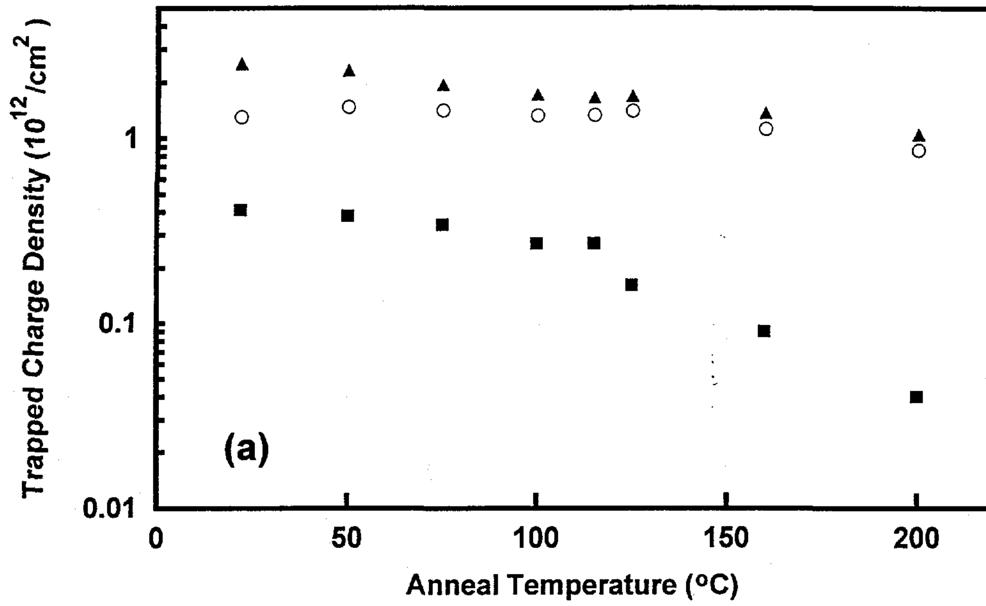
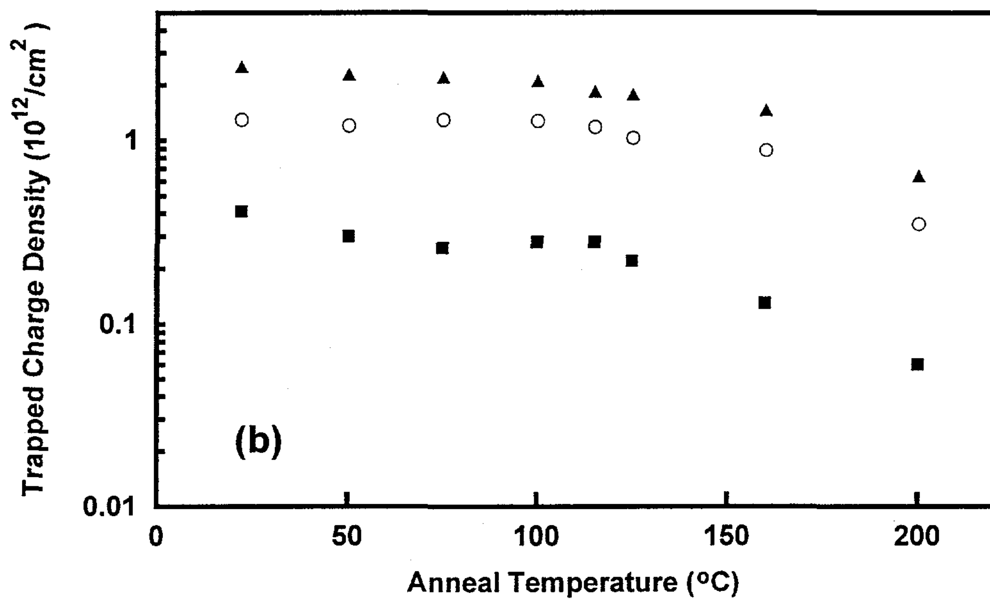
Figure Captions

Figure 1. Trapped-positive-charge (triangles), deep trapped-electron (circles), and shallow-trapped electron (squares) densities following 0.25 h anneals at (a) 0 V and (b) –10 V after radiation exposure to 2 Mrad(SiO_2) at 10 V for 0.0053 cm^2 capacitors with 45-nm radiation-hardened oxides.

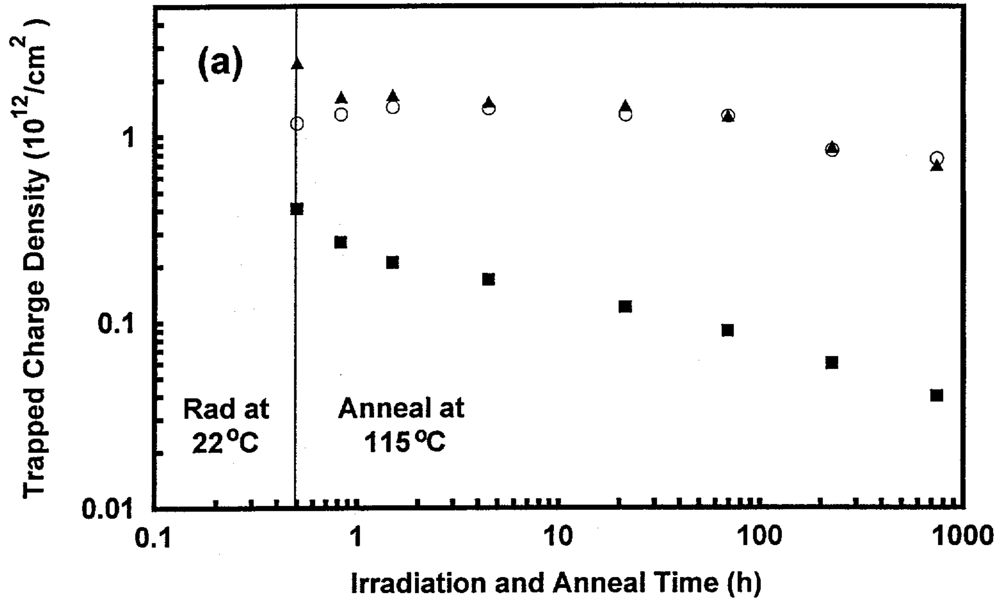
Figure 2. Trapped-positive-charge (triangles), deep trapped-electron (circles), and shallow-trapped electron (squares) densities as a function of anneal time at 115°C at (a) 0 V and (b) –10 V following radiation exposure to 2 Mrad(SiO_2) at 10 V for 0.0053 cm^2 capacitors with 45-nm radiation-hardened oxides.

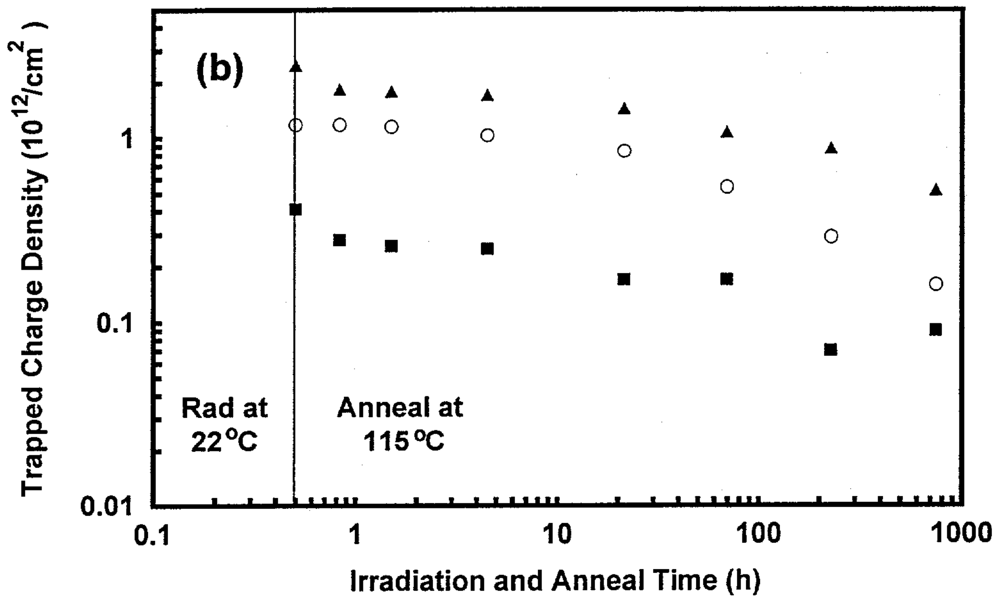
Figure 3. Densities of deep (squares) and shallow (circles) trapped electrons for 0 V (solid symbols) and –10 V (open symbols) (a) 0.25 h isochronal or (b) 115°C isothermal anneals following radiation exposure to 2 Mrad(SiO_2) at 10 V for 0.0053 cm^2 capacitors with 45-nm radiation-hardened oxides.



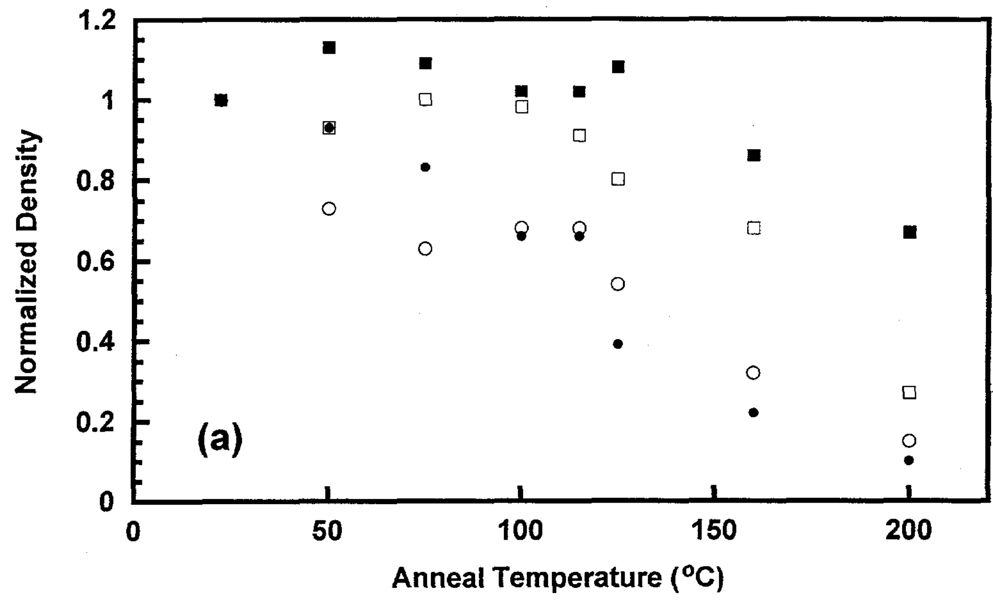


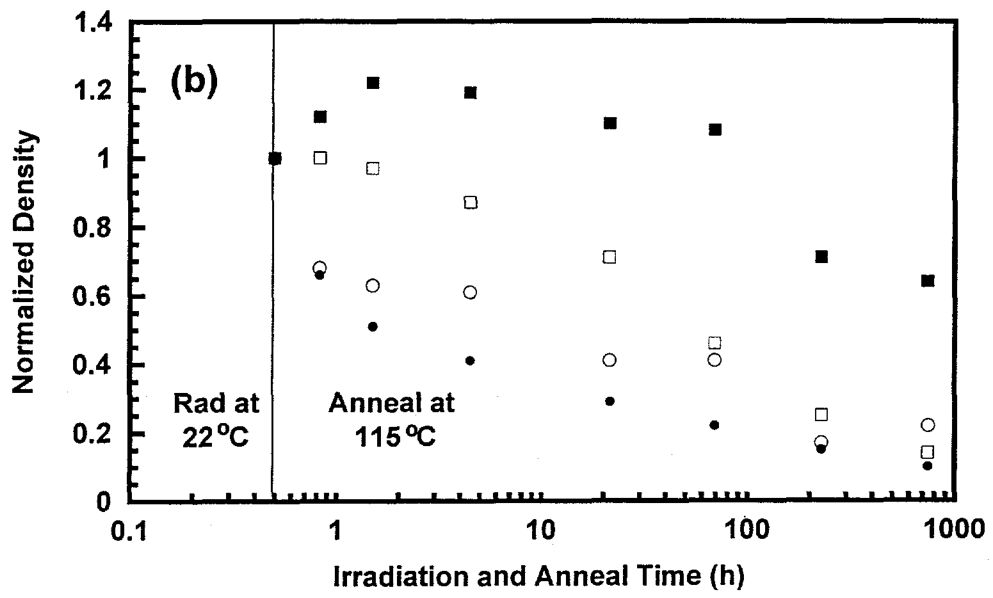
Fleetwood, APL Fig. 1





Fleetwood, APL. Fig. 2





Fleetwood, APL, Fig. 3