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Calculation and Validation of Thermomechanical Stresses in Flip Chip BGA Using the ATC4.2 Test Vehicle*

David W. Peterson, Steven N. Burchett, James N. Sweet and Robert T. Mitchell
Sandia National Laboratories
PO Box 5800
Albuquerque, NM 87185-1082

Luu Nguyen
National Semiconductor
PO Box 58090
Santa Clara, CA 95052

Abstract

We report the first *in situ* measurements of thermomechanical stresses in a 1000 I/O 250 μm pitch piezoresistive flip chip test chip assembled to a 755 I/O 1.0 mm pitch 35 mm Ball Grid Array (BGA). The BGA substrates employed "build-up" dielectric layers containing micro-vias over conventional fiberglass laminate cores. Experimental data, which include *in situ* stress and die bending measurements, were correlated to closed form and Finite Element Method (FEM) calculations. Cracking and delamination were observed in some of the experimental groups undergoing temperature cycling. Through use of bounding conditions in the FEM simulations, these failures were associated with debonding of the underfill fillet from the die edge that caused stresses to shift to weaker areas of the package.

Introduction

This work focuses on thermomechanical stresses present in a flip chip test vehicle that was designed to meet the 1997 NTRS flip chip substrate requirement in the cost-performance category. This requirement calls for a 12 mm die with 900-1000 I/O on 250 μm pitch on a 35 mm Ball Grid Array (BGA) substrate with 600-700 I/O on 1.0 mm pitch. The actual test vehicle used the 11.56 mm ATC04 piezoresistor test chip repatterned to a 1004 bump area array (making it an ATC4.2) assembled to a 35 mm BGA substrate with 755 I/O. The experimental approach follows that of earlier work with the ATC4.1 test vehicle which examined thermomechanical stresses in flip chip on board (FCOB) [1]. Independent measurements of die curvature and *in situ* stress were used to validate and refine analytical and FEM calculations of deflection and stress. The latter were also mutually independent in the sense that analytical results were based on direct measurements of CTE and bending modulus on coupons and FEM calculations were based on data sheet properties of the constitutive elements of each assembly.

Experimental

Test Vehicle

The ATC4.2 Flip Chip Test Chip is a redistributed area array version of the ATC04 Assembly Test Chip that is 11.56 mm on an edge and contains 100 addressable stress sensing cells, ring oscillators, and heaters described in detail elsewhere [2]. The area array consists of 1004 eutectic solder bumps applied by two suppliers (Bmp1 and Bmp2) with slightly different bump technologies, although both used BCB (benzocyclobutene) for dielectric and Cu for interconnect layers. Due to a design incompatibility only one of two bump suppliers (Bmp2) furnished die capable of providing stress measurements.

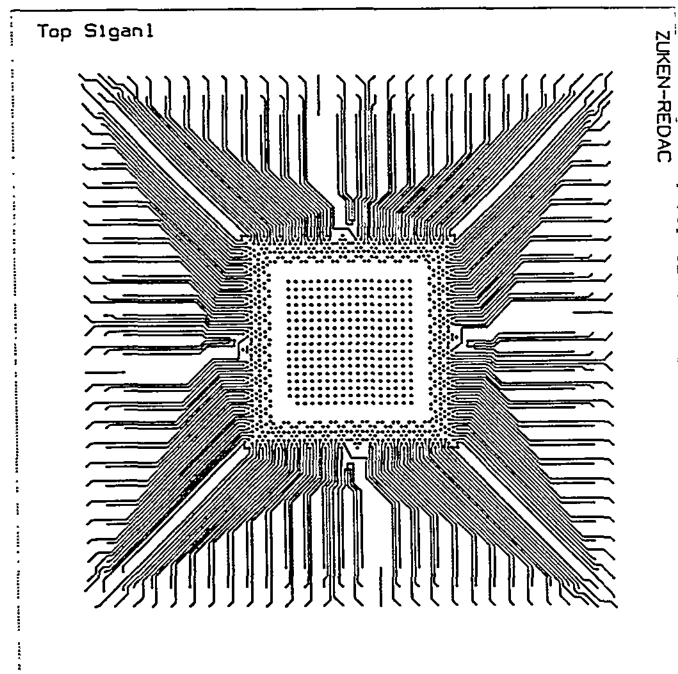

Fig. 1. Top layer die pad layout and outer row escape routing of the Zuken-Redac layout of the 35 mm ATC4.2 BGA substrate. Flip chip pads for the 1004 I/O 250 μm pitch die are in the center. The BGA array on the bottom contains 755 solder balls on 1.0 mm pitch.

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The BGA substrate design incorporates three perimeter rows of off-grid die pads on 250 μm pitch using a "clamshell" technique first described by Gasparini and Bhattacharyya maximizing escape routing of an area array with a minimum number of layers [3]. The actual layout was furnished by Zuken-Redac as part of a voluntary contribution to this work. The first layer die pad layout and escape routing for this design is shown in Fig. 1.

The Zuken-Redac design was used by two suppliers of PC boards to fabricate BGA substrates, SubA and SubB, shown in cross-section in Figs. 2 and 3. Both use fiberglass reinforced cores and epoxy build-up (B/U) layers containing microvias for layer-to-layer interconnection. SubA has a thinner core and uses three B/U layers and SubB has a thicker core with two B/U layers.

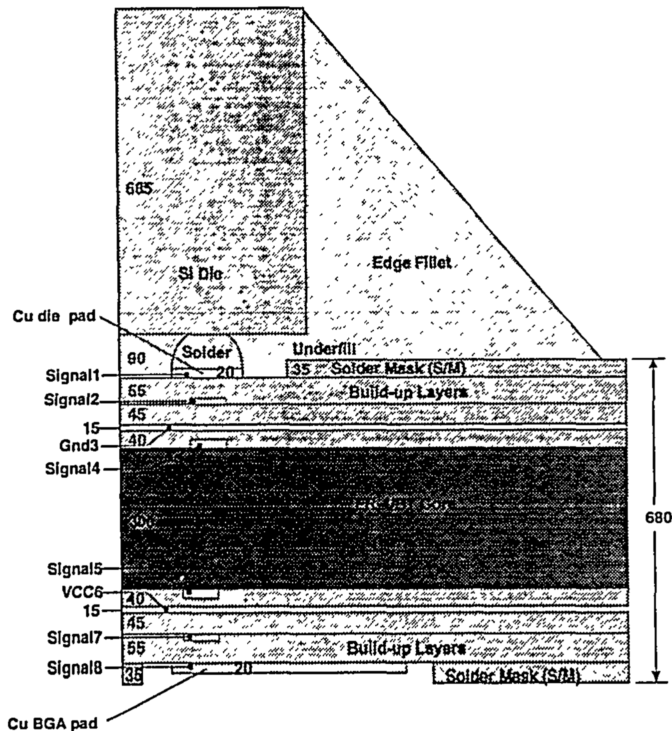

Fig. 2. Cross-section of SubA with thickness dimensions in microns.

TABLE I
Material Properties used in FEM calculations

	E (GPa)	Tg (°C)	α1 (10^{-6}/°C)	α2 (10^{-6}/°C)	υ
Silicon	120	n/a	2.6	n/a	0.34
Copper	107.6	n/a	16.1	n/a	0.334
UF1	5.8	145	40	unk	0.3
UF2	8.5	140	26	87	0.3
UF3	11	125	31	89	0.3
Solder Mask A	0.25	105	60	160	0.25
Solder Mask B	5.8	132	49	120	0.25
Build-upA	5.8	190	70	n/a	0.3
Build-upB	3.1	119	78	176	0.3
CoreA	2.45	190	14	n/a	0.2
CoreB	16.4	170	14.7	unk	0.2

Table I contains the test vehicle material properties used in the FEM analysis. The properties for Si are averages of the minimum and maximum anisotropic values in the [100] and [110] directions. Underfill and substrate properties were obtained from the respective vendors. Analytical calculations used properties contained in Table II that were derived from direct measurements of CTE and bending modulus on bare coupons.

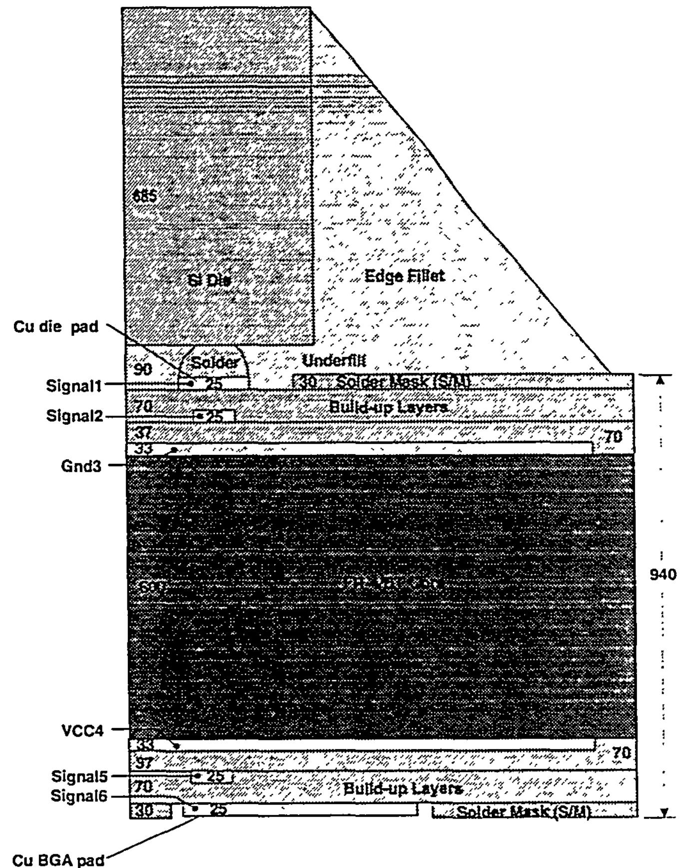

Fig. 3. Cross-section of SubB with thickness dimensions in microns.

TABLE II
Laminate properties used in analytical calculations

	E (GPa)	α (10^{-6}/°C)	υ	Thickness (μm)
SubA	8.8	21.8	0.25	680
SubB	10.9	19.3	0.25	940

Experimental Procedure

ATC4.2 die solder bumped by two bump suppliers, Bmp1 and Bmp2, were flip chip assembled to SubA and SubB substrates using three underfills, UF1, UF2, and UF3. Celestica performed flip chip assembly including attachment and coining of eutectic solder balls on the BGA side. Bmp1 die were assembled to both substrate splits but Bmp2 die were only assembled to SubA splits. This resulted in a total of 9 experimental legs (see Table III). Since Bmp2 die were assembled only to SubA substrates, *in situ* stress data were only available for parts in this leg. Assemblies were classified

as Level 3 moisture sensitive at National Semiconductor using Test Method A112-A of EIA/JEDEC Standard 22. All parts in the 9 experimental legs underwent Level 3 moisture preconditioning and temperature cycling (T/C) from –45 to +125 °C. Electrical tests and C-mode Scanning Acoustic Microscopy (C-SAM) inspection were performed at 0, 100, 200, 300, 500 and 1500 T/C intervals, and are continuing to failure at publication. Electrical tests included 4-point resistance measurements of corner solder balls, microvias and van der Pauw sheet resistance structures, daisy chain continuity and piezoresistor measurements. C-SAM images of the underfill interface were used to detect and monitor failures in the die-to-substrate interface.

TABLE III
Splits in the experimental matrix

Split	Solder bump supplier	Substrate supplier	Underfill supplier
1	Bmp1	SubA	UF1
2	Bmp1	SubA	UF2
3	Bmp1	SubA	UF3
4	Bmp1	SubB	UF1
5	Bmp1	SubB	UF2
6	Bmp1	SubB	UF3
7	Bmp2	SubA	UF1
8	Bmp2	SubA	UF2
9	Bmp2	SubA	UF3

Deflection Measurements

Die curvature at room temperature were measured along the x-axis and y-axis of the die backside using a Mahr S8P profilometer with a Focodyn laser stylus. Parts were aligned in a machined fixture to ensure repeatable measurements along the die centerline in both directions. Data were collected along a 10 mm path straddling the geometric die center and vertical deflections were calculated for a 7.14 mm segment of this path. The average of the x and y deflection measurements were calculated for each part. Table IV contains measurements taken at the 200 T/C inspection interval.

TABLE IV
Measurements of die curvature over a 7.14 mm arc

Experimental Split (Nr. parts)	Average Deflection (μm)	Standard Deviation (μm)
Bmp1/SubA/UF1 (9)	9.1	0.2
Bmp1/SubA/UF2 (9)	8.5	0.1
Bmp1/SubA/UF3 (9)	9.0	0.1
Bmp1/SubB/UF1 (9)	8.0	0.2
Bmp1/SubB/UF2 (9)	8.0	0.1
Bmp1/SubB/UF3 (9)	8.1	0.1
Bmp2/SubA/UF1 (4)	8.7	0.1
Bmp2/SubA/UF2 (4)	8.4	0.2
Bmp2/SubA/UF3 (4)	8.7	0.2

Experimental Stress Measurements

The second independent measure of die stress was based on piezoresistor data from 100 rosettes distributed across each ATC4.2 die. Piezoresistors formed on CMOS [100] are sensitive to in-plane compressive and shear components of the stress tensor but cannot detect out-of-plane components that are generally of the most interest in terms of packaging reliability. However, the in-plane data can be used to validate in-plane results from analytical and FEM calculations and, by inference, out-of-plane predictions. These data will be presented in the Discussion section where we compare experimental, analytical and FEM results.

2D Stress Analysis

Radius of curvature and the distribution of in and out-of-plane stresses were estimated using the tri-material form of Suhir's model described in [4] with improvements for out-of-plane shear and peel stress calculation in [5]. Although this model does not take into account the effect of the flip chip edge fillet, it provides a good prediction of stress maximums and die deflection. Die and underfill properties were taken from Table I and substrate properties from Table II. Radius of curvature data were converted to die deflections over a 7.14 mm arc so that they could be more easily compared to measured deflections. These results are contained in Table V. Analytical and FEM calculations are very dependent on estimations of the stress-free temperature. For this work, it was assumed to be the Tg of the underfill listed in Table I, so that $\Delta T = Tg - 25$ °C.

TABLE V
Calculations of maximum σ_{yy}, σ_{zz}, and τ_{yz} and radius of curvature converted to die deflection from Suhir. Maximum σ_{yy} is located at die center, maximum σ_{zz} and τ_{yz} are at die edge.

Experimental Split	σ_{yy} max (Mpa)	σ_{zz} max (Mpa)	τ_{yz} max (Mpa)	Deflection (μm)
SubA/UF1	-108	7.3	17.5	9.3
SubA/UF2	-102	6.2	16.9	8.8
SubA/UF3	-93	4.9	16.8	8.0
SubB/UF1	-104	-0.01	15.6	8.9
SubB/UF2	-98	-0.3	15.1	8.5
SubB/UF3	-88	-.3	14.9	7.6

3D Stress Analysis

The 3D FEM was applied to a quarter section model of the BGA assembly to predict the stress, strain and deformation response due to the cool down from the underfill cure step. For this analysis we assume the stress-free temperature to be the cure temperature of the underfill (160 °C). The viscoelastic model used for polymer materials take into account the Tg of the materials in calculating stress. The model specifically accounts for each layer in the substrate and includes the edge fillet but neglects the 251 solder balls in the underfill region. To capture the stress distributions, the model size was greater than 500,000 elements. These simulations were performed using the Sandia quasi-static analysis code JAS3D on six parallel processors of a DEC-8400.

Table VI contains stress maximums for the components σ_{yy}, σ_{zz}, and τ_{yz} along the centerline half-length of the die surface and die deflections over a 7.14 mm arc to facilitate

comparison to curvature measurements. These calculations were done for the three SubB underfill splits and included one for UF2 that neglected the fillet. The latter experienced problems with numerical oscillations in the last few elements approaching the die edge, so the σzz and τyz maximums, which occur at tehe edge, are correct in sign but uncertain in magnitude. Recalculation of the no-fillet case along with calculation of the remaining SubA cases are ongoing at the time of printing.

TABLE VI
FEM calculations of maximum σyy, σzz, and τyz along the centerline half-length of the die surface and deflection over a 7.14 mm arc. Maximum σyy is located at die center, maximum σzz and τyz are at die edge. (NF stands for no edge fillet.)

Experimental Split	σyy max (Mpa)	σzz max (Mpa)	τyz max (Mpa)	Deflection (μm)
SubB/UF1	-103	-24	24	9.3
SubB/UF2	-101	-15	21	9.1
SubB/UF3	-102	-28	27	9.0
SubB/UF2/NF[1]	-101	33	17	9.1

[1]Although the sign and general shape of the "no fillet" data appear correct, the maximums are questionable due to numerical oscillations in the last few elements approaching the die edge.

Results/Discussion

Correlation of Stress Analysis Methods

There are two relatively simple methods for estimating thermal stress in a CMOS die flip chip attached to an organic substrate: backside deflection and *in situ* stress measurement. The former is easy but prone to experimental error and misinterpretation., In CMOS technology, the latter can not sense the stress components of most interest. Both are useful when comparing relative *differences* in stress that are anticipated in material "A" vs. "B" types of experiments, and both can be used to increase confidence in the results of analytical and FEM calculations.

Fig. 4 contains measurements of backside deflection taken after 200 T/Cs plotted in a normal probability distribution for each of the substrate and underfill experimental splits. (These data are averaged in Table IV.) It can be deduced from these data that SubB imposes less stress on the die than SubA. This correlates with analytical estimates in Table V and FEM estimates in Table VI. However, the effect of underfill apparent in the analytical and FEM estimates does not appear in Fig. 4. Small differences in curvature due to underfill appear to be hidden in larger part-to-part statistical variance in curvature (and stress). Given that assumption, the SubA/UF2 data stand out. We associate this with edge delamination in all parts in this group during the course of temperature cycling. Edge delamination will be discussed in more detail below.

2D Analytical methods for calculating thermal stress in a flip chip package often assume, among other things, one infinite dimension in the x-y plane, constant radius of curvature through the z-axis, no edge fillet, and are limited to stress distributions along the finite axis in the x-y plane. Stress maximums, die deflection, and stress distributions in the interior region of the uniformly deflected (constant radius of curvature in x-y plane) die can be quite accurate if the calculations are based on reliable material property data.

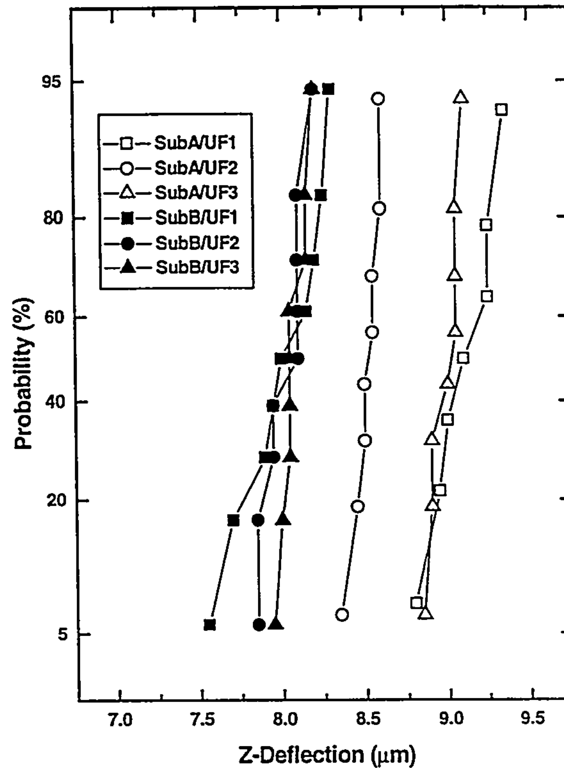

Fig. 4. Normal probability plot of die backside deflection measurements after 200 T/C for three underfills and two substrates. Open symbols are data from SubA split and filled symbols are data from SubB. Displacement of the SubA/UF2 distribution is associated with edge delaminations present in all parts of this group.

3D FEM calculations are also highly dependent on reliable property data. Since the FEM specifically models each layer in the substrate, the resulting calculations are based on material properties of uncertain accuracy for each layer from numerous sources. Drastically different elastic moduli for the two core materials and solder masks in Table I, for example, seem questionable, but had to be accepted ultimately when verified by both sources.

FEM calculations in Table VI show a spread across the three SubB underfill splits of 3% in σyy max and die deflection in contrast to analytical calculations in Table V that show spreads greater than 17% for the same predictions. The measured die deflections for the same group varied by less than 2% suggesting that the FEM is doing better at capturing the effect of underfill. FEM results show greatest sensitivity to underfill in maximum σzz, which varies 86% UF2→UF3.

In order of increasing deflection, both FEM and analytical results rank the underfills: UF3→UF2→UF1. Analytical maximum σyy and τyz follow the same order, but the FEM order is UF2→UF3→UF1 for σyy, and UF2→UF1→UF3 for σzz, and τyz. Interestingly, both *in situ* data based on a small split of Bmp2/SubA parts and the underfill "stress intensity

factor" ranking of (E)x(ΔT)x(CTE) show the order UF2→UF1→UF3 (although it's for σ*yy* in the *in situ* case).

In-plane compressive stress along the *y*-axis of the die surface centerline is measurable with CMOS piezoresistors and can be estimated with analytical methods, making it a suitable quantity for comparison of stress analysis methods. Fig. 5 contains a plot of σyy along the normalized half-length and includes typical ATC4.2 measurement data of SubA/UF2 parts starting at baseline and continuing through the first 200 T/Cs (–45 to +125 °C). These data are overlaid with curves representing the analytical and FEM calculations for SubB/UF2. (SubA FEM calculations were not available at time of publication.) The Suhir stress diminishes to zero at the edge in accordance with classical bending theory but the FEM curve stops short due to the edge fillet. The two calculations match within 3% in the die center region of constant stress for UF1 and UF2, but is 16% different for UF3. This is likely due to the unusually low Tg and thus ΔT used for the analytical calculation. FEM used the same Tg but included the effects of α2 between cure temperature and Tg.

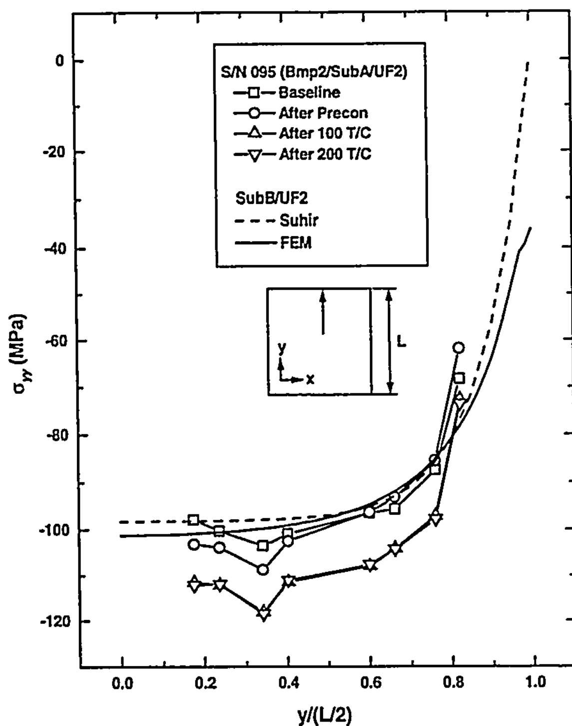

Fig. 5. Plot of σ*yy* distribution (compressive stress on the *y*-plane in the *y*-direction) along the normalized centerline half-length of the die surface. Symbols denote experimental data for a part in Bmp2/SubA/UF2 split. Dotted line is Suhir calculation that neglects edge fillet effects and dashed line is from FEM that includes edge fillet. (The latter two curves are based on SubB as SubA calculations were unavailable.)

The experimental data in Fig. 5 contains two anomalies present in all the *in situ* measurements. First are kink(s) which are known from previous work [1] to be due to stress gradients surrounding solder balls that are in varying proximities to the piezoresistor rosettes. Second is a trend toward increasing stress that appears to end at some point around the first 100 T/Cs for which we offer no explanation at this time.

Thermal Stress Damage

Three kinds of early damage were observed during the course of temperature cycling: die cracking, edge delamination, and radial fillet cracking. Die cracks start at the die edge under the edge fillet and proceed in the die plane emerging somewhere on the inverted die surface. These cracks are not visible on the outside of the package and can only be detected with C-SAM. Fig. 6 contains a C-SAM image of a typical cracked die. Cracking was only observed in the SubA splits for UF1 and UF3. This correlates to greater stress on SubA/UF1 and SubA/UF3 die and less stress on SubA/UF2 die suggested by deflection distributions in Fig. 4.

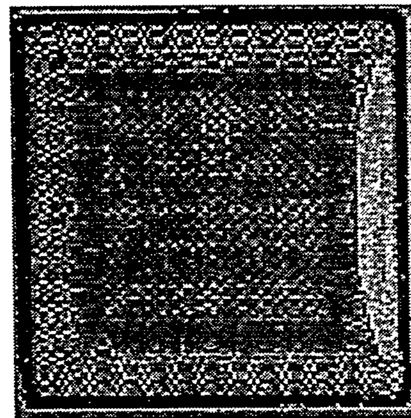

Fig. 6. C-SAM reflection image of part S/N 018 in split Bmp1/SubA/UF1 after 100 T/C showing initial detection of die cracking.

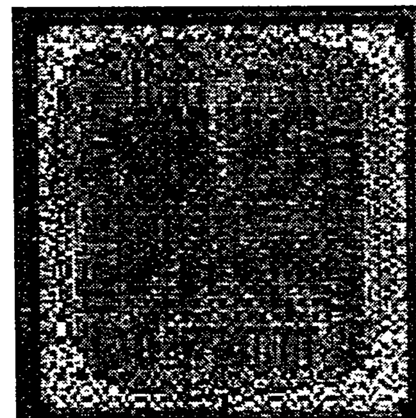

Fig. 7. C-SAM reflection image of part S/N 032 in split Bmp1/SubA/UF2 after 200 T/C showing delamination of the underfill to die surface interface. All parts in this leg showed similar delaminations.

Significant edge delamination occurred in all 9 parts in the Bmp1/SubA/UF2 split. Fig. 7 contains a C-SAM image of one part in this group taken at the 200 T/C off-line testing interval. A low voltage SEM inspection of this part showed debonding of the edge fillet around the entire perimeter. (See Fig. 8) It is assumed that the remaining parts in this split contain similar

debonding. The Bmp1/SubB/UF2 split, which is identical to this split in every way except for substrate, exhibits minor edge delamination in 2 of 9 parts. The Bmp2/SubA/UF2 split, which is identical except for the solder bump supplier (die are from another wafer lot), also shows minor edge delamination in 2 of 4 parts.

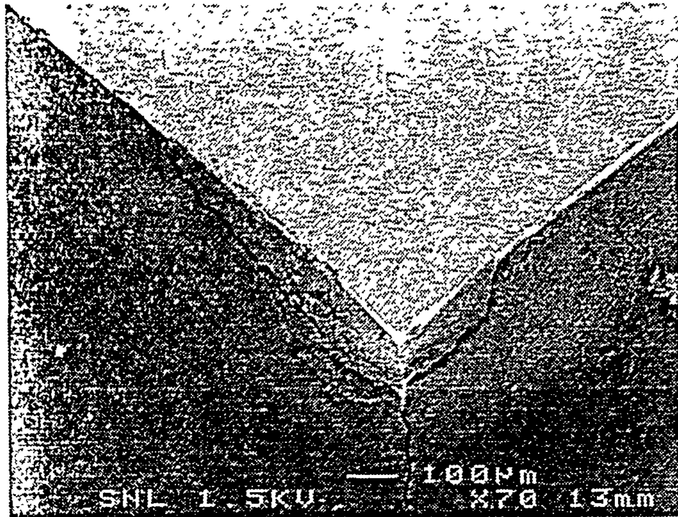

Fig. 8. SEM micrograph of S/N 032 from Bmp1/SubA/UF2 split after 200 T/Cs showing debonding and radial cracking of the edge fillet typical of parts in this group. Debonded region is continuous around the die perimeter.

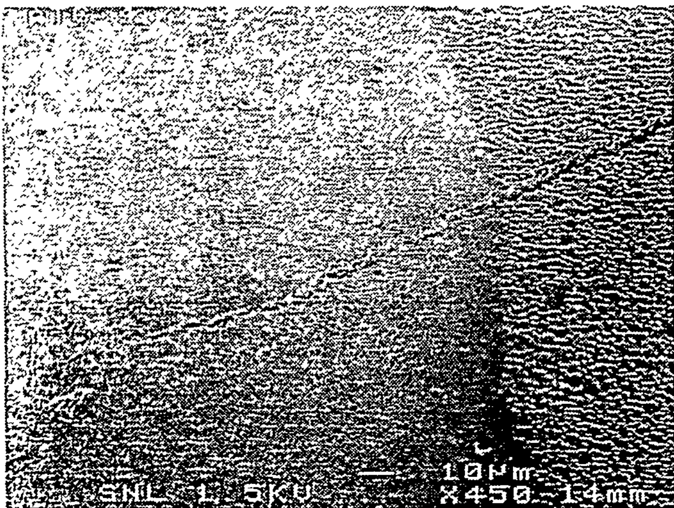

Fig. 9. SEM micrograph of S/N 032 from Bmp1/SubA/UF2 split after 200 T/Cs showing continuation of the radial crack shown in Fig. 8 from the edge fillet on the right into the solder mask and possibly the build-up dielectric on the left.

The third early damage mechanism observed is radial crack propagation from die corners through the underfill edge fillet and into the substrate. This was evident in every corner of every part in the SubA groups during the course of temperature cycling. The SEM micrograph in Fig. 9 shows the radial crack in Fig. 8 proceeding into the solder mask covering the top build-up layer of the substrate. These cracks are self-limiting in length as they move away from the die footprint region but may extend into one or more layers of the build-up dielectric. Due to the small sample size in the experimental splits, we do not plan on cross-sectioning these parts to confirm crack depths until the completion of temperature cycling. The SubB groups exhibit minor cracks in only a few corners scattered across the UF2 and UF3 splits and none in the SubB/UF1 split after 500 T/Cs.

Edge Fillet Damage Theory

The out-of-plane shear stress component τzy is very small except near the flip chip edges where it increases exponentially. This component is responsible for cyclic shear strain induced fatigue failures of solder balls around the periphery of the die. We would expect the edge fillet to reduce the magnitude of this stress, however, this is not confirmed by FEM results. The distribution of τzy along the normalized centerline half-length of the die surface plotted in Fig. 10 does not indicate a significant difference in shape with and without the edge fillet.

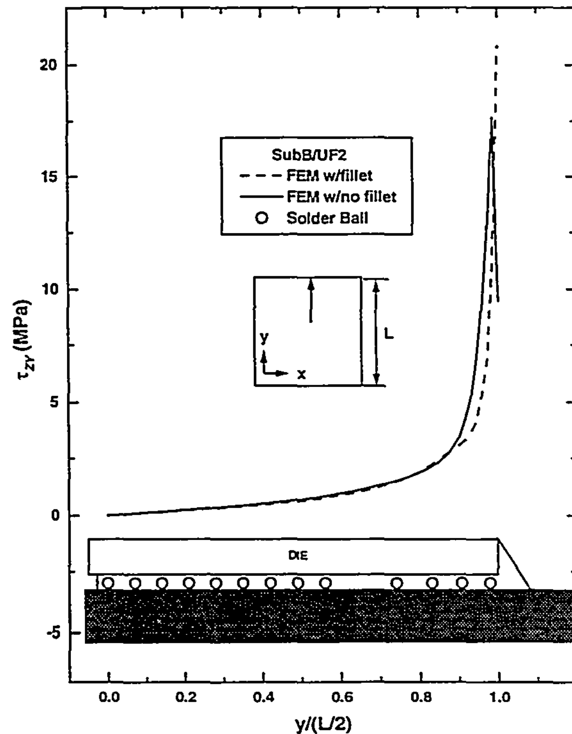

Fig. 10. Plot of τzy distribution (shear stress on the z-plane in the y-direction) along the normalized centerline half-length of the die surface. Dashed line is FEM calculation for SubB/UF2 with edge fillet effects, solid line is case without edge fillet. Location of solder balls relative to stress distribution are shown for reference.

The edge fillet significantly affects the peel stress component σzz. According to FEM simulations, this stress is tensile at the die perimeter without an edge fillet and highly compressive with an edge fillet. This is evident in Table VI and can be seen graphically in Fig. 11 where the distribution of σzz analytical and FEM calculations with and without fillet are plotted. (The no-fillet FEM simulation had numerical oscillations close to the edge, so we added a most likely

trajectory to the plot.) The no-fillet case results in tensile conditions at the edge while the presence of the fillet tends to "squeeze" the edge of die into the substrate due to the CTE mismatch between it and the Si die.

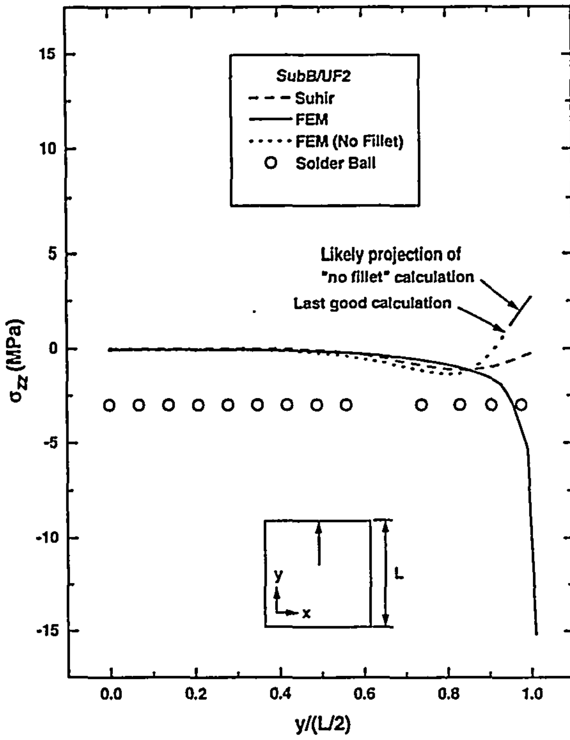

Fig. 11. Plot of σ_{zz} peel stress distribution along the normalized centerline half-length of the die surface. Dotted line is from Suhir (neglects edge fillet effects), dashed line is FEM with edge fillet, and dash-dot line is FEM with no edge fillet. Solder ball locations are shown for reference.

Edge delaminations observed in the Bmp1/SubA/UF2 split are attributed to complete debonding of the fillet-to-die edge interface. We speculate, lacking supporting evidence from simulations that are still in process, that a *partial* debond of the edge fillet will create a tensile stress riser along the die edge. Fig. 12 contains FEM calculations of the shear stress distribution on the die edge (*y*-plane) in the *z* direction along the normalized height of the edge for the die center and die corner. Curiously, this component shows little variation from UF2→UF3 even though the peel stress σ_{zz} in the same location varies by over 86% (Table VI). The distribution in Fig. 12 shows a large negative stress at the top and positive at the bottom suggesting that the die edge is under *compression* by the fillet. A partial debond starting at the top would cause the peak negative (downward) stress to move along with the debond tip. The unbonded part of the edge would respond to the tendency of the die to straighten resulting in a large tensile stress concentration at the debond tip. This could lead to die cracking during temperature cycles if coincident with other risk factors such as wafer saw damage and high general die stress due to non-ideal underfill and substrate properties.

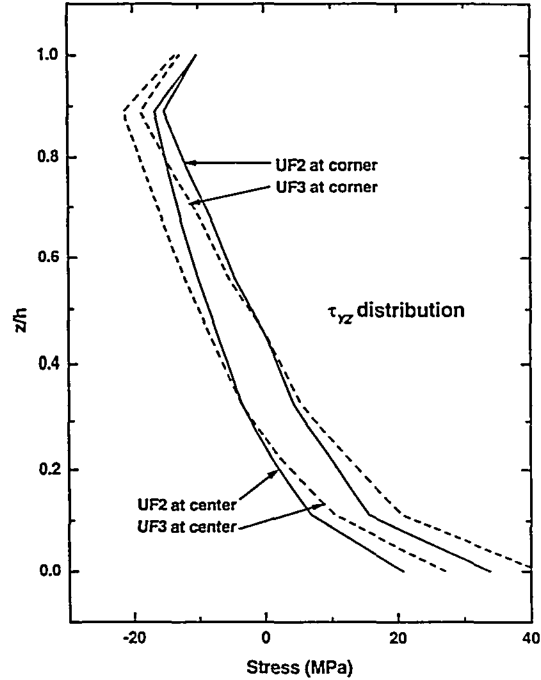

Fig. 12. Distribution of shear stress in the *y*-plane in the *z*-direction along the normalized edge of the die from SubBUF2 and SubBUF3 FEM calculations.

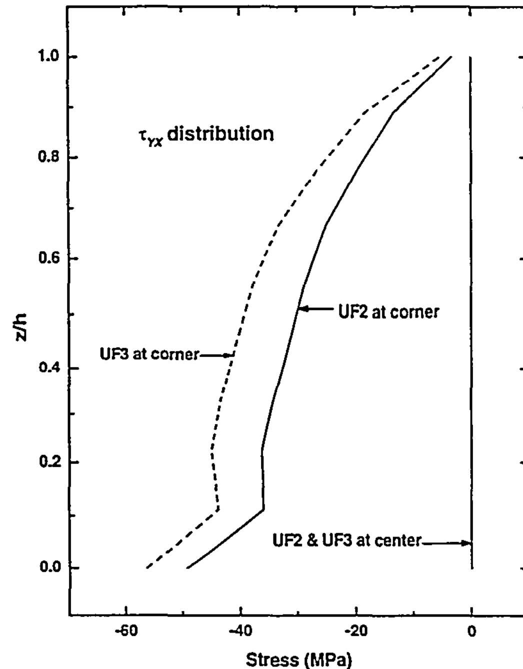

Fig. 13. Distribution of shear stress in the *y*-plane in the *x*-direction along the normalized edge of the die from SubBUF2 and SubBUF3 FEM calculations.

Radial cracking, the third damage mechanism observed, can be explained by examining in-plane stresses within the edge fillet. The fillet is under tension similar to a rubber band stretched around a box. FEM simulations show when it is properly bonded to the die edge, the tensile stress is relatively

uniform around the perimeter, peaking slightly at die centerlines. Shear stress between the fillet and die edge are zero at the centerlines and maximum at the corners. (See Fig. 13.) Debonding would be expected to start at the highest shear region in the corner resulting in a build up of tensile stress that increases with increasing debonded area. The resulting tensile stress concentration at the corner is relieved by radial cracking.

Conclusions

Partial and complete debonding of the fillet-to-die edge interface were observed in flip chip BGA parts that exhibited die cracking and underfill-to-die interfacial edge delamination during temperature cycling. Die cracking is more likely in assemblies under greater stress and in combination with rough or dicing-saw damaged edges, but appears to be triggered by stress risers at the tip of a partially debonded edge fillet. Edge delamination, on the other hand, requires complete debonding of the edge fillet in order to initiate.

Cracks emanating from die corners through the edge fillet and proceeding radially into and along the surface of the solder mask and build-up dielectric were associated with the same debonding of the fillet-to-die edge interface. FEM simulations show relatively uniform tensile stresses in the edge fillet when bonded that become concentrated at the die corner after debonding.

The critical role of the edge fillet in preventing delamination within the underfill region raises questions about the reliability of fillet-less wafer level processes currently under development.

Analytical calculations are very useful for estimating much of the response of an FCOB assembly to thermal stress but can be misleading near the die edge due to the effect of the edge fillet.

3D FEM simulation is still the only practical way of gaining insight into the behavior of a complex assembly such as FCOB under thermal stress. This technique leads naturally to material and process optimization of the underfill and edge fillet.

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